



June 2000  
Revised June 2000

# FSTD16211

## 24-Bit Bus Switch with Level Shifting

### General Description

The Fairchild Switch FSTD16211 provides 24-bits of high-speed CMOS TTL-compatible bus switching. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. A diode to  $V_{CC}$  has been integrated into the circuit to allow for level shifting between 5V inputs and 3.3V outputs.

The device is organized as a 12-bit or 24-bit bus switch. When  $\overline{OE}_1$  is LOW, the switch is ON and Port 1A is connected to Port 1B. When  $\overline{OE}_2$  is LOW, Port 2A is connected to Port 2B. When  $\overline{OE}_{1/2}$  is HIGH, a high impedance state exists between the A and B Ports.

### Features

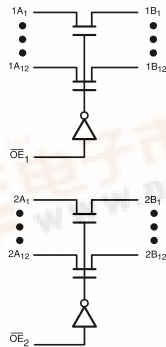
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low  $I_{CC}$ .
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

### Ordering Code:

Order Number	Package Number	Package Description
FSTD16211MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Diagram



### Connection Diagram

NC	1	56	$\overline{OE}_1$
1A <sub>1</sub>	2	55	$\overline{OE}_2$
1A <sub>2</sub>	3	54	1B <sub>1</sub>
1A <sub>3</sub>	4	53	1B <sub>2</sub>
1A <sub>4</sub>	5	52	1B <sub>3</sub>
1A <sub>5</sub>	6	51	1B <sub>4</sub>
1A <sub>6</sub>	7	50	1B <sub>5</sub>
GND	8	49	GND
1A <sub>7</sub>	9	48	1B <sub>6</sub>
1A <sub>8</sub>	10	47	1B <sub>7</sub>
1A <sub>9</sub>	11	46	1B <sub>8</sub>
1A <sub>10</sub>	12	45	1B <sub>9</sub>
1A <sub>11</sub>	13	44	1B <sub>10</sub>
1A <sub>12</sub>	14	43	1B <sub>11</sub>
2A <sub>1</sub>	15	42	1B <sub>12</sub>
2A <sub>2</sub>	16	41	2B <sub>1</sub>
2A <sub>3</sub>	17	40	2B <sub>2</sub>
V <sub>CC</sub>	18	39	2B <sub>3</sub>
2A <sub>4</sub>	19	38	GND
2A <sub>5</sub>	20	37	2B <sub>4</sub>
2A <sub>6</sub>	21	36	2B <sub>5</sub>
2A <sub>7</sub>	22	35	2B <sub>6</sub>
2A <sub>8</sub>	23	34	2B <sub>7</sub>
2A <sub>9</sub>	24	33	2B <sub>8</sub>
2A <sub>10</sub>	25	32	2B <sub>9</sub>
2A <sub>11</sub>	26	31	2B <sub>10</sub>
2A <sub>12</sub>	27	30	2B <sub>11</sub>
	28	29	2B <sub>12</sub>

### Truth Table

Inputs		Inputs/Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

### Pin Descriptions

Pin Name	Description
$\overline{OE}_1, \overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B

FSTD16211 24-Bit Bus Switch with Level Shifting



**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Switch Voltage ( $V_S$ ) (Note 2)	-0.5V to +7.0V
DC Input Control Pin Voltage ( $V_{IN}$ )(Note 3)	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ ) $V_{IN} < 0V$	-50mA
DC Output ( $I_{OUT}$ )	128mA
DC $V_{CC}/GND$ Current ( $I_{CC}/I_{GND}$ )	+/- 100mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150 °C

**Recommended Operating Conditions** (Note 4)

Power Supply Operating ( $V_{CC}$ )	4.5V to 5.5V
Input Voltage ( $V_{IN}$ )	0V to 5.5V
Output Voltage ( $V_{OUT}$ )	0V to 5.5V
Input Rise and Fall Time ( $t_r, t_f$ )	0nS/V to 5nS/V
Switch Control Input	0nS/V to DC
Switch I/O	0nS/V to DC
Free Air Operating Temperature ( $T_A$ )	-40 °C to +85 °C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:**  $V_S$  is the voltage observed/applied at either A or B Ports across the switch.

**Note 3:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**Note 4:** Unused control inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40\text{ °C to }+85\text{ °C}$			Units	Conditions
			Min	Typ (Note 5)	Max		
$V_{IK}$	Clamp Diode Voltage	4.5			-1.2	V	$I_{IN} = -18mA$
$V_{IH}$	HIGH Level Input Voltage	4.5-5.5	2.0			V	
$V_{IL}$	LOW Level Input Voltage	4.5-5.5			0.8	V	
$V_{OH}$	HIGH Level	4.5-5.5	See Figure 3			V	
$I_I$	Input Leakage Current	5.5			±1.0	μA	$0 \leq V_{IN} \leq 5.5V$
		0			10	μA	$V_{IN} = 5.5V$
$I_{OZ}$	OFF-STATE Leakage Current	5.5			±1.0	μA	$0 \leq A, B \leq V_{CC}$
$R_{ON}$	Switch On Resistance (Note 6)	4.5		4	7	Ω	$V_{IN} = 0V, I_{IN} = 64mA$
		4.5		4	7	Ω	$V_{IN} = 0V, I_{IN} = 30mA$
		4.5		35	50	Ω	$V_{IN} = 2.4V, I_{IN} = 15mA$
$I_{CC}$	Quiescent Supply Current	5.5			1.5	mA	$OE_1 = OE_2 = GND$ $V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
					10	μA	$OE_1 = OE_2 = V_{CC}$ $V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	5.5			2.5	mA	One input at 3.4V Other inputs at $V_{CC}$ or GND

**Note 5:** Typical values are at  $V_{CC} = 5.0V$  and  $T_A = +25\text{ °C}$

**Note 6:** Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

## AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$		Units	Conditions	Figure Number
		$C_L = 50\text{ pF, } R_U = R_D = 500\Omega$				
		$V_{CC} = 4.5 - 5.5\text{ V}$				
		Min	Max			
$t_{PHL}, t_{PLH}$	Prop Delay Bus to Bus (Note 7)		0.25	ns	$V_I = \text{OPEN}$	Figures 1, 2
$t_{PZH}, t_{PZL}$	Output Enable Time	1.5	5.5	ns	$V_I = 7\text{ V}$ for $t_{PZL}$ $V_I = \text{OPEN}$ for $t_{PZH}$	Figures 1, 2
$t_{PHZ}, t_{PLZ}$	Output Disable Time	1.5	6.5	ns	$V_I = 7\text{ V}$ for $t_{PLZ}$ $V_I = \text{OPEN}$ for $t_{PHZ}$	Figures 1, 2

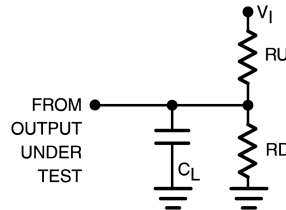
**Note 7:** This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical ON resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

### Capacitance (Note 8)

Symbol	Parameter	Typ	Max	Units	Conditions
$C_{IN}$	Control Pin Input Capacitance	3.5		pF	$V_{CC} = 5.0\text{ V}$
$C_{IO}$	Input/Output Capacitance	5.5		pF	$V_{CC}, \overline{OE} = 5.0\text{ V}$

**Note 8:**  $T_A = +25\text{ }^\circ\text{C}$ ,  $f = 1\text{ MHz}$ , Capacitance is characterized but not tested.

### AC Loading and Waveforms

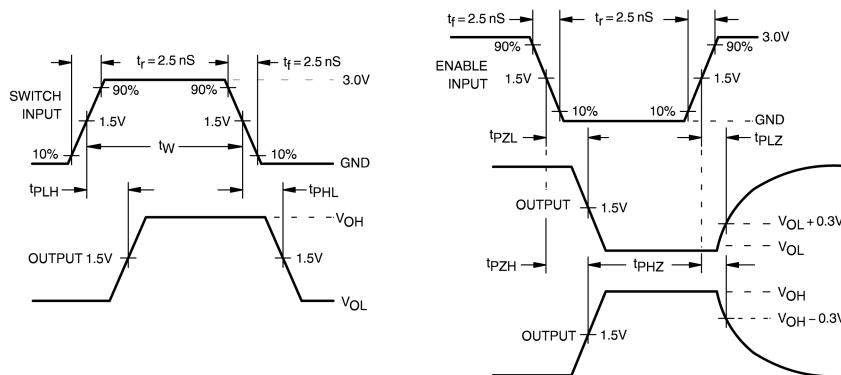


**Note:** Input driven by 50Ω source terminated in 50Ω

**Note:**  $C_L$  includes load and stray capacitance

**Note:** Input PRR = 1.0 MHz,  $t_W = 500\text{ ns}$

**FIGURE 1. AC Test Circuit**



**FIGURE 2. AC Waveforms**

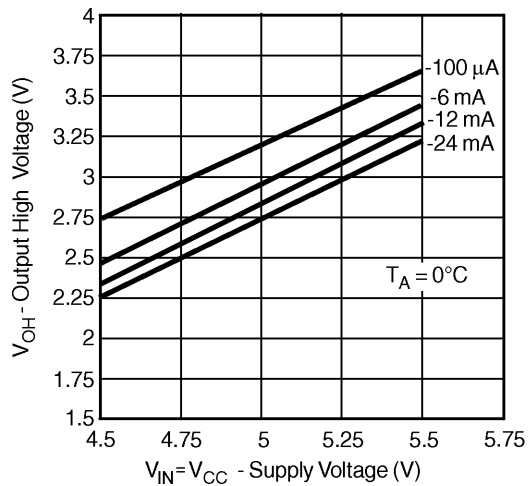
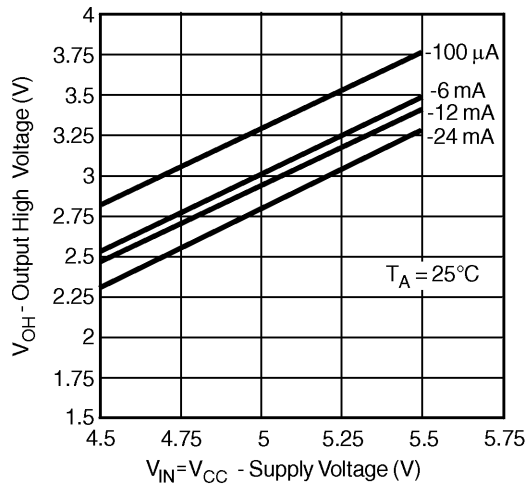
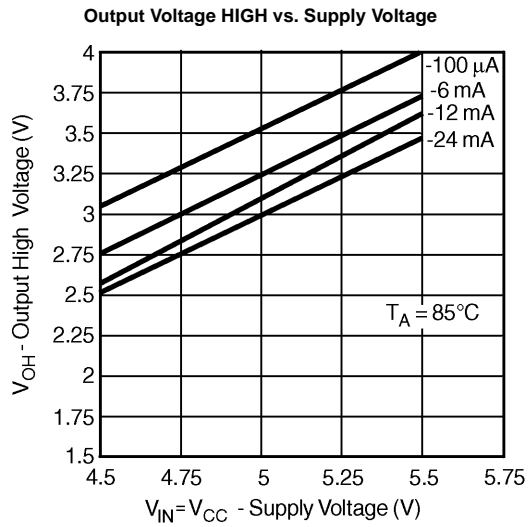
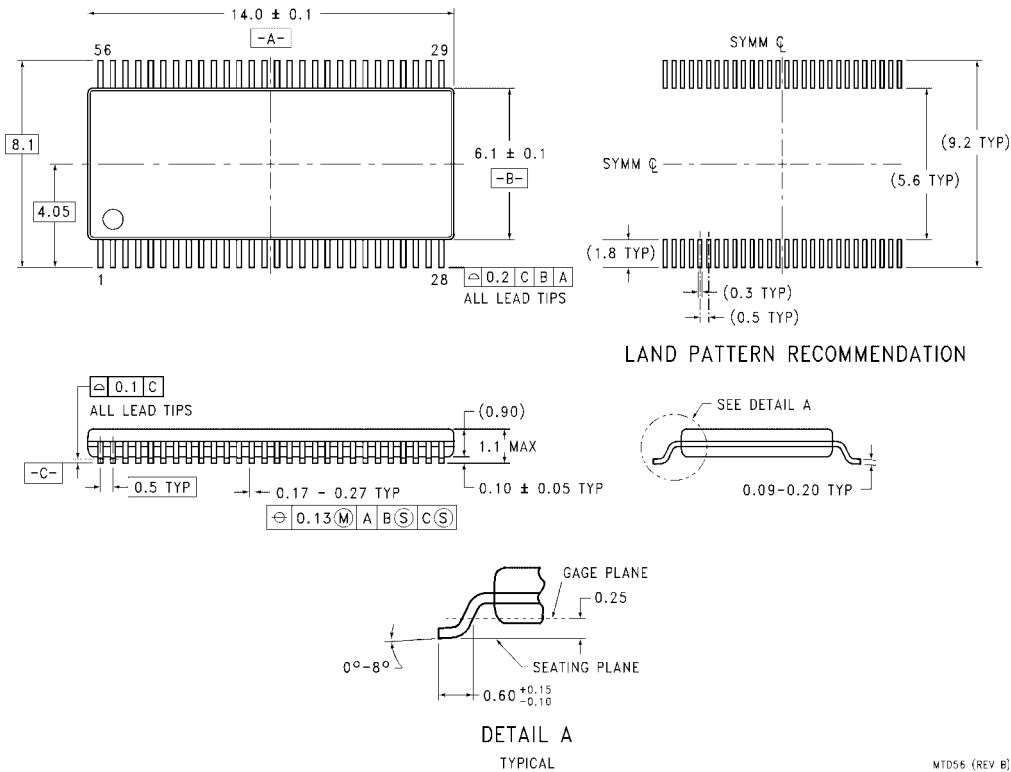


FIGURE 3.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
Package Number MTD56**

MTD56 (REV B)

**Technology Description**

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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