

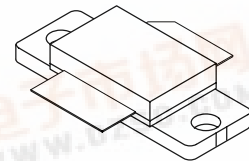
The RF MOSFET Line
RF Power Field Effect Transistor
N-Channel Enhancement-Mode Lateral MOSFET

MRF6522-70R3

Designed for GSM 900 frequency band, the high gain and broadband performance of this device make it ideal for large-signal, common source amplifier applications in 26 volt base station equipment.

- Specified Performance @ Full GSM Band, 921-960 MHz, 26 Volts
 Output Power, P1dB — 80 Watts (Typ)
 Power Gain @ P1dB — 16 dB (Typ)
 Efficiency @ P1dB — 58% (Typ)
- Available in Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

921 - 960 MHz, 70 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFET



CASE 465D-05, STYLE 1
NI-600

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Drain Current — Continuous	I_D	7	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	159 0.9	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.1	$^\circ\text{C}/\text{W}$

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 20 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Gate-Source Leakage Current (V _{GS} = 20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 300 μAdc)	V _{GS(th)}	2	3	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 400 mAdc)	V _{GS(Q)}	3	4	5	Vdc
Drain-Source On-Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	—	0.15	0.6	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	2	3	—	S

DYNAMIC CHARACTERISTICS

Input Capacitance (1) (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{iss}	—	130	—	pF
Output Capacitance (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{oss}	41	47	52	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	2.4	3	3.4	pF

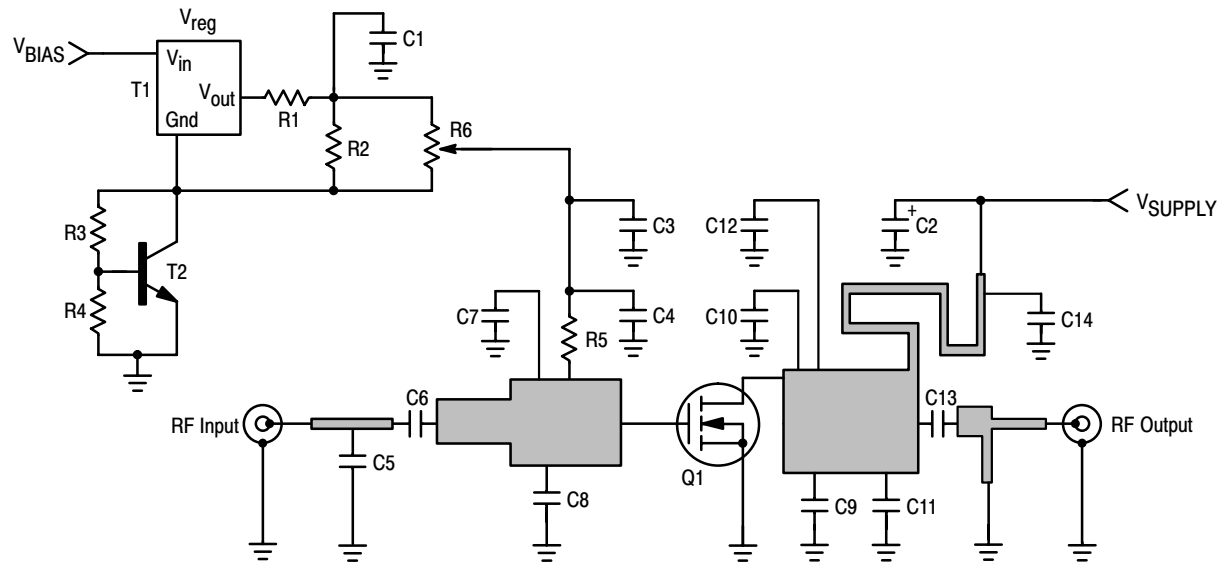
FUNCTIONAL TESTS (In Motorola Test Fixture)

Output Power (2) (V _{DD} = 26 Vdc, I _{DQ} = 400 mA, f = Full GSM Band 921 - 960 MHz)	P _{1dB}	73	80	—	W
Common-Source Amplifier Power Gain @ P _{1dB} (Min) (2) (V _{DD} = 26 Vdc, I _{DQ} = 400 mA, f = Full GSM Band 921 - 960 MHz)	G _{ps}	14	16	18	dB
Drain Efficiency @ P _{out} = 50 W (V _{DD} = 26 Vdc, I _{DQ} = 400 mA, f = Full GSM Band 921 - 960 MHz)	η ₁	47	51	—	%
Drain Efficiency @ P _{1dB} (2) (V _{DD} = 26 Vdc, I _{DQ} = 400 mA, f = Full GSM Band 921 - 960 MHz)	η ₂	—	58	—	%
Input Return Loss @ P _{out} = 50 W (V _{DD} = 26 Vdc, I _{DQ} = 400 mA, f = 921 MHz and 960 MHz f = 940 MHz)	IRL	— —	— —	- 10 - 15	dB
Output Mismatch Stress (2) (V _{DD} = 26 Vdc, I _{DQ} = 400 mA, f = Full GSM Band 921 - 960 MHz, VSWR = 5:1, All Phase Angles)	Ψ	No Degradation In Output Power Before and After Test			

(1) Value excludes the input matching.

(2) To meet application requirements, Motorola test fixtures have been designed to cover full GSM 900 band ensuring batch-to-batch consistency.

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C1	1.0 μ F Chip Capacitor (0805)	R3	1.2 k Ω Chip Resistor (0805)
C2	10 μ F, 35 Vdc Tantalum Capacitor	R4	2.2 k Ω Chip Resistor (0805)
C3	100 nF Chip Capacitor	R5	220 Ω Chip Resistor (0805)
C4, C6, C14	22 pF Chip Capacitors, ACCU-P (0805)	R6	5.0 k Ω SMD Potentiometer
C5	2.7 pF Chip Capacitor, ACCU-P (0805)	T1	LP2951 Micro-8
C7, C8, C13	4.7 pF Chip Capacitors, ACCU-P (0805)	T2	BC847 SOT-23
C9, C10	8.2 pF Chip Capacitors, ACCU-P (0805)		
C11, C12	2.2 pF Chip Capacitors, ACCU-P (0805)		
R1	10 Ω Chip Resistor (0805)		
R2	1.0 k Ω Chip Resistor (0805)		

SUBSTRATE G1180 0.8 mm

Figure 1. MRF6522-70 Test Circuit Schematic

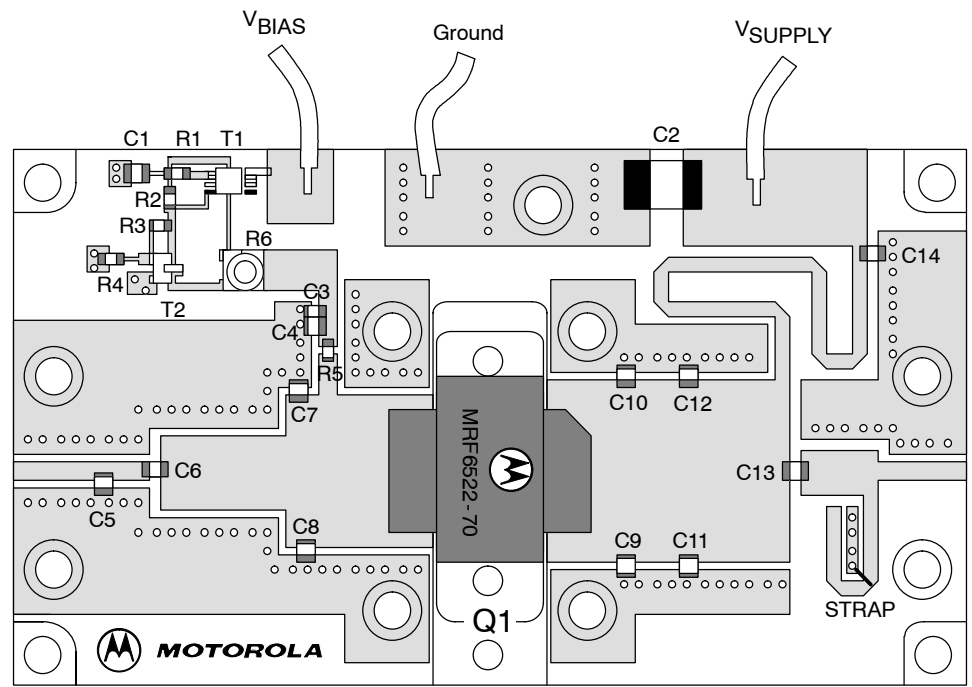


Figure 2. MRF6522-70 Test Circuit Component Layout

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TYPICAL CHARACTERISTICS

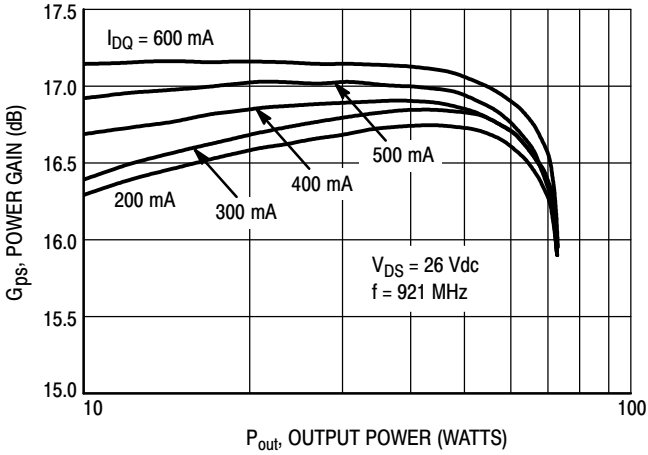


Figure 3. Power Gain versus Output Power

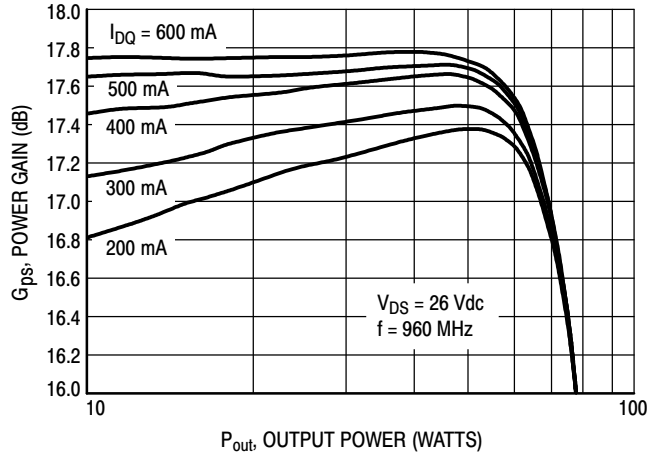


Figure 4. Power Gain versus Output Power

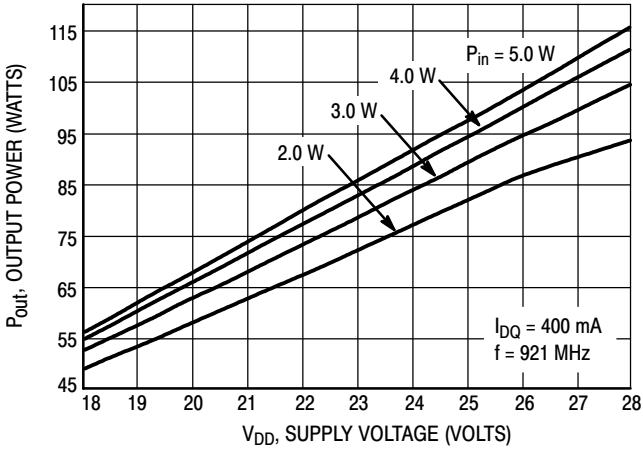


Figure 5. Output Power versus Supply Voltage

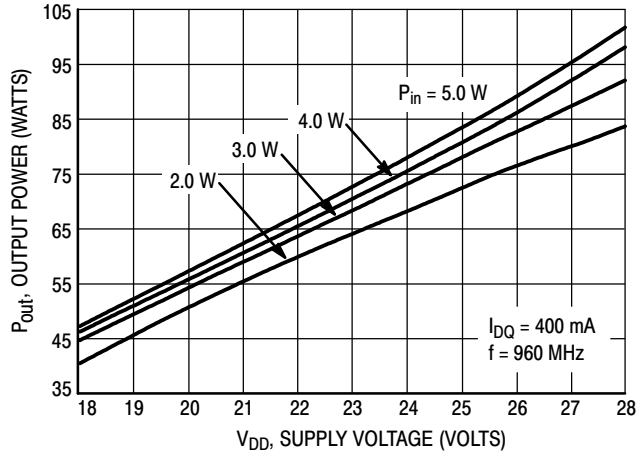


Figure 6. Output Power versus Supply Voltage

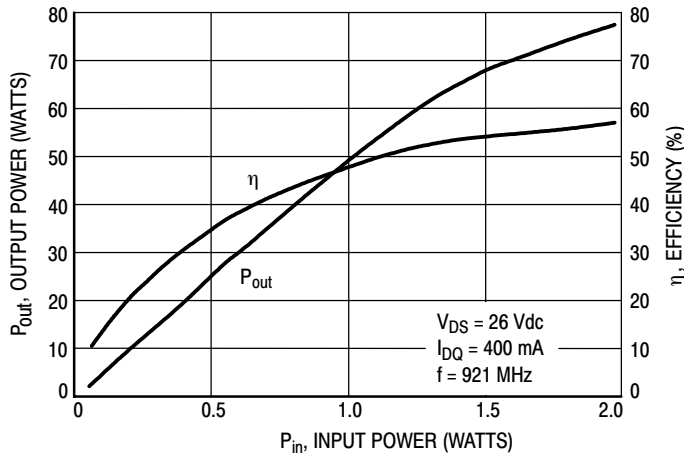


Figure 7. Efficiency and Output Power versus Input Power

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TYPICAL CHARACTERISTICS

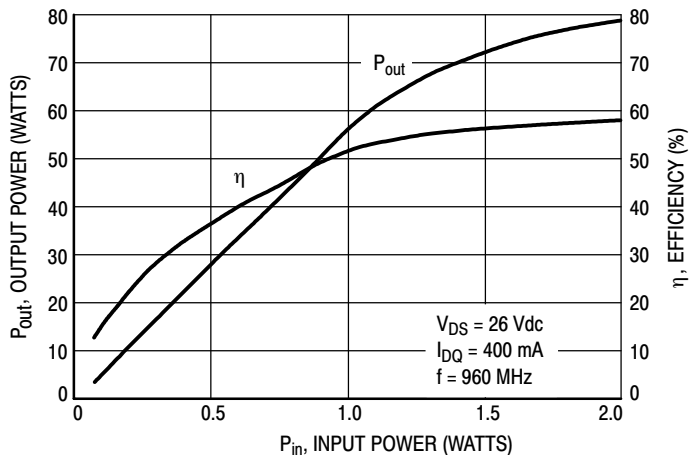


Figure 8. Efficiency and Output Power versus Input Power

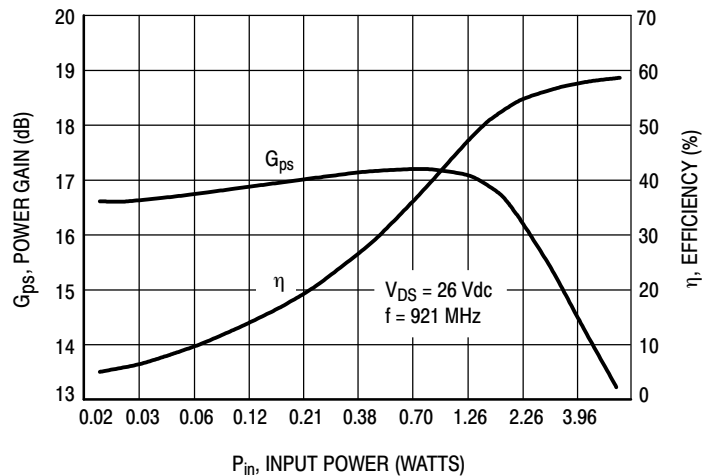


Figure 9. Power Gain and Efficiency versus Input Power

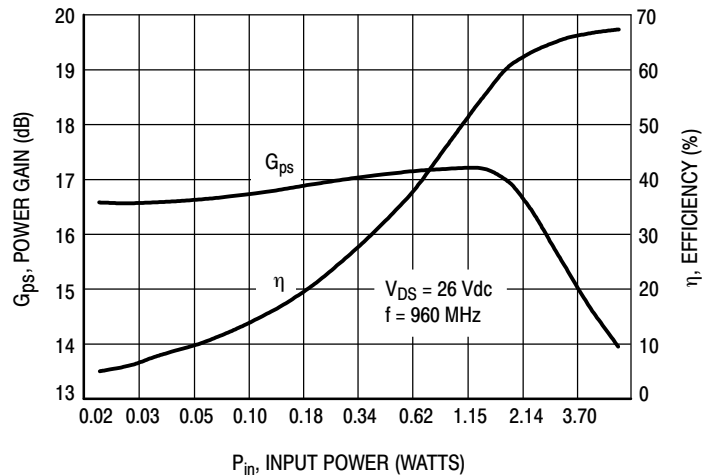


Figure 10. Power Gain and Efficiency versus Input Power

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TYPICAL CHARACTERISTICS

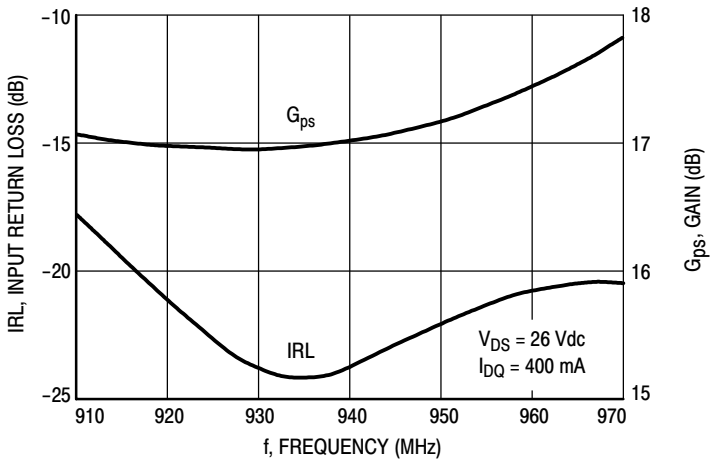
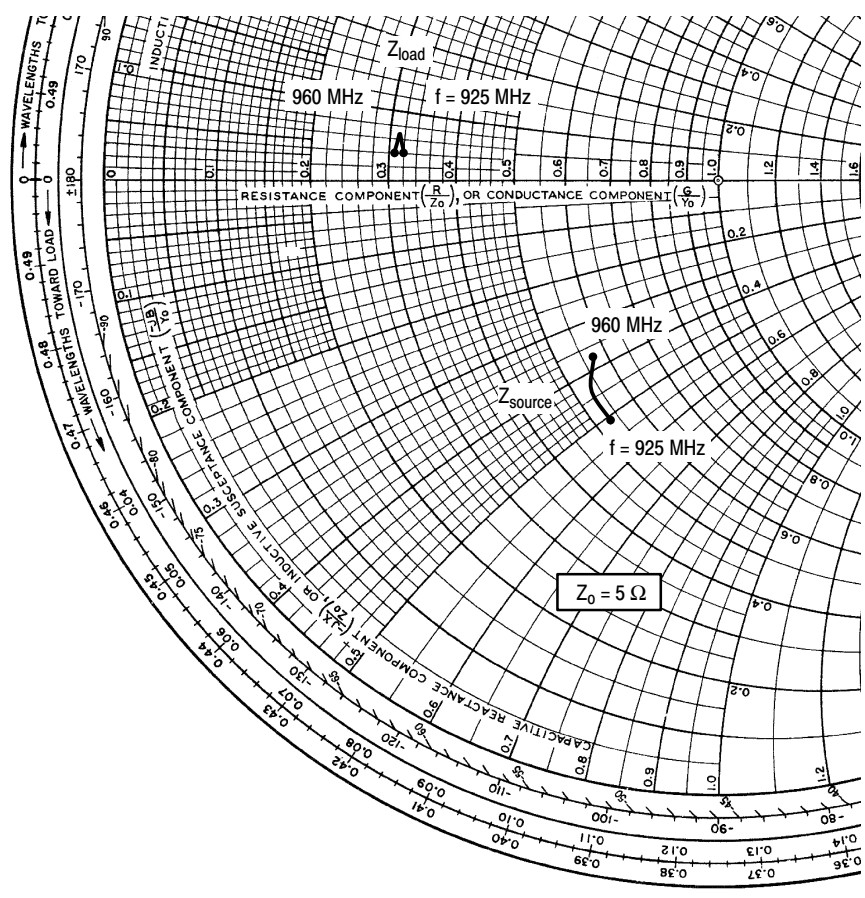


Figure 11. Performance in Broadband Circuit (at Small Signal)

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$V_{SUPPLY} = 26 \text{ Vdc}$, $I_{BIAS} = 400 \text{ mA}$, CW = Room Temperature

f MHz	Z_{source} Ω	Z_{load} Ω
925	$2.65 - j2.53$	$1.62 + j0.2$
940	$2.67 - j2.14$	$1.56 + j0.34$
960	$2.85 - j1.87$	$1.55 + j0.2$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

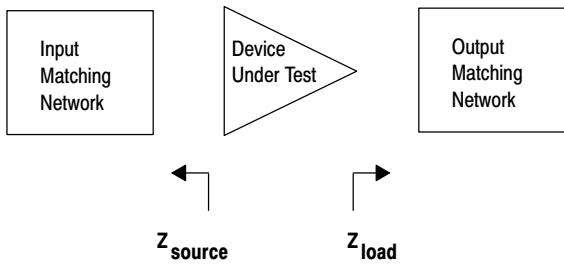
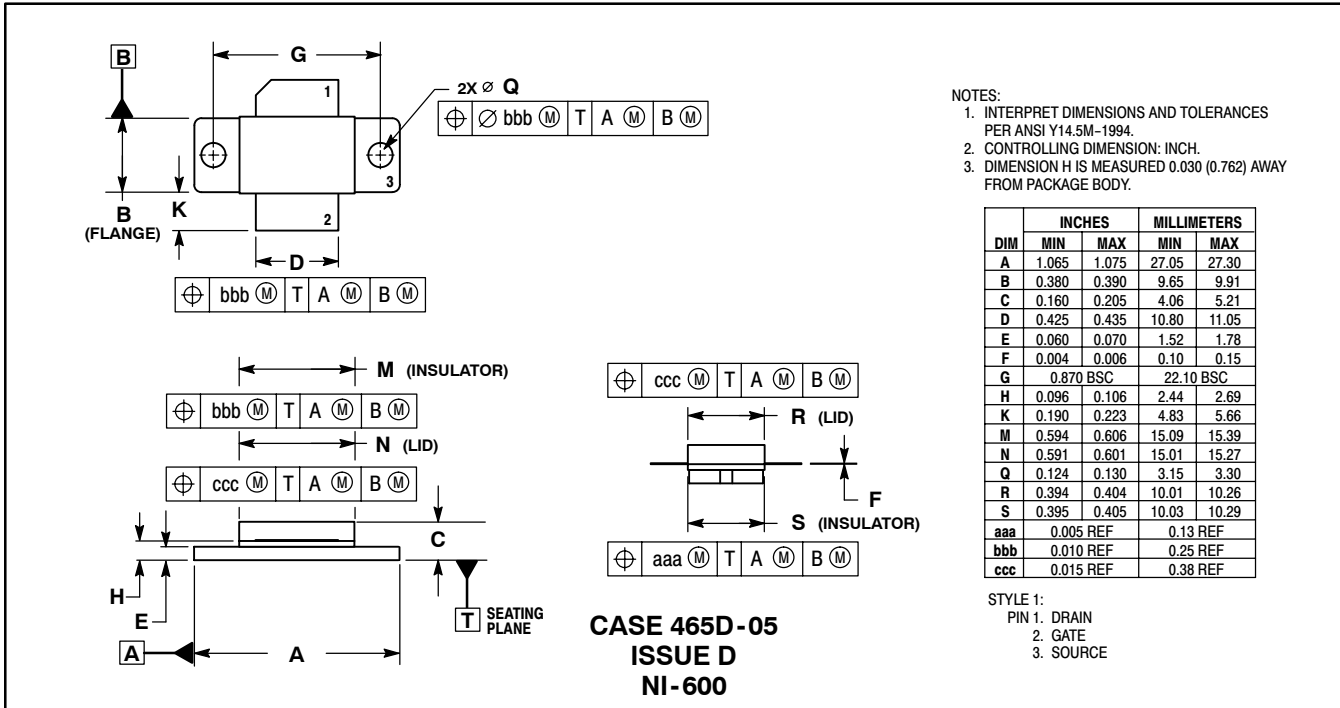


Figure 12. Series Equivalent Source and Load Impedance

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PACKAGE DIMENSIONS



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