AK7716

20bit 2ch ADC + 24bit 4ch DAC with Audio DSP

General Description

The AK7716 is a highly integrated audio processing IC, including 4 24-bit output D/A channels, a stereo 20-bit input A/D, on-chip DSP. High quality analog performance is provided by quad D/A with 113dB dynamic range, and stereo A/D with 98dB dynamic range. These converters support the standard audio sampling frequencies of 48,44.1 and 32kHz.

The programmable DSP is optimized for audio signal processing. The design allows up to 512 execution lines per audio sample cycle, with multiple functions per line. The AK7716 has a self-boot capability, using an external EEPROM.

The AK7716 can be used to implement complete sound field control, such as echo, 3D, parametric equalization, etc. It is packaged in a 100-lead LQFP package.

Features

DSP:

- **Word length: 24-bit (Data RAM)**
- **Instruction cycle time: 40.69ns (512fs, fs=48kHz)**
- **Multiplier: 24 x 16 → 40-bit**
- **Divider: 24 / 24 → 16-bit**
- **ALU: 34-bit arithmetic operation (Overflow margin: 4bit)**
- **24-bit arithmetic and logic operation**
- **Shift+Register: 1, 2, 3, 4, 8 and 15 bits shifted left**
- **1, 2, 3, 4, 8 and 15 bits shifted right**
- **Other numbers in parentheses are restricted. Provided with indirect shift function**
- **Program RAM: 448 x 32-bit**
- **Coefficient RAM: 384 x 16-bit**
- **Data RAM: 256 x 24-bit**
- **Offset RAM: 48 x 20-bit**
- **External Memory: Up to16Mbit DRAM or up to 1Mbit SRAM**
- **Sampling frequency: 32kHz to 48kHz**
- **Serial interface port for micro-controller**
- **Master clock: 512fs, 384fs, 256fs**
- **Master/Slave operation**
- **Serial signal input port (2 to 6 ch): 16/20/24-bit : Output port (4 to 8 ch): 24-bit**
- **Self-boot function using 32kbit E^2PROM AK93C95A**

ADC: 2 channels

- **20-bit 64x Over-sampling delta sigma**
- **DR, S/N : 98dB**
- **S/(N+D) : 92dB @-0.5dBFS**
- **Digital HPF (fc = 1Hz)**
- **Single-ended or Full-differential Input**

DAC: 4 channels

- **24-bit 128x Over-sampling advanced multi-bit**
- **DR, S/N : 113dBA**
- **S/(N+D) : 90dB @-10dBFS, 83dB @0dBFS**
- **Full-differential Output**
- **SMUTE function**

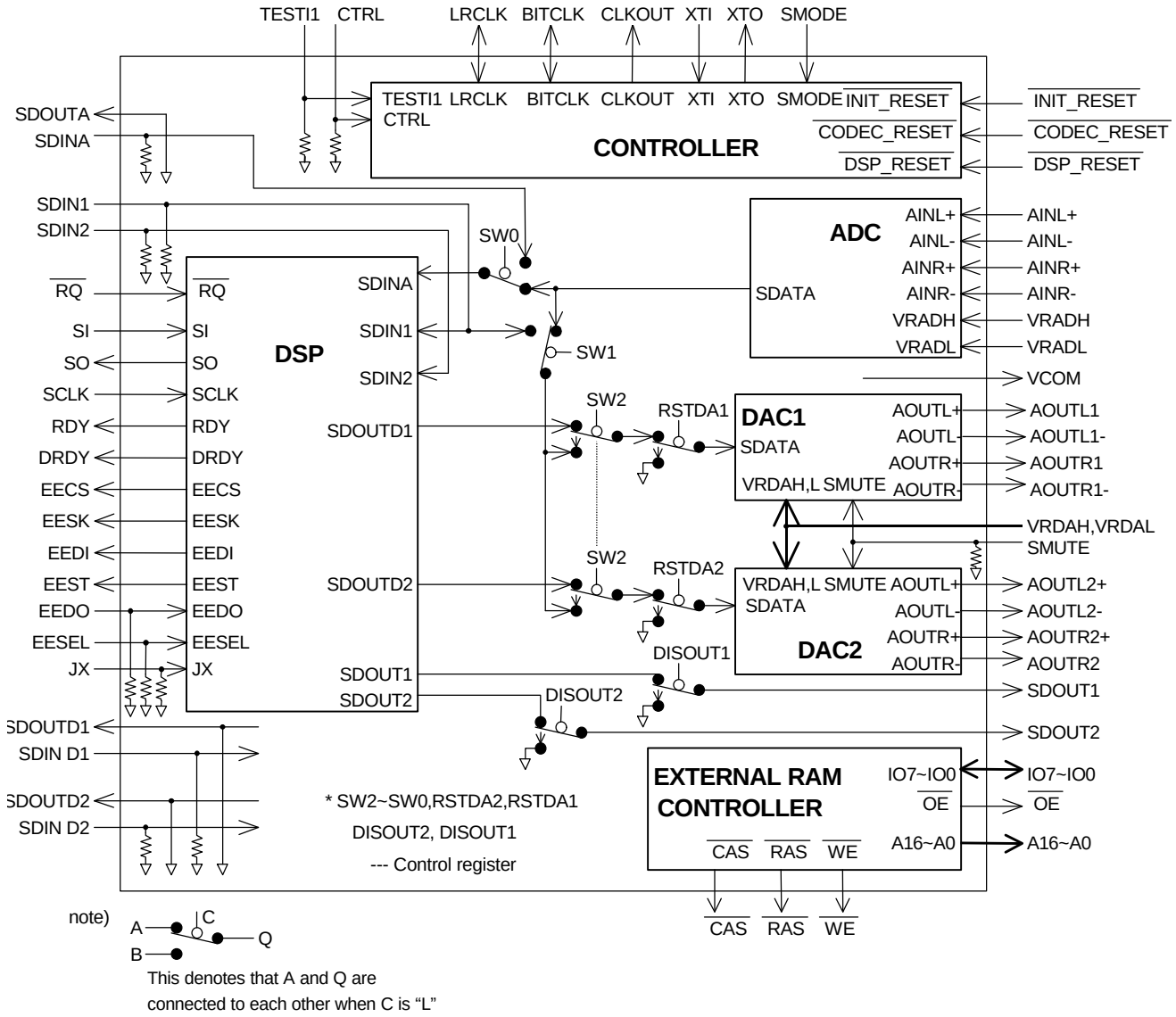
Other

- **Power supply: +5V±5%**
- **Operating temperature range: -40°C~85°C**
- **Package: 100pin LQFP (0.5mm pitch)**

Block diagram

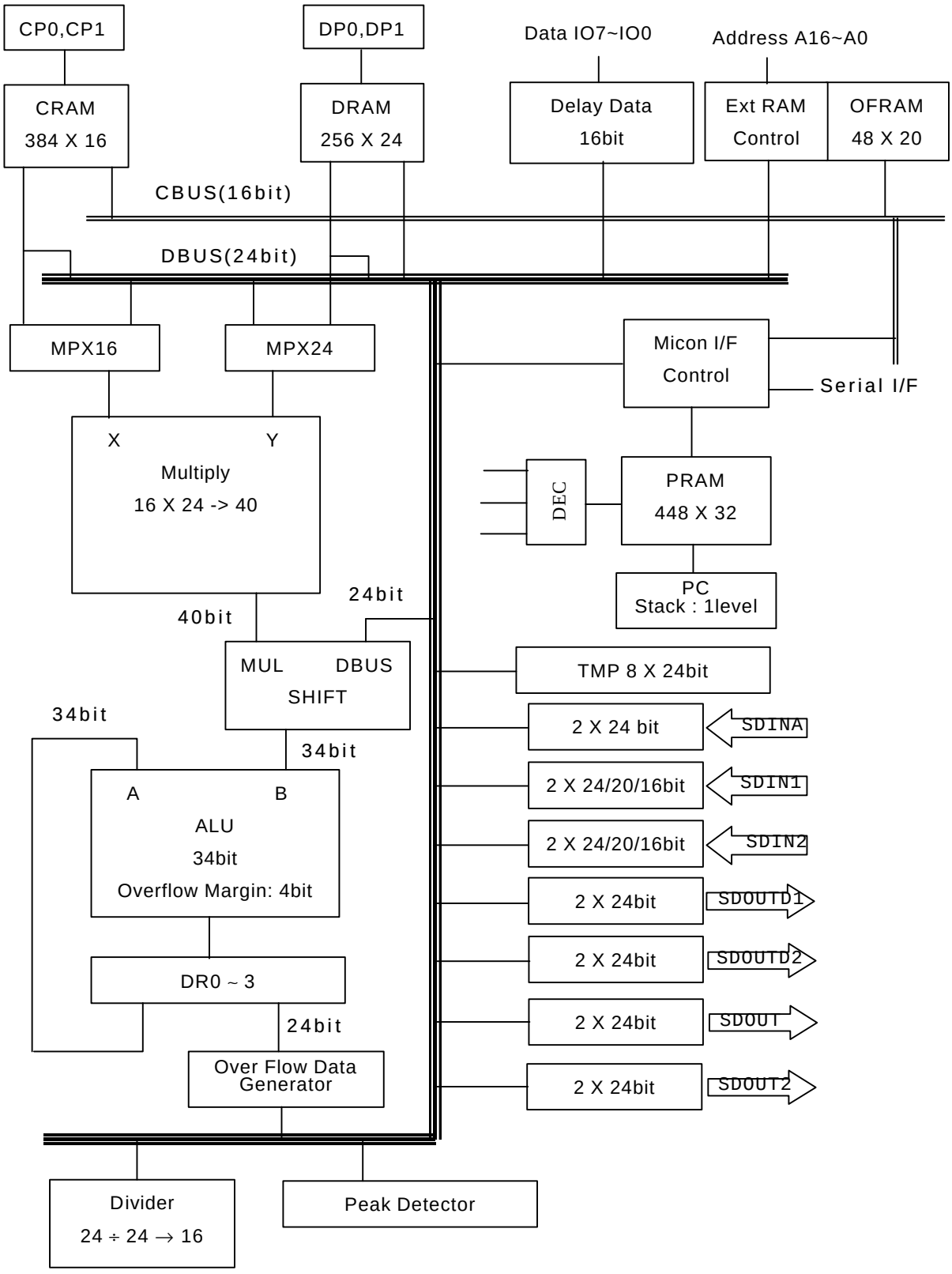
- **For standard operation (Internal connection mode: initial settings)**

* OPCL: L Internal connection mode



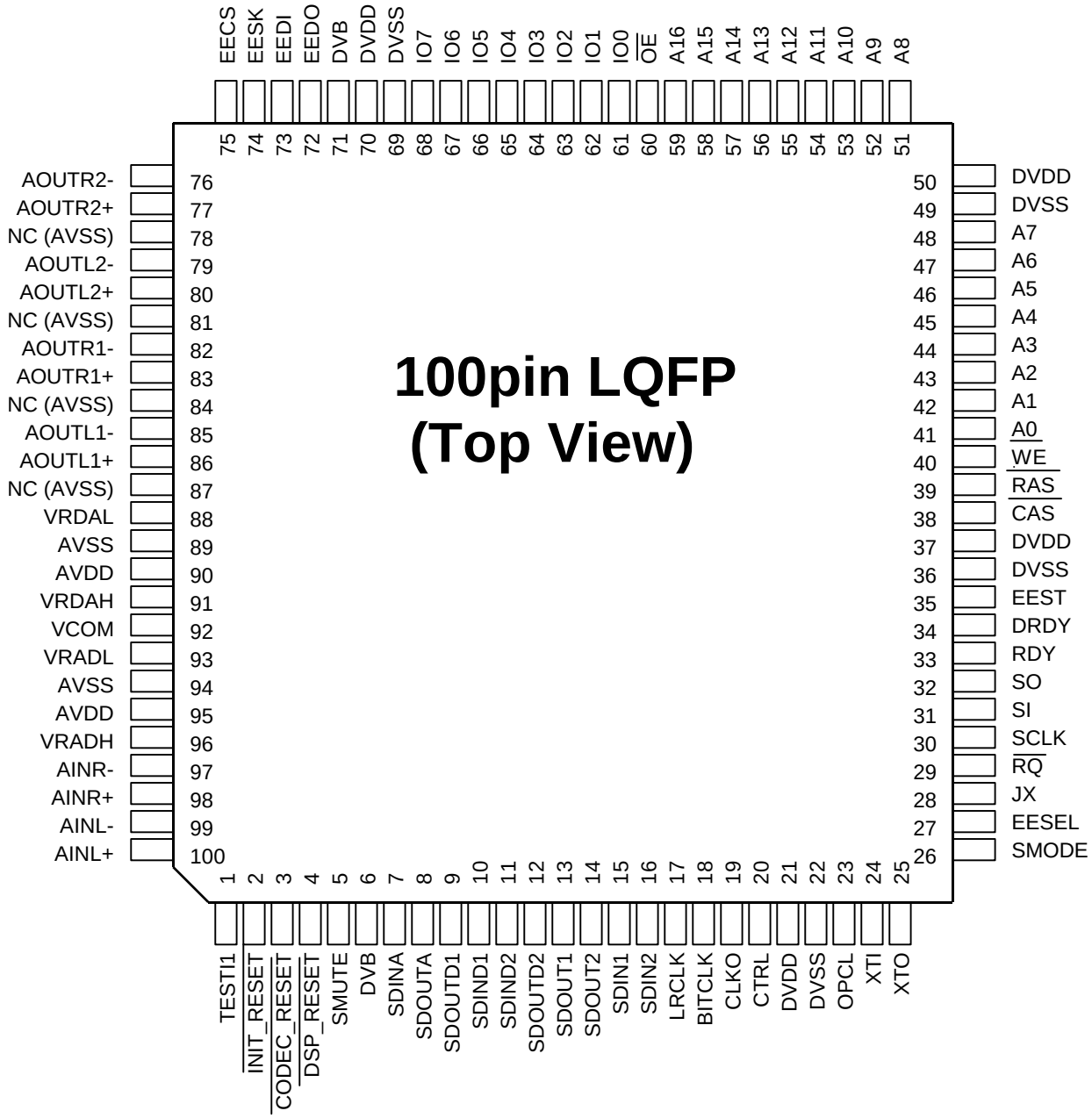
This block diagram is a simplified illustration of the AK7716; it is not a circuit diagram.

- **Block Diagram of AK7716 DSP Section**



Description of Input/Output Pins

(1) Pin layout



Note: [ ] Items enclosed in boxes are provided with pulldown functions.

(2) Pin function

Pin No.	Pin name	I/O	Function	Classification
1	TESTI1	I	**Test pin: Leave open or connect to DVSS. (Pulldown)**	Test
2	$\overline{\text{INIT\_RESET}}$	I	**Reset pin (for initialization)** Used to input “L” initialize the AK7716 at power-on	Reset Control
3	$\overline{\text{CODEC\_RESET}}$	I	**Reset pin** **Reset for CODEC section.**	
4	$\overline{\text{DSP\_RESET}}$	I	**Reset pin** **Reset for DSP section.**	
5	SMUTE	I	**Soft mute pin (Pulldown)** Digital Soft mute for DAC. SMUTE=”H”: Soft mute start. SMUTE=”L”: Soft mute release.	Digital section Soft mute
6	DVB	-	**+5V power supply (Silicon substrate potential)**	Power supply
7	SDINA	I	**DSP Serial data input pin (Pulldown)** OPCL=”L”: Disabled. Leave opens or connect to DVSS. OPCL=”H”: Compatible with MSB justified 24 bits.	Digital section Serial input/output data
8	SDOUTA	O	ADC Serial data output pin OPCL=”L”: Outputs “L”. (Leave Open) OPCL=”H”: Outputs MSB justified 20-bit data.	
9	SDOUTD1	O	**DSP Serial data output pin** OPCL=”L”: Outputs ”L”. (Leave Open) OPCL=”H”: Outputs MSB justified 24-bit data.	
10	SDIND1	I	**DAC1 Serial data input pin (Pulldown)** OPCL=”L”: Disabled. Leave opens or connect to DVSS. OPCL=”H”: Compatible with MSB justified 24 bits.	
11	SDIND2	I	**DAC2 Serial data input pin (Pulldown)** OPCL=”L”: Disabled. Leave opens or connect to DVSS. OPCL=”H”: Compatible with MSB justified 24 bits	
12	SDOUTD2	O	**DSP Serial data output pin.** OPCL=”L”: Outputs ”L”. OPCL=”H”: Outputs MSB justified 24-bit data.	
13	SDOUT1	O	**DSP Serial data output pin.** Outputs MSB justified 24-bit data.	
14	SDOUT2	O	**DSP Serial data output pin.** Outputs MSB justified 24-bit data.	
15	SDIN1	I	**DSP Serial data input pin (Pulldown)** Compatible with MSB/LSB justified 24, 20 and 16 bits.	Digital section Serial input data
16	SDIN2	I	**DSP Serial data input pin (Pulldown)** Compatible with MSB/LSB justified 24, 20 and 16 bits.	

Pin No.	Pin name	I/O	Function	Classification
17	LRCLK	I/O	**LR channel select Clock pin** SMODE="L": Slave mode: Inputs the fs clock. SMODE="H": Master mode: Outputs the fs clock.	System clock
18	BITCLK	I/O	**Serial bit clock pin** SMODE="L": Slave mode: Inputs 64 fs or 48 fs clocks. SMODE="H": Master mode: Outputs 64 fs clocks.	
19	CLKO	O	**Clock output pin** Outputs the XTI clock. Allows the output to be set to "L" when CTRL is “H”.	
20	CTRL	I	**Clock output control pin** **CTRL=”L”: CLKO is enable.** **CTRL=”H”: CLKO outputs ”L”.**	Control
21	DVDD	-	**Power supply pin for digital section 5V (typ)** +5V Digital power supply.	Power supply
22	DVSS	-	**Digital ground pin**	
23	OPCL	I	**ADC/DAC connection selector pin (Pulldown)** OPCL=”L” (Leave open or connect to DVSS). OPCL=”H”: Disconnected mode.	Control
24	XTI	I	**Master clock input pin** Connect a crystal oscillator between this pin and the XTO pin, or input the external CMOS clock signal XTI pin.	System clock
25	XTO	O	**Crystal oscillator output pin** When a crystal oscillator is used, it should be connected between XTI and XTO. When the external clock is used, keep this pin open	
26	SMODE	I	**Slave/master mode selector pin** Set LRCLK and BITCLK to input or output mode. SMODE="L": Slave mode (LRCLK and BITCLK are set to input mode.) SMODE="H": Master mode (LRCLK and BITCLK are set to output mode.)	Control
27	EESEL	I	**EEPROM boot up selector pin. (Pull down)** In case of loading program data from EEPROM, set EESEL=”H” (EEPROM should use the AK93C95A or compatible.)	EEPROM Control
28	JX	I	**External condition jump pin (Pulldown)**	Microcomputer interface

Pin No.	Pin name	I/O	Function	Classification
29	$\overline{RQ}$	I	**Microcomputer interface writes request pin.** $\overline{RQ}$ ="L": Microcomputer interface enable.	Microcomputer interface
30	SCLK	I	**Microcomputer interface serial data clock pin.** When SCLK does not use, leave SCLK="H".	
31	SI	I	**Microcomputer interface serial data input and serial data output control pin.** When SI does not use, leave SI="L".	
32	SO	O	**Serial data output pin for Microcomputer interfaces.**	
33	RDY	O	**Data write ready output pin for Microcomputer interface.**	
34	DRDY	O	**Output data ready pin for Microcomputer interface.**	
35	EEST	O	**EEPROM write status pin.** When the data should be program loading is finish from EEROM, EEST changes "L' to "H". After EEST changes to "H" then the micro interface is enabled.	EEPROM Control
36	DVSS	-	**Ground pin for digital section.**	Power supply
37	DVDD	-	**Power supply pin for digital section 5V (typ)**	
38	$\overline{CAS}$	O	**$\overline{CAS}$ Pin for external DRAM.**	External RAM Inteface
39	$\overline{RAS}$	O	**$\overline{RAS}$ pin for external DRAM**	
40	$\overline{WE}$	O	**Writes enable pin for external SRAM/DRAM.**	
41 ~ 48	A0 ~ A7	O	**Address output for external RAM (A0~A7)**	
49	DVSS	-	**Ground pin for digital section 0V.**	Power supply
50	DVDD	-	**Power supply pin for digital section 5V (typ)**	
51 ~ 59	A8 ~ A16	O	**Address output for external RAM (A8~A16)**	External RAM Interface
60	$\overline{OE}$	O	**Output enable signal output for external SRAM/DRAM.**	
61 ~ 68	IO0 ~ IO7	I/O	**Data input / output for external SRAM / DRAM.** These pins work as output pin unless READ data from external RAM instruction. If it does not connect external RAM then leave open.	
69	DVSS	-	**Ground pin for digital section 0V.**	Power supply
70	DVDD	-	**Power supply pin for digital section 5V (typ)**	
71	DVB	-	**Power supply pin 5V (typ) (Silicon substrate potential)**	
72	EEDO	I	**Serial input from EEPROM. (Pulldown)** Connect with DO pin of AK93C95A.	EEPROM Control
73	EEDI	O	**Serial output pin for EEPROM.** Connect with DI pin of AK93C95A.	
74	EESK	O	**Serial clock output pin for EEPROM** Connect with SK pin of AK93C95A	
75	EECS	O	**Chip select signal output pin for EEPROM** Connect with CS pin of AK93C95A	

Pin No.	Pin name	I/O	Function	Classification
76	AOUTR2-	O	**DAC2 Rch analog inverted output pin.**	Analog section
77	AOUTR2+	O	**DAC2 Rch analog non-inverted output pin.**	
78	NC	-	**Non connection pin** Connect with AVSS.	
79	AOUTL2-	O	**DAC2 Lch analog inverted output pin.**	
80	AOUTL2+	O	**DAC2 Lch analog non-inverted output pin.**	
81	NC	-	**Non connection pin.** Connect with AVSS.	
82	AOUTR1-	O	**DAC1 Rch analog inverted output pin.**	
83	AOUTR1+	O	**DAC1 Rch analog non-inverted output pin.**	
84	NC	-	**Non connection pin.** Connect with AVSS.	
85	AOUTL1-	O	**DAC1 Lch analog inverted output pin.**	
86	AOUTL1+	O	**DAC1 Lch analog non-inverted output pin.**	
87	NC	-	**Non connection pin.** Connect with AVSS.	
88	VRDAL	I	**DAC Reference voltage input pin** Normally, connect to AVSS (pin 89).	
89	AVSS	-	**Analog ground 0V**	Power supply
90	AVDD	-	**Power supply pin for analog section 5V (typ) (Silicon substrate potential)**	
91	VRDAH	I	**DAC Reference voltage input pin** Normally, connect to AVDD (pin 90), and connect 0.1μF and 10μF capacitors between this and VRDAL.	Analog section
92	VCOM	O	**Common voltage pin for analog section** Connect 0.1uF and 10uF capacitors between this and AVSS. Do not use for the external circuit.	
93	VRADL	I	**ADC Reference voltage input pin.** Normally, connect to AVSS(pin 94)	
94	AVSS	-	**Analog ground 0V**	Power supply
95	AVDD	-	**+5V Analog Power supply (Silicon substrate potential)**	
96	VRADH	I	**ADC Reference voltage input pin.** Normally, connect to AVDD (pin 95), and connect 0.1uF and 10uF capacitors between this pin and VADL.	Analog section
97	AINR-	I	**ADC Rch analog inverted input pin.**	
98	AINR+	I	**ADC Rch analog non-inverted input pin.**	
99	AINL-	I	**ADC Lch analog inverted input pin.**	
100	AINL+	I	**ADC Lch analog non-inverted input pin.**	

Absolute maximum rating

(AVSS, DVSS = 0 V: All voltages indicated are relative to the ground.)

Item	Symbol	Min	Max	Unit
Power supply voltage				
Analog (AVDD and DVB)	VA	-0.3	6.0	V
Digital (DVDD) (Note 1)	VD	-0.3	6.0 or (VA+0.3)	V
Input current (except for power supply pin)	IIN	-	±10	mA
Analog input voltage AINL+, AINL-, AINR+, AINR-, VRADH, VRADL, VRDAH, VRDAL	VINA	-0.3	VA+0.3	V
Digital input voltage (Note 1)	VIND	-0.3	VA+0.3	V
Operating ambient temperature	Ta	-40	85	°C
Storage temperature	Tstg	-65	150	°C

Note: 1. Must not exceed the maximum rating of 6.0 V (namely, VD ≤ (VA+ 0.3 V) ≤ 6.0 V).
(VA is a power supply to supply silicon substrate potential.)

WARNING: Operation at or beyond these limits may result in permanent damage of the device.
Normal operations are not guaranteed under these critical conditions in principle.

Recommended operating conditions

(AVSS, DVSS = 0 V: All voltages indicated are relative to the ground.)

Items		Min	Typ	Max	Unit
Power supply voltage					
Board (DVB), AVDD	VA	4.75	5.0	5.25	V
DVDD	VD	4.75	5.0	VA	V
Reference voltage (VREF)					
VRADH, VRDAH Note 1)	VRH		VA		V
VRADL, VRDAL Note 2)	VRL		0.0		V

Note 1) VRADH and VRDAH normally connect with AVDD.
Note 2) VRADL and VRADL normally connect with AVSS.

Note: 1. VA must rise simultaneously with or earlier than VD, and VD must fall simultaneously with or earlier than VA.
2. When starting and stopping the power supply, meet the absolute maximum rating condition: VD ≤ (VA+0.3 V).
It is generally recommended to use at VD ≤ VA. However, the VD must be 4.75 volts or more.
3. The analog input voltage and output voltage are proportional to the VRADH and VRDAH voltages.

Electric characteristics

(1) Analog characteristics

(Unless otherwise specified, Ta = 25°C; AVDD, DVDD, DVB = 5.0V; VRADH = AVDD, VRADL = AVSS, VRDAH = AVDD, VRDAL = AVSS; fs = 44.1 kHz; BITCLK = 64 fs; XTI = 256 fs; Signal frequency 1 kHz; measuring frequency = 20 Hz to 20 kHz; 20 bits; DSP section in the reset state; ADC with all differential inputs)

	Parameter	Min	Typ	Max	Unit
ADC Section	Resolution			20	Bits
	Dynamic characteristics				
	S/(N+D) (-0.5dB) (Note 1)	86	92		dB
	Dynamic range (A filter) (Note 2)	93	98		dB
	S/N (A filter)	93	98		dB
	Inter-channel isolation (f =1 kHz)	90	105		dB
	DC accuracy				
	Inter-channel gain mismatching		0.1	0.3	dB
	Gain drift		50		ppm/°C
	Analog input				
	Input voltage (Note 3)	±1.9	±2.0	±2.1	Vp-p
	Input impedance		220		kΩ
DAC section	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) (0 dB) (-10dB) (-20dB) (-60dB)	75	83 90 88 50		dB
	Dynamic range (-60 dB) (A filter) (Note 2)	107	113		dB
	S/N (A filter)	107	113		dB
	Inter-channel isolation (f = 1 kHz) (Note 4)	90	105		dB
	DC accuracy				
	Inter-channel gain mismatching (Note 4)		0.2	0.5	dB
	Gain drift		50		ppm/°C
	Analog output				
	Output voltage (AOUT+) – (AOUT-) (Note 5)	5.1	5.6	6.1	Vp-p
	Load resistance	5			kΩ

Note:
1. In case of the using single-ended input this value does not guarantee.
2. Indicates S/(N+D) when -60 dB signal is applied.
3. The full scale for analog input voltage (ΔAIN = (AIN+) - (AIN-)) can be represented by (±FS = ±(VRADH-VRADL) × 0.4).
4. Specified for L and R of each DAC.
5. This value is the case of VRDAH=AVDD. The full-scale of output voltage (0dB) is proportional to VRDAH.

(2) DC characteristics

(VDD=AVDD=DVDD=DVB=5.0V±5%,Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
High level input voltage	VIH				
Input pins other than XTI, TEST1, EEDO and IO7~0		2.4			V
XTI, TEST1, EEDO and IO7~0 pins		70%VDD			V
Low level input voltage	VIL				
Input pins other than XTI, TEST1, EEDO and IO7~0				0.6	V
XTI, TEST1, EEDO and IO7~0 pins				30%VDD	V
High level output voltage Iout=-100μA	VOH	VDD-0.5			V
Low level output voltage Iout=100μA	VOL			0.5	V
Input leak current Note 1)	Iin			±10	μA
Input leak current Pull down pin Note 1)	Iid		100		μA

Note: 1. The pull down pins is not included.
2. The pull down pins is as follows (Typ 50kΩ):
TESTI1, SMUTE, SDINA, SDIND1, SDIND2, SDIN1, SDIN2, CTRL, OPCL, JX, EESEL, EEDO

Note: Regarding the input/output levels in the text, the low level will be represented as "L" or 0, and the high level as "H" or 1. In principle, "0" and "1" will be used to represent the bus (serial/parallel) such as registers.

(3) Current consumption

(AVDD=DVB,DVDD=5.0V±5%, Ta=25°C; master clock (XTI)=24.576MHz=512fs[fs=48kHz]; when operating for DAC 4 channel with 1kHz sinusoidal wave full-scale input to each of ADC 2ch analog input pins)

Power supply				
Parameter	Min	Typ	Max	Unit
Power supply current				
1) During operation				
a) AVDD+DVB		48		mA
b) DVDD Note 1)		58		mA
c) Total(a+b)		106	140	mA
2) $\overline{\text{INIT RESET}}$ ="L" (Reference value) Note 2)		8		mA
Power consumption				
1) During operation				
a) AVDD+DVB		240		mW
b) DVDD Note 1)		290		mW
c) Total(a+b)		530	740	mW
2) $\overline{\text{INIT RESET}}$ ="L" (Reference value) Note 2)		40		mW

Note 1 Varies slightly according to the frequency used and contents of the DSP program.
Note 2 This is a reference value in case of using the crystal oscillator.
Because of the most of power current at the initial reset state is oscillator section,
the varies slightly according to the types of crystal oscillators and external circuits.

(4) Digital filter characteristics

Values described below are design values cited as references.

4-1) ADC Section :

(Ta=25°C; AVDD,DVDD,DVB=5.0V±5%; fs=44.1kHz)

parameter		Min	Typ	Max	Unit
Pass band (-0.02dB)	PB	0		20.00	kHz
(-6.0dB)		0		22.05	kHz
Stop band (Note 1)	SB	24.35			kHz
Pass band ripple (Note 2)	PR			±0.005	dB
Stop band attenuation (Note 3,4)	SA	80			dB
Group delay (Ts=1/fs)	GD		29.3		Ts

Note: 1 These frequencies scale with sampling frequency (fs).
2 The pass band is from DC to 19.75kHz from DC when fs = 44.1kHz.
3 The stop band is from 27.56kHz to 2.795MHz when fs = 44.1kHz.
4 When fs = 44.1kHz, the analog modulator samples analog input at 2.8224MHz.
The input signal is not attenuated by the digital filter in the maltiple bands (n x 2.8224MHz ± 20.21kHz; n=0, 1, 2, 3...) of the sampling frequency.

4-2) DAC section

(Ta=25°C; AVDD,DVDD,DVB=5.0V±5%; fs=44.1kHz)

Parameter	Symbol	min	typ	max	Unit
Digital filter					
Pass band ±0.07dB (Note 1)	PB	0		20.0	kHz
(-6.0dB)		-	22.05	-	kHz
Stop band (Note 1)	SB	24.1			kHz
Pass band ripple	PR			±0.07	dB
Stop band attenuation	SA	47			dB
Group delay (Note 2)	GD	-	16		1/fs
Digital filter+SCF					
Amplitude characteristics 0 to 20.0kHz			±0.5		dB

Note: 1 The pass band and stop band frequencies are proportional to "fs" (system sampling rate), and represents PB=0.4535fs(@-0.06dB) and SB=0.546fs, respectively.
2 This calculated delay time which occurs in the digital filter is from setting the 24-bit data of both channels on input register to the output of analog signal.

(5) Switching characteristics

5-1) System clock

(AVDD=DVB,DVDD=5.0V±5%,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Master clock (XTI)					
a) With a crystal oscillator:					
256fs: frequency	fMCLK	11.000	11.2896	12.288	MHz
384fs: frequency	fMCLK	12.288	16.9344	18.432	MHz
512fs: frequency	fMCLK	16.384	22.5792	24.576	MHz
b)With a external clock:					
Duty factor (≤18.432MHz) (>18.432MHz)		40 45	50 50	60 55	%
256fs:frequency : High level width : Low level width	fMCLK tMCLKH tMCLKL	11.000 30 30	11.2896	12.288	MHz ns ns
384fs:frequency : High level width : Low level width	fMCLK tMCLKH tMCLKL	12.288 20 20	16.9344	18.432	MHz ns ns
512fs:frequency : High level width : Low level width	fMCLK tMCLKH tMCLKL	16.384 16 16	22.5792	24.576	MHz ns ns
Clock rise time Clock fall time	tCR tCF			6 6	ns ns
LRCLK Sampling frequency	fs	32	44.1 1	48	kHz fs
Slave mode :clock rise time Slave mode :clock fall time	tLR tLF			10 10	ns ns
BITCLK Note 1)	fBCLK	48	64		fs
Slave mode: High level width Slave mode: Low level width	tBCLKH tBCLKL	100 100			ns ns
Slave mode :clock rise time Slave mode :clock fall time	tBR tBF			6 6	ns ns

Note 1) 48fs mode can be use only at slave mode.

5-2) Reset

(AVDD=DVB,DVDD=5.0V±5%,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
$\overline{\text{INIT RESET}}$ Note 2)	tRST	150			ns
$\overline{\text{DSP RESET}}$	tRST	150			ns
$\overline{\text{CODEC RESET}}$	tRST	150			ns

Note 2) "L" is acceptable when power is turned on, but "H" needs stable master clock input.

5-3) Audio interface

(AVDD=DVB,DVDD=5.0V±5%,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Slave mode					
BITCLKfrequency	fBCLK	48	64		fs
BITCLK low level width	tBCLKL	100			ns
BITCLK high level width	tBCLKH	100			ns
Delay time from BITCLK"↑" to LRCLK	tBLRD	40			ns
Delay time from LRCLK to BITCLK "↑"	tLRBD	40			ns
Delay time from LRCLK to serial data output	tLRD			70	ns
Delay time from BITCLK to serial data output	tBSOD			70	ns
Serial data input latch hold time	tBSIDS	40			ns
Serial data input latch setup time	tBSIDH	40			ns
Master mode					
BITCLK frequency	fBCLK		64		fs
BITCLK duty factor			50		%
Delay time from BITCLK"↑" to LRCLK	tBLRD	40			ns
Delay time from LRCLK to BITCLK"↑"	tLRBD	40			ns
Delay time from LRCLK to serial data output	tLRD			70	ns
Delay time from BITCLK to serial data output	tBSOD			70	ns
Serial data input latch hold time	tBSIDS	40			ns
Serial data input latch setup time	tBSIDH	40			ns

5-4) Microcomputer interface

(AVDD=DVB,DVDD=5.0V±5%,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Microcomputer interface signal					
$\overline{RQ}$ Fall time	tWRF			10	ns
$\overline{RQ}$ Rise time	tWRR			10	ns
SCLK fall time	tSF			10	ns
SCLKrise time	tSR			10	ns
SCLK low level width	tSCLKL	150			ns
SCLK high level width	tSCLKH	150			ns
Microcomputer to AK7716					
Time from $\overline{RESET}$ "↓" to $\overline{RQ}$ "↓"	tREW	200			ns
Time from $\overline{RQ}$ "↑" to $\overline{RESET}$ "↑" Note 1)	tWRE	200			ns
$\overline{RQ}$ high level width	tWRQH	200			ns
Time from $\overline{RQ}$ "↓" to SCLK"↓"	tWSC	200			ns
Time from SCLK"↑" to $\overline{RQ}$ "↑"	tSCW	6 x tMCLK			ns
SI latch setup time	tSIS	100			ns
SI latch hold time	tSIH	100			ns
AK7716 to microcomputer					
Time from SCLK"↑" to DRDY"↓"	tSDR			3 x tMCLK	ns
Time from SI"↑"to DRDY"↓"	tSIDR			3 x tMCLK	ns
SI high level width	tSIH	3 x tMCLK			ns
Delay time from SCLK"↓" to SO output	tSOS			100	ns
AK7716 to microcomputer (RAM DATA read-out)					
SI latch setup time (SI="H")	tRSISH	100			ns
SI latch setup time (SI="L")	tRSISL	100			ns
SI latch hold time	tRSIH	100			ns
Time from SCLK"↓" to SO(PRAM)	tSOPD			100	ns
Time from SCLK"↓" to SO(CRAM,OFRAM)	tSOCOD			100	ns

Note 1) Except for external jump code set at reset state.

5-5) External RAM interface

1) Read/Write Interface Timing of External RAM (Static RAM)
(AVDD,DVDD,DVB=5.0V±5%, Ta=-40~85°C, CL=20pF, XTI=22.5792MHz)

Parameter	Symbol	min	Max	Units
Address delay time from $\overline{OE}$ Low to High (Writing)	tAOEW	-15	15	ns
Address delay time from $\overline{OE}$ High to Low (Reading)	tAOER	-15	15	ns
Access time	tWCY	100		ns
Address set-up time	tWD	25		ns
Data set time	tDS	70		ns
Data hold time	tDH	5		ns
Pulse width to write	tWP	35		ns

2) Read/Write Interface Timing of External RAM (Dynamic RAM) (Fast Page Mode Read Cycle / Early Write Cycle)
(AVDD, DVDD, DVB=5.0V ± 5%, Ta=-40~85°C, CL=20pF, XTI=22.5792MHz)

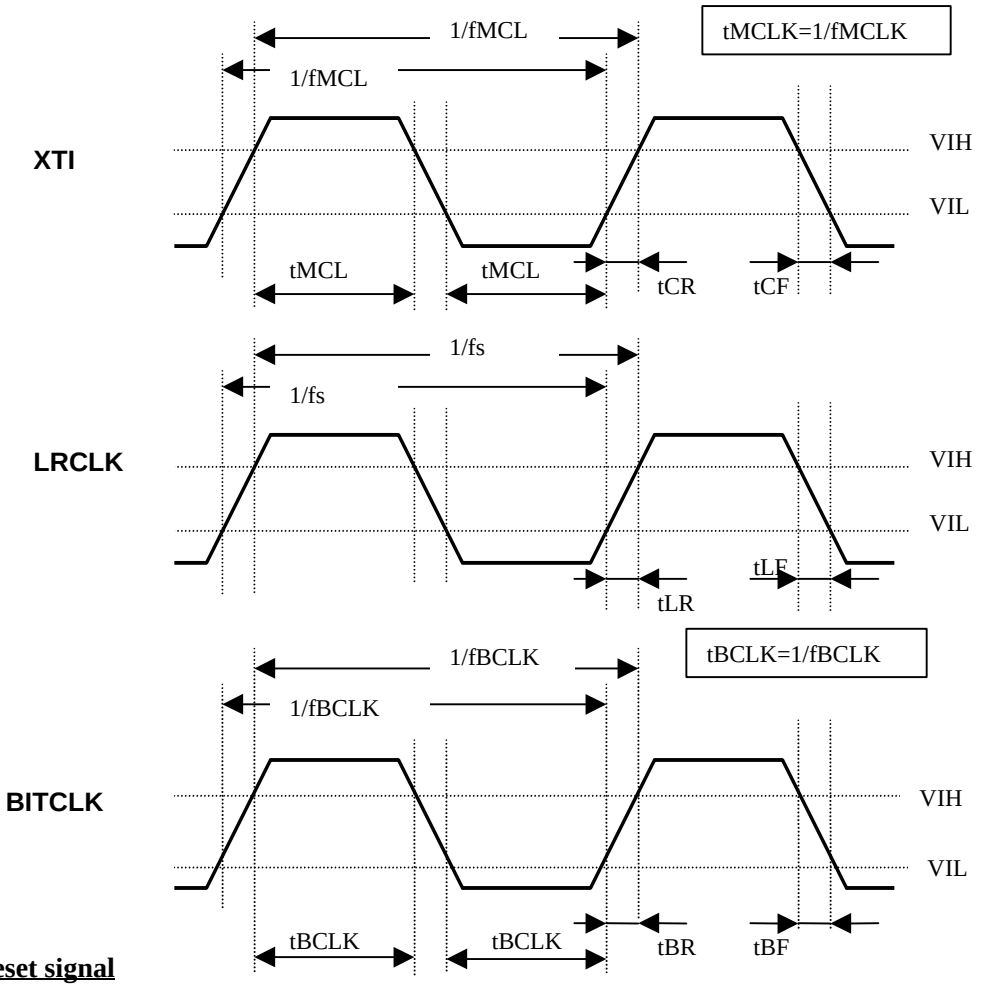
Parameter	Symbol	min	Max	Units
Access time	tRAC	85		ns
Address delay time from $\overline{OE}$ "L" to "H" (Writing)	tAOEW	-15	15	ns
Write command setup time	tWCS	20		ns
Write command hold time	tWCH	20		ns
Address delay time from $\overline{OE}$ "H" to "L" (Reading)	tAOER	-15	15	ns
Read command setup time	tRCS	85		ns
Read command hold time to $\overline{CAS}$	tRCH	20		ns
Read command hold time to $\overline{RAS}$	tRRH	35		ns
$\overline{RAS}$ preceded address setup time	tSURA	0		ns
$\overline{RAS}$ followed address hold time	tHRA	5		ns
$\overline{CAS}$ preceded address setup time	tSUCA	0		ns
$\overline{CAS}$ followed address hold time	tHCLCA	35		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20		ns
$\overline{RAS}$ hold time	tRSH	20		ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	20		ns
Data setup time	tSUD	35		ns
Data hold time after write	tHWLD	35		ns
Pulse width of $\overline{CAS}$ "H"	tWCH	20		ns
Pulse width of $\overline{CAS}$ "L"	tWCL	35		ns

3) Refresh Interface Timing of External RAM (Dynamic RAM) (CAS before RAS Refresh)
(AVDD, DVDD, DVB=5.0V±5%, Ta=-40~85°C, CL=20pF, XTI=22.5792MHz)

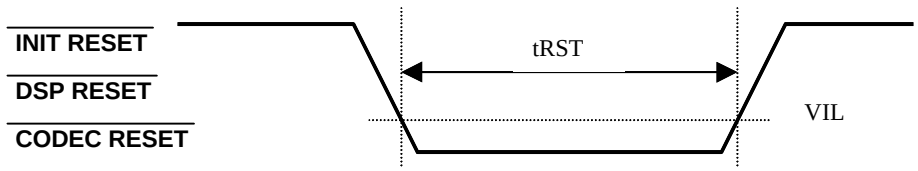
Parameter	Symbol	Min	Max	Units
Read cycle	tCRD	260		ns
Pulse width of $\overline{RAS}$ "H"	tWRH	85		ns
Pulse width of $\overline{RAS}$ "L"	tWRL	170		ns
$\overline{RAS}$ Pre-charge / $\overline{CAS}$ hold time	tRPC	70		ns
$\overline{CAS}$ setup time at auto refresh	tSUR	5		ns
$\overline{CAS}$ hold time at auto refresh	tHRRC	100		ns

(6) Timing waveform

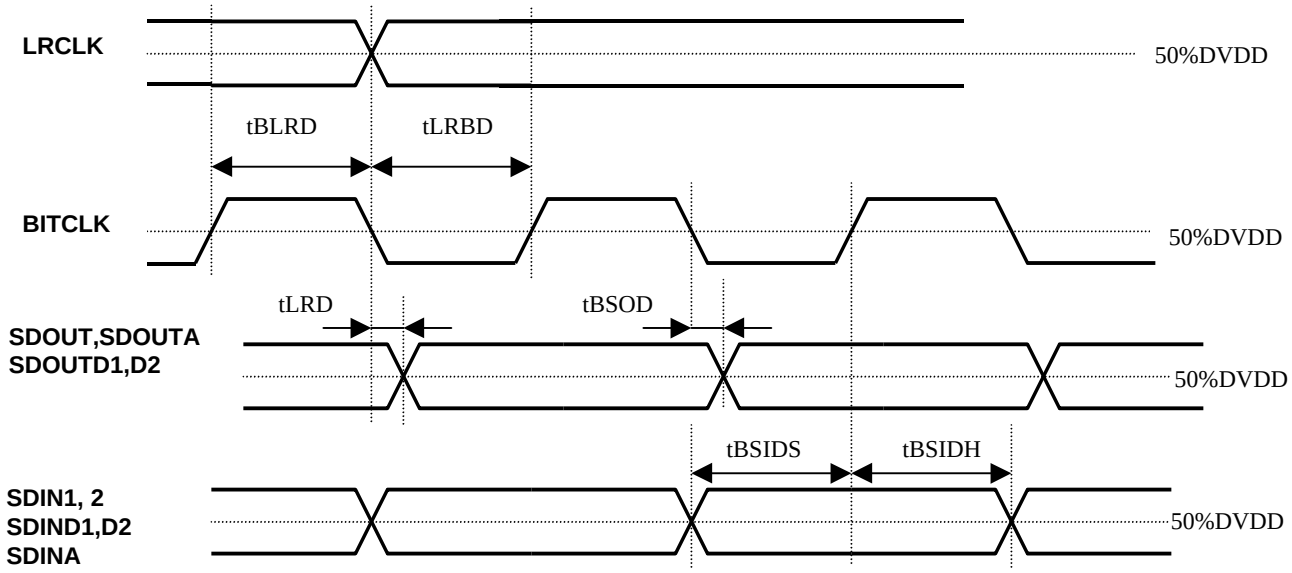
6-1) System clock



6-2) Reset signal

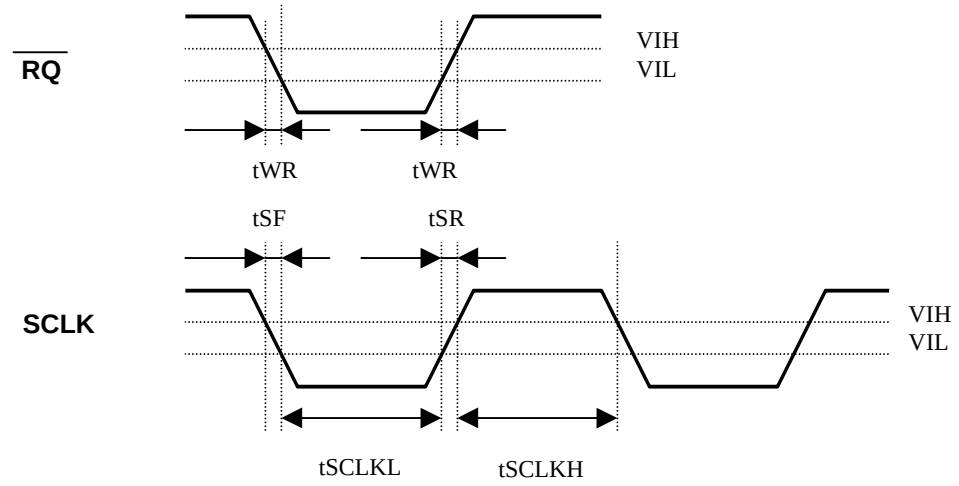


6-3) Audio interface

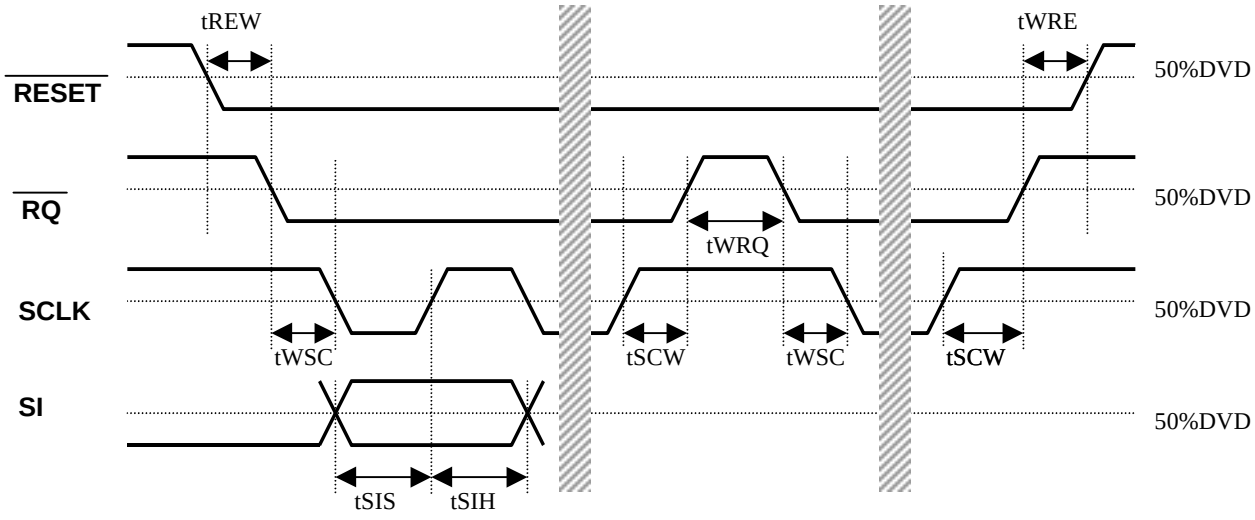


6-4) Microcomputer interface

- Microcomputer interface signals



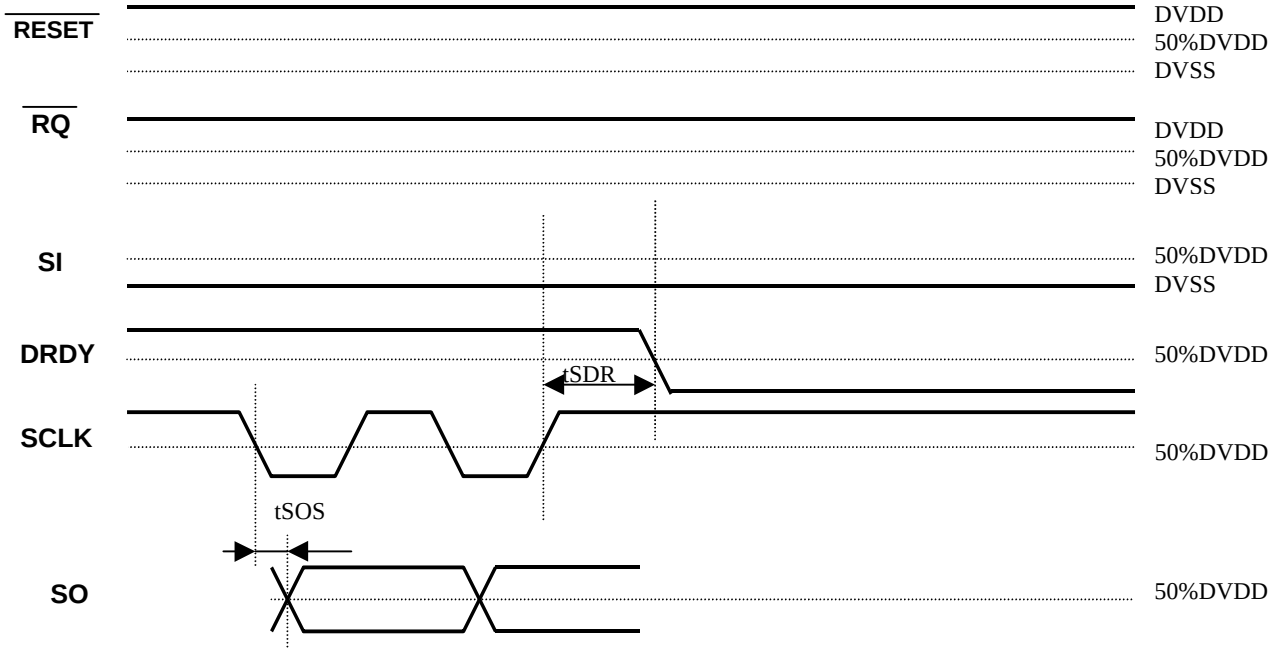
- Microcomputer to AK7716



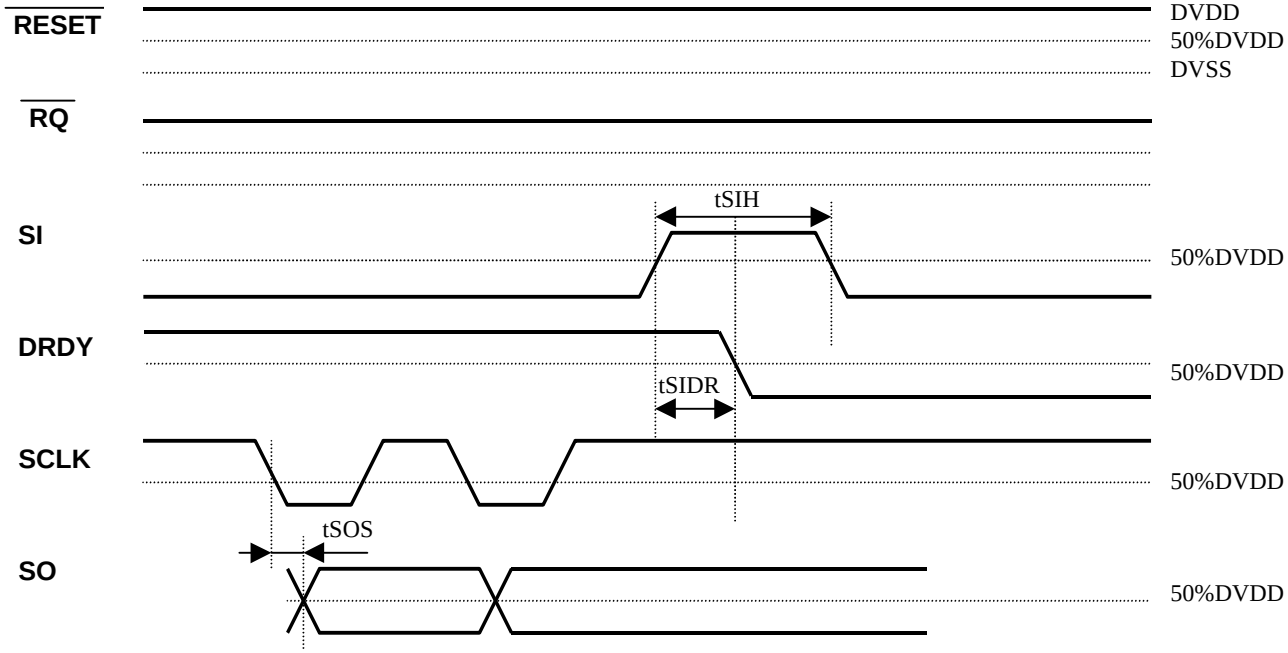
NOTE : Timing for RUN state is the same except that $\overline{\text{RESET}}$ is set to a "H"
$\overline{\text{RESET}}$ represents system reset in normal use.

- AK7716 to Microcomputer (DBUS data)

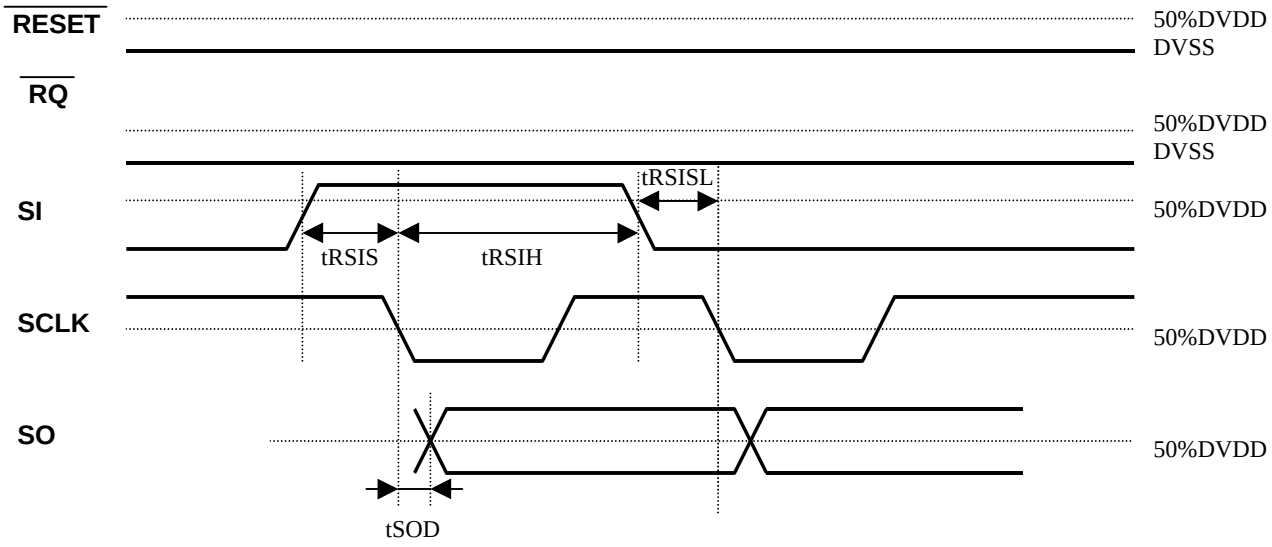
1) DBUS data in case of 24 bit data output.



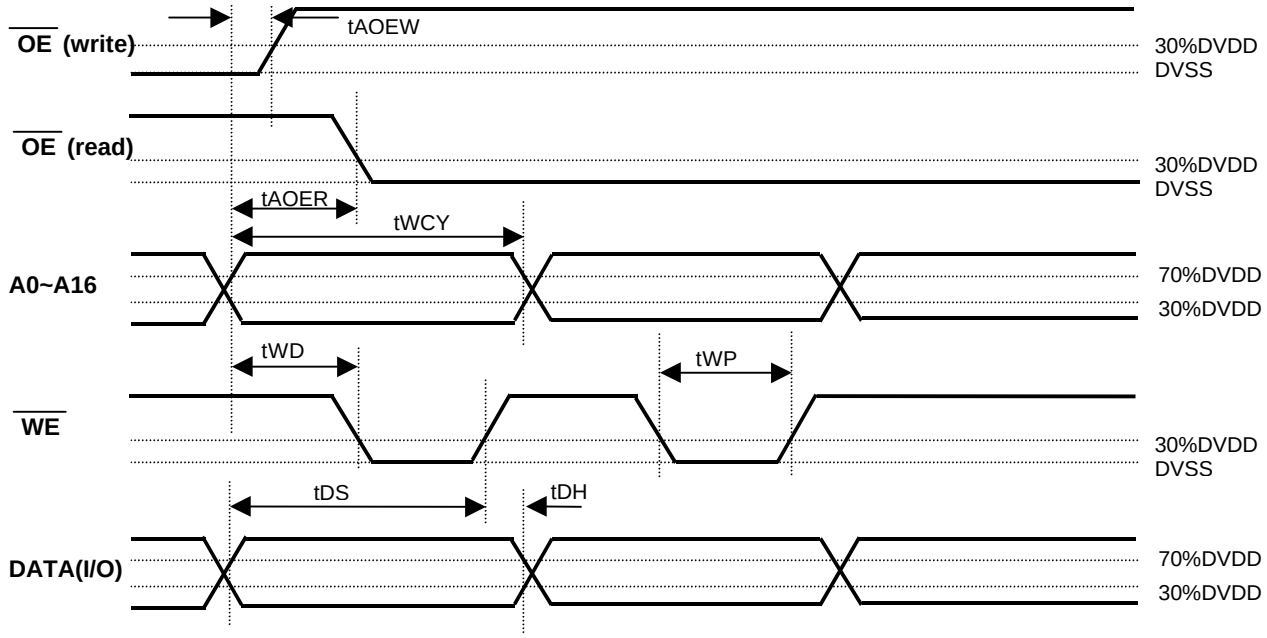
2) DBUS data less than 24 bits data output (in case of using SI)



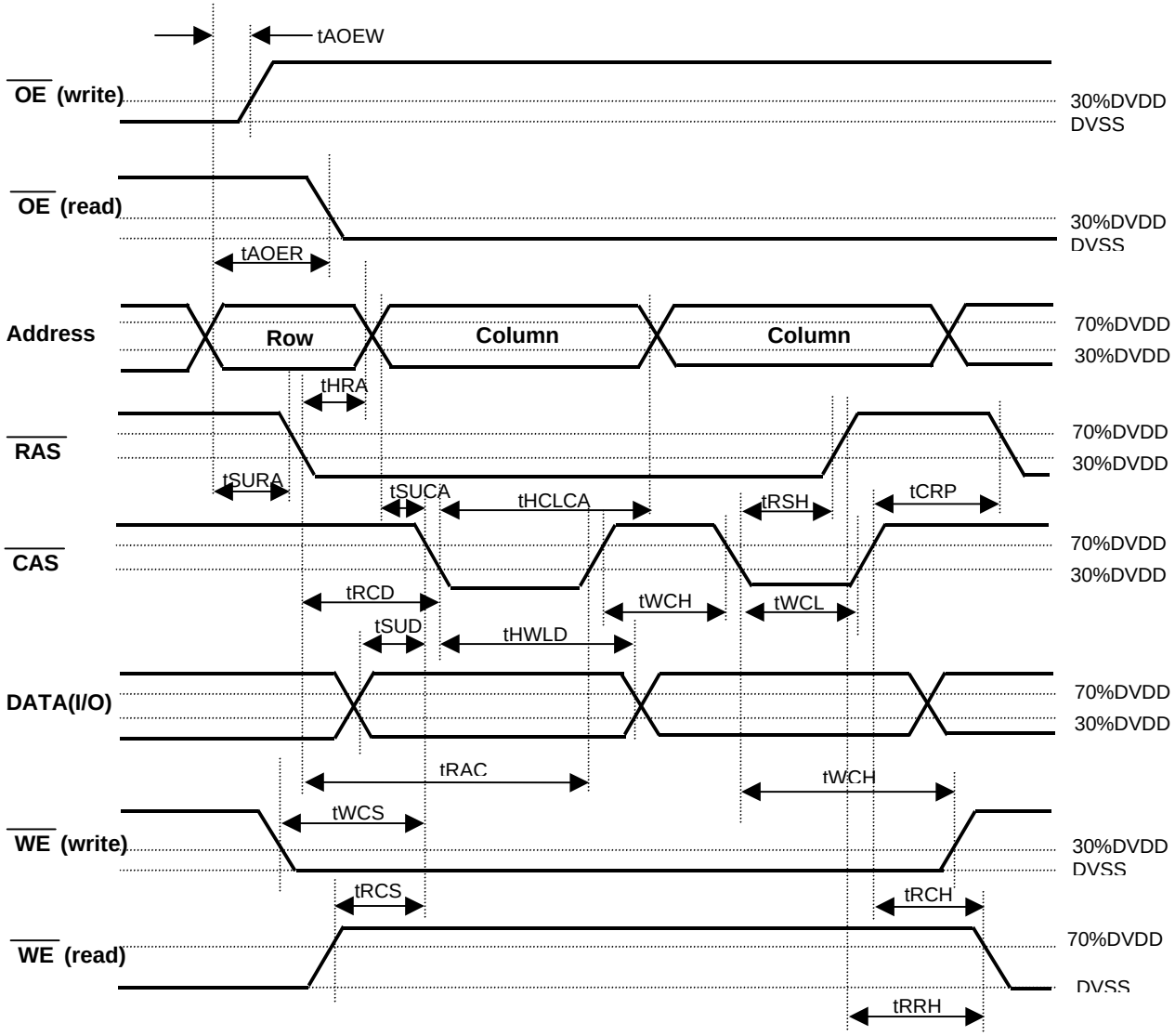
- AK7716 to Microcomputer (RAM DATA Read-out)



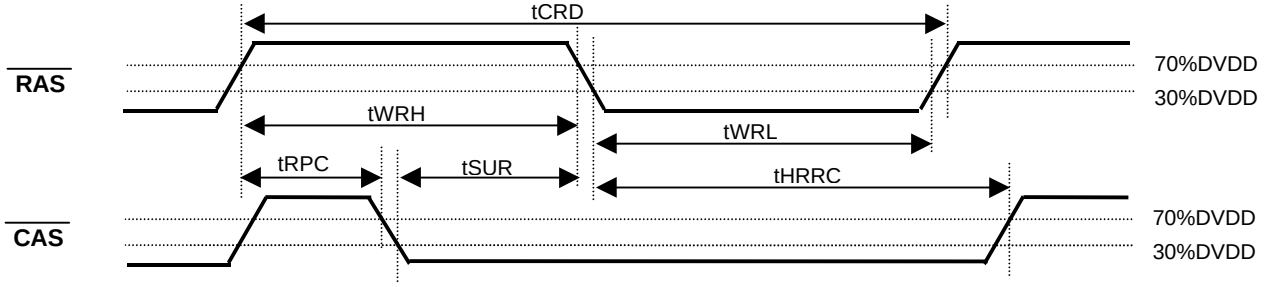
- AK7716 Read/Write Interface Timing of External SRAM



- AK7716 Read/Write Interface Timing of External DRAM



- AK7716 Refresh Interface Timing of External DRAM (CAS before RAS Refresh)



Function Description

(1) Various setting

1-1) OPCL(pin 23): ADC and DAC connection selector pin (See Block Diagram)

- Normally, OPCL is used in "L" or open. (Internal connection mode)
  In this case, ADC output and DAC1/DAC2 inputs are directly connected to the DSP internally. At this time, leave the SDINA (pin 7), SDIND1 (pin 10) and SDIND2 (pin 11) open or set to "L".
  It should be noted that "L" is output from the SDOUTA (pin 8), SDOUTD1 (pin 9) and SDOUTD2 (pin 12).
- When the OPCL is set to "H", the ADC output and DAC1/DAC2 inputs can be used independently from the DSP. (Input/output formats are restricted.)

(Note) SDINA supports only the MSB-justified 24-bit input (including I^2S compatibility).
SDOUTA supports only the MSB-justified 20-bit output (including I^2S compatibility).
SDIND1 and SDIND2 support only the MSB-justified 20-bit inputs (including I^2S compatibility).

1-2) CTRL (pin 19) : clock output control pins

CLKO will output a constant “L” or “H” by setting this pin to “L”.
When setting this pin to “H”, CLKO will output the frequency that is setting by control register.

1-3) SMODE (pin 26) : slave and master mode selector pin

Sets LRCLK (pin 17) and BITCLK (pin 18) to either inputs or outputs.
a) Slave mode :SMODE="L"
LRCLK(1fs) and BITCLK (64fs or 48fs) become inputs.
b) Master mode: SMODE="H"
LRCLK (1fs) and BITCLK (64fs). become outputs.

(2) Control registers

The control registers can be set via the microcomputer interface in addition to the control pins.
These registers are consisted by 4 parts and each register is 8-bit.
For the value to be written in the control registers see the description of the interface with microcomputer.
The following describes the control register map

TEST: for TEST (input 0,X: it ignore input data, but should input 0).

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
60h	70h	CONT0	CKS1	CKS0	DIF	DIF1	DIF0	DISCK	SELCKO	X	00h
64h	74h	CONT1	RAMCLR	RAMSEL1	RAMSEL0	PARSEL	ERAMAD	DATARAM	TEST	X	00h
68h	78h	CONT2	TEST	SF1	SF0	RSTDA2	RSTDA1	TEST	TEST	X	00h
6Ch	7Ch	CONT3	RSTAD	SW2	SW1	SW0	DISOUT2	DISOUT1	MSET	X	00h

Data can be loaded into the control registers only when $\overline{\text{DSP RESET}}$ ="L" and $\overline{\text{CODEC RESET}}$ ="L". If used otherwise, on operation error will occur. Do not attempt to change any value in the control register when $\overline{\text{DSP RESET}}$ ="H" or when $\overline{\text{CODEC RESET}}$ ="H".

CONT0 can be set only at system reset.

2-1) CONT0 : clock and interface selector

This register is enable only at system reset state ($\overline{\text{DSP\_RESET}}$ ="L", $\overline{\text{CODEC\_RESET}}$ ="L")

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
60h	70h	CONT0	CKS1	CKS0	DIF	DIF1	DIF0	DISCK	SELCKO	X	00h

① **D7,D6: Master clock selector**

Mode	D7	D6	
1	0	0	512fs
2	0	1	384fs
3	1	0	TEST mode (Don't use).
4	1	1	256fs

② **D5:DIF Audio interface selector**

0:AKM method

1: I^2S compatible (In this case, all input / output pins are I^2S compatible.)

③ D4,D3:DIF1,DIF0 SDIN1,SDIN2 Input mode selector

Mode	D4	D3	
1	0	0	MSB justified (24bit)
2	0	1	LSB justified (24bit)
3	1	0	LSB justified (20bit)
4	1	1	LSB justified (16bit)

Note) When D5= 1, the state is I^2S compatible independently of mode setting, however set to Mode 1.

④ **D2:DISCK LRCLK,BITCLKOutput control**

0: Normal Operation

1: This setting can fix BITCLK="L" and LRCLK="H" at master mode.

(Note In case of I^2S compatible setting, it become LRCLK="L".)

This setting is available only for use the AK7716 analog input and analog output.

⑤ **D1:SELCKO CLKO Output selector.**

0:CLKO outputs the same frequency as XTI.

1:CLKO outputs 1/2 frequency of XTI.

Note) In the case of select 1, after setting CONT0 (when the last clock of SCLK rise up) CLKO will change its frequency. So, the click noise comes out at this change.

Until $\overline{\text{INIT\_RESET}}$ changes to "L" or changes control register, the output frequency does not change.

Phase matching between CLKO and XTI is done at $\overline{\text{INIT\_RESET}}$ ="L".

⑥ **D0: Always 0**

Note) Underlines of the setting of ①~⑥mean default setting.

2-2) CONT1: RAM control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
64h	74h	CONT1	RAMCLR	RAMSEL1	RAMSEL0	PARSEL	ERAMAD	DATARAM	TEST	X	00h

① **D7:RAMCLR Data reset and clear functions after RESET relese.**
0:Use (Normal setting)
1:Not use (for testing)

Normally, select 0. After release of system RESET ($\overline{\text{DSP RESET}}$ ="L", $\overline{\text{CODEC RESET}}$ ="L"), internal counter begins to start and it will issue a reset pulse near the rising point of 1fs clock (normally it is inverted LRCK phase).
In case of master mode, it is the rising point of the first LRCLK. In case of slave mode, it is 3rd LRCLK after release of the system RESET.
After the internal control circuit issues a reset pulse, the AK7716 will write all 0 data into all-internal RAM and external RAM. It takes 12,500LRCLK(max) whatever external RAM selected. (LRCLK = 1/fs, fs=44.1kHz : 283ms , fs=48kHz : 260ms)

② **D6,D5:RAMSEL1,RAMSEL2 External RAM type selector.**

Mode	D6	D5	
1	0	0	SRAM 1Mbit
2	0	1	DRAM 1Mbit
3	1	0	DRAM 4Mbit
4	1	1	DRAM 16Mbit

③ **D4:PARASEL Parallel output selector**
0:Normal operation
1:Test mode
In the case of setting PARASEL=1, DBUS(Data bus) data outputs 24-bit to A16~A1 and IO7~IO0 (MSB first).

④ **D3:ERAMAD External RAM addressing mode selector**
0:Ring addressing mode
1:Linear addressing mode

⑤ **D2:DATARAM DATARAM addressing mode selector**
0:Ring addressing mode
1:Linear addressing mode
DATARAM has 256-word x 24-bit and has 2 addressing pointer (DP0, DP1).
The Ring addressing mode: Its start address increments 1 by every sampling time.
The Linear addressing mode: Its start address is always same, DP0 = 00h and DP1 = 80h.

⑥ **D1:TEST**
0:Normal operation. (Use at 0)
1: TEST mode.
This is an internal test mode and should not be used, please set this value to "0".

⑦ **D0: Input always 0**

Note) Underlines of the setting of ①~⑥ mean default setting.

2-3) CONT2 : DA control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
68h	78h	CONT2	TEST	SF1	SF0	RSTDA2	RSTDA1	TEST	TEST	X	00h

① **D7:TEST**
0:Normal operation (Use at 0)
1:TEST mode
This is an internal test mode and should not be used, please set this value to "0".

② **D6,D5:SF1,SF0 Soft-mute cycle time setting (Default : D6=D5="0")**

Mode	D6	D5	
1	0	0	1016LRCLK cycle
2	0	1	-
3	1	0	508 LRCLK cycle
4	1	1	2032 LRCLK cycle

③ **D4:RSTDA2 DA2 Reset control**
0:Normal operation
1:DA2 Reset

In the case of not using DA2, set this value to "1" and DA2 will RESET.
This can be useful for saving power consumption.
The output signals of AOUTL2+, AOUTL2-, AOUTR2+ and AOUTR2- pins will be AVDD/2.
When changing to normal operation, set this value to "0" at system reset.

④ **D3:RSTDA1 DA1 Reset control**
0:Normal operation
1:DA1 Reset

In the case of not using DA1, set this value to "1" and DA1 will be in RESET.
This can be useful for saving power consumption.
The output signals of AOUTL1+, AOUTL1-, AOUTR1+ and AOUTR1- pins will be AVDD/2.
When changing to normal operation, set this value to "0" at system reset.

⑤ **D2:TEST**
0:Normal operation (Use at 0)
1:TEST mode
This is an internal test mode and should not be used, please set this value to "0".

⑥ **D1:TEST**
0:Normal operation (Use at 0)
1:TEST mode
This is an internal test mode and should not be used, please set this value to "0".

⑦ **D0: Always input 0**

Note) Underlines of the setting of ①~⑥ mean default setting.

2-4) CONT3: Other control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
6Ch	7Ch	CONT3	RSTAD	SW2	SW1	SW0	DISOUT2	DISOUT1	MSET	X	00h

① **D7:RSTAD**

0:Normal operation

1:ADC Reset

In the case of not using ADC, set this value to "1" and ADC will be in RESET.
This can be useful for saving power consumption.
The digital output signals of ADC will 00000h.
When changing to normal operation, set this value to "0" at system reset.

② **D6,D5:SW2,SW1 internal path setting**

D6	D5	
0	0	Normal opration

③ **D4:SW0 internal path selector**

0:Normal operation

1:SDINA select

In the case of internal connection (OPCL="L") and set this D4 to "1", the SDINA path will connect to DSP directly.
(Its format is MSB justified 24-bit, or in the case of setting I^2S then I^2S)
If this setting selected, ADC can not use, so D7 should be set to "1".

④ **D3:DISOUT2 SDOUT2 Disable**

0:Normal operation

1:SDOUT2="L"

⑤ **D2:DISOUT1 SDOUT1 Disable**

0:Normal operation

1:SDOUT1="L"

⑥ **D1:MSET Random number generator circuit selector**

0:Unused

1:Used

This DSP has a single feedback type shift-register [24,21,19,18,17,16,15,14,14,19,9,5,1] s independently from calculation block.
This register changes the data in every sampling time. And its output connected with DBUS, so in case of selected MSRG command at program code, then 24-bit random data will appear in every sampling.
In the case of using this random number generator, please set D1=1.

⑦ **D0: Always input 0**

Note) Underlines of the setting of ①~⑥ mean default setting.

(3) Power supply startup sequence

Turn on the power by setting to $\overline{\text{INIT RESET}}$ = "L", $\overline{\text{DSP RESET}}$ = "L" and $\overline{\text{CODEC RESET}}$ = "L".

Then the AK7716 is initialized by setting to $\overline{\text{INIT RESET}}$ = "H". Note 1)

Initialization by $\overline{\text{INIT RESET}}$ is sufficient if it is done only when the power is turned on.

VREF become operating state and VCOM value rises to AVDD/2. The stable time depends on external capacitor.

The setting $\overline{\text{CODEC RESET}}$ to "H" should be after VCOM value is stabled to AVDD/2.

(In case of using 0.1uF and 10uF capacitors, it takes about 100msec.)

Normally, $\overline{\text{INIT\_RESET}}$ setting is only done at turn on power.

Note 1): Set to $\overline{\text{INIT RESET}}$ = "H" after setting the oscillation when a crystal oscillator is used.

This setting time may differ depending on the crystal oscillator and its external circuit.

NOTE: Do not stop the system clock (slave mode: XTI, LRCLK, BITCLK, master mode: XTI) except when $\overline{\text{INIT RESET}}$ = "L".

If these clock signals are not supplied, excess current will flow due to dynamic logic that is used internally, and an operation failure may result.

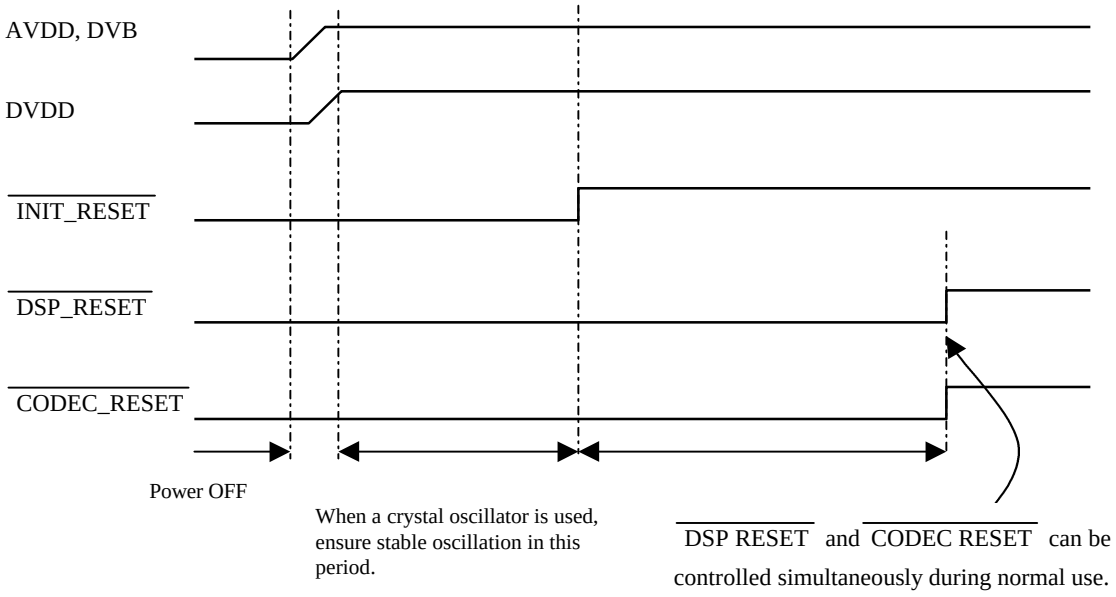


Fig. Power supply startup sequence

(4) Resetting

The AK7716 has three reset pins: $\overline{\text{INIT RESET}}$, $\overline{\text{DSP RESET}}$ and $\overline{\text{CODEC RESET}}$.

The $\overline{\text{INIT RESET}}$ pin is used to initialize the AK7716, as shown in "Power supply startup sequence section 3)."

$\overline{\text{DSP RESET}}$ and $\overline{\text{CODEC RESET}}$ are normally controlled simultaneously. The system is reset when $\overline{\text{DSP RESET}}$ = "L" and $\overline{\text{CODEC RESET}}$ = "L". (Description of "reset" is for "system reset".)

Under the condition of system reset, the program write operation is normally performed (except for write operation during running). During the system reset phase, the ADC and DAC sections are also reset. (The digital section of ADC output is MSB first 00000h and the analog section of DAC output is AVDD/2)

CLKO is output even during the system reset phase if CTRL = “L”, but LRCLK and BITCLK in the master mode will be inactive.

The system reset is released by setting either $\overline{\text{DSP RESET}}$ or $\overline{\text{CODEC RESET}}$ to "H", and this will activate the internal counter. This counter generates LRCLK and BITCLK in the master mode: however, a hazard may occur when a clock signal is generated. When the system reset is released in the slave mode, internal timing will be actuated in synchronization with "↑" of LRCLK (when the standard input format is used). Timing between the external and internal clocks is adjusted at this time. If the phase difference in LRCLK and internal timing is within about -1/16 to 1/16 of the input sampling cycle (1/fs) during the operation, the operation is performed with internal timing remaining unchanged. If the phase difference exceeds the above range, the phase is adjusted by synchronization with "↑" of LRCLK (when the standard input format is used). This is a circuit to prevent failure of synchronization with the external circuit. For some time after returning to the normal state after loss of synchronization, normal data will not be valid. If you want to change the clock, do so while the system is in reset.

The ADC section can output 516-LRCLK after its internal counter started. (The internal counter starts at the first rising edge of LRCLK at master mode. In case of slave mode, it starts end of 2LRCLK after release of system reset.)

When $\overline{\text{DSP RESET}}$ is set to “H”, the reset state is cancelled, and the external RAM clear (“0” data writes) and the internal DRAM clear are executed from the rising edge of LRCLK. This period takes 12400 * 1/fs [sec] at 512fs mode and 16540 * 1/fs [sec] at 384fs mode. (fs : sampling frequency). After this “data reset function”, the function of [7-3) Write during RUN phase] is acceptable.

The AK7716 performs normal operation when both $\overline{\text{DSP RESET}}$ and $\overline{\text{CODEC RESET}}$ are set to "H".

When $\overline{\text{INIT RESET}}$, $\overline{\text{DSP RESET}}$ or $\overline{\text{CODEC RESET}}$ changes, the status of DAC section also changes to Power down or Release mode, and it causes a click noise on the output. In this case SMUTE function is not effective, an external mute circuit in this case is necessary to avoid any click noise.

After the internal control circuit issues a reset pulse, the AK7716 will write all 0 data into all-internal RAM and external RAM. It takes 12,500LRCLK(max) whatever external RAM selected. (LRCLK = 1/fs, fs=44.1kHz : 283ms , fs=48kHz : 260ms) See.2-2)-①

(5) System clock

The required system clock is XTI (256 fs/384 fs/512 fs), LRCLK (fs) and BITCLK (64 fs) in the slave mode, and is XTI (256 fs/384 fs/512 fs) in the master mode.
LRCLK corresponds to the standard digital audio rate (32 kHz, 44.1 kHz, and 48 kHz).

Fs	XTI (Master clock)			BITCLK
	256fs	384fs	512fs	64fs
32.0kHz	Can not use	12.2880MHz	16.3840MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.576MHz	3.0720MHz

5-1) Master clock (XTI pin)

The master clock is obtained by connecting a crystal oscillator between the XTI pin and XTO pin or by inputting an external clock into the XTI pin while the XTO pin is left open.

5-2) Slave mode

The required system clock is XTI (256 fs/384 fs/512 fs), LRCLK (1 fs) and BITCLK (48/64 fs).
The master clock (XTI) and LRCLK must be synchronized, but the phase is not critical.

5-3) Master mode

The required system clock is XTI (256 fs/384 fs/512 fs). When the master clock (XTI) is input, LRCLK (1 fs) and BITCLK (64 fs) will be outputted from the internal counter synchronized with the XTI.

LRCLK and BITCLK will not be active during initial reset ($\overline{\text{INIT RESET}}$ = "L") and system reset

($\overline{\text{DSP RESET}}$ = $\overline{\text{CODEC RESET}}$ = "L").

(6) Audio data interface (internal connection mode)

The serial audio data pins SDIN1, SDIN2 and SDOUT (OPCL = L: Internal connection mode) are interfaced with the external system, using LRCLK and BITCLK. The data format is MSB-first 2's complement. Normally, the input/output format, in addition to the standard format used by AKM, can be changed to the I^2S compatible mode by setting the control register "CONT0 DIF(D4) to 1". (In this case, all input/output audio data pin interface are in the I^2S compatible mode.)

The input SDIN1 and SDIN2 formats are MSB justified 24-bit at initialization. Setting the control registers CONT0: DIF1, DIF0 will cause them to be compatible with LSB justified 24-bit, 20-bit and 16-bit.

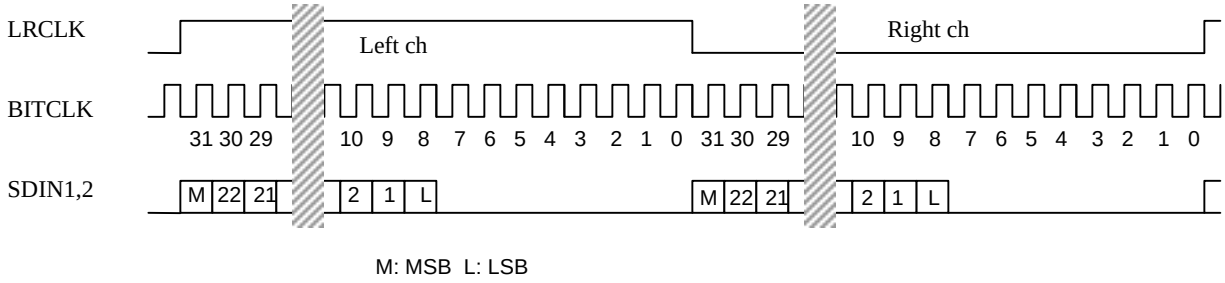
However, inidividul setting of SDIN1 and SDIN2 is not allowed.

The output SDOUT1 and SDOUT2 are fixed at 24 bits.

At slave mode BITCLK corresponds to not only 64fs but also 48fs. But, we recommend 64fs. Following formats describe 64fs examples.

6-1) Standard input format (DIF = 0: default set value)

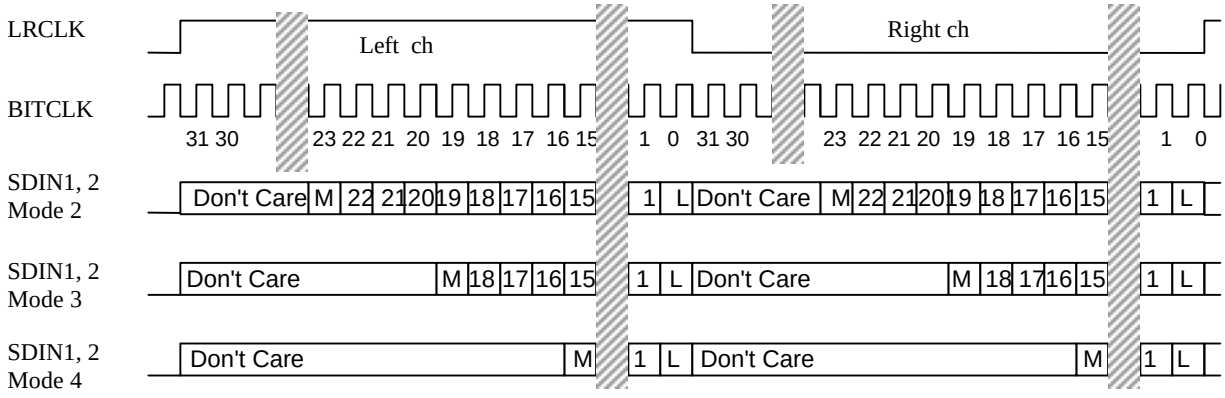
a) Mode 1 (DIF1, DIF0 = 0,0: default set value)



M: MSB L: LSB

* When you want to input the MSB-justified 20-bit data into SDIN1 and 2, input four "0s" following the LSB.

b) Mode 2, Mode 3, Mode 4



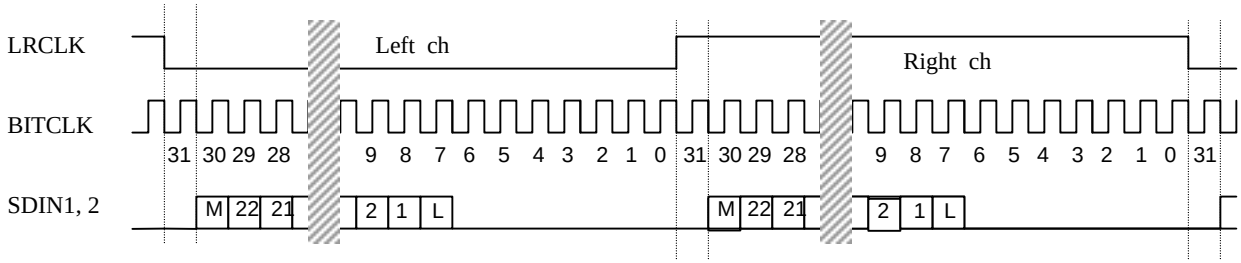
M: MSB , L : LSB

SDIN1, 2 Mode 2: (DIF1, DIF0) = (0, 1) LSB justified 24-bit

SDIN1, 2 Mode 3: (DIF1, DIF0) = (1, 0) LSB justified 20-bit.

SDIN1, 2 Mode 4: (DIF1, DIF0) = (1, 1) LSB justified 16-bit

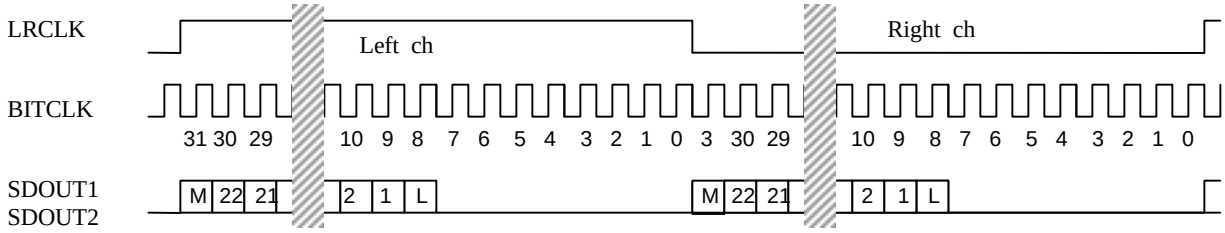
6-2) I²S compatible input format (DIF=1)



M : MSB, L : LSB

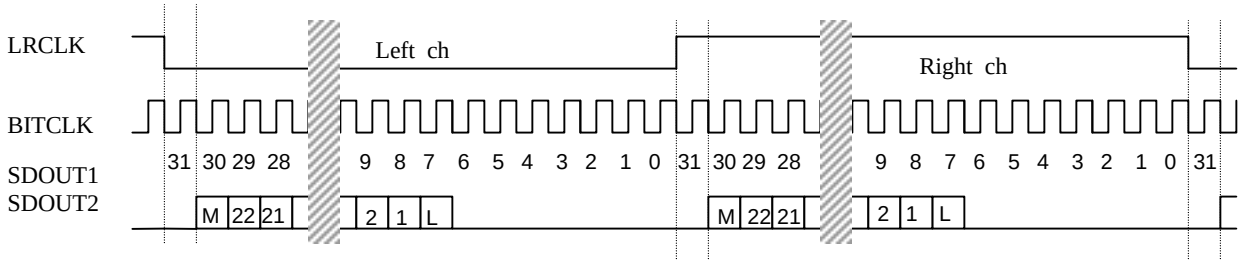
Mode 1: (DIF1, DIF0) = (0, 0) must be set.

6-3) Standard output format (DIF=0: default set value)



M : MSB, L :

6-4) I²S compatible output format (DIF=1)



M : MSB , L : LSB

(7) Interface with microcomputer

The interface to a microcomputer is provided by 6 control signals; $\overline{CS}$ (Chip Select Bar), $\overline{RQ}$ (ReQuest Bar), SCLK (Serial data input CLocK), SI (Serial data Input), SO (Serial data Output), RDY (ReaDY) and DRDY (Data ReaDY).
In the AK7716, two types of operations are provided; writing and reading during the reset phase (namely, system reset) and those during the run phase. During the reset phase, writing of the control register, program RAM, coefficient RAM, offset RAM, external conditional jump code, and reading of the program RAM, coefficient RAM and offset RAM, are enabled. During the run phase, writing of coefficient RAM, offset RAM and external conditional jump code, and reading of data on the DBUS (data bus) from the SO, are enabled.

When the AK7716 needs to transfer data to the microcomputer, it starts by $\overline{RQ}$ going "L".

The AK7716 reads SI data at the rising point of SCLK, and outputs to SO at the falling point of SCLK.
The AK7716 accepts first data as command then address data or some kinds of data input / output starts.

When $\overline{RQ}$ changes to "H", then one command is finished. So, new command requests needs to set $\overline{RQ}$ to "L" again.

When the DBUS data read, leave $\overline{RQ}$ ="H". (It does not need command code input."

When it needs to clear the output buffer (MICR), the SI pin uses for control. In this case, it is necessary to protect against a noise as SCLK.
Command code table is as follow.

Command code list

Conditions for use	Code name	Command code		Note:
		WRITE	READ	
RESET phase	CONT0	60h	70h	For the function of each bit, See the description of Control Registers.
	CONT1	64h	74h	
	CONT2	68h	78h	
	CONT3	6Ch	7Ch	
	PRAM	C0h	C1h	
	CRAM	A0h	A1h	
	OFRAM	90h	91h	
	External condition jump	C4h	-	
	Test	82h	-	Reserved for test
RUN phase	CRAM rewrite preparation	A8h	-	It needs to do before CRAM rewrite.
	CRAM rewrite	A4h	-	
	OFRAM rewrite preparation	98h	-	It needs to do before OFRAM rewite.
	OFRAM rewrite	94h	-	
	External condition jump	C4h	-	Same command as RESET

NOTE: Do not send other than the above command codes. Otherwise, operation error may occur.
If there is no communication with the microcomputer, set the SCLK to "H" and the SI to "L" for use.

7-1) Write during reset phase

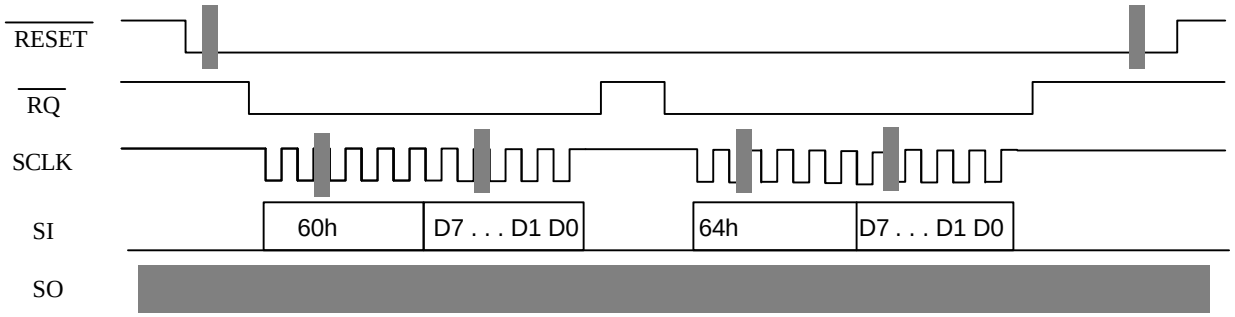
7-1-a) Control register write (during reset phase)

The data comprises a set of 2 bytes those are used to perform control register write operations (during reset phase). When all data has been entered. The new data is sent at the rising point of 16th count of SCLK.

Data transfer procedure

① Command code	60h,64h,68h,6Ch
② Control data	(D7 D6 D5 D4 D3 D2 D1 D0)

For the function of each bit, see the description of Control registers, see section 2).



Control registers write operation

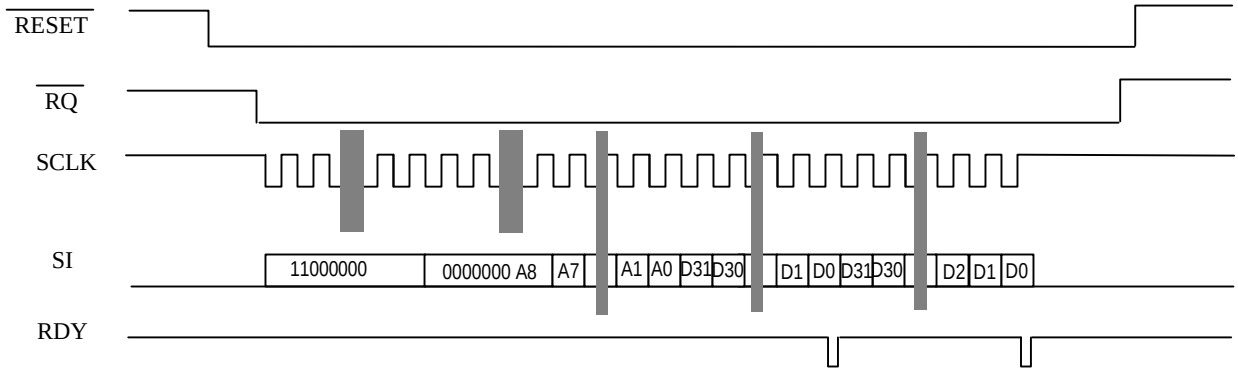
Note) It must be set always 0 to D0.

7-1-b) Program RAM write (during reset phase)

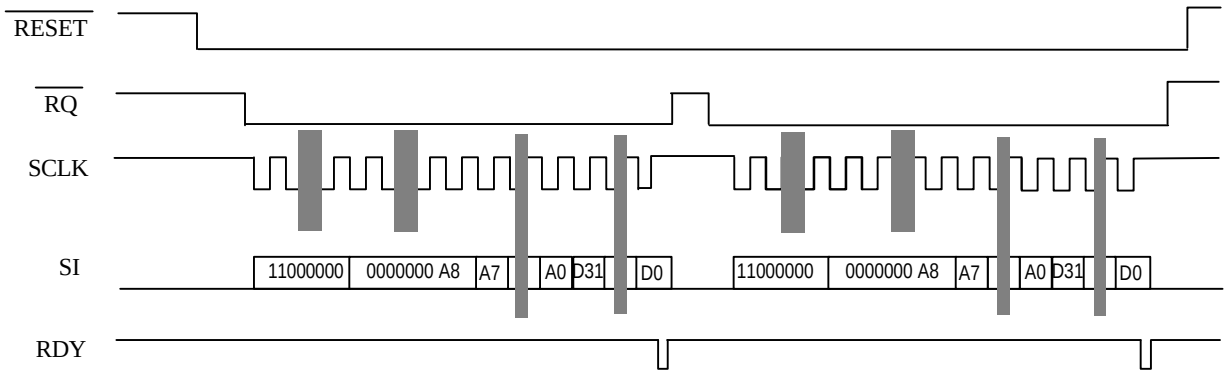
Program RAM write operation is performed during the reset phase according to the data comprising a set of 7 bytes. When all data have been transferred, the RDY terminal is set to "L". Upon completion of writing into the PRAM, RDY returns "H" to allow the next data bitinput. When data of continuous addresses are written, input the data as they are. (No command code or address is required.) To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L" again. Then input the command code, address and data in that order. (For $\overline{RESET}$, operate both $\overline{CODEC\ RESET}$ and $\overline{DSP\ RESET}$ simultaneously.)

Data transfer procedure

① Command code	C0h (1 1 0 0 0 0 0 0)
② Address upper	(0 0 0 0 0 0 0 A8)
③ Address lower	(A7 . . . . . A0)
④ Data	(D31 . . . . . D24)
⑤ Data	(D23 . . . . . D16)
⑥ Data	(D15 . . . . . D8)
⑦ Data	(D7 . . . . . D0)



Input of continuous address data into PRAM



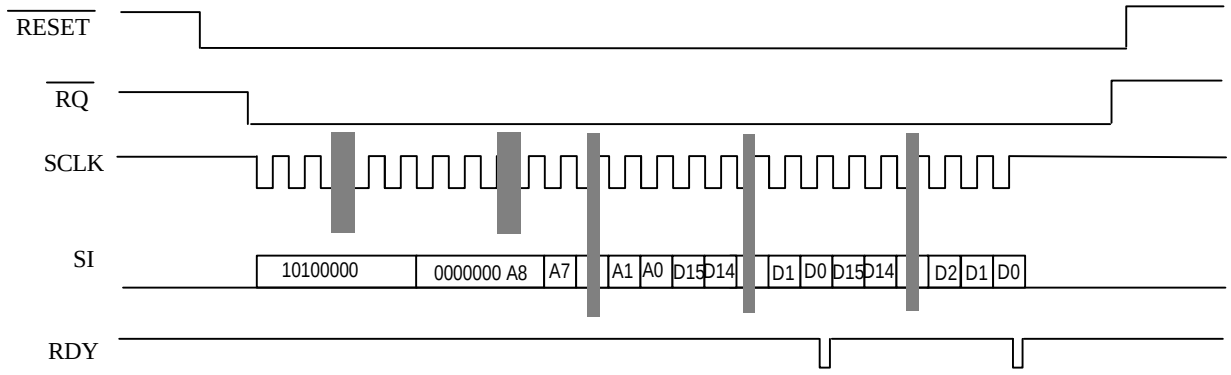
Input of discontinuous address data into PRAM

7-1-c) Coefficient RAM write (during reset phase)

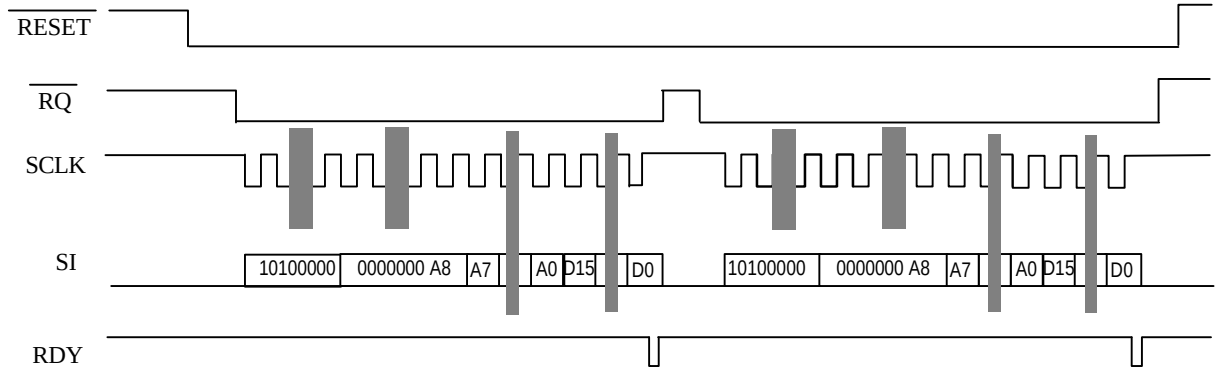
The data comprising a set of 5 bytes is used to perform coefficient RAM write operations (during reset phase). When all data has been transferred, the RDY terminal goes to "H". Upon completion of writing into the CRAM, it goes to "H" to allow the next data to be inputed. When data of continuous addresses are written, input the data as they are. To write discontinuous data, shift the $\overline{\text{RQ}}$ terminal from "H" to "L". Then input the command code, address and data in that order.
(For $\overline{\text{RESET}}$, operate both $\overline{\text{CODEC RESET}}$ and $\overline{\text{DSP RESET}}$ Simultaneously.)

Data transfer procedure

① Command code	A0h (1 0 1 0 0 0 0 0)
② Address upper	(0 0 0 0 0 0 0 A8)
③ Address lower	(A7 . . . . . A0)
④ Data	(D15 . . . . . D8)
⑤ Data	(D7 . . . . . D0)



Input of continuous address data into CRAM



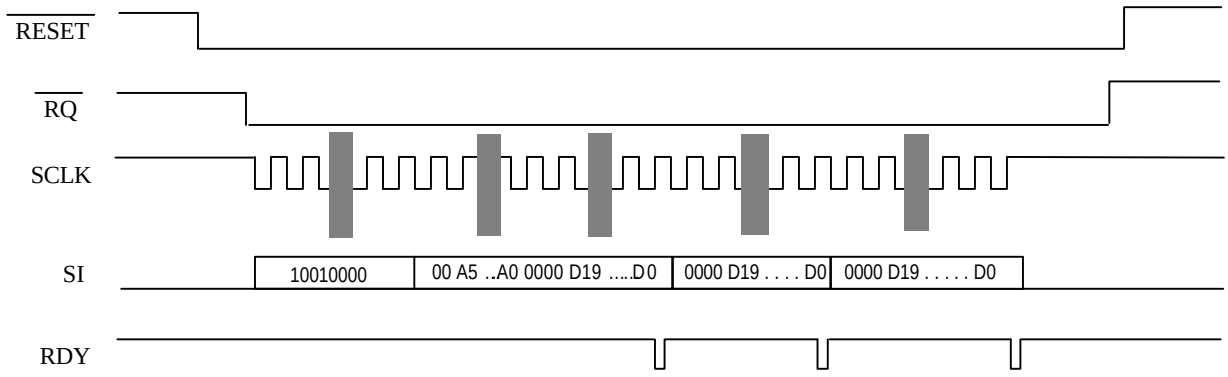
Input of discontinuous address data into CRAM

7-1-d) Offset RAM write (during reset phase)

The data comprising a set of 5 bytes is used to perform offset RAM write operations (during reset phase). When all data has been transferred, the RDY terminal goes to "H". Upon completion of writing into the OFRAM, it goes to "H" to allow the next data to be input. When data of continuous addresses are written, input the data as they are. To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L". Then input the command code, address and data in that order.
(For $\overline{RESET}$, operate both $\overline{CODEC\ RESET}$ and $\overline{DSP\ RESET}$ Simultaneously.)

Data transfer procedure

① Command code	90h	(1 0 0 0 1 0 0 0 0)
② Address		(0 0 A5 A4 . . . . A0)
③ Data		(0 0 0 0 D19 . . . D16)
④ Data		(D15 . . . . . D8)
⑤ Data		(D7 . . . . . D0)

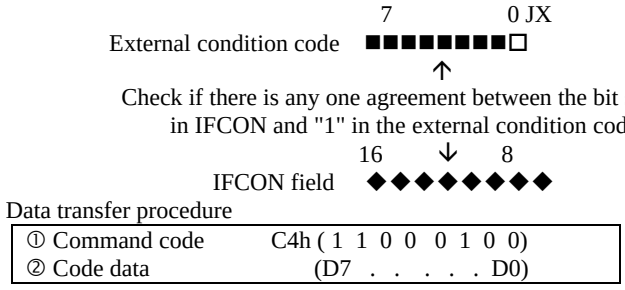


Input of data into OFRAM

7-1-e) External conditional jump code write (during reset phase)

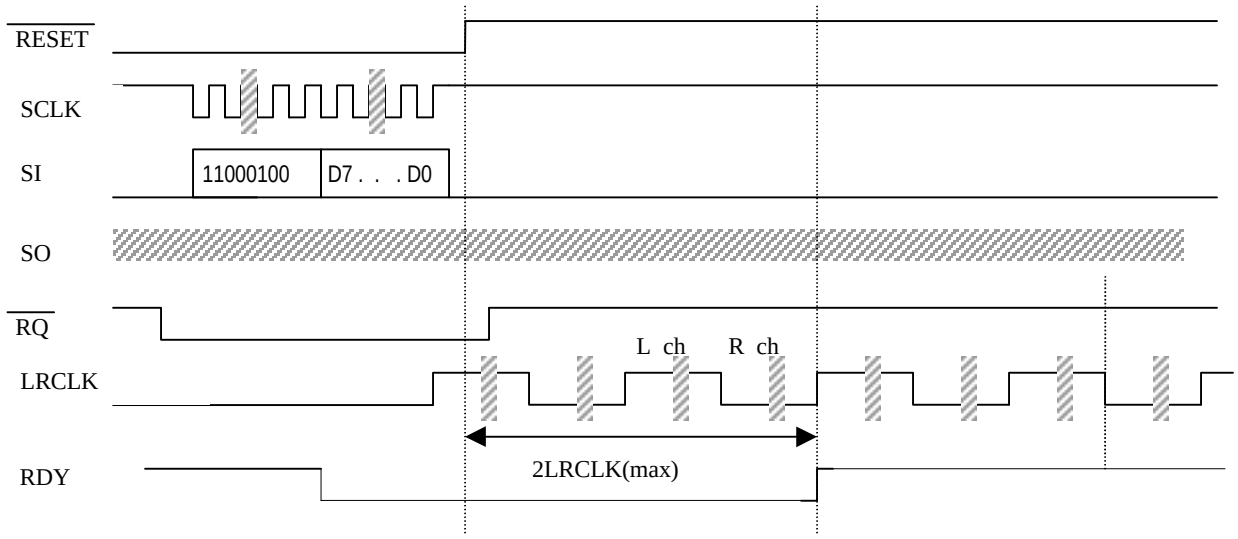
The data comprising a set of two bytes is used to perform an external conditional jump code write operation. The data can be inputed during both the reset and operation phases, and the input data are set to the specified register at the leading edge of the LRCLK. When all data bits have been transferred, the RDY terminal goes to "L". Upon completion of writing, it goes to "H". A jump command will be executed if there is any one agreement between "1" of each bit of external condition code 8 bits (soft set) plus 1 bit (hard set) at the external input terminal JX and "1" of each bit of the IFCON field. The data during the reset phase can be written only before release of the reset, after all data has been transferred. $\overline{RQ}$ Transition from "L" to "H" in the write operation during the reset phase must be execured after three LRCLK in the slave mode, one LRCLK in master mode, respectively, from the trailing edge of the LRCLK after release of the reset. Then the RDY goes to "H" after capturing the rise of the next LRCLK. A write operation from the microcomputer is disabled until the RDY goes to "H". The IFCON field provides external conditions written on the program.

Note: It should be noted that the LRCLK phase is inverted in the I2S-compatible state.



Data transfer procedure

① Command code	C4h (1 1 0 0 0 1 0 0)
② Code data	(D7 . . . . . D0)



Timing for external conditional jump write operation (during reset phase)

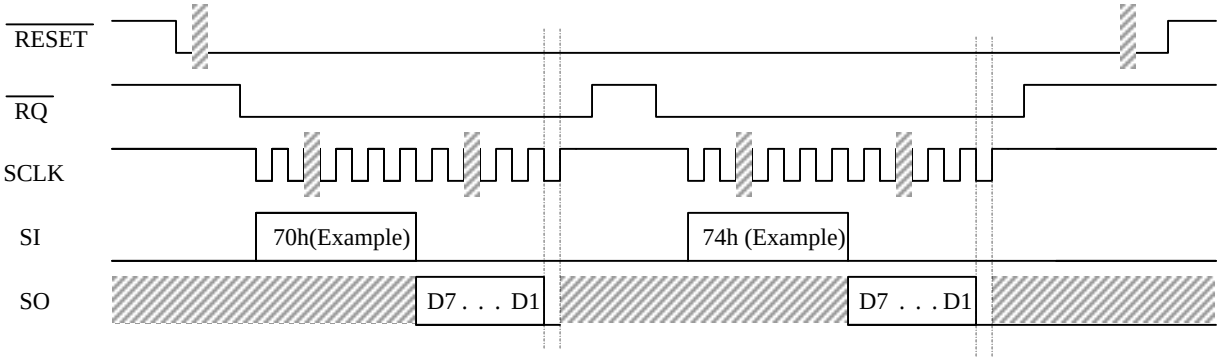
7-2) Read during reset phase

7-2-a) Control register data read (during reset phase)

To read data written into the control registers, input the command code and 16 bits of SCLK. After input command code, the data of D7 to D1 outputs from SO in synchronization with the falling edge of SCLK. D0 is invalid, so please ignore this bit.

Data transfer procedure

① Command code 70h,74h,78h,7Ch



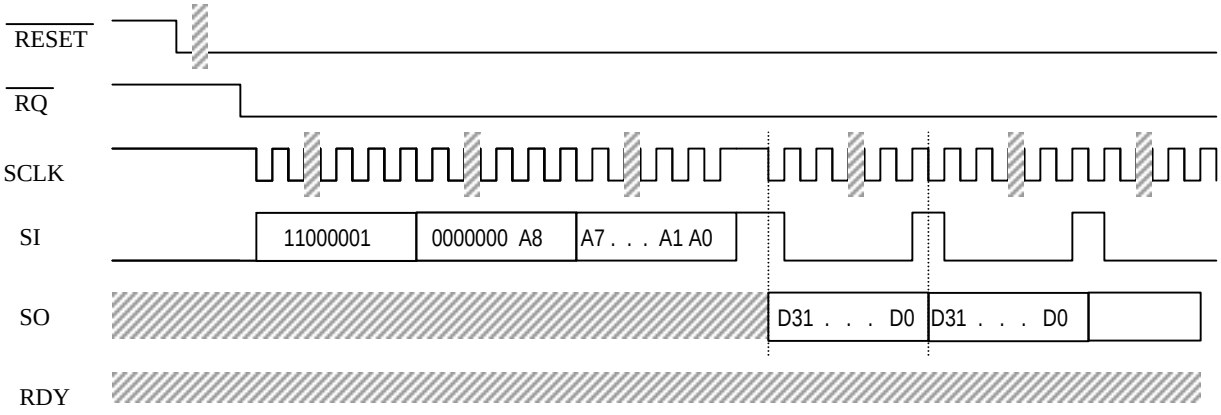
Reading of Control Register data

7-2-b) Program RAM read (during reset phase)

To read data written into PRAM, input the command code and the address you want to read out. After that, set SI to "H" and SCLK to "L". Then the data is clocked out from SO in synchronization with the falling edge of SCLK. (Ignore the RDY operation that will occur in this case.)
If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

Data transfer procedure

①Command code input C1h (1 1 0 0 0 0 0 1)
②Read address input (0 0 0 0 0 0 0 A8)
(A7 . . . . A0)



Reading of PRAM data

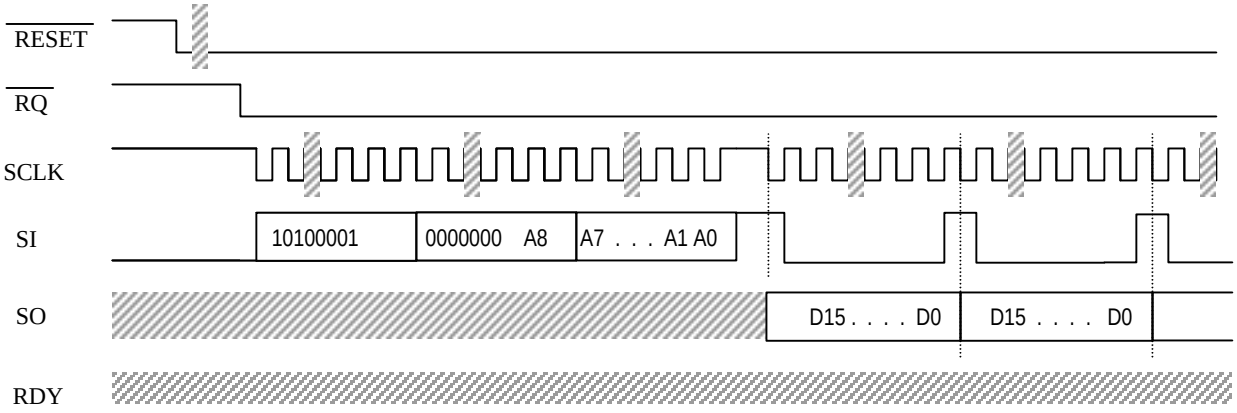
7-2-c) CRAM data read (during reset phase)

To read out the written coefficient data, input the command code and the address you want to read out. After that, set SI to "H" and SCLK to "L". Then, the data is clocked out from SO in synchronization with the falling edge of SCLK.
If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

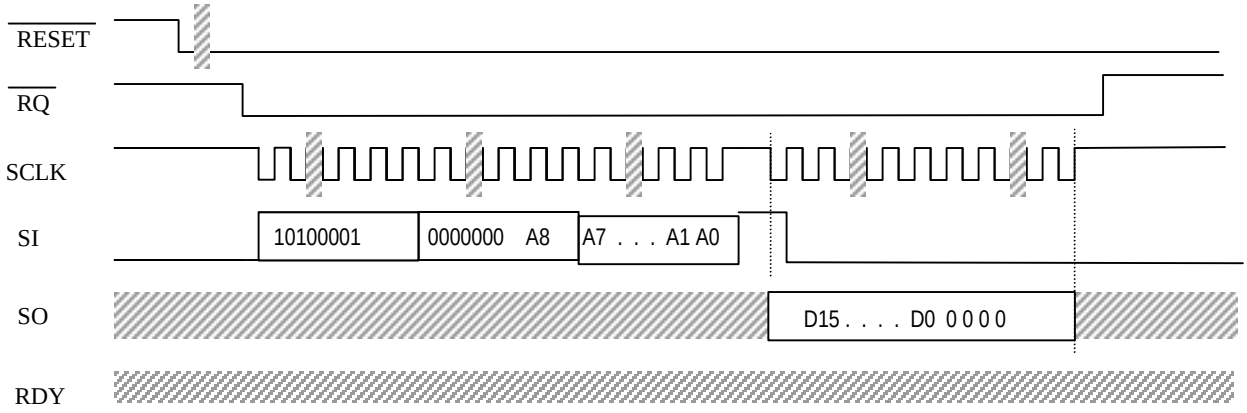
Note: This method should be read more than two data.
But, if it needs to read only one data, then it should be input more than 20-bit SCLK and ignore LSB 4-bit.

Data transfer procedure

① Command code A1h	(1 0 1 0 0 0 0 1)
② Address upper	(0 . . . . . A8)
③ Address lower	(A7 . . . . . A0)



Reading of CRAM data(more than 2 data)



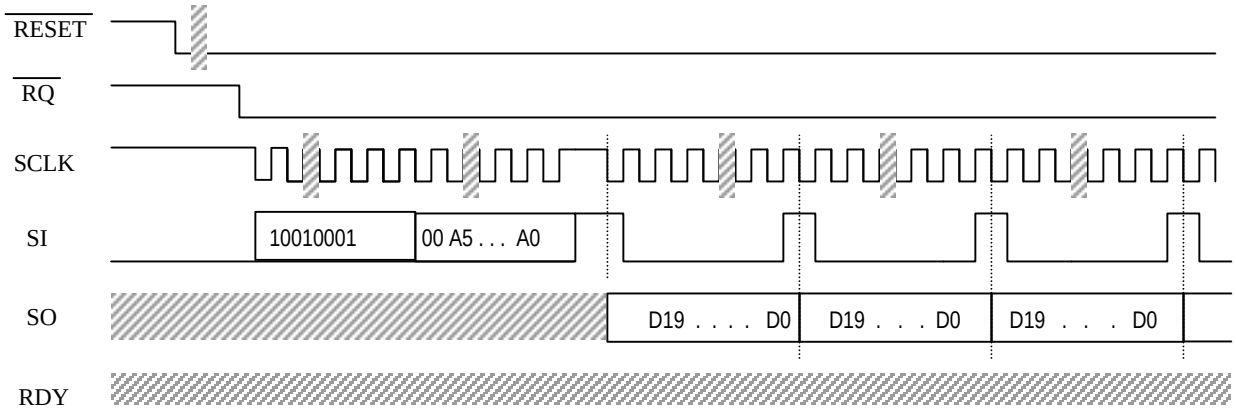
Reading of CRAM data (1 data only)

7-2-d) OFRAM data read (during reset phase)

The written offset data can be read out during the reset phase. To read it, input the command code and the address you want to read. After that, set SI to "H" and SCLK to "L". This completes preparation for outputting the data. Then set SI to "L", and the data is clocked out in synchronization with the falling edge of SCLK. If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to “H”.

Data transfer procedure

① Command code	91h (1 0 0 0 1 0 0 0 1)
② Address	(0 0 A5 . . . . A0)



Reading of OFRAM data

7-3) Write during RUN phase

7-3-a) CRAM rewrite preparation and write (during RUN phase)

This function is used to rewrite CRAM (coefficient RAM) during the program execution. After inputting the command code, you can input a maximum of 16 data bytes of a continuous address you want to rewrite.
Then input the write command code and rewrite the leading address. Every time the RAM address to be rewritten is specified, the contents of RAM are rewritten. The following is an example to show how five data bytes from address "10" of the coefficient RAM are rewritten:

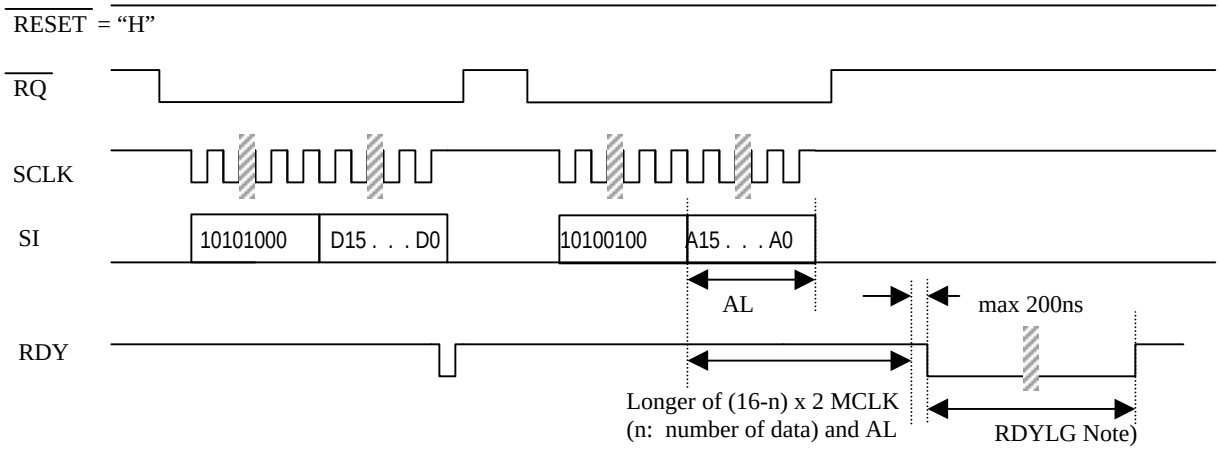
Coefficient RAM execution address 7 8 9 10 11 13 16 11 12 13 14 15

Rewrite position

Note that address "13" is not executed until address "12" is rewritten.

Data transfer procedure

* Preparation for rewrite	① Command code	A8h (1 0 1 0 1 0 0 0)
	② Data	(D15 . . . . D8)
	③ Data	(D7 . . . . . D0)
* Rewrite	① Command code	A4h (1 0 1 0 0 1 0 0)
	② Address upper	(0 0 0 0 0 0 0 A8)
	③ Address lower	(A7 . . . . A0)



Note: The RDY signal will go to high within the maximum of two LRCLKs if the RDYLG width is programmed to ensure a new address to be rewritten within one sampling cycle.

CRAM rewriting preparation and writing

7-3-b) OFRAM rewrite preparation and write (during RUN phase)

This function is used to rewrite OFRAM (offset RAM) during program execution. After inputting the command code, you can input a maximum of 16 data bytes of a continuous address you want to rewrite.
Then input the write command code and rewrite the leading address. Every time the RAM address to be rewritten is specified, the contents of RAM are rewritten. The following is an example to show how five data bytes from address "10" of the coefficient RAM are rewritten:

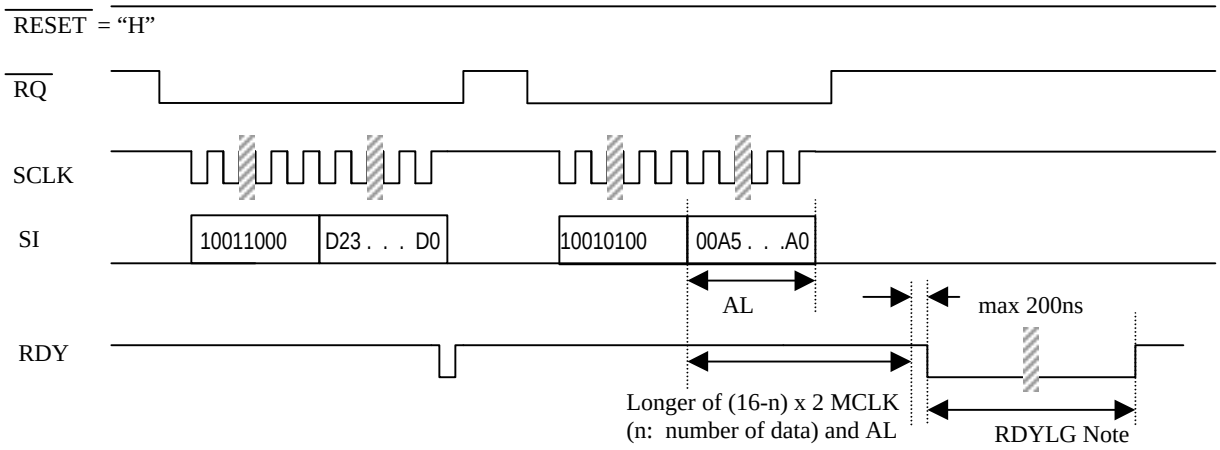
Offset RAM execution address 7 8 9 10 11 13 16 11 12 13 14 15

Rewrite position ↓ ↓ ↑ ↓ ↓ ↓

Note that address "13" is not executed until address "12" is rewritten.

Data transfer procedure

* Preparation for rewrite	① Command code	98h (1 0 0 0 1 1 0 0 0)
	② Data	(D23 . . . . . D16)
	③ Data	(D15 . . . . . D8)
	④ Data	(D7 . . . . . D0)
* Rewrite	① Command code	94h (1 0 0 0 1 0 1 0 0)
	② Address	(0 0 A5A4 . . . A0)



Note: The RDY signal will go to high within the maximum of two LRCLKs if the RDYLG width is programmed to ensure a new address to be rewritten within one sampling cycle.

OFRAM rewriting preparation and writing

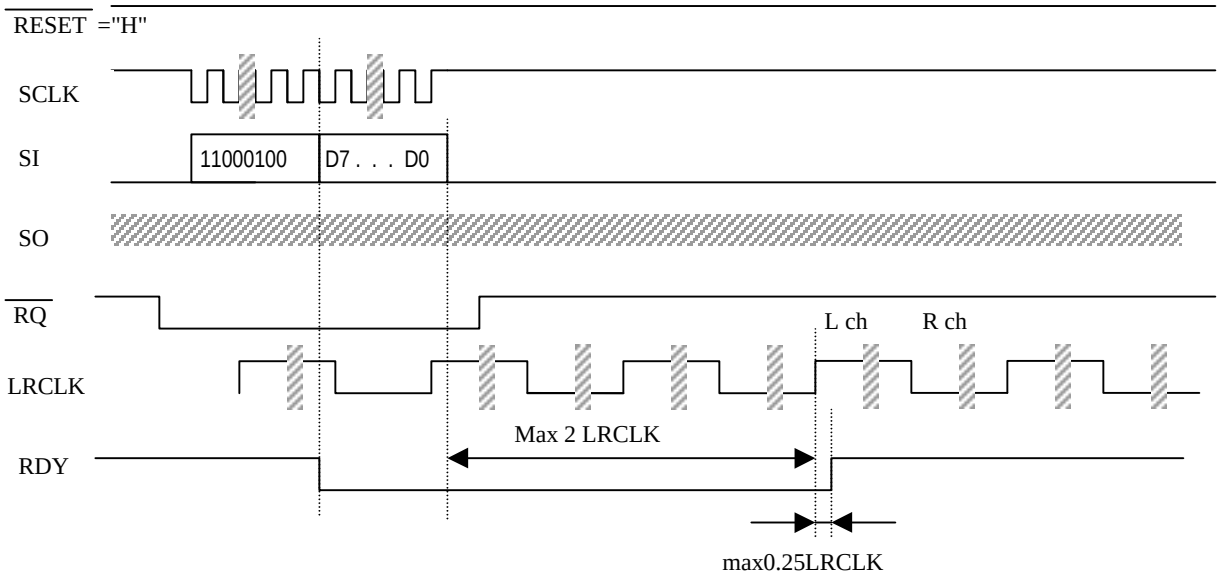
7-3-c) External conditional jump code rewrite (during RUN phase)

Data comprising a set of two bytes is used to write the external conditional jump code. Data can be input during both the reset and operation phases, and input data is set to the specified register at the rising edge of LRCLK. When all data has been transferred, the RDY terminal goes to "L". Upon completion of writing, it goes to "H". A jump command will be executed if there is any one agreement between each bit of the 8-bit external condition code and "1"of each bit of the IFCON field. A write operation from the microcomputer is disabled until RDY goes to "H".

Note: The LRCLK phase is inverted in the I2S-compatible state.

Data transfer procedure

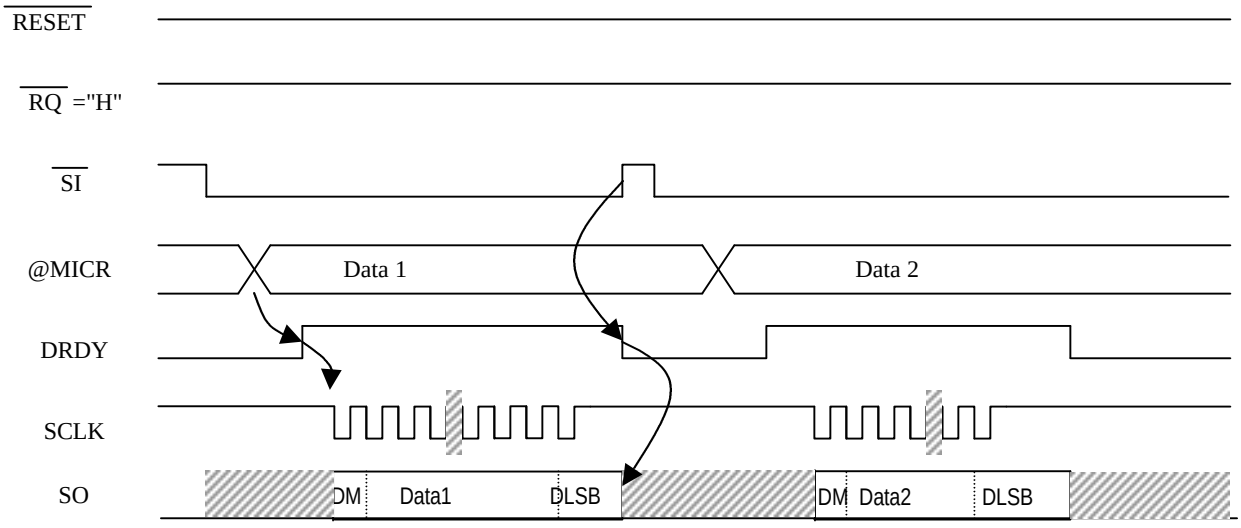
① Command code	C4h (1 1 0 0 0 1 0 0)
② Code data	(D7 . . . . . D0)



External condition jump write timing (during RUN phase)

7-4) Read-out during RUN phase (SO output)

SO outputs data on DBUS (data bus) of the DSP section. Data is set when @MICR the DST field specifies. Setting of data allows DRDY to go to "H", and data is output synchronized with the falling edge of SCLK. When $\overline{CS}$ goes to "H", DRDY goes to "L" to wait for the next command. Once DRDY goes to "H", the data of the last @MICR command immediately before DRDY goes to "H" will be held until $\overline{CS}$ goes to "H", and subsequent commands will be rejected.
A maximum of 24 bits are output from SO. After the required number of data (not exceeding 24 bits) is taken out by SCLK, the next data can be output by setting $\overline{CS}$ to "H".



SO read (during RUN phase)

(8) Interface for the EEPROM

8-1) How to use

AK7716 has an interface for the EEPROM. After release of I $\overline{\text{INIT\_RESET}}$. It can load the data of PRAM, CRAM, OFRAM and its control register setting value automatically. This function can save the memory area of microcomputer.

The proper EEPROM is the AKM AK93C95A or compatible serial one.

In case of using this function, it should write a data as 8-2) PROGRAM MAP for EEPROM.

How to use this function is as follow;

At first sets the EESEL to ”H”, (after crystal oscillator start, in case of using crystal), then $\overline{\text{INIT\_RESET}}$ pin sets to ”H”.

By this action, the internal counter starts to work and the AK7716 generate the control signal EECS, EESK and EEDI for EEPROM. Then the AK7716 is loaded the data from EEDO pin of the EEPROM. When finishes all data reading, then EECS, EESK and EEDI pins change to ”L” and EEST pin (the status pin of EEPROM interface) changes to H” and notice the finish of loading.

After EEST changes from “L” to “H”, the microcomputer interface pin is able to use even if EESEL leaving “H”.

In case of RELOAD again, leave EEST “H” and control the initial reset pin. (After sets $\overline{\text{INIT\_RESET}}$ to L” then sets $\overline{\text{INIT\_RESET}}$ to ”H” again.)

8-2) PROGRAM MAP for EEPROM

Write the data from address of 0 to 1360 (decimal) as following table.

EEPROM ADDRESS	Directed of the AK7716 parts	Contents of DATA	
		Upper 8bit	Lower 8bit
0	PRAM	00000000b	C0h (Command code)
1		0000000000000000b	
2		DATA(MSB,30,. . .,17,16)b ADDRESS 0	
3		DATA(15,14, . . . ,1,LSB)b ADDRESS 0	
. . .		. . .	
896		DATA(MSB,30, . . . ,17,16)b ADDRESS 447	
897		DATA(15,14, . . . ,1,LSB)b ADDRESS 447	
898	CRAM	00000000b	A0h (Command code)
899		0000000000000000b	
900		DATA(MSB,14, . . . ,1,LSB)b ADDRESS 0	
901		DATA(MSB,14, . . . ,1,LSB)b ADDRESS 1	
. . .		. . .	
1282		DATA(MSB,14, . . . ,1,LSB)b ADDRESS 382	
1283		DATA(MSB,14, . . . ,1,LSB)b ADDRESS 383	
1284	OFRAM	90h (Command code)	00000000b
1285		0000,DATA(MSB,18, . . . ,9,8	
1286		7,6, . . . ,1,LSB)b ADD 0	0000,DATA(MSB,18,17,16
1287		15,14, . . . ,1,LSB)b ADDRESS 1	
. . .		. . .	
1354		0000,DATA(MSB,18, . . . ,9,8	
1355		7,6, . . . ,1,LSB)b ADD 46	0000,DATA(MSB,18,17,16
1356		15,14, . . . ,1,LSB)b ADDRESS 47	
1357	CONT0	60h (Command code)	DATA(MSB,6,. . . ,1,LSB)b
1358	CONT1	64h (Command code)	DATA(MSB,6,. . . ,1,LSB)b
1359	CONT2	68h (Command code)	DATA(MSB,6,. . . ,1,LSB)b
1360	CONT3	6Ch (Command code)	DATA(MSB,6,. . . ,1,LSB)b

Note) Write 0 data for the address does not use.

(9) ADC section high-pass filter

The AK7716 incorporates a digital high-pass filter (HPF) for cancelling the section DC offset in the ADC section. The HPF cut-off frequency is about 1 Hz (fs = 48 kHz). This cut-off frequency is proportional to the sampling frequency (fs).

	48kHz	44.1kHz	32kHz
Cut-off frequency	0.93Hz	0.86Hz	0.62Hz

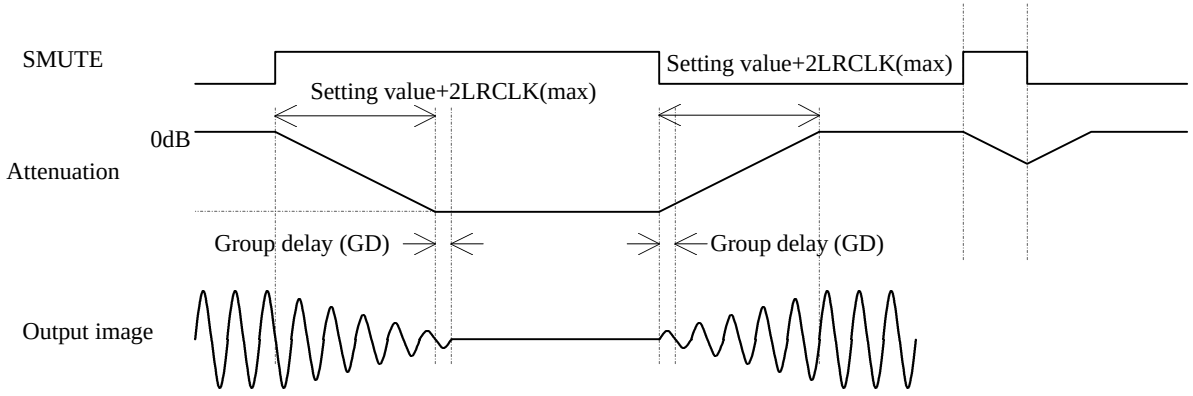
(10) Soft mute operation of DAC section

Soft mute operation is performed at digital domain of DAC section. This works both DAC1 and DAC2. When SMUTE goes to "H", the signal is attenuated by -∞ during the time that is set by control registers SF1 (D6) and SF0 (D5) of CONT2 + 2LRCLK(max) cycles. (When SF1=0,SF0=0 then its attenuation time is 1016(min) to 1018(max) LRCLK.)

When SMUTE is returned to "L", the mute is cancelled and output attenuation gradually changes to 0dB during the time that is set by control registers. If the soft mute is cancelled within the setting time after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is enable at $\overline{\text{CODEC\_RESET}}$ is "H". (DAC section during RUN phase).

After attenuated to -∞(0), it may make a click noise when the release operation of system reset ($\overline{\text{CODEC\_RESET}}$ ="L" and $\overline{\text{DSP\_RESET}}$ ="L") or CODEC reset ($\overline{\text{CODEC\_RESET}}$ ="L"). Because the DAC sections change to reset phase.

However, the attenuation value does not initialize by $\overline{\text{CODEC\_RESET}}$ or $\overline{\text{DSP\_RESET}}$. Only $\overline{\text{INIT\_RESET}}$ can initialize this value.



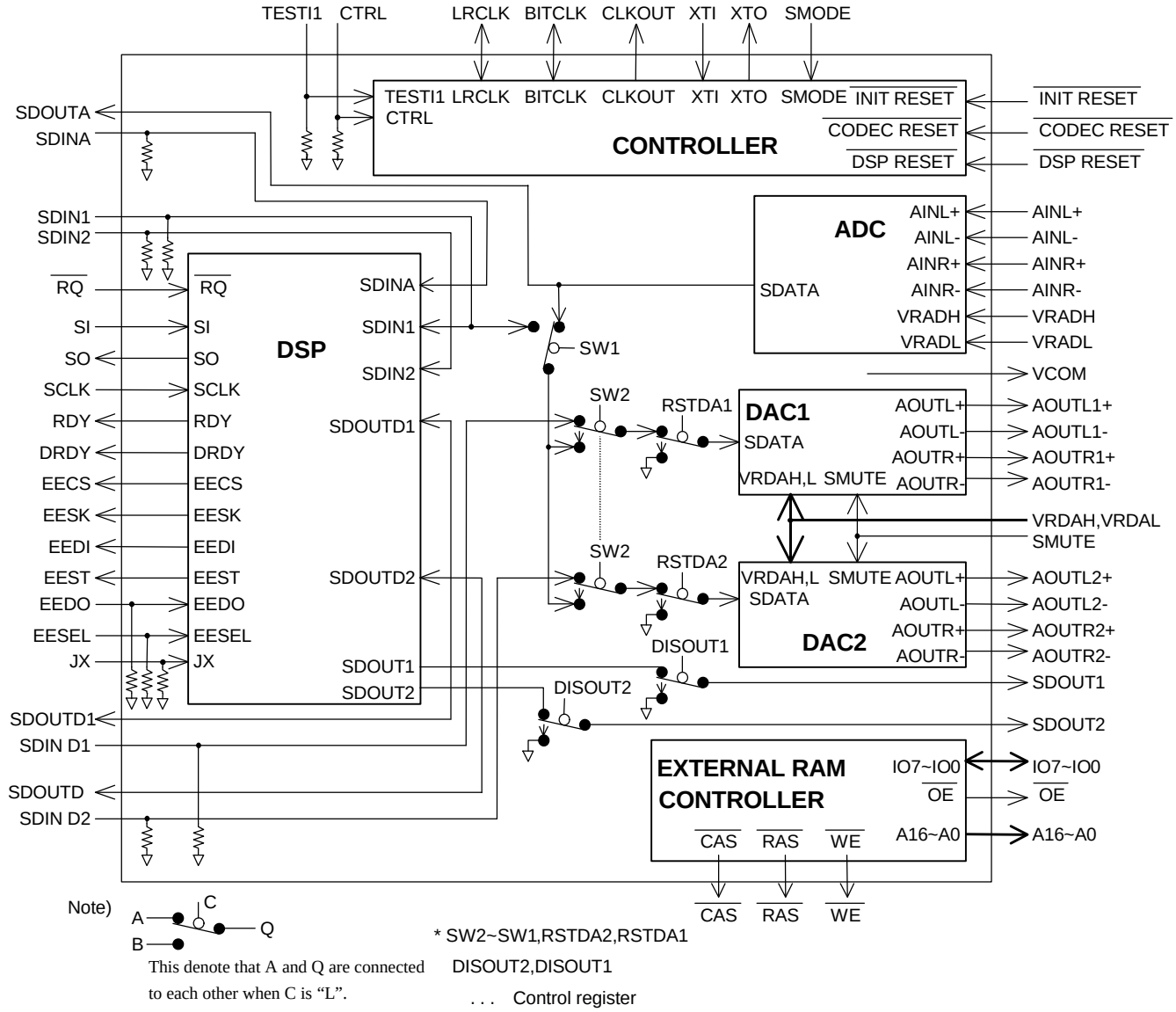
Soft-mute function

(11) Special use

11-1) External connection mode

Normally, OPCL is used at "L" (internal connection mode), but when OPCL is set to "H", the ADC output and DAC1/DAC2 inputs can be used independently form DSP. (External connection mode)

OPCL = "H": External connection mode



The following shows the input/output interface in external connection mode:

- SDINA for MSB-first 24-bit input (including I^2S compatibility)
- SDOUTA for MSB-first 20-bit output (including I^2S compatibility)
- SDOUTD1 and SDOUTD2 for MSB-first 24-bit outputs (including I^2S compatibility)
- SDIND1 and SDIND2 for MSB-first 20-bit inputs (including I^2S compatibility)

Conversion between the input/output standard format and I^2S is interlocked with the control register DIF, similar to the case for internal connection mode.

11-2) Use as ADC and DAC (mainly for test)

Only the ADC and DAC sections can be operated while keeping the DSP section in the reset state with the independent control of $\overline{\text{DSP RESET}}$ and $\overline{\text{CODEC RESET}}$. (When no DSP processing is required, power saving and noise reduction can be expected. However, the ADC data cannot be output in internal connection mode. In external connection mode, it is output from SDOUTA.)

In internal connection mode, setting of the control registers allows the following operations to be performed:

a) ADC to DAC1 and DAC2 (Analog to Analog)
The ADC output data is directly connected over to DAC1 and DAC2. (SW2 = 1, SW1 = 0)
When input to the DAC2 is not required, set RSTDA2 = 1.
(When input to the DAC1 is not required, set RSTDA1 = 1.)

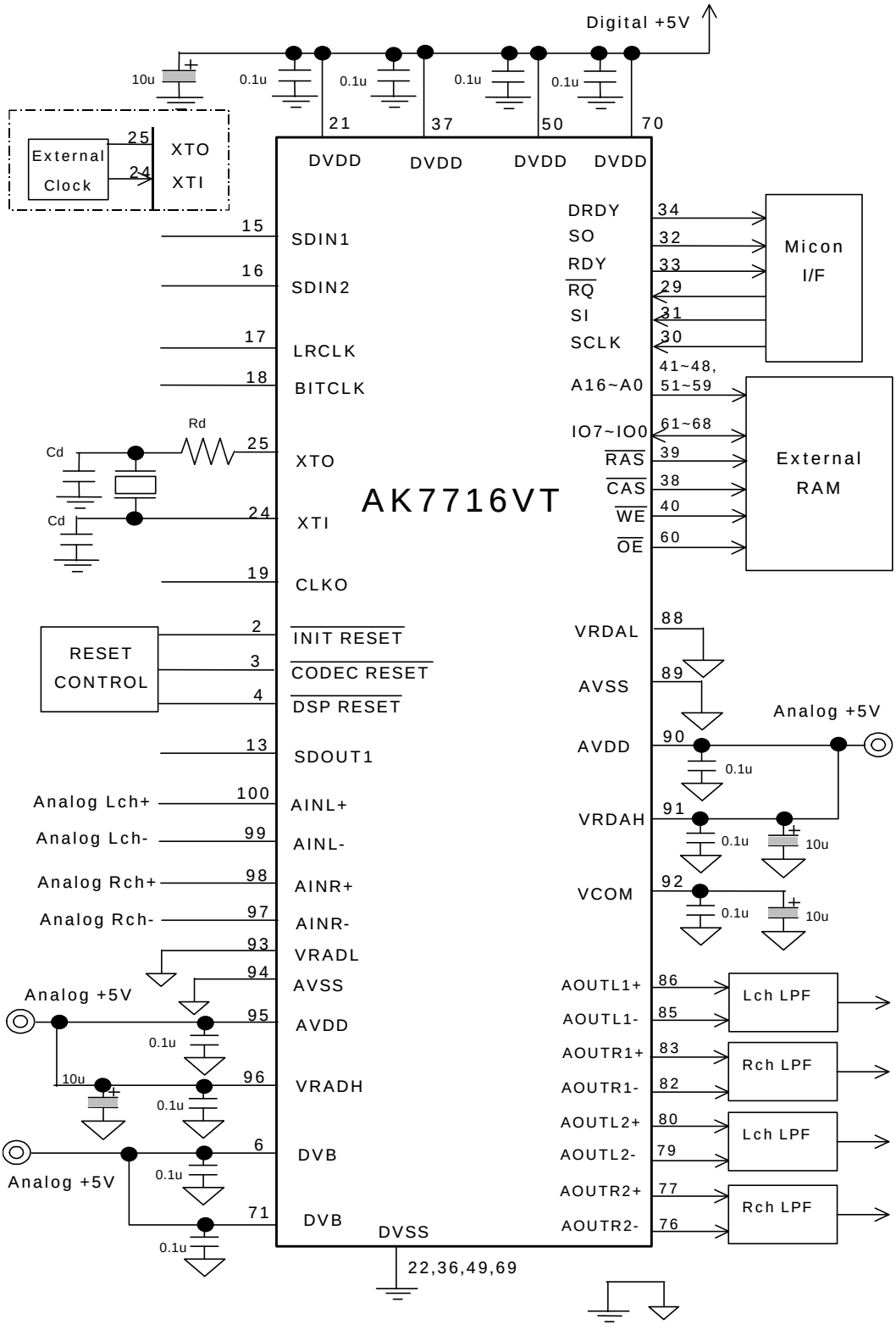
b) SDIN1 to DAC1 and DAC2
SDIN1 input data is directly connected to DAC1 and DAC2. (SW2 = 1, SW1 = 1)
In this case, only the MSB-justified 24-bit input (including I^2S compatibility) is supported.
When input to DAC2 is not required, set RSTDA2 = 1.
(When input to DAC1 is not required, set RSTDA1 = 1.)

For this operation, set only $\overline{\text{CODEC RESET}}$ to "H" after setting the control registers during the system reset phase ($\overline{\text{DSP RESET}}$ = $\overline{\text{CODEC RESET}}$ = "L"). To make a new setting, be sure to perfom the system reset.

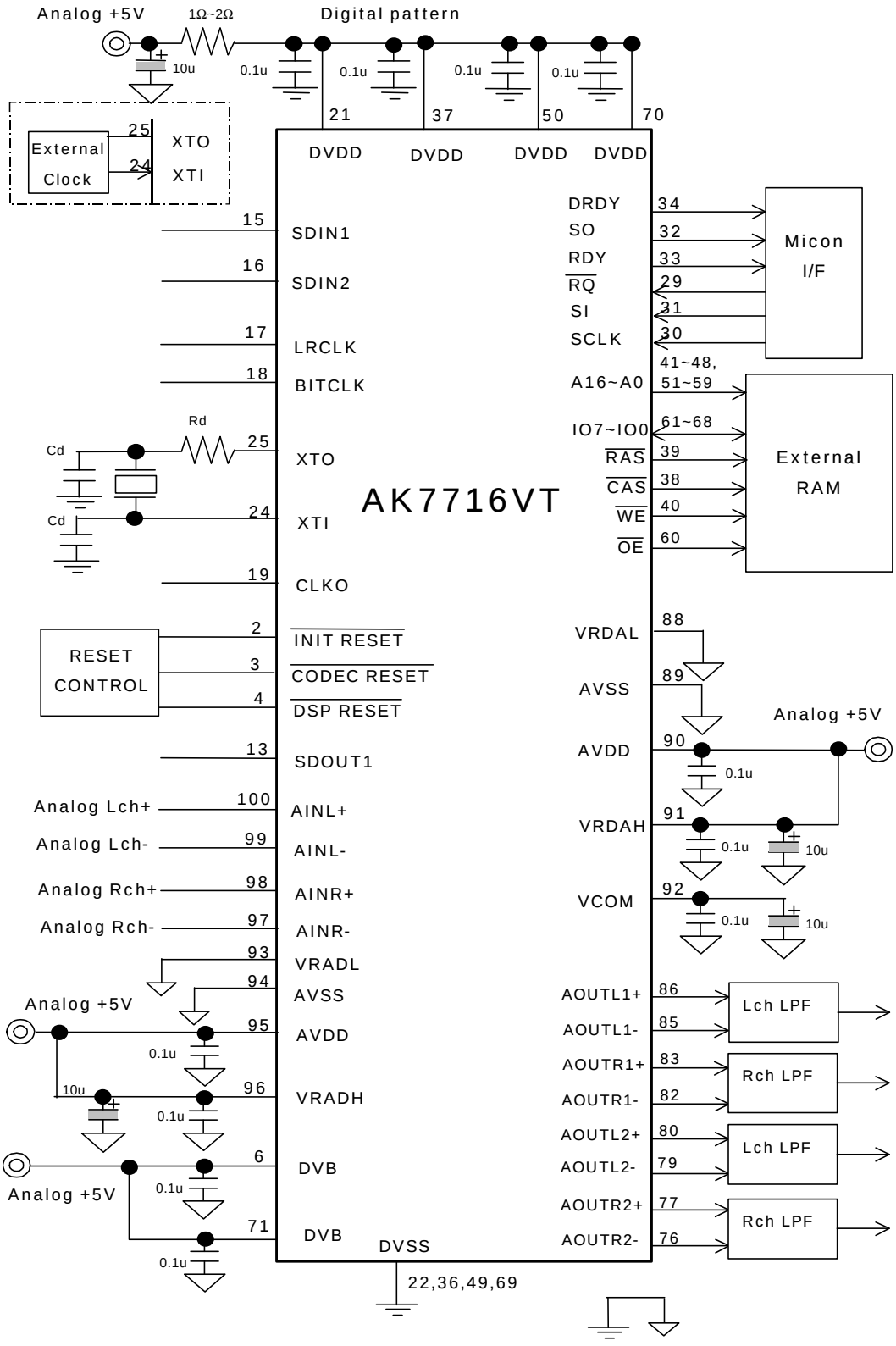
System Design

(12) Example circuit (Internal connected mode OPCL : "L")

See 12-2) Peripheral circuit also.



12-1) Example circuit: Internal connected mode OPCL : "L" ; Example for 12-2-3)-②
See 12-2) Peripheral circuit also.

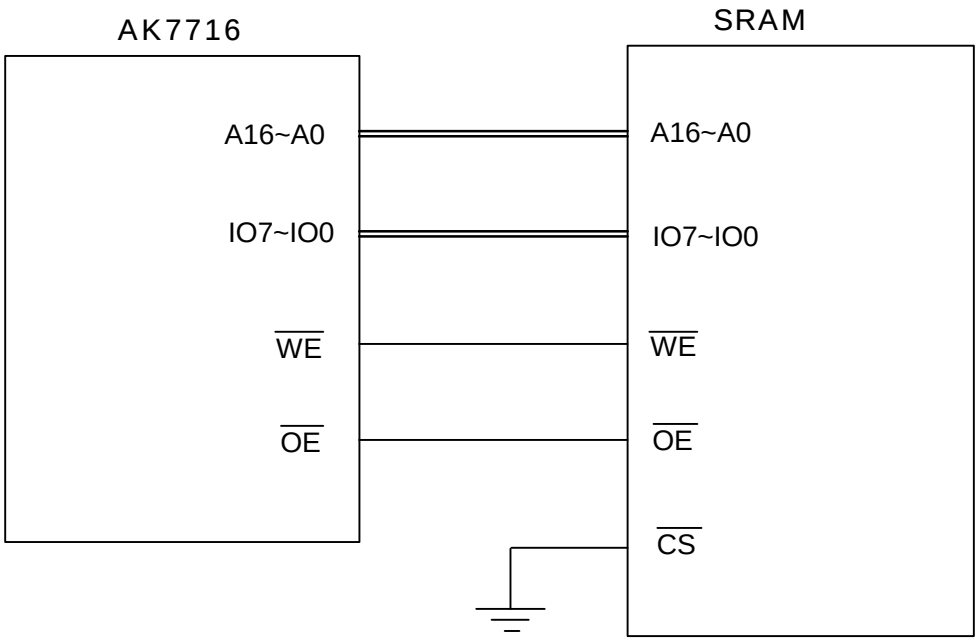


12-2) Peripheral circuit

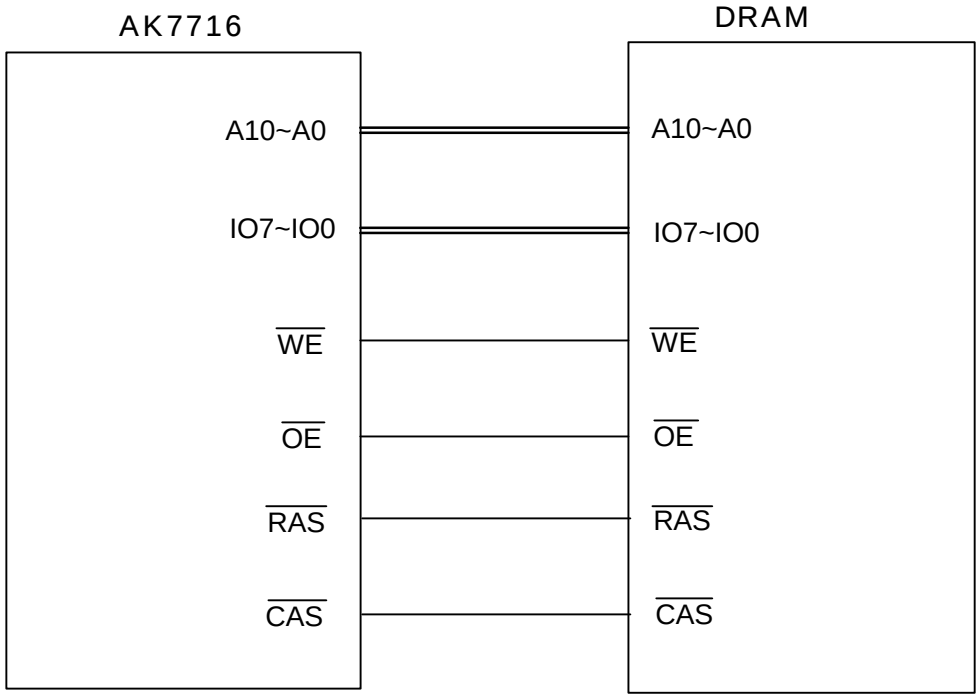
12-2-1) Connect with external RAM

The connections to external RAM (SRAM or DRAM) are as follows. It should be as short as possible to connect line.
Leave open, if it does not use external RAM.

① **SRAM**



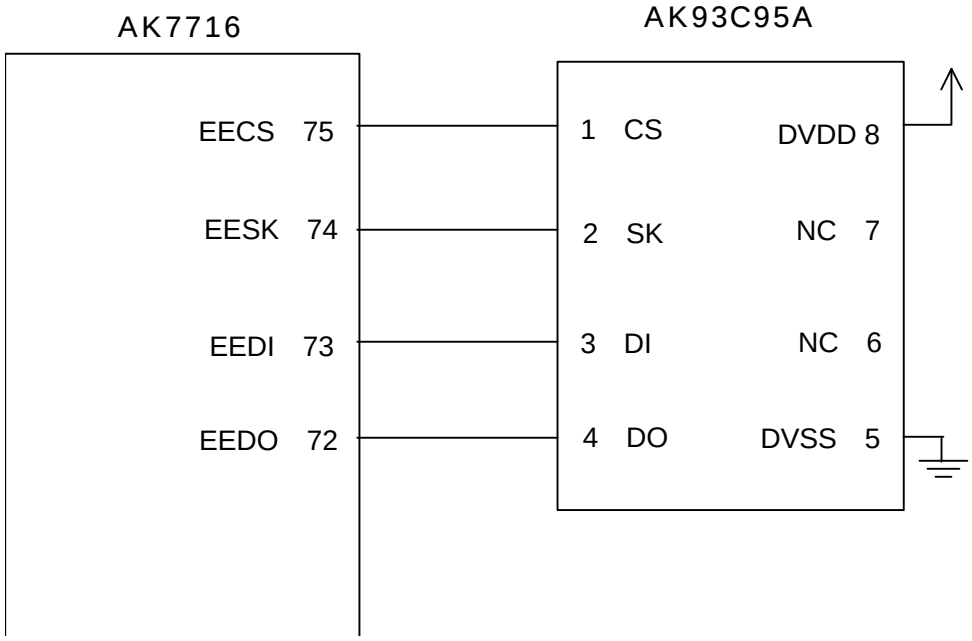
② **DRAM**



12-2-2) Connect with EEPROM

The connection to EEPROM (AK93C95A) is as follow. It can connect directly because of pin assignment. It should be as short as possible to connect line.

In case of not using EEPROM function, output pins (EECS, EESK, EEDI and EEST) leave open. Input pins (EEDO and EESEL) leave open or connect to DVSS.



12-2-3) Ground and power supply

① To minimize digital noise coupling, AVDD and DVDD should be individually de-coupled at the AK7716. System analog power is supplied to AVDD and DVB. AVDD and DVB are connected to each other through the IC board, and eventually have several ohms of resistance. If the set of AVDD and DVB and DVDD are driven by individual power sources, start up AVDD and DVB simultaneously with DVDD, or start up AVDD and DVB first.

Generally, power supply and ground wires must be connected separately according to the analog and digital systems. Connect them at a position close to the power source on the PC board. Decoupling capacitors, and ceramic capacitors of small capacity in particular, should be connected at positions as close as possible to the AK7716.

② If the absolute maximum rating conditions of a power supply cannot be maintained depending on the system, it is recommended to supply the AK7716 power from the same regulator. Power patterns must be separated into analog and digital patterns. For a digital pattern, connection must be made through an appropriate 1~2-ohm resistor from the regulator. In this case, the capacitor with the larger capacity must be connected to the analog side.

12-2-4) Reference voltage

The input voltage difference between the VRADH pin and the VRADL pin determines the full scale of analog input, while the potentials difference between the VRDAH pin and the VRDAL pin determines the full scale of the analog output. Normally, connect AVDD to VRADH and VRDAH, and connect 0.1µF ceramic capacitors from them to AVSS. VCOM is used as the common voltage of the analog signal.

To shut out high frequency noise, connect a 0.1µF ceramic capacitor in parallel with an appropriate 10µF electrolytic capacitor between this pin and AVSS. The ceramic capacitor in particular should be connected at a position as close as possible to the pin.

No load should be connected to the VCOM pin. To avoid coupling to the AK7716, digital signals and clock signals in particular should be kept away as far as possible from the VRADH, VRADL, VRDAH, VRDAL and VCOM pins.

12-2-5) Analog input

Analog input signals are applied to the modulator through the differential input pins of each channel. The input voltage is equal to the differential voltage between AIN+ and AIN- (ΔVAIN = (AIN+) - (AIN-)), and the input range is $\pm$FS = $\pm$(VRADH - VRADL) × 0.4. When VRADH = 5V and VRADL = 0V, the input range is within ±2.0 V. The output code format is given in terms of 2's complements.

When fs = 48 kHz, the AK7716 samples the analog input at 3.072 MHz. The digital filter eliminates noise from 30 kHz to 3.042 MHz. However, noise is not rejected in the bandwidth close to 3.072 MHz. Most audio signals do not have large noise in the vicinity of 3.072 MHz, so a simple RC filter is sufficient.
A/D converter reference voltage is applied to the VRADH and VRADL pins. Normally, connect AVDD to VRADH, and AVSS to VRADL. To eliminate high frequency noise, connect a 0.1µF ceramic capacitor in parallel with a 10µF electrolytic capacitor between the VRADH pin and VRADL.

The analog source voltage to the AK7716 is +5 V. Voltage of AVDD + 0.3 V or more, voltage of AVSS - 0.3 V or less, and current of 10 mA or more must not be applied to analog input pins (AINL and AINR). Excessive current will damage the internal protection circuit and will cause latch-up, thereby damaging the IC. Accordingly, if the surrounding analog circuit voltage is ±15 V, the analog input pins must be protected from signals with the absolute maximum rating or more.

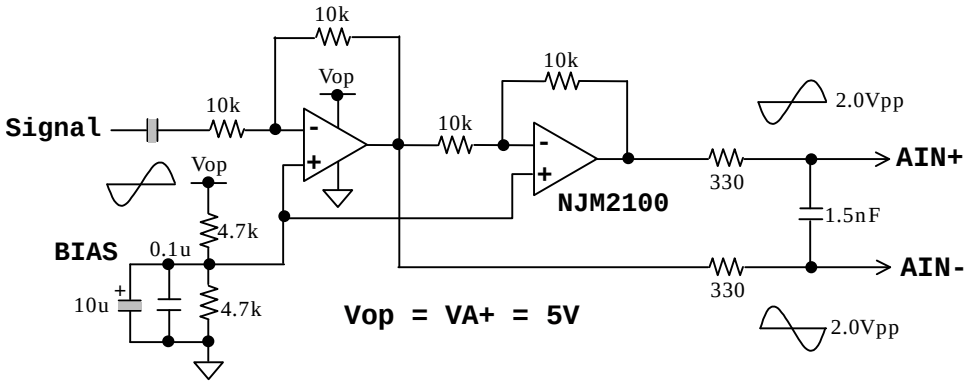


Fig. 1 Example of input buffer circuit (differential input)

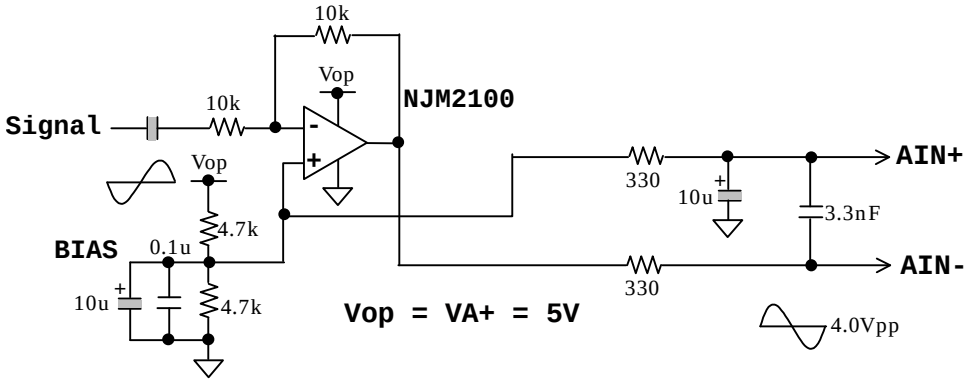


Fig. 2 Example of input buffer circuit (single ended input)

An analog signal can be applied to the AK7716 is single ended mode. In this case, apply the analog signal (the full scale is 4.0 Vpp when the internal reference voltage is used) to the AIN-input, and bias to the AIN+input. However, use of a low saturated operational amplifier is recommended if the operational amplifier is driven by the 5-volt power supply. The electrolytic capacitor connected to AIN+ is effective for reducing the second harmomics.
(See Fig. 2.)

12-2-6) Analog output

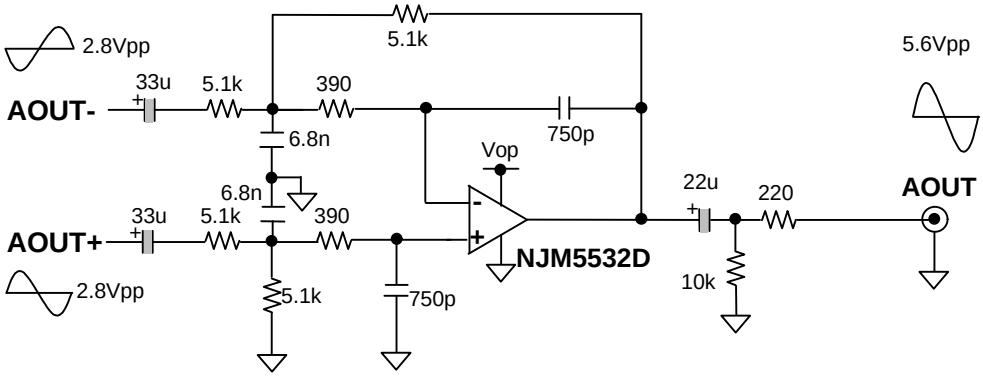


Fig. 3 Example of output LPF circuit

The analog output s are full differential outputs and nominally 2.8Vpp (typ @ VREF=5V) centered in the internal common voltage about (AVDD/2). The differential outputs are summed externally, VAOUT=(AOUT+)-(AOUT-) between AOUT+ and AOUT-.
If the summing gain is 1, the output range is VAOUT = 5.6Vpp(typ@ VREF=5V). The bias voltage of external summing circuit is supplied externally.
The input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal AOUT is 0V for 000000H(@24bit).

The internal switched-capacitor filter and external LPF attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

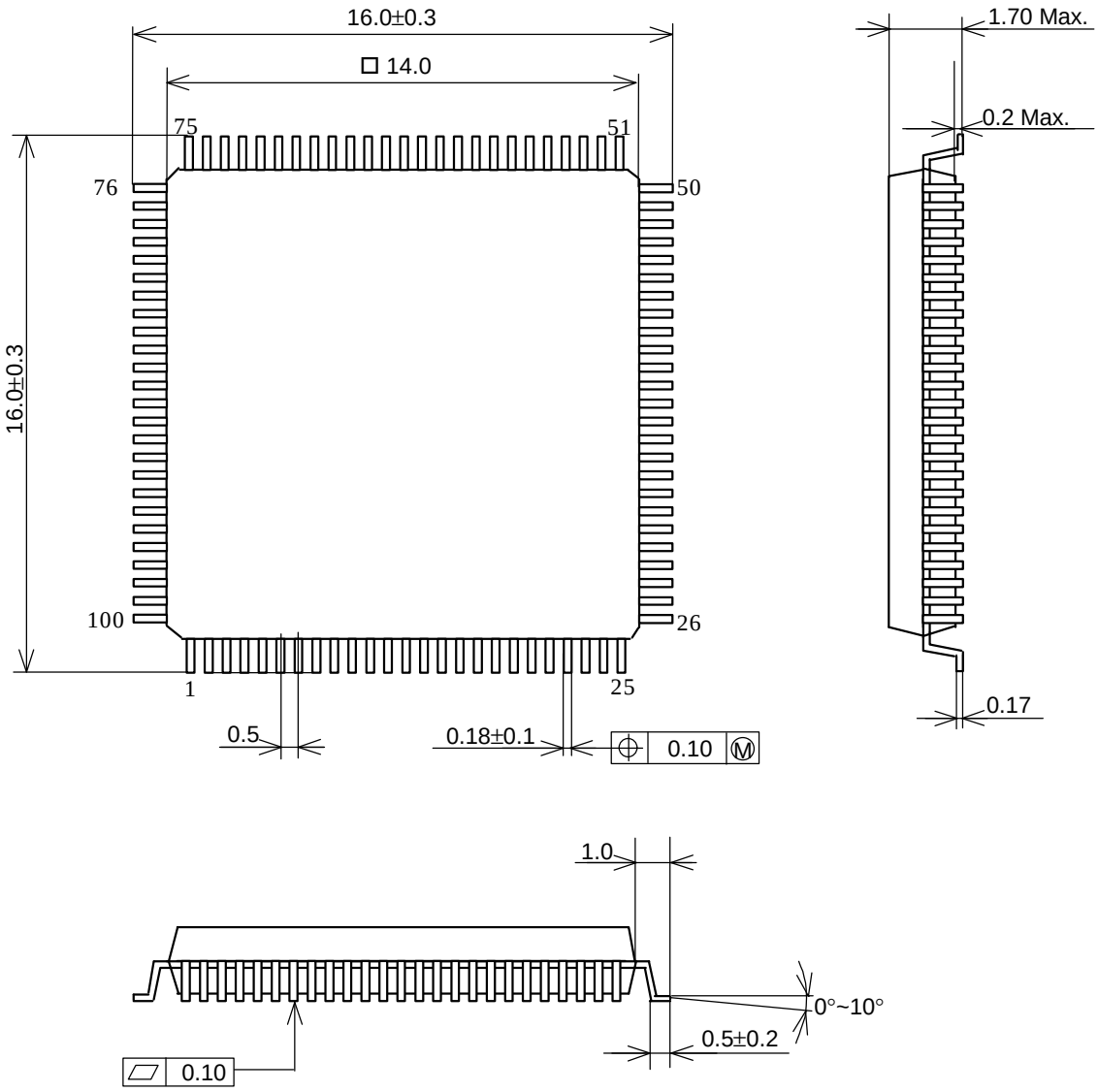
Differential outputs can eliminate few mV+AVDD/2 DC offset on analog outputs with capacitors.
Fig.3 shows the example of external op-amp circuit summing the differential outputs.

12-2-7) Connection to digital circuit

To minimize the noise resulting from the digital circuit, connect CMOS logic to the digital output. The applicable logic family includes the 4000B, 74HC, 74AC, 74ACT and 74HCT series.

Package

- 100-pin LQFP (Unit : mm)



- Material & Lead finish

Package:	Epoxy
Lead-frame:	Copper
Lead-finish	Soldering plate

Marking

Meanings of XXXXAAA
XXXX: Time of manufacture (numeral)
AAA: Lot numbers (Alphabet)