Preliminary

Am2075

ISDN Digital Exchange Controller (IDEC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Four independent HDLC channels**
- **64-byte FIFO storage per channel and direction**
- **Handling of basic HDLC functions**
  - Flag detection/generation
  - Zero deletion/insertion
  - CRC checking/generation
  - Check for abort
- **Single connection and quad connection modes**
- **IOM™ interface or PCM interface**
- **Programmable time slots and channel data rates (up to 4 Mb/s)**
- **Different methods of contention resolution**
- **Address recognition**
- **Standard microprocessor interface, multiplexed or non-multiplexed address and data buses**
- **Vectored interrupt**
- **Advanced CMOS technology**
- **Power consumption less than 50 mW**

GENERAL DESCRIPTION

The Am2075, ISDN Digital Exchange Controller (IDEC™), is a serial HDLC data communication circuit with four independent channels. Its telecommunication-specific features make it especially suited for use in variable data rate PCM systems. In addition, the device contains sophisticated switching functions and implements automatic contention resolution between packet data from different sources.

Its applications include communication multiplexers, peripheral ISDN line cards, packet handlers, and X.25 packet switching devices. The IDEC is a fundamental building block for networks with either centralized, decentralized, or mixed-signaling architectures for packet data handling.

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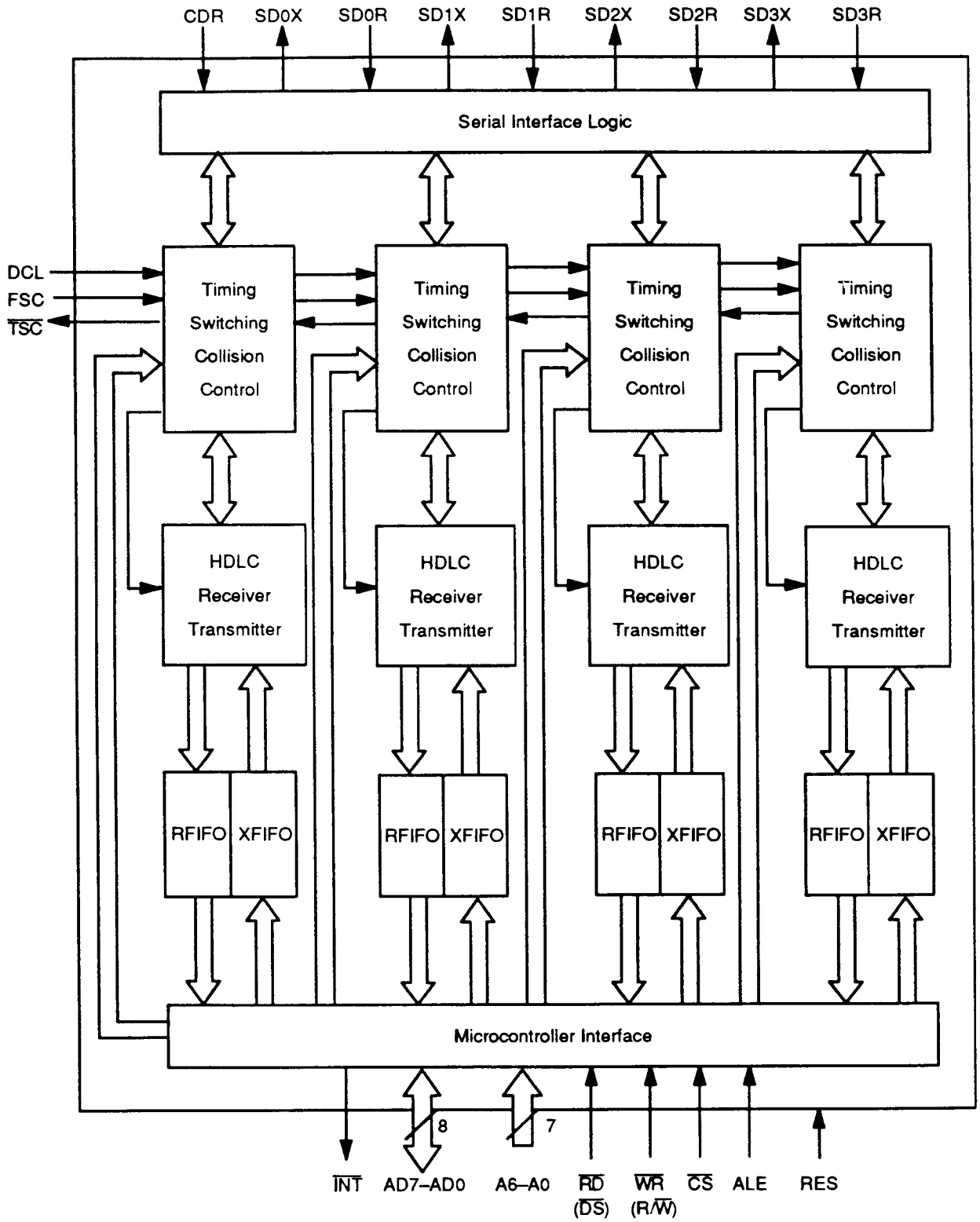
BLOCK DIAGRAM



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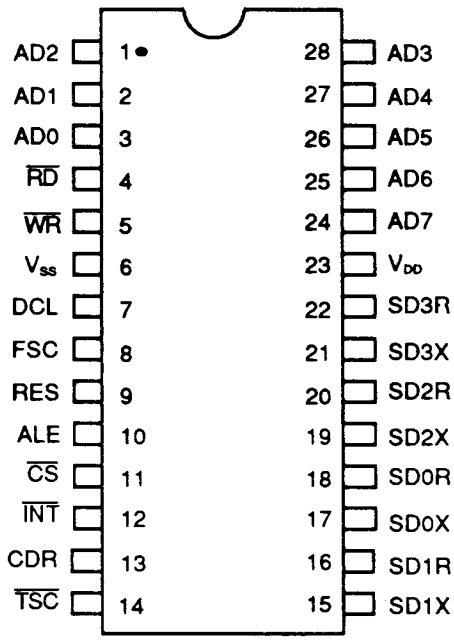
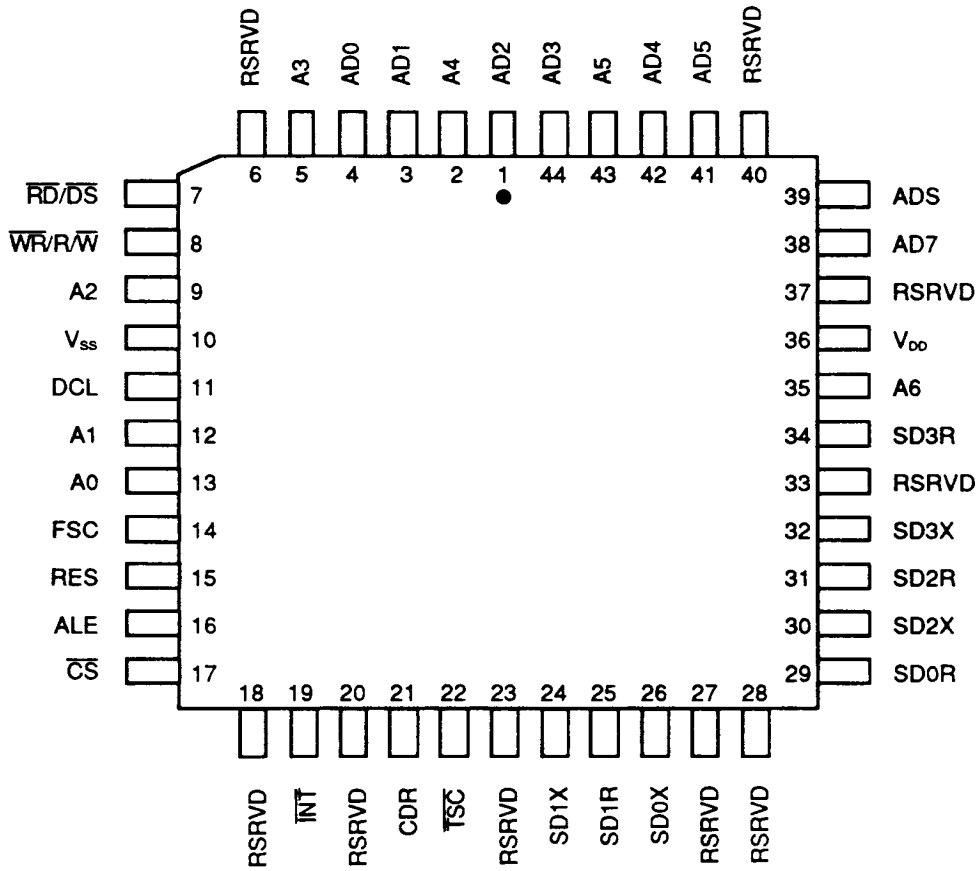
CONNECTION DIAGRAMS
Top View

28-Pin DIP



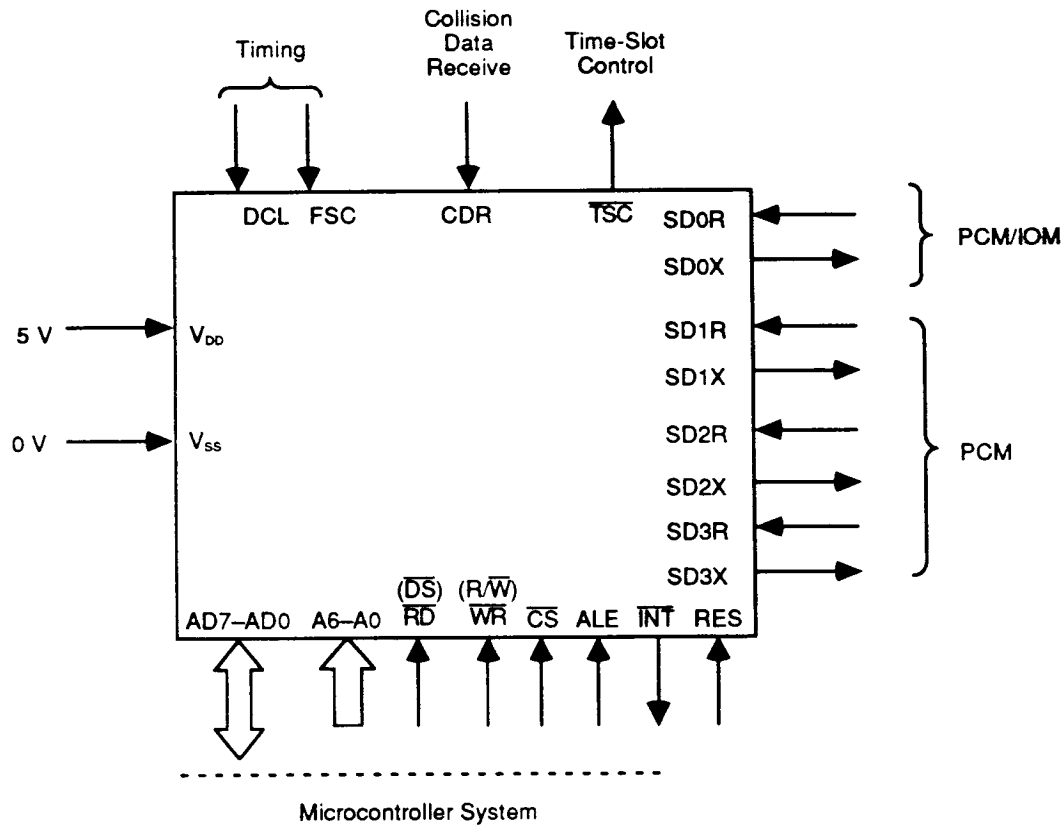
44-Pin PLCC



Note: Pin 1 is marked for orientation.

11134C-ConnDgrm

LOGIC SYMBOL



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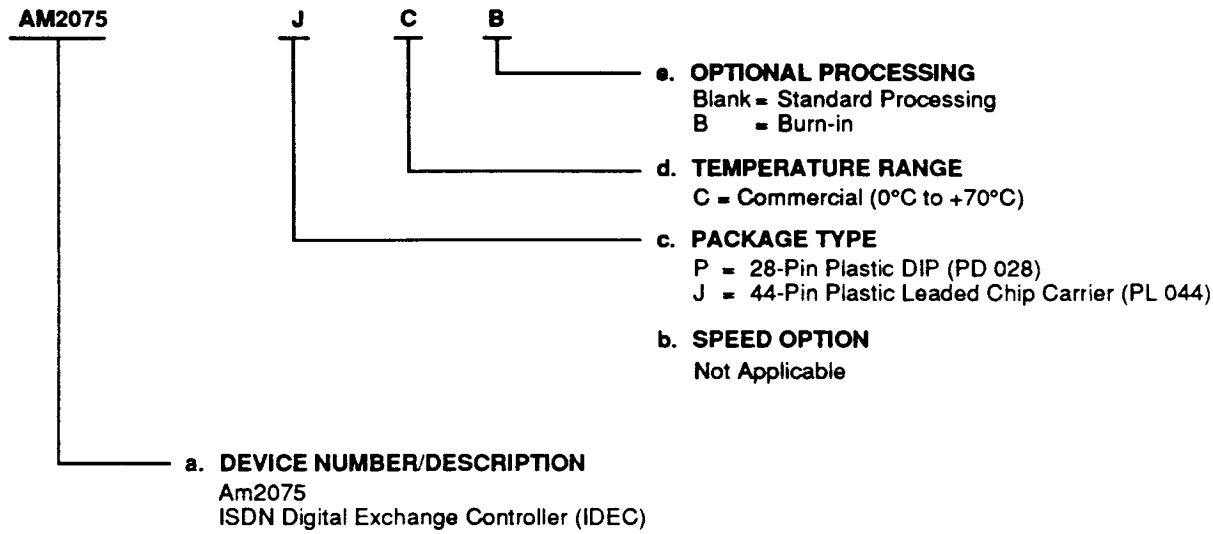
ORDERING INFORMATION

Standard Products

AMD® standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM2075	PC, JC, PCB, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

A6–A0
Address Bus (Inputs)

These inputs interface to the system's address bus to select an internal register for a read or write access. Only provided in the PLCC package and only active if a demultiplexed microprocessor interface is selected.

AD7–AD0
Address-Data Bus (Inputs/Outputs)

The multiplexed Address Data Bus transfers data and commands between the microprocessor system and the IDEC.

ALE
Address Latch Enable (Input)

A High on this line indicates an address on the external address-data bus, selecting one of the internal registers.

CDR
Collision Data Receive (Input)

$\overline{CS}$
Chip Select (Input)

A Low on this line selects the IDEC for a read/write operation.

DCL
Data Clock (Input)

Supplies a clock signal either equal to or twice the data rate.

$\overline{DS}$
Data Strobe (Input)

The rising edge marks the end of a valid read or write operation (Motorola® bus mode). Only provided in the PLCC package.

FSC
Frame Synchronization (Input)

$\overline{INT}$
Interrupt Request (Output)

This line is activated when the IDEC requests an interrupt. It is an open-drain output.

$\overline{RD}$
Read (Input)

A Low on this line indicates a read operation (Intel® bus mode).

RES
Reset (Input)

A High on this input forces the IDEC into reset state.

R/$\overline{W}$
Read/Write (Input)

A High on this line indicates a valid microprocessor access as a read operation. A Low indicates a microprocessor access as a write operation (Motorola bus mode). Only provided in PLCC package.

SD3R–SD0R
Serial Data Receive (Inputs)

SD3X–SD0X
Serial Data Transmit (Outputs)

SD2X is a collision output in Master mode.

$\overline{TSC}$
Time Slot Control (Output)

Supplies a control signal for an external driver.

$\overline{WR}$
Write (Input) or Read/Write (Input)

A Low on this line indicates a write operation (Intel bus mode).

V_{DD}
+5-V Supply Voltage (Input)

V_{SS}
Ground (Input)

FUNCTIONAL DESCRIPTION

General Functions and Device Architecture

The IDEC is an HDLC controller which handles four HDLC communication channels, each channel fully independent and programmable by its own register set. The circuit performs the following functions:

- Extraction (reception) and insertion (transmission) of the HDLC data packets in a time-division multiplex-bit stream.
- Implementation of the basic HDLC functions of the Layer 2 protocol.
- Interfacing of the data packets to the microprocessor bus. For the temporary storage of data packets, overlapping FIFO structures are used per channel and direction.
- Switching of data between serial interfaces.
- Implementation of different types of collision resolution.
- Test functions.

Operating Modes

Each HDLC controller of the IDEC is assigned to one time channel governed either by time slot assignment or by an external strobe signal. Two basic configurations are distinguished (Figure 1).

- In the quad-connection configuration, the four HDLC controllers (A–D) are connected to individual time-multiplexed communication lines.
- In the single-connection configuration, the four HDLC channels are all connected to one time-multiplexed communication line.

In the quad-connection configuration, two modes are distinguished as follows:

- Each connection is a time-slotted highway; the lengths and positions of the time slots are programmable (quad-connection time slot mode).
- Each connection is a communication line; the time channels are marked by an external strobe signal (quad-connection common control mode).

In the single-connection configuration, two modes are distinguished as follows:

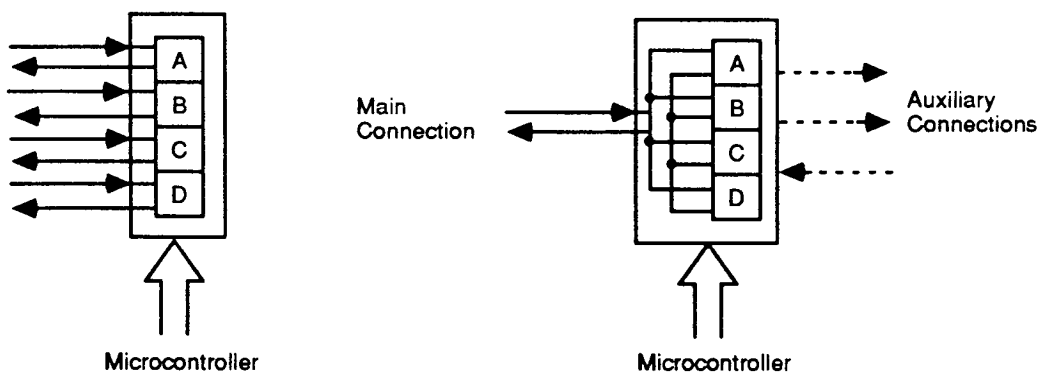
- The connection is a standard IOM interface with predefined channel positions (single-connection IOM mode).
- The connection is a time-slotted highway (single-connection time slot mode).

A time-slotted highway will sometimes be referred to as a PCM highway, or PCM.

Table 1. Four Basic Operating Modes of the IDEC

MDS1	MDS0	Mode Description
0	0	Single-connection time slot mode
0	1	Quad-connection common control mode
1	0	Single-connection IOM mode
1	1	Quad-connection time slot mode

The four modes of operation are illustrated in Figure 2. Using channel-by-channel programming, one of a number of collision detection modes may be selected in each of the basic modes of operation. For future reference, they are also depicted in Figure 2.



a. Quad Connection

b. Single Connection

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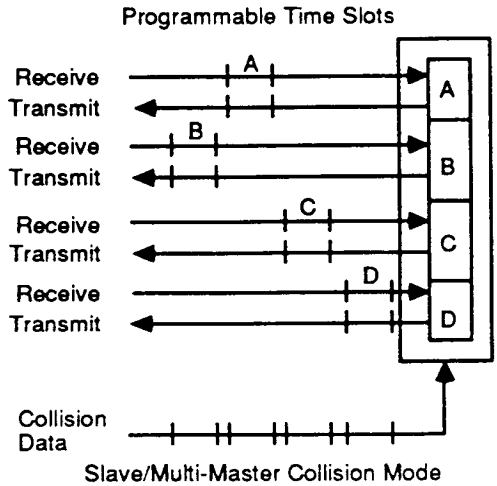
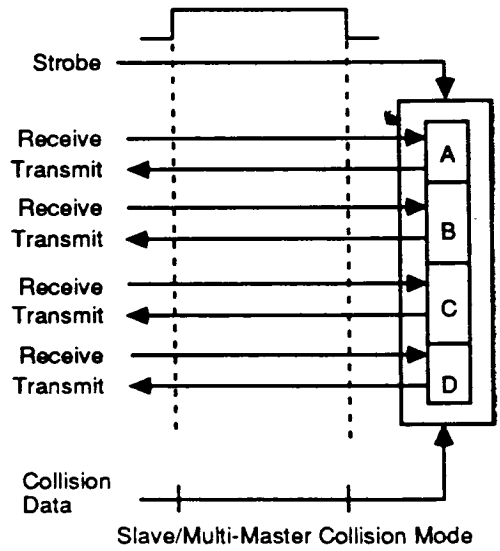
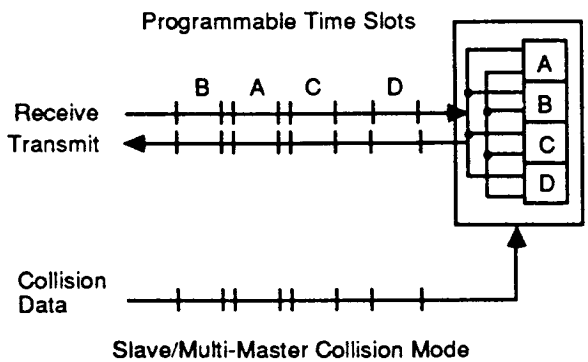
Figure 1. Connection Configurations



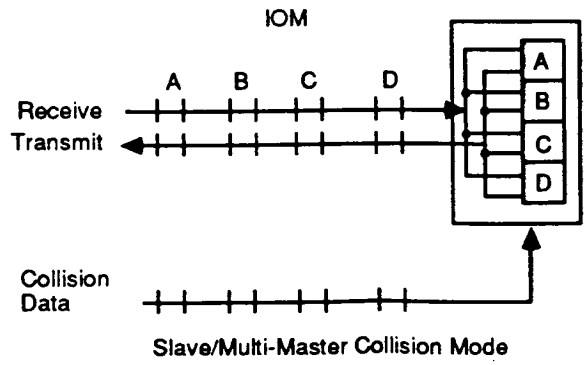
a. Quad-Connection TS Mode



b. Quad-Connection Common Control Mode



c. Single-Connection TS Mode



d. Single-Connection IOM Mode

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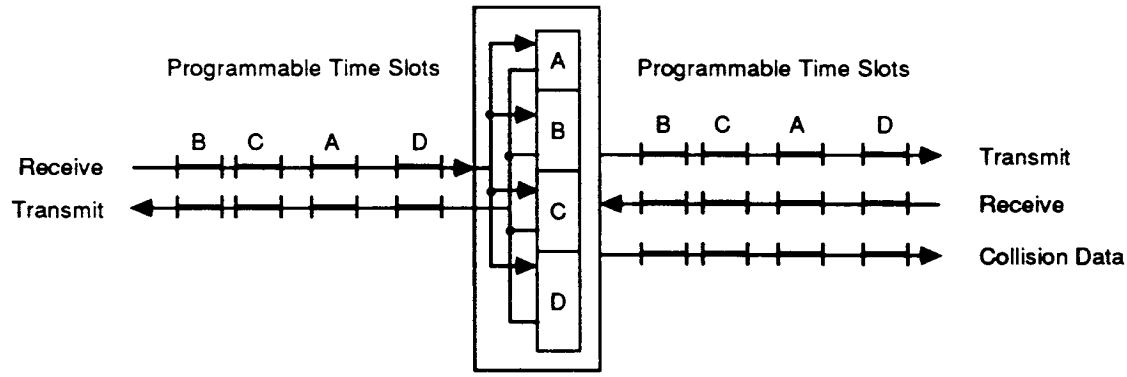
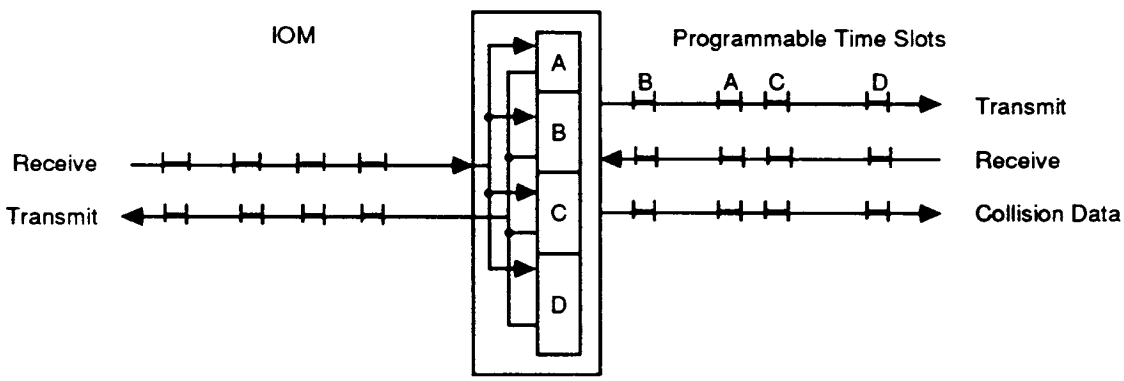
Figure 2. Operating Modes of the IDEC



Master Collision Mode

e. Single-Connection TS Mode



Master Collision Mode

f. Single-Connection IOM Mode

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Figure 2. Operating Modes of the IDEC (continued)

Interfaces

Microcontroller Interface

The IDEC is programmable over an 8-bit parallel microcontroller interface. Easy and fast microprocessor access is provided by 8-bit address decoding on chip. The interface consists of 13 (20) lines and is directly compatible with processors of the multiplexed and demultiplexed address/data bus types (Intel or Motorola processor families).

In addition to 8-bit processors, the IDEC supports a direct connection to 16-bit processors. Thus, through an internal address transformation, it is possible to access all IDEC registers using either even microprocessor addresses only or odd microprocessor addresses only.

Serial Interfaces

Depending on the selected mode, the IDEC supports four physically separate, full-duplex serial interfaces, or one full-duplex serial interface.

In addition to the data input and output lines, the serial interface requires a common data clock (input DCL) and a frame synchronization signal (input FSC). Input data is latched on the falling edge of DCL and output data is clocked on the rising edge of DCL. The IDEC may be programmed so that the data clock rate is either equal to the data rate, or twice the data rate.

Individual Functions

Channel Access

The four HDLC controllers of the IDEC are connected to the serial interfaces as shown in Table 3. The table indicates the selection of the data channel, the selectable time-slot widths, the output driver type, and the function of the active-Low Time-Slot Control ($\overline{TSC}$) output in each of the operating modes.

The data output is set in a high-impedance state outside the time channel where data is transmitted.

Quad-Connection Time Slot Mode

Channel selection is performed via the Time Slot Select registers (TSR). For each HDLC channel, the 8-bit TSR register gives the position of a time slot with a 2-bit resolution. The length of the time slot, either 1, 2, 7 or 8 bits, can be selected using the MODE register (CCS1, 0). These parameters are common to the receive and the transmit channel. If the number of bits in a PCM frame is 256 or 512, the (FSC) need not be provided at every PCM frame start because bit counters are automatically reset at frame end. When the PCM frame length is not equal to either 256 or 512 bits, the frame synchronization signal has to be provided at the beginning of every PCM frame.

Table 2. Microcontroller Interface Signals of the IDEC

Symbol	Type	Name and Function
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O I/O I/O I/O I/O I/O I/O I/O	**Address-Data Bus**. The multiplexed address/data microprocessor interface bus mode is selected. These lines transfer data and commands between the microprocessor and the IDEC. If a demultiplexed mode is used, these lines interface with the system data bus.
A6–A0	I	**Address Bus**. These inputs interface to the system's address bus to select an internal register for a read or write access. Only provided in the PLCC package and only active if a demultiplexed microprocessor interface is selected.
$\overline{CS}$	I	**Chip Select**. A Low on this signal selects the IDEC for a read/write operation.
$\overline{WR}$	I	**Write**. This signal indicates a write operation, active low Intel bus mode.
R/$\overline{W}$	I	**Read/Write**. At High, identifies a valid microprocessor access as a read operation. At Low, identifies a microprocessor access as a write operation (Motorola bus mode). Only provided in the PLCC package.
$\overline{RD}$	I	**Read**. This signal indicates a read operation, active Low (Intel bus mode).
$\overline{DS}$	I	**Data Strobe**. The rising edge marks the end of a valid read or write operation (Motorola bus mode). Only provided in the PLCC package.
$\overline{INT}$	OD	**Interrupt Request**. The signal is activated when the IDEC requests an interrupt. It is an open drain output.
ALE	I	**Address Latch Enable**. In the Intel type multiplexed microprocessor interface mode a High on this line indicates an address of an internal register on the external address/ data bus. In the Intel type demultiplexed microprocessor interface mode this line should be connected to V_{SS}. In the demultiplexed Motorola type microprocessor interface mode it should be connected to V_{DD}.

The $\overline{TSC}$ output line marks the timeslot when data is transmitted/received by the HDLC Controller B.

The position of a time slot with respect to FSC, as a function of the TSR register contents, is shown in Figure 3.

Quad-Connection Common Control Mode

Channel selection is performed by an active High strobe signal provided through the Frame Synchronization Signal (FSC) input. The strobe signal is common to all four HDLC channels. The $\overline{TSC}$ output is active when the FSC strobe is active.

Single-Connection TS Mode

The time slots selected by the TSR registers all pertain to the same PCM highway. The programming of a channel otherwise proceeds exactly as explained above. The Time-Slot Control (TSC) output line marks the time slots when data is transmitted/received by any of the four controllers.

Single-Connection IOM Mode

The IOM is an interface where a frame is composed of *n* IOM channels ($n \geq 1$; $n = 8$ in Figure 4a). Each IOM channel has a unique structure. It consists of two 8-bit bytes, corresponding to the ISDN B channels, a monitor byte, and a control byte of which the first two bits are allocated to the ISDN D channel. In the single connection IOM mode, the serial interface has an IOM frame structure and the four HDLC channels are assigned to the D bits of four consecutive IOM channels. The choice whether the four HDLC controllers are assigned to IOM channels 0–3 or 4–7 is governed by the microcontroller bit VIS (Common Configuration Register). See Figure 4b.

To program the single-connection IOM mode (CCR: MDS1, MDS0 = 10)

- with the slave mode (MODE3–0:CMS1, CMS0 = 01), or;
- with the multi-master mode (MODE3–0:CMS1, CMS0 = 10), or;
- with the unconditional transfer mode (MODE3–0: CMS1, CMS0 = 00)

this additional programming has to be made:

MODE0:CCS1,CCS0 = 00 bin
MODE1:CCS1,CCS0 = 00 bin
MODE2:CCS1,CCS0 = 00 bin
MODE3:CCS1,CCS0 = 00 bin

TSR0 = 0C hex
TSR1 = 1C hex
TSR2 = 2C hex
TSR3 = 3C hex

Table 3. HDLC Controller Channel Selection and Characteristics

Mode		Channel Input				Channel Output				Output	Channel Characteristics		Time-Slot	
MDS1	MDS0	A	B	C	D	A	B	C	D	Driver	Channel Select	Channel Width	Control ($\overline{TSC}$)	Description
0	0	SD0R	SD0R	SD0R	SD0R	SD0X	SD0X	SD0X	SD0X	PP or OD	TSR A–D registers	1,2,7,8	TSR A–D	Single-connection TS mode
0	1	SD0R	SD1R	SD2R	SD3R	SD0X	SD1X	SD2X	SD3X	PP or OD	FSC strobe	Arbitrary	FSC inverted	Quad-connection common control mode
1	0	SD0R	SD0R	SD0R	SD0R	SD0X	SD0X	SD0X	SD0X	OD	Fixed 2-bit TSs	2	Fixed 2-bit TSs A–D	Single-connection IOM mode
1	1	SD0R	SD1R	SD2R	SD3R	SD0X	SD1X	SD2X	SD3X	PP or OD	TSR A–D registers	1,2,7,8	TSR B	Quad-connection TS mode

OD = Open-drain driver.
PP = Push-pull driver.
The output driver type refers to the SD0X (or SD0X, SD1X, SD2X, SD3X) outputs.
$\overline{TSC}$ is a push-pull signal.

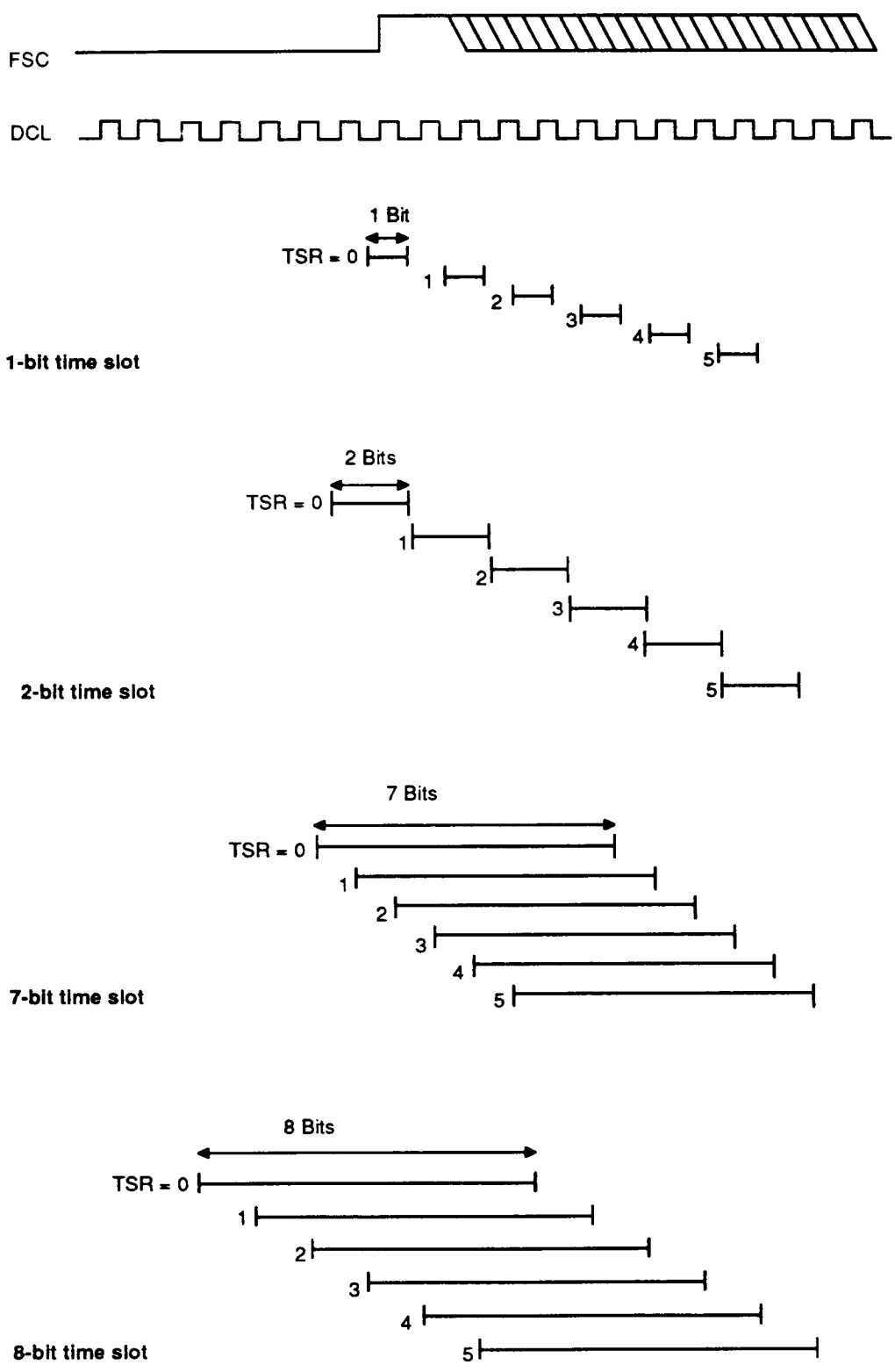

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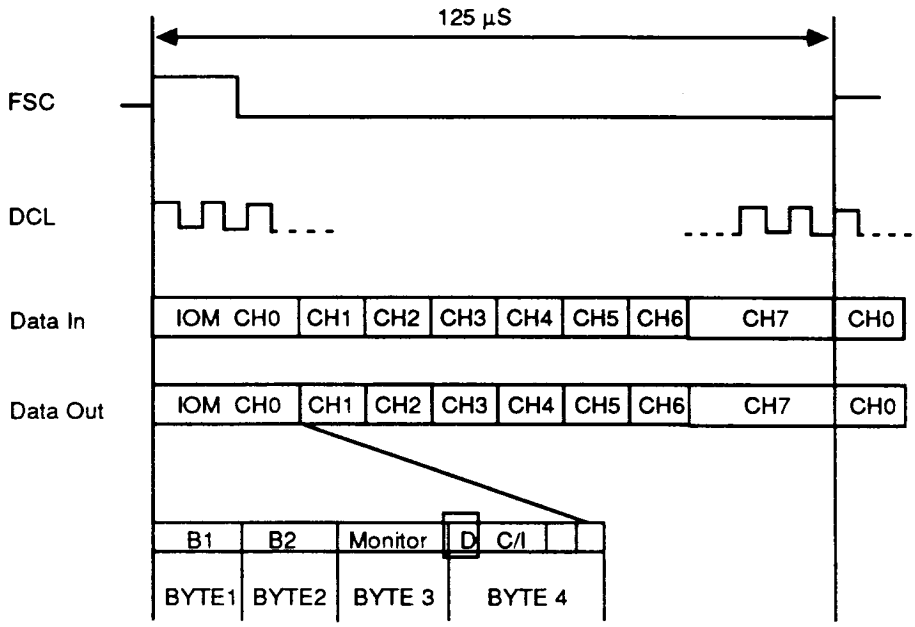
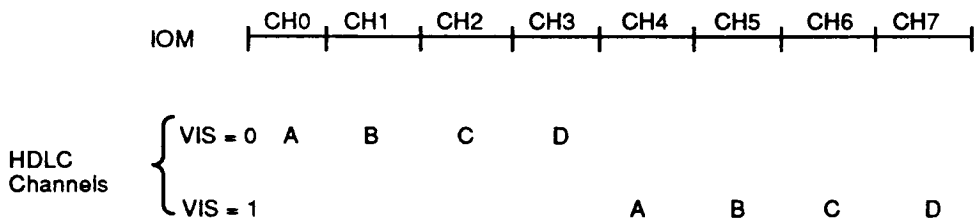
Figure 3. Position of Time Slot for Different Channel Widths as a Function of TSR Register Contents



a. Multiplexed Frame Structure of the IOM Interface (*n* = 8)



b. Assignment of HDLC Channels in IOM Mode

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Figure 4. IOM Interface and HDLC Channels

HDLC Communication Functions

Basic HDLC Functions

Each of the four controller channels handles the following basic HDLC functions.

Receive direction:

- Flag detection.
  A zero followed by six consecutive ones and another zero is recognized as a flag.
- Zero delete.
  A zero after five consecutive ones within an HDLC frame is deleted.
- CRC checking.
  The CRC field of an HDLC frame is checked according to the generator polynomial X^{16} $X^{12}+X^5+1$.
- Check for abort.
  Seven or more consecutive ones are interpreted as an abort sequence.
- Check for idle.
  Fifteen or more consecutive ones are interpreted as idle, and reported to the processor via a status bit.
- Minimum length checking.
  Reception of frames with less than three bytes between opening and closing flag is not reported to the microcontroller.

Transmit direction:

- Flag generation.
  A flag is generated at the beginning and at the end of every frame.
- Zero insert.
  A zero is inserted after five consecutive ones within an HDLC frame.
- CRC generation.
  The CRC field of the transmitted frame is generated according to the generator polynomial $X^{16}+X^{12}+X^5+1$.
- Abort sequence generation.
  An HDLC frame may be terminated with an abort sequence under software control or due to a FIFO underrun condition.
- Interframe time fill.
  As interframe time fill, either flags or idle (continuous 1s) may be transmitted.

Reception and Transmission Functions

FIFO Structure

Each HDLC controller uses a 64-byte FIFO per direction for the intermediate storage of data packets. All data bytes between the opening flag and the CRC field of an HDLC frame are passed through the FIFO.

The Receive and Transmit FIFOs are both divided in two blocks of 32 bytes each: one accessible to the microcontroller and one inaccessible to the microcontroller. While the microcontroller is reading (Receive FIFO) or writing (Transmit FIFO) data in one 32-byte block, the other block is filled (Receive FIFO) or emptied (Transmit FIFO) by the IDEC. Therefore, the length of the received or transmitted frame is not limited by the FIFO size.

Reception of Frames

Before a receive frame is stored, its address (the first byte following the opening flag) may optionally be compared against three fixed values.

SAPG	Group SAPI	63_D
SAPS	Signaling SAPI	0_D
SAPP	Packet SAPI	16_D

Each address compare may be individually enabled or disabled for each HDLC channel via bits AC0, 1, 2, 3 (ACR register).

Table 4. Address Compare Logic

SCM	SCG	SCS	SGP	Effect	
0	0	0	0	Accept all frames	
	0	0	1	Reject frames with	SAPP (16_D)
	0	1	0		SAPS (0_D)
	0	1	1		SAPS (0_D) and SAPP (16_D)
	1	0	0		SAPG (63_D)
	1	0	1		SAPG (63_D) and SAPP (16_D)
	1	1	0		SAPG (63_D) and SAPS (0_D)
	1	1	1		SAPG (63_D), SAPS (0_D) and SAPP (16_D)
1	0	0	0	Reject all frames	
	0	0	1	Accept frames with	SAPP (16_D)
	0	1	0		SAPS (0_D)
	0	1	1		SAPS (0_D) and SAPP (16_D)
	1	0	0		SAPG (63_D)
	1	0	1		SAPG (63_D) and SAPP (16_D)
	1	1	0		SAPG (63_D) and SAPS (0_D)
	1	1	1		SAPG (63_D), SAPS (0_D) and SAPP (16_D)

The effect of a match is programmable as shown in Table 4. In the table it is assumed that the address compare enable bit (AC) is set for the channel in question. If AC=0, all valid receive frames in that channel are accepted.

In the case of a frame less than 64 bytes long, the whole frame may be stored in the Receive FIFO. After the first 32 bytes have been received, the device prompts the microcontroller to read data from the receive FIFO (Receive Pool Full (RPF) interrupt). Having done this, the microcontroller releases the FIFO. This is effected by the Receive Message Complete (RMC) software command, after which the rest of the frame, when ready, is made available to the microcontroller (Figure 6).

When a whole frame shorter than 32 bytes, or the final part of a frame longer than that becomes available, this is indicated by a RME (Receive Message End) interrupt status, instead of RPF (Receive Pool Ready).

In the case of frames at least 64 bytes long, the microcontroller will repeatedly be promoted by interrupt to read out the FIFO by blocks of 32 bytes (except possibly the final block). Again, after reading a block, the microcontroller acknowledges the data by a software command and thus releases the FIFO. If this is not done before an additional 32 data bytes are received, the next data byte will lead to a data overflow condition.

In the case of several shorter frames up to seventeen may be stored inside the HDLC controller. After an interrupt (RME), one frame is available in the FIFO for the microcontroller to read. Up to sixteen other frames may be stored in the meanwhile in the upper half of the FIFO (Figure 7a). When the microcontroller releases the current data block from the FIFO by software command, the next frame becomes available and the corresponding space is freed in the upper half for a subsequent frame(s) (Figure 7b).

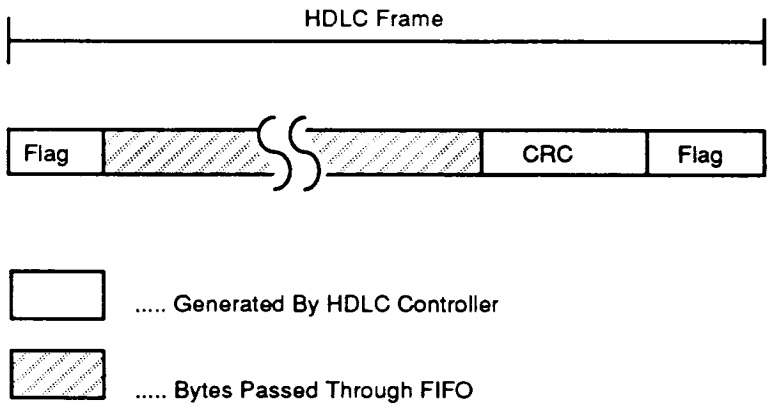

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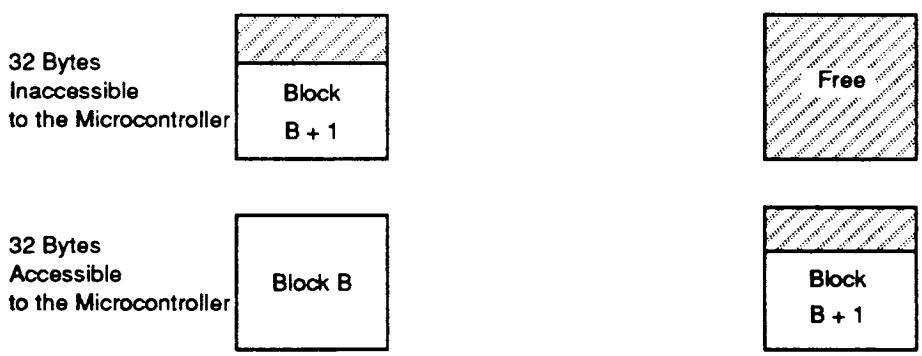
Figure 5. HDLC Frame Structure

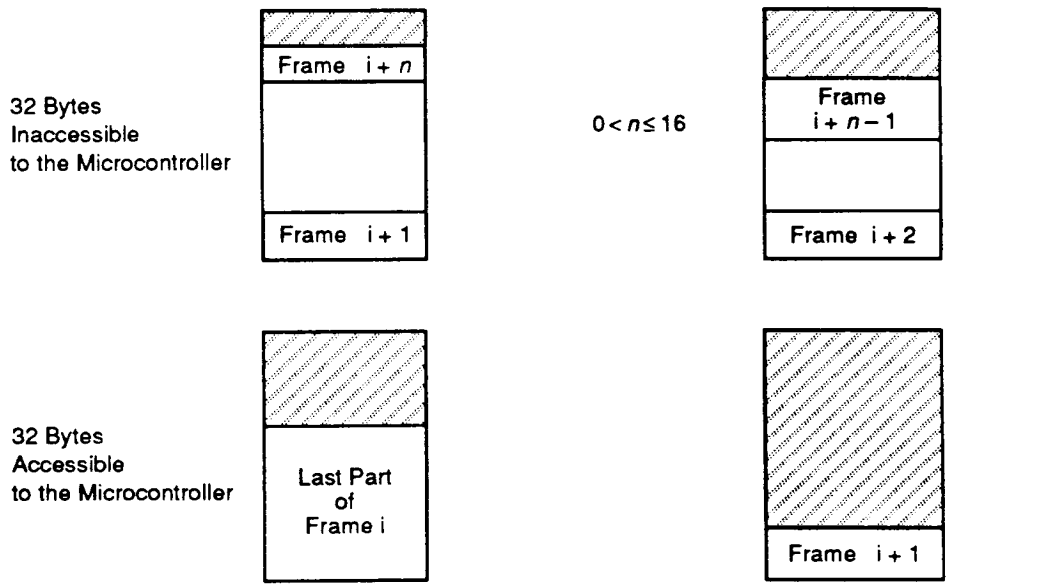


a. Prior to Microcontroller Acknowledgment

b. After to Microcontroller Acknowledgment

11134C–008

Figure 6. Receive FIFO in the Case of a Frame no Longer than 64 Bytes



a. Prior to Microcontroller Acknowledgment **b. After Microcontroller Acknowledgment**

11134C–009

Figure 7. Receive FIFO in the Case of Short Frames

The interrupts accumulating in the process are incorporated into a queue and transferred one by one to the microcontroller along with additional information about the frame. In particular, the frame length is stored in a register. Information such as frame aborted yes/no, CRC error yes/no, data overflow yes/no, is included in an extra byte stored in the FIFO after the last byte of the corresponding frame.

Every interrupt has to be acknowledged by the microcontroller. A full FIFO at the beginning of a frame will lead to a frame overflow condition.

If the microcontroller does not wish to preserve an incoming frame, the possibility exists to ignore it. When the corresponding command (RMD) is issued, the part of the frame stored is deleted and the rest of the entire frame will be ignored.

Transmission of Frames

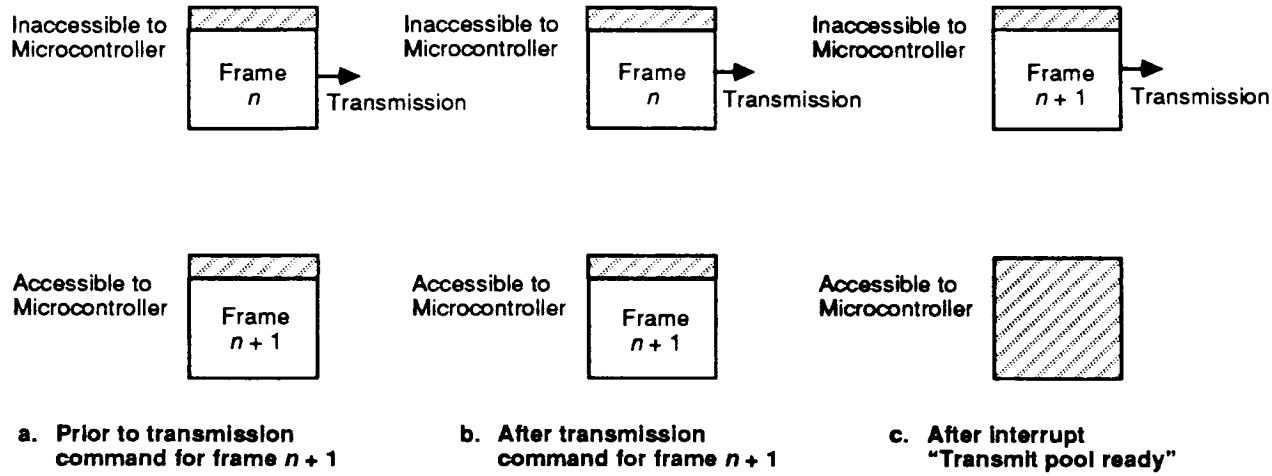
2 × 32 bytes of intermediate storage are provided per HDLC controller in the transmit direction. After up to 32 bytes have been written to the FIFO, transmission is started by a software command (XHF). If the previous transmission is still underway when a new transmission command is issued, microcontroller access to the FIFO will be blocked until the first transmission is completed (Figure 8). This means that at most one complete frame may be written to the FIFO before a transmission has to be initiated. If a transmission request does not include a frame end indicator (XME), the HDLC controller will request the next data block via an interrupt if the FIFO contains not more than 32 bytes. This procedure will be repeated until the microcontroller indicates that the frame is to be closed.

In the case when this indication is not given and there is no more data ready for transmission, the frame is terminated with an abort sequence and the microcontroller is notified via a Transmit Data Underrun (XDU) interrupt. The frame may also be aborted per software command. The completed transmission of an HDLC frame is reported by a Transmit Pool Ready (XPR) interrupt status.

Collision Control and Switching Functions

The IDEC possesses flexible collision control capabilities which are totally transparent to the microcontroller. The collision control modes allow using the circuit in statistical multiplexing applications or in centralized or decentralized packet switches. Each of the four HDLC controllers is individually programmed in one of four modes by its own register bits CMS1–0 (Collision Mode Select).

Table 5 lists the four collision modes that can be selected, along with the auxiliary I/O lines used in each case. The outputs SD1X and SD2X can be selected to be of the open-drain or of the push-pull type.



11134C–010

Figure 8. Transmit FIFO

Table 5. Collision Modes of the IDEC

CMS1	CMS0	Description	Auxiliary I/O			
			Data In	Data Out	Coll In	Coll Out
0	0	Unconditional transmission				
0	1	Slave mode			CDR	
1	0	Multi-master mode			CDR	
1	1	Master mode	CDR	SD1X		SD2X

Unconditional Transmission Mode

The HDLC controller transmits frames without collision detection on the transmit line (time channel).

Slave Mode

The input CDR (Collision Data Receive) is used to control transmission of frames. This input is common to all HDLC controllers which are programmed in the slave mode.

Transmission is inhibited by a Low on the CDR input. If CDR becomes Low during the transmission of a frame, the frame is aborted by the HDLC controller, and the data output is set to high impedance. (Refer to Figure 9.)

The state of CDR is evaluated by the HDLC controller only in the time channel used for transmission by that controller.

When CDR is switched High, interframe time fill is marked in the transmit-time channel if no transmission request is pending; otherwise, transmission starts at the first available instant. Transmission of a previously aborted frame is automatically restarted by the HDLC controller if the beginning of the frame is still available in the transmit FIFO. Otherwise, an interrupt to the microcontroller indicates that the transmission has failed.

The slave mode is applicable in all of the basic operation modes, in both single-connection and in quad-connection applications. However, there is only one CDR line. This could be a restriction in the following cases:

- The IDEC is configured in the quad-connection common control mode and more than one HDLC controller is operated in the slave mode;
- When a time slot is used by more than one HDLC controller in the slave mode.

In both cases, more than one controller is evaluating the CDR line during the same time interval, and when CDR goes Low, they all stop transmitting.

Multi-Master Mode

In the multi-master mode the controllers perform a bus access procedure and collision detection in their assigned time channel(s). As a result, any number of IDECs can be assigned to one physical channel, where they perform statistical multiplexing.

Collisions are detected by automatic comparison of each transmitted bit with the bit received over the CDR input. For this purpose, a logical and of the bits transmitted by parallel controllers is formed and connected to the input CDR. This may be implemented most simply by defining the output line driver to be of the open drain type (ODS = 1). Consequently, the logical and of the outputs is formed by simply tying them together (wired or). The result is returned to the CDR input of all parallel circuits.

The multi-master mode is applicable in all operating modes, in both single-connection and quad-connection applications. In the quad-connection mode, those output lines (SD3X–SD0X) for which this collision mode is selected may be connected to CDR. The four HDLC controllers may either be programmed to transmit in separate time channels or in the same time channel. A prerequisite for the multi-master mode is that the inter-frame time fill used is idle.

During multi-master operation when a mismatch between a transmitted bit and the bit on CDR is detected, the HDLC controller stops sending further data and its output is set to high impedance (Refer to Figure 10). As soon as it detects the transmit bus to be idle again, the controller automatically attempts to re-transmit its frame. By definition, the bus is assumed idle when x consecutive ones are detected in the transmit channel. Normally x is equal to 8.

An automatic priority adjustment is implemented in the multi-master mode. Thus, when a complete frame is successfully transmitted, x is increased to 10, and its value is restored to 8 when a row of ten 1s is detected on the bus. Furthermore, transmission of a new frame may be started by the HDLC controller after the tenth 1. This multi-master, deterministic-priority management ensures an equal right of access of every HDLC controller to the transmission medium, thereby avoiding blocking situations.

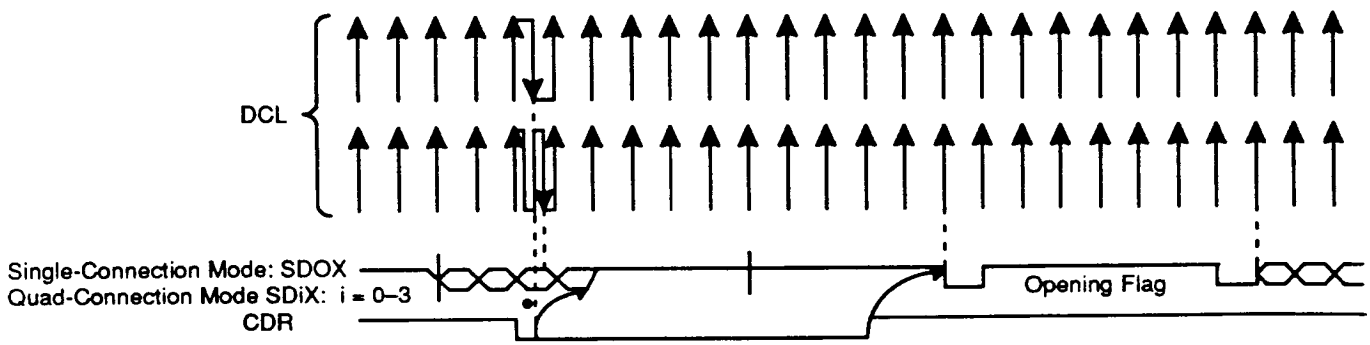
Master Mode

The master mode requires three auxiliary connections; data input CDR, data output SD1X, and collision data out SD2X. This mode is applicable only in single-connection operation. In the master mode (refer to Figure 11), the controller performs two functions:

- Switching of data packets between the main connection SD0X, SD0R and the auxiliary input and output (CDR, SD1X).
- Resolution of collisions between data from the auxiliary connection and HDLC frames from the local microcontroller.

In the TS mode, the time slot programmed via the Time-Slot Select Register (TSR) applies simultaneously to SD0X/SD0R and to the auxiliary lines CDR, SD1X, SD2X. In the IOM mode, the TSR register selects a time channel on the auxiliary connections CDR, SD1X and SD2X only (however, the channel width selected should be two bits, as on the IOM interface, to ensure a correct data throughput).

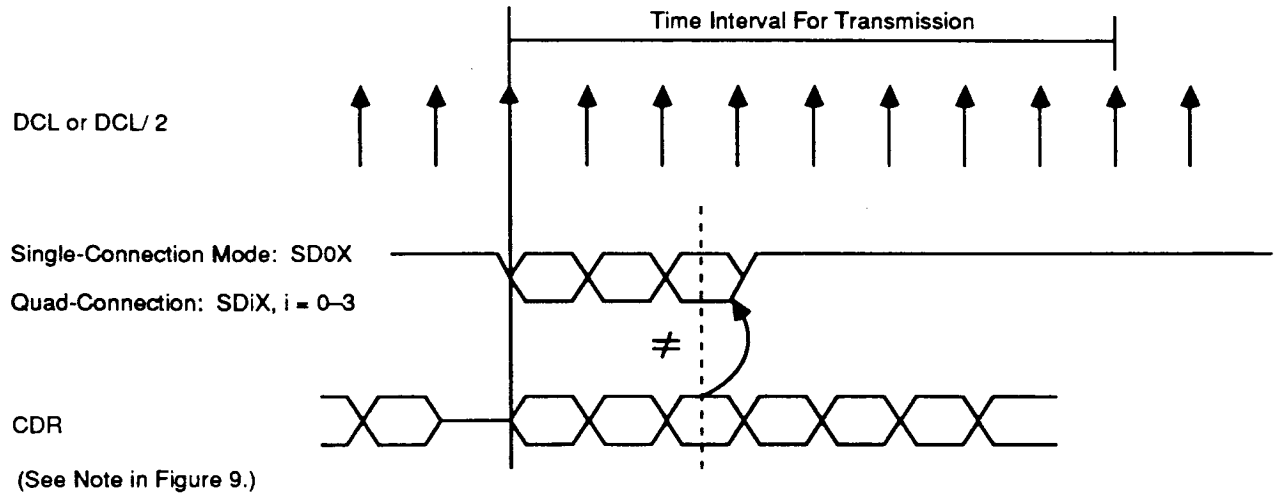
The switching of data from SD0R to SD1X is transparent. The switching of data from CDR to SD0X depends on the state of the HDLC controller (transmit/no transmit) and on selected priorities, as follows.



Note: The CDR input is evaluated:
—At the falling edge of DCL, for a DCL rate equal to the data rate.
—At the falling edge of DCL immediately preceding the rising edge; used for transmission for a DCL rate twice the data rate.

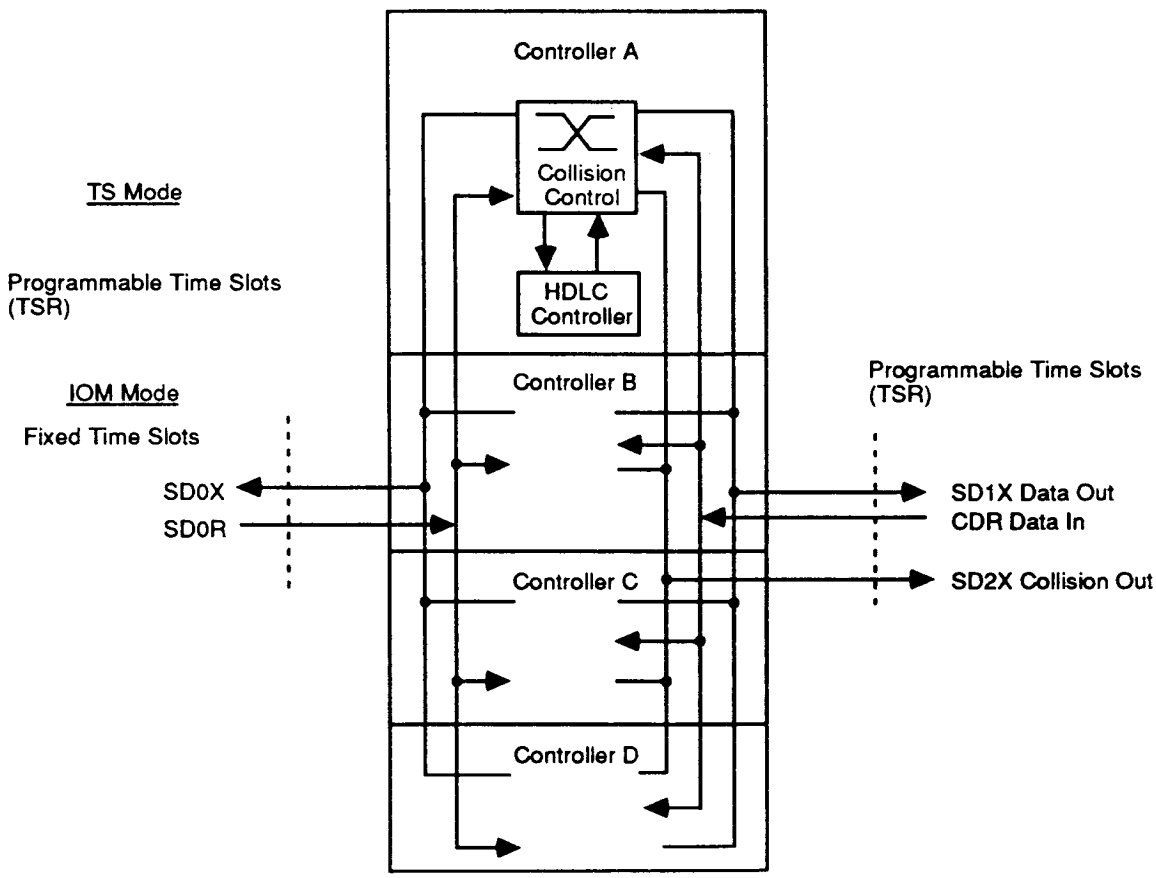
11134C–011

Figure 9. Transmission Control in the Slave Mode (Example)



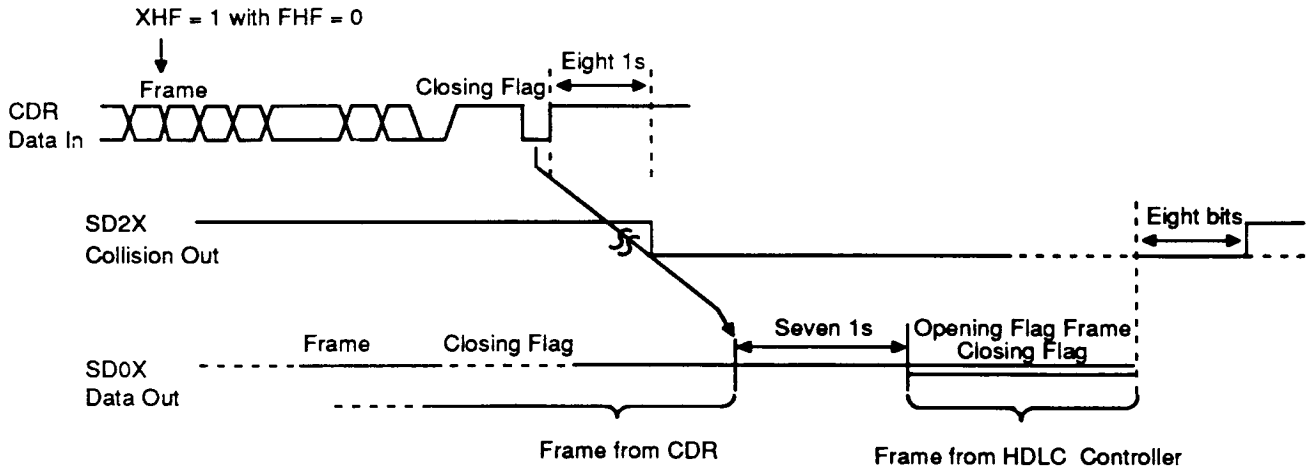
11134C–012

Figure 10. Collision Detection In the Multi-Master Mode (Example)

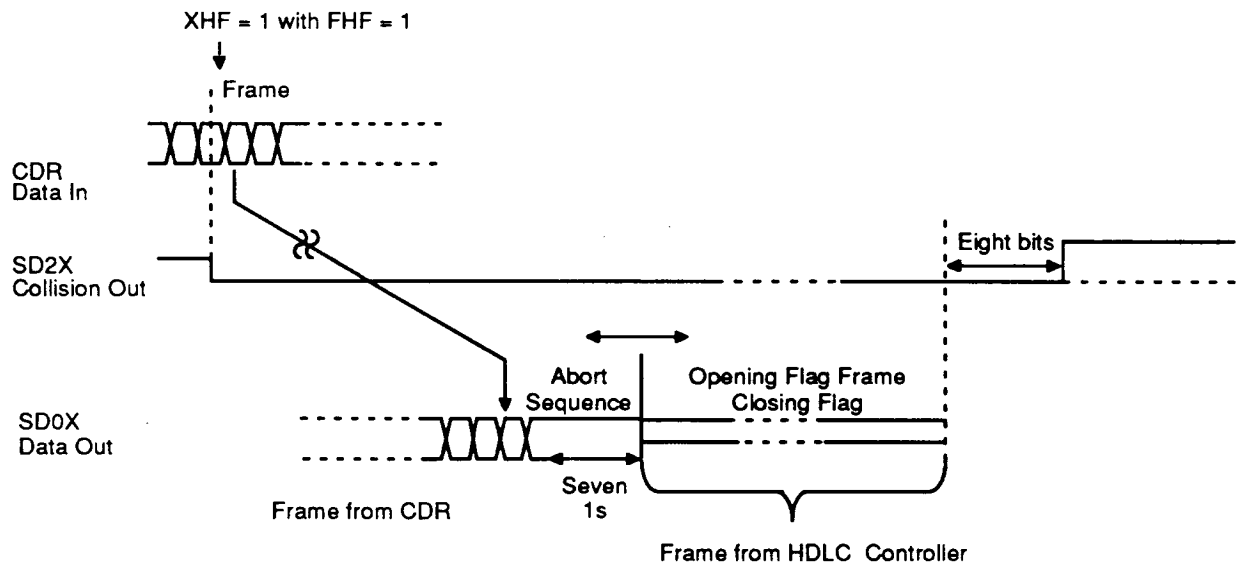


11134C–013

Figure 11. I/O Connections In the Master Mode



a. XHF Comm and with FHF = 0



b. XHF Command with FHF = 1

11134C–014

Figure 12. Collision Resolution in the Master Mode with Programmable Priority (FHF)

When no transmission command is issued to the HDLC controller, data is transparently switched through from CDR to SD0X. When a transmit request is issued, but the Force HDLC Frame (FHF) bit is not set to 1, the data currently being received (if any) on CDR is given priority. The HDLC controller starts transmitting its frame on SD0X only after CDR is detected to be idle; in other words, when a row of eight 1s is observed on CDR. Simultaneously, SD2X is set Low to indicate that no data will be accepted on CDR input data line.

Figure 12a shows the time relation between CDR (data in) and SD2X (collision out) as well as the logical relation between SD2X and SD0X (data out). The figures are simplified in that the grouping of bits into time slots on SD0X, and on SD2X/CDR is not depicted.

When a transmit command is issued and the Force HDLC Frame (FHF) bit is set to 1, the frame currently being received on CDR is aborted. Seven 1s are appended to the last bit of the aborted frame on SD0X,

after which the HDLC controller starts transmitting its frame (Figure 12b).

In both cases, SD2X is set High again after a delay of eight bit-times following the last 0 of the closing flag, to indicate that data is accepted on the CDR input data line. However, if a new transmit command is issued before that time, SD2X remains Low and transmission of the new frame starts immediately after the eighth 1.

Note on data delay in Master Mode

The data bits are switched from SD0R to SD1X and from CDR to SD0X with a minimum delay as shown in Figures 13 and 14.

Two cases are distinguished:

a. TS mode.
   In this case the time slots on SD0R/SD0X and on CDR/SD1X are identical. The data delay from CDR to SD0X is one bit, whereas the delay from SD0R to SD1X is two bit-times.

b. IOM mode with identical channel (time slot) on SD0R/SD0X and CDR/SD1X. This case is identical to the previous one.

c. IOM mode with a time slot on CDR/SD1X which does not coincide with the IOM channel bits on SD0R/SD0X. In this case, the data bits undergo (in addition to the inherent delay due to the different bit positions) a delay of one bit-time from CDR to SD0X, whereas no additional bit delay is introduced when going from SD0R to SD1X.

Test Functions

A test loop is provided in each of the four HDLC controllers of the IDEC. When the test loop is activated, the input and the output of the HDLC channel are connected together. The test loop control is independent for each HDLC channel (bit TLP).

The test loop is either transparent (forward data is outputted on the line) or non-transparent (forward data is not outputted on the line), depending on the selected model. In the quad-connection common control mode and in the single-connection IOM mode, the loops are transparent. In the other cases they are non-transparent. During a non-transparent loop, the data output is high impedance inside the assigned time channel.

Applications

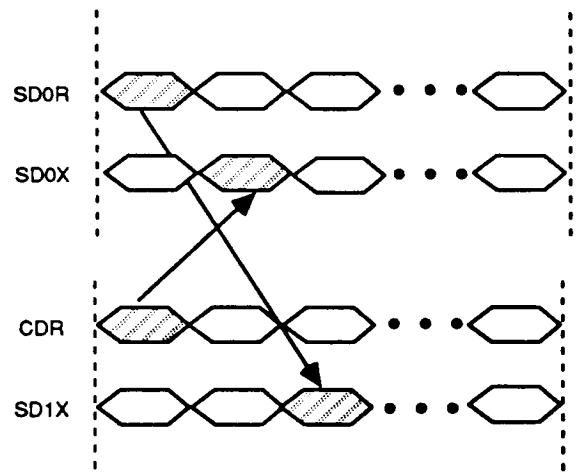
Communication Multiplexers

The four independent serial HDLC communication channels implemented in the IDEC make the circuit suitable for use in communication multiplexers. The collision detection/resolution capability of the circuit allows statistical multiplexing of packets in one or several physical data communication channels; for example, in DMI (mode 3) applications.

Centralized Signaling/Data Packet Handlers

The IDEC can be used in central packet handlers of ISDN networks to process signaling or packet data of four ISDN subscribers. In this application, it may be used with or without the Am2055 Extended PCM Interface Controller (EPIC™).

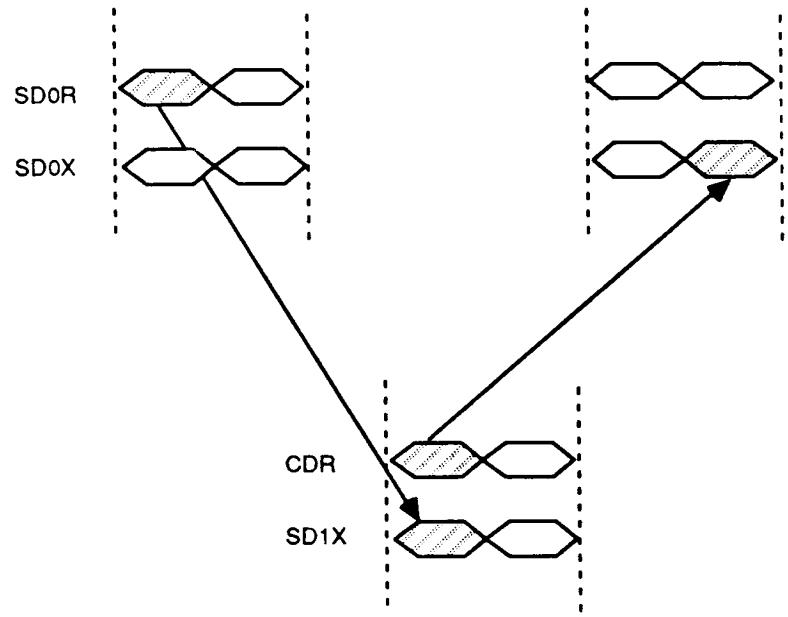
The IDEC can be connected to the IOM interface of the EPIC that is connected to the PCM system highway. The EPIC implements concentration and time slot assignment functions. As an alternative, the IDEC may be directly connected to PCM highways (Figure 15).



Bit delay for coinciding channel/time slot position on SD0R/SD0X and on CDR/SD1X.

11134C–015

Figure 13. Bit Delay from SD0R/CDR to SD1X/SD0X (Minimum Delay)



Bit delay for non-identical channel/time slot position on SD0R/SD0X and on CDR/SD1X (possible only when SD0R/SD0X is an IOM interface).

11134C–016

Figure 14. Bit Delay from SD0R/CDR to SD1X/SD0X

The size (from 1 to 8 bits) and the position of the time slot associated with each HDLC controller are software programmable. In addition to the receive and transmit data highways, the IDEC accepts a third input connection for collision detection purposes. The mode of collision detection is programmable. A collision highway (or time slot) can be used for remote collision control, as a clear to send lead, or for local contention resolution among several IDECs.

Line Cards in Decentralized or Mixed Signaling/Data Packet Handling Architectures

The IDEC can be used on peripheral line cards to process D-channel packets for ISDN subscribers. An Am2055 Extended PCM Interface Controller (EPIC) has the Layer 1 controlling capacity and a B-channel switching capacity for a total of 32 subscribers. The B- and D-channels and the control information for eight subscribers are carried over one IOM interface. Thus a line card dimensioned for 32-ISDN subscribers may employ up to eight IDECs, two for each IOM connection (Figure 16). The Am82525 High Level Serial Communication Controller (HSCX™) with two HDLC channels, or another IDEC, may be used to transmit and receive signaling via the system highway in a common channel. Again, such a common channel may be shared among several line cards, due to the statistical multiplexing capability of these controllers.

In completely decentralized D-channel processing architectures, the processing capacity of a line card is usually dimensioned to avoid blocking situations even under maximum conceivable D-channel traffic conditions. It may sometimes be more advantageous to perform p-packet handling in a centralized manner while keeping s-packet handling on the line cards. A statistical increase in p-packet traffic then has no effect on the line card and can be easily dealt with by one of the modular architectures for a central packet handler shown in the previous section. A more effective sharing of the total p-packet handling capacity is the result, especially in a situation where p-packet traffic patterns vary widely from one subscriber group to another.

The use of IDEC in the mixed D-channel processing architecture is illustrated in Figure 17. The additional transparent data connections supported by the IDEC enable a merging of p- and s-packets into one D-channel. Possible collision situations are dealt with by the IDEC which uses either the additional collision detect line (Figure 17a), or a time slot on the system highway (Figure 17b) from the line card to the central packet handler.

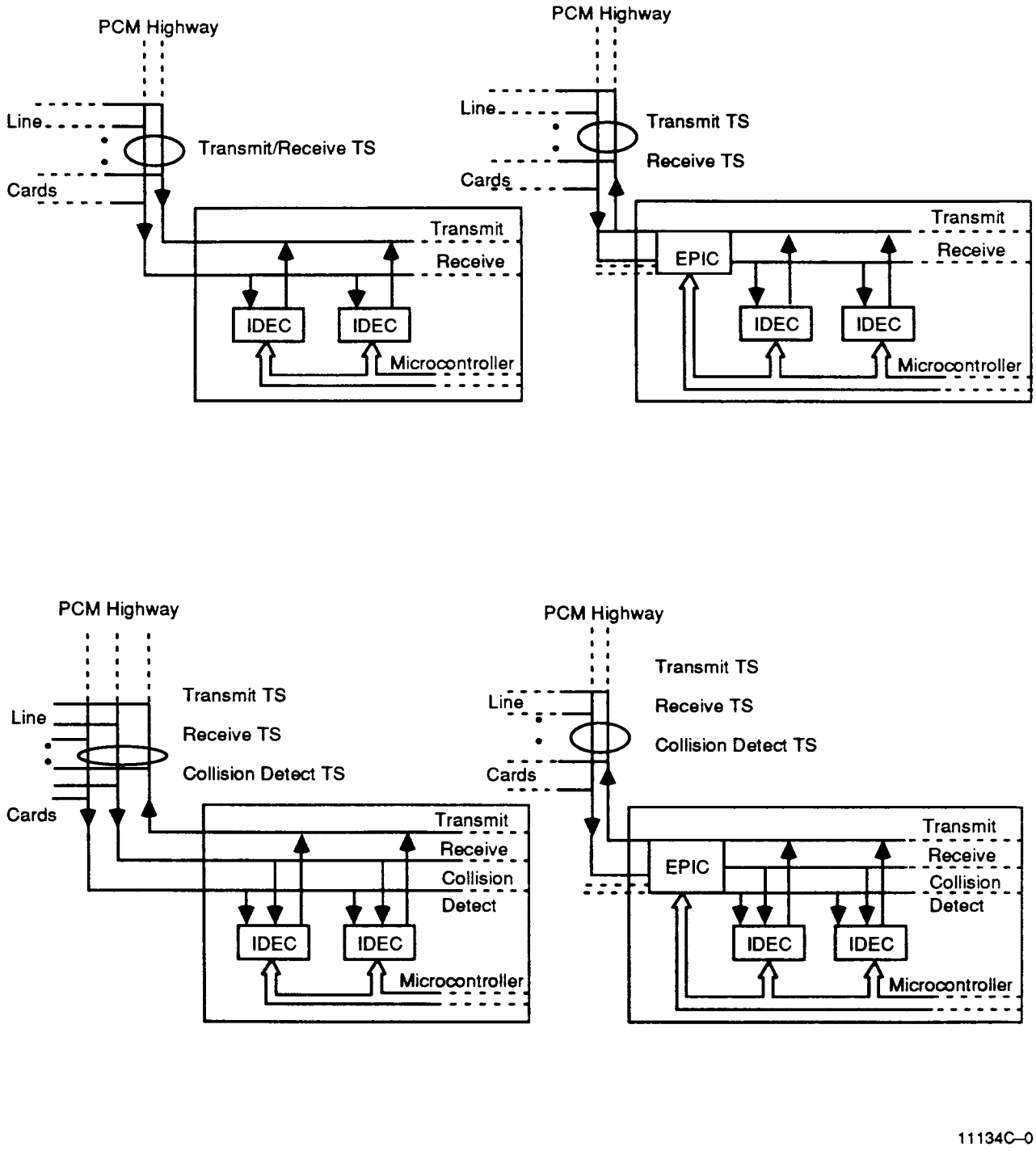
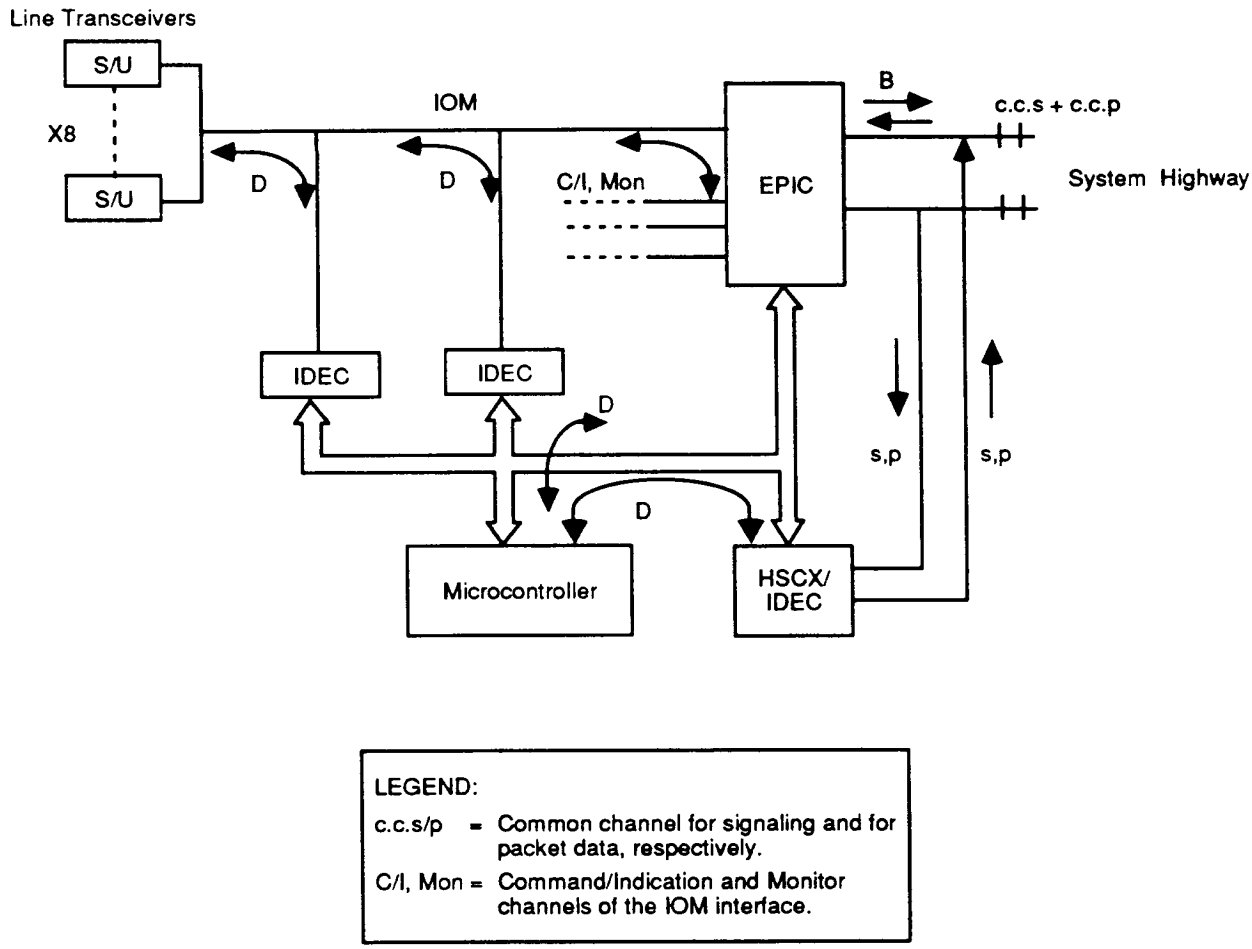
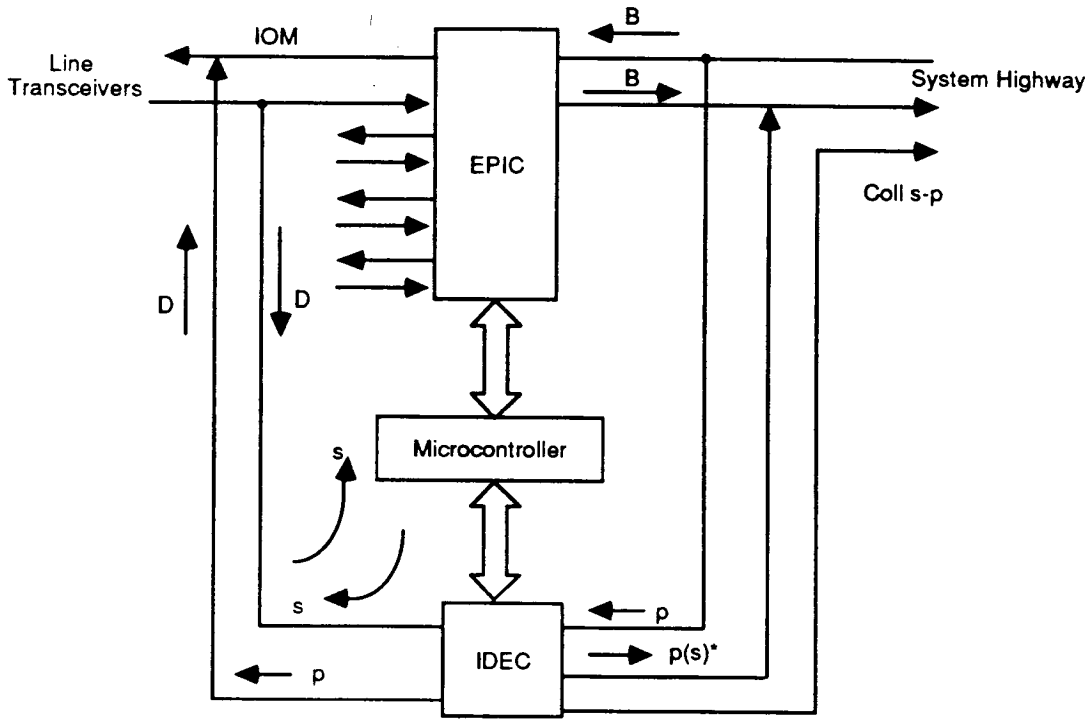


Figure 15. Use of IDEC in Central Signaling/Data Packet Handlers



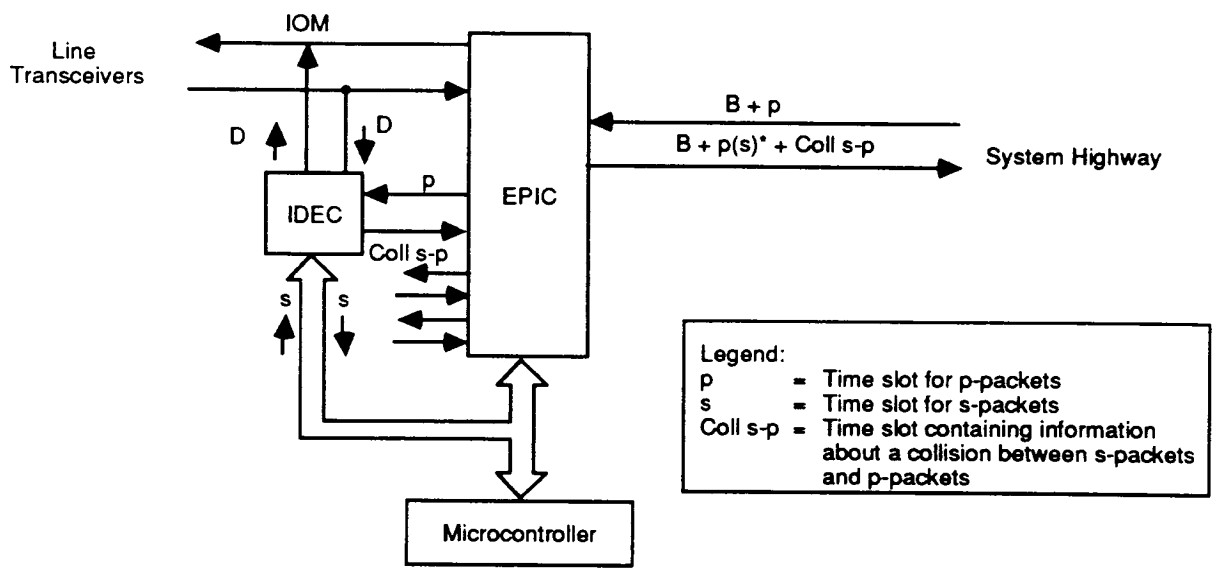
11134C–018

Figure 16. Line Card in a Decentralized D-Channel Handling Architecture



*s-packets will be discarded by the receiver

a. Additional Collision Detect Line



b. Time Slot on the System Highway

11134C–019

Figure 17. IDEC on a Line Card in a Mixed D-Channel Processing Architecture

OPERATIONAL DESCRIPTION

Microprocessor Interface Operation

There are three microcontroller interface types for IDEC:

1. Motorola type with control signals $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$; Address bus A6–A0; Data bus AD7–AD0.
2. Intel non-multiplexed bus type with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$; Address bus A6–A0; Data bus AD7–AD0.
3. Or of the Intel multiplexed address/data bus type with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE; Address/Data bus AD7–AD0.

For a non-multiplexed bus including the Motorola type microprocessor interface the PLCC 44 package of the IDEC needs to be used, since only this package provides the additional pins for a separate 7-line address bus.

The ALE input is used to control the interface type as follows:

ALE tied to V_{DD} ⇒ type (1)
ALE tied to V_{SS} ⇒ type (2)
Edge on ALE ⇒ type (3)

The occurrence of an edge on ALE, either positive or negative, at any time during the operation immediately selects interface type (3). A return to one of the other interface types is possible only if a hardware reset is issued.

Reset

After a hardware reset (pin RES), the configuration/command register bits are zeroed. No interrupts are active and all outputs are in a high impedance state. Table 7 sums up the state of the IDEC immediately after a hardware reset has been applied.

Table 6. Microcontroller Interface Summary

ALE	Interface	Bus Type	Address Bus	Data Bus	Control Pins					
					DIP-28			PLCC-44		
					11	5	4	17	8	7
Tied to V_{DD}	Motorola	Non-multiplexed	A6–A0	AD7–AD0	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{CS}$	R/$\overline{W}$	$\overline{DS}$
Tied to V_{SS}	Intel	Non-multiplexed	A6–A0	AD7–AD0	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$
Switching	Intel	Multiplexed	AD7–AD0	AD7–AD0	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$

Table 7. State of IDEC after a Hardware Reset

Register	Register Name	Value after Hardware Reset (hex)	Meaning
Common	ACR	00	Address comparison disabled.
Registers	CCR	00	Single connection TS mode interrupt vector may be read on AD bus bits 3–0. Bits per frame: 257 to 512. Bit rate is equal to clock rate. Output drivers are of the push-pull type.
	VISR	00	No interrupt from any IDEC channel.
	VISM	00	All channel interrupts are enabled.
Individual	ISTA	00	No interrupts from channel i.
Registers	ISM	00	All channel i interrupts enabled.
i = A,B,C,D	STAR	50	Transmit FIFO is ready to be written to. Receive line is idle.
	CMDR	00	No commands.
	MODE	00	Test loop not active. No collisions will be detected (unconditional transmission). Interframe time fill = idle. Receiver deactivated. Channel i disabled (high impedance output). Channel capacity is 2-bits/time slot.
	RFBC	00	Zero bytes received.
	TSR	00	Time slot 0 selected.

Table 8. Initialization of IDEC (Common Bits)

Function	Register	Bits	Effect
Configuration	CCR	MDS1–MDS0	Basic configuration and timing mode
Serial interface characteristics	CCR	ODS CRS	Output driver type is open-drain or push-pull Clock rate = 1 or 2x data rate
		BNS	Number of bits per PCM frame
Interrupt configuration	VISM CCR	MIC3–MIC0 VIS	Mask any HDLC channel(s) VISR may be read on AD bus bits 3–0 or 7–4
HDLC address recognition features	ACR	SCM SCG, SCS, SCP AC3–AC0	Address compare mode: accept/reject Selection of compare addresses Address compare on/off for HDLC channel 0, 1, 2, 3

Table 9. Initialization of HDLC Channels (Channel-per-Channel)

Function	Register	Bits	Effect
Serial interface	MODE	CMS1–CMS0 CCS1–CCS0	Collision mode Channel capacity
	TSR	TSR7–TSR0	Time slot
HDLC controller	MODE	ITF TLP CAC	Interframe time fill pattern Test loop Activate channel (enable receiver + transmitter, enable data outputs)
		RAC	Activate HDLC receiver

INITIALIZATION

The purpose of the initialization is to set the IDEC into a state where it is able to correctly transfer HDLC frames and to manage collisions according to the requirements of the application.

The initialization process is divided into two phases. First, the common settings are determined via the registers CCR and VISM. These registers determine the number of HDLC channels used, the serial interface configuration, and common characteristics of the serial input/output connections (Table 8).

During the second phase, each of the HDLC channels is initialized via its own register set as shown in Table 9.

The optional address comparison mode for each HDLC channel is selected by programming the ACR register, located in the common address space (Table 8).

INTERRUPT STRUCTURE

Special events are reported to the processor by an interrupt logic in the IDEC. This logic allows the connection of more than one IDEC to one interrupt input of a microcontroller.

The interrupt structure of the IDEC is depicted in Figure 18. Each HDLC channel of the circuit has its own Interrupt Status Register (ISTA) where up to five possible interrupt causes may be read directly. When an interrupt occurs in one of the HDLC channels, the corresponding bit is set in the ISTA register and the interrupt line (INT) is activated. Simultaneously, a bit in the Vectored Interrupt Status Register (VISR) is set that indicates which of the four HDLC channels initiated the interrupt. Thus, to determine the cause of an interrupt, the microcontroller performs successively a read of the VISR register (address 36/3F) and a read of the ISTA register which was indicated by the contents of VISR.

A read of the ISTA clears the register and deactivates the $\overline{INT}$ line.

The position that the four bits of the VISR occupy on the AD7–AD0 bus when the register is read, is programmable via the Vectored Interrupt Selection bit (VIS, CCR register). Thus, when VIS = 0, the VISR bits are read on AD bit positions 3–0, and when VIS = 1, VISR bits are read on AD bit positions 7–4. Unoccupied bit positions on the bus remain in a high impedance state.

The bits in VISR can be selectively masked by setting the corresponding bits in the Vectored Interrupt Status Mask (VISM) register to prevent one or several controllers from generating an interrupt. In that case, interrupts remain internally stored (pending) but are not displayed in the VISR or ISTA registers. Further, ISTA interrupts pertaining to a particular channel may be selectively masked via the Interrupt Status Mask register of that channel. Pending interrupts cause the $\overline{INT}$ line to be activated, and they will be reported via ISTA (and VISR) only when the mask bits in ISM (and VISM) have been reset.

PROCESSING

After being initialized via the configuration/mode registers listed in Tables 8 and 9, the IDEC is operational.

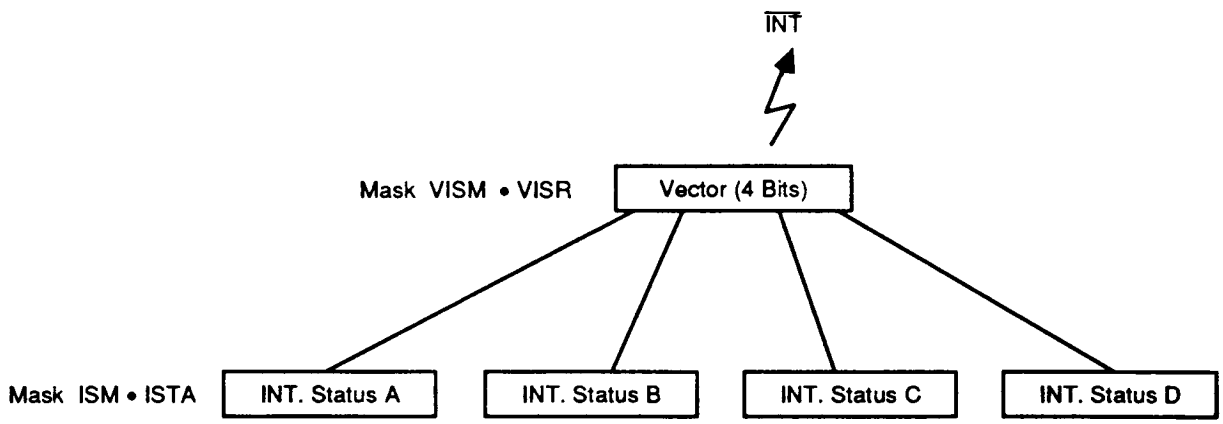
The control of the data transfer is performed by commands from the microcontroller written in the Command Register (CMDR). Events pertaining to the data transfer are reported by the Interrupt Status Register (ISTA) pointed to by the Vectored Interrupt Status Register (VISR). Other events that do not lead to interrupts may be monitored with the Status Register (STAR), and information about the receive frames is found in the RFIFO and in the Receive Frame Byte Counter (RFBC) Register.

The powerful FIFO logic, which consists of a 2 × 32 byte receive and a 2 × 32 byte transmit FIFO per channel, as well as an intelligent FIFO controller, builds a flexible interface to the upper protocol layers implemented in the microcontroller.

RECEIVE FRAME PROCESSING

Reception of HDLC frames with three or more bytes between the opening and closing flags is always reported to the microcontroller if address comparison is not enabled (AC = 0). If address comparison is enabled, the reception of the frame is dependent on the first byte of the received HDLC frame address field and the selected features of the address compare function (Table 4). All bytes between the opening flag and the CRC field are stored in the RFIFO.

When the frame (excluding the CRC field) is not longer than 31 bytes, the whole frame is transferred in one block. The reception of the frame is reported by the Receive Message End (RME) interrupt. The length of the frame can be read out from an 8-bit register (RFBC). A status byte is appended to the data in the RFIFO after an RME interrupt. It includes information about the frame, such as frame aborted yes/no or CRC valid yes/no. The frame and the status byte remain stored until the microcontroller issues an acknowledgment (Receive Message Complete: RMC).



11134C–020

Figure 18. Interrupt Structure of the IDEC

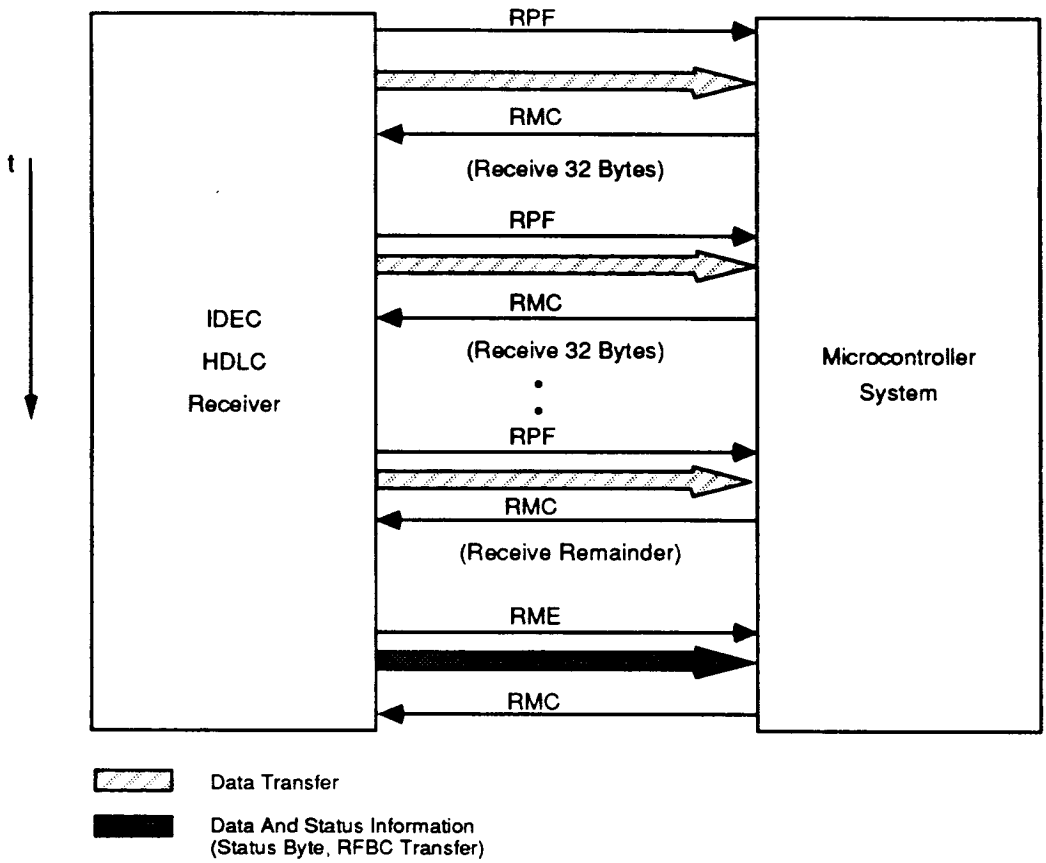


Figure 19. Reception of an HDLC Frame

A frame longer than 31 bytes is transferred to the microcontroller in blocks of 32 bytes plus one remainder block of length 0 to 31 bytes plus status byte. The reception of a 32 byte block is reported by a Receive Pool Full (RPF) interrupt and the data in RFIFO remains valid until this interrupt is acknowledged (RMC). This process is repeated until the reception of the remainder block reported by RME (Figure 19). Bits 4–0 of the RFBC register represent the number of bytes stored in the RFIFO (including the status byte). Bits 7–5 indicate the total number of 32 byte blocks that were stored until the reception of the remainder block. Bits 7–5 do not overflow when the counter status 7 has been reached and indicate in this case a message length greater than 223 bytes.

The contents of the RFBC register are valid only after the occurrence of the RME interrupt, and remain valid until the microprocessor issues an acknowledgment (RMC). All receive interrupts accumulated in the meantime are stored (along with the status bytes and respective frame lengths) inside the controller and transferred one by one to the microcontroller after each RMC acknowledgment. If a frame could not be stored due to a full FIFO, the microcontroller is informed of this via the Receive Frame Overflow interrupt (RFO).

TRANSMIT FRAME PROCESSING

After checking the XFIFO status by polling the Transmit FIFO Write Enable (XFW) bit or after a Transmit Pool Ready (XPR) interrupt, up to 32 bytes may be entered by the microcontroller in XFIFO. Transmission of an HDLC frame is started when the Transmit HDLC Frame (XHF) command is issued. The HDLC controller will request another data block by an XPR interrupt if there are no more than 32 bytes in XFIFO and the frame close command bit (Transmit Message End XME) has not been set. When XME is set, all remaining bytes in XFIFO are transmitted, the CRC field and the closing flag of the HDLC frame are appended, and the controller generates a new XPR interrupt (Figure 20).

The microcontroller does not necessarily have to transfer a frame in blocks of 32 bytes. As a matter of fact, the sub-blocks issued by the microcontroller and separated by an XHF command can be between 1 and 32 bytes long.

If the XFIFO runs out of data and the XME command bit has not been set, the frame will be terminated with an abort sequence (seven 1s) followed by interframe time fill, and the microcontroller will be advised by a Transmit Data Underrun (XDU) interrupt. An HDLC frame may also be aborted by setting the Transmit Reset (XRES) command bit.

Table 10 gives a summary of possible interrupts from the HDLC controller and the appropriate reaction to these interrupts.

Table 11 lists the most important commands which are issued by a microcontroller by setting one or several bits in the Command Register (CMDR).

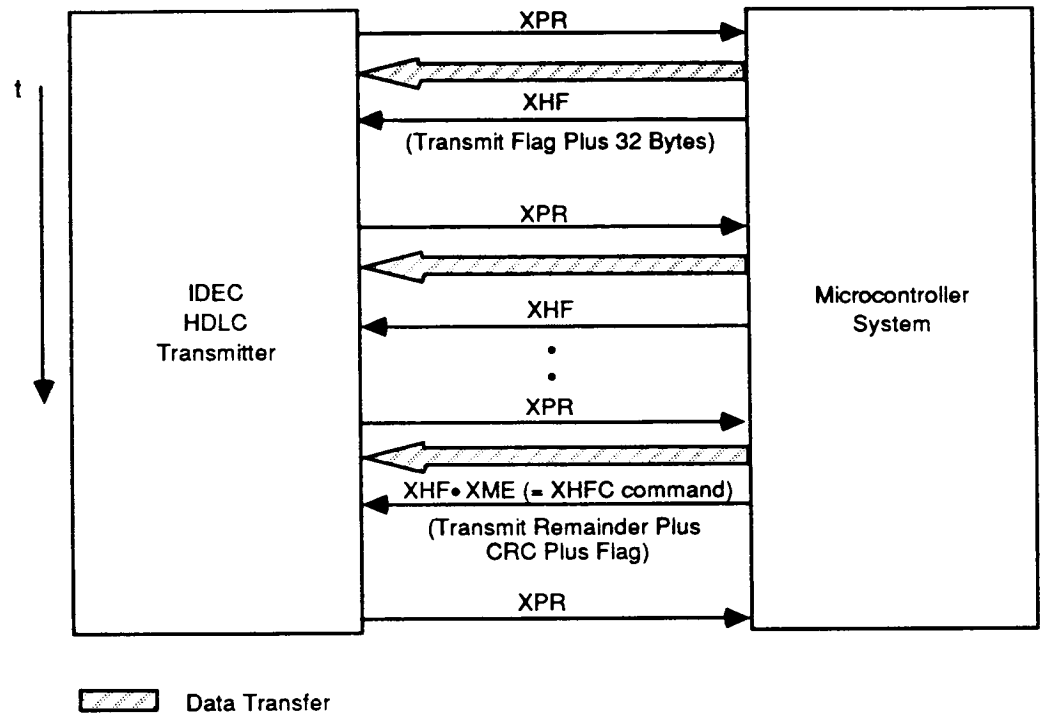


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Figure 20. Transmission of an HDLC Frame

Table 10. Possible Interrupt Causes and Reactions

Mnemonic	Meaning	Reaction
RPF	Receive Pool Full	Read 32 bytes from RFIFO and acknowledge with RMC.
RME	Receive Message End	Read RFBC 4–0 bytes from RFIFO and acknowledge with RMC.
RFO	Receive Frame Overflow	Error report for statistical purposes (loss of a complete frame). Probable cause: deficiency in software.
XPR	Transmit Pool Ready	Write data bytes in the XFIFO if the frame currently being transmitted is not finished or a new frame is to be transmitted, and issue an XHF (and possible XME) command.
XDU	Transmit Data Underrun	Acknowledged by a read of the ISTA. Possible causes: excessive software reaction times or transmit data collision.

Table 11. List of Commands

Mnemonic	HEX	Bit 7–0	Meaning
RMC	80	1000 0000	**Receive Message Complete**. Acknowledges a block (RPF) or a frame (RME) stored in the RFIFO.
RRES	40	0100 0000	**Reset HDLC Receiver**. The RFIFO is cleared and the receiver enters the hunt phase.
RMD	20	0010 0000	**Receive Message Delete**. The part of the frame in the RFIFO is deleted and the rest of the frame will be ignored by the receiver.
XHF	08	0000 1000	**Transmit HDLC Frame**. Enables the transmission of the block entered last in the XFIFO. The frame is not yet complete.
XHFC	0A	0000 1010	**Transmit HDLC Frame** and close it with CRC and flag.
F_XHF	0C	0000 1100	Same as preceding, but used in Master mode to enforce a transmission even in the case of a collision.
F_XHFC	0E	0000 1110	
XRES	01	0000 0001	**Reset Transmitter**. Clears the XFIFO; any frame currently being transmitted is aborted.

DETAILED REGISTER DESCRIPTION

Register Address Layout

The register set consists of:

- One configuration register common to all four channels(CCR).
- A maskable vectored interrupt status register (VISR, VISM).

And, for each of the four channels, a set of individual registers (Figure 21).

In order to support the use of a 16-bit microcontroller, each register can be accessed with an even and an odd address value.

The address map of the individual registers of each channel is shown in Table 12. In order to obtain the actual address of a register, a base has to be added to the address given in the table, as follows:

base = 00 for channel A
40 for channel B
80 for channel C
C0 for channel D

Table 12. Address Map of HDLC Channel Registers

Address Even		Address Odd	Read	Write
00	to	1F	RFIFO	XFIFO
20	or	29	ISTA	ISM
28	or	21	STAR	CMDR
22	or	2B	MODE	MODE
2C	or	25	RFBC	TSR

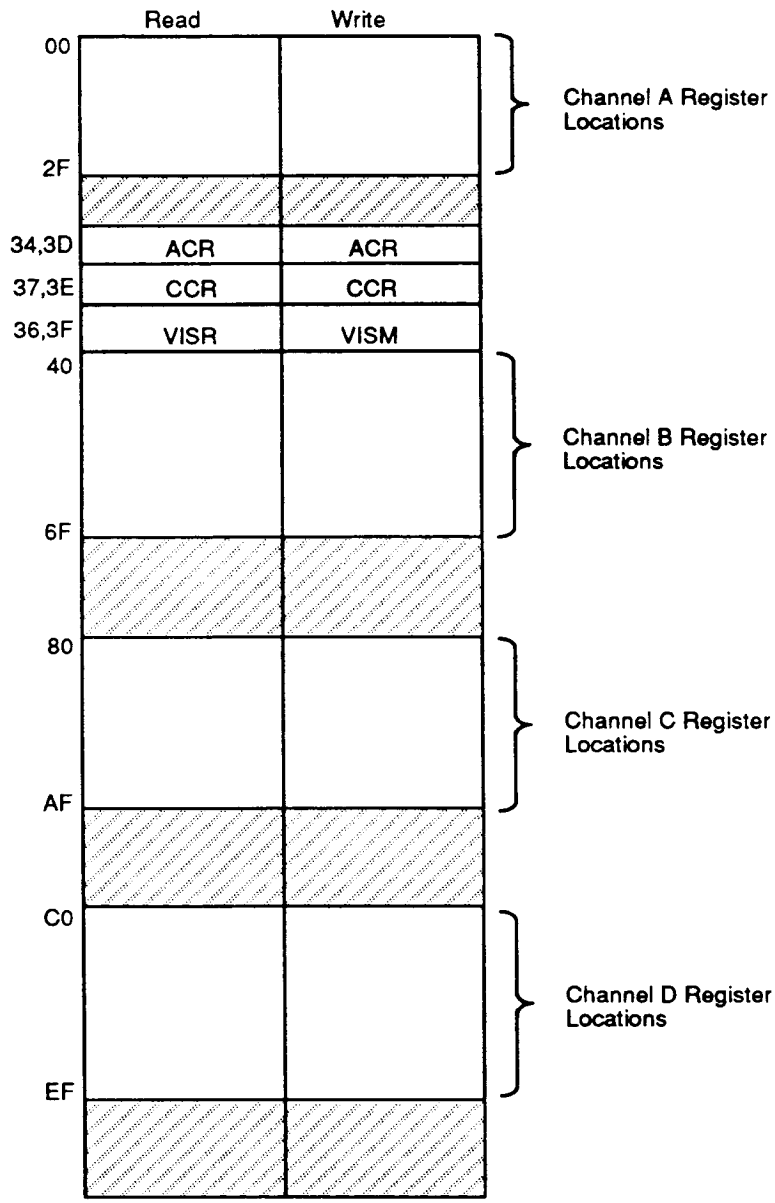

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Figure 21. IDEC Register Map

Register Description

Common Registers

Common Configuration Register (CCR) Address: 37/3E$_H$ Read/Write. Value after reset: 00$_H$

7							0
MDS1	MDS0	VIS	0	0	BNS	CRS	ODS

MDS1, 0 Mode Select

MDS1	MDS0	Description
0	0	Single-connection TS mode
0	1	Quad-connection common control mode
1	0	Single-connection IOM mode
1	1	Quad-connection TS mode

VIS Vectored Interrupt Selection

1 IOM channel 4 to 7 (IOM mode), microprocessor bus bits 4 to 7 for VISR
0 IOM channel 0 to 3 (IOM mode), microprocessor bus bits 0 to 3 for VISR

BNS Bit Number Select

1 PCM frame is between 257 to 512 bits long
0 PCM frame is at most 256 bits long

CRS Clock Rate Selection

1 DCL clock rate is equal to twice the data rate
0 DCL clock rate is equal to the data rate

ODS Output Driver Selection

1 Open drain
0 Three-state

The ODS bit selects the driver type simultaneously on all data outputs (and control output SD2X in Master mode). However, in the single-connection IOM mode, SD0X is open-drain, independent of the value of ODS.

Address Compare Register (ACR) Address: 34/3D$_H$ Read/Write. Value after reset: 00$_H$.

7							0
AC3	AC2	AC1	AC0	SCM	SCG	SCS	SCP

AC3–AC0 Address Compare for channel A–D on (1) or off (0). The first byte following the opening flag of a receive frame will be compared against reference values if ACi = 1 and the frame is accepted or rejected on the basis of the comparison. If ACi = 0, all valid HDLC frames in that channel are stored.

SCM SAPI Compare Mode

1 Accept HDLC frames for which the first address byte matches selected SAPI values.
0 Reject HDLC frames for which the first address byte matches selected SAPI values.

SCG SAPI Compare Group

1 The first byte of a received HDLC frame is compared with Group SAPI SAPG (63$_D$).
0 The first byte of a received HDLC frame is not compared with SAPG.

SCS SAPI Compare Signaling

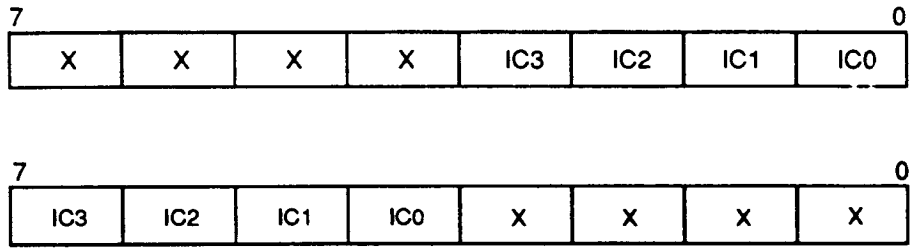
1 The first byte of a received HDLC frame is compared with Signaling SAPI SAPS (0$_D$).
0 The first byte of a received HDLC frame is not compared with SAPS.

SCP SAPI Compare Packet

1 The first byte of a received HDLC frame is compared with Packet SAPI SAPP (16$_D$).
0 The first byte of a received HDLC frame is not compared with SAPP.

The HDLC address compare logic is shown in Table 4.

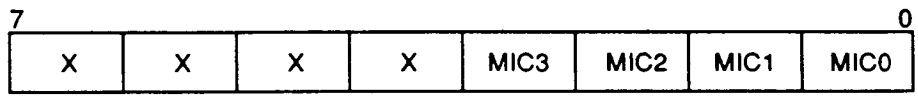
Vectored Interrupt Status Register (VISR) Address: 36/3F$_H$ Read. Value after reset: 00$_H$



IC0–IC3 Interrupt from Channel A–D

When VISR is read, these four bits are placed on the microprocessor data bus with an offset determined by bit VIS (register CCR). Other bit positions on the bus remain in high impedance.

Mask for Vectored Interrupt Status Register (VISM) Address: 36/3F$_H$ Write. Value after reset: 00$_H$



MIC0–MIC3 Mask for Interrupt from Channel A–D.

The mask bits are active High.

A masked interrupt is not visible when VISR is read. Instead, it remains internally stored (pending). Any pending interrupt is generated and the corresponding IC3–0 bit is set when the mask bit is reset to zero.

Individual Channel Registers

FIFOs

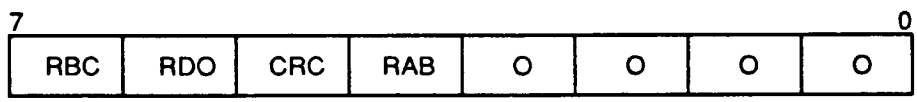
RFIFO (read), XFIFO (write) Address: Base + 00 to 1F$_H$.

The FIFOs have an identical address range. All the 32 addresses give access to the current FIFO location.

Note on RFIFO: The RFBC (Receive Frame Byte Counter) register bits 0 to 4 indicate the number of bytes currently accessible to the microcontroller in the visible 32-byte RFIFO pool. If more bytes are read, the data read after RFBC accesses is the old data loaded in that part of the RFIFO previous to the current data. For more than 32 accesses, the RFIFO will be read cyclically (modulo 32). This will not disturb the next received frame.

Note on XFIFO: If more than 32 bytes are written to the XFIFO (without a transmit command), an XDOV interrupt is generated. The byte that was entered first (first byte to be sent) will be continuously overwritten by the extra write operations.

When the closing flag of a receive frame is detected, a status byte is appended to the data in the RFIFO. The RFBC includes the status byte. This status byte has the following format:



RBC Receive Byte Count

The length of the received frame (excluding flags and Frame Check Sequent (FCS)) is $n \times 8$ bits if RSC = 1 (n = {1,2,3,...}). The length is not a multiple of 8 bits if RBC = 0.

RDO Receive Data Overflow

If RDO = 1, part of the frame has been lost because the receive FIFO was full.

CRC CRC Check

The received FCS bytes were correct if CRC = 1.

RAB Receive Abort

RAB = 1 implies that the received frame was aborted.

A status byte equal to A0$_H$ indicates a correctly received frame.

Status/Command Registers

Interrupt Status Register (ISTA) Address: Base + 20/29H Read. Value after reset: 00H

7							0
RME	RPF	RFO	XPR	XDU	X	X	X

RME Receive Message End.

One complete frame of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the RFIFO, including the status byte. The number of bytes stored is given by RFBC bits 4–0.

RPF Receive Pool Full

32 bytes of a frame have arrived in the RFIFO. The frame is not yet completely received.

RFO Receive Frame Overflow

At least one complete frame was lost because no storage space was available in the RFIFO.

XPR Transmit Pool Ready

One data block may be entered into the XFIFO.

XDU Transmit Data Underrun

Transmitted frame was terminated with an abort sequence because either:

1. No data was available for transmission in XFIFO and no XME command was issued or;
2. A collision has occurred after at least one block of data has been completely transmitted, and thus an automatic retransmission cannot be attempted.

Note: It is not possible to transmit frames when an XDU interrupt remains unacknowledged.

Mask for Interrupt Status Register (ISM) Address: Base + 20/29H Write. Value after reset: 00H.

Each interrupt source in the ISTA register can be selectively masked by setting to 1 the corresponding bit in ISM. Masked interrupts are not indicated when ISTA is read. Instead, they remain internally stored and pending. An interrupt is generated after the mask is reset to zero.

Status Register (STAR) Address: Base + 21/28H Read. Value after reset: 50H.

7							0
XDOV	XFW	BSY	RNA	X	X	VN1	VN0

XDOV Transmit Data Overflow

More than 32 bytes have been written into the XFIFO.

XFW Transmit FIFO Write Enable

Data can be entered into the XFIFO.

BSY Busy state on the receive line

A 0 in this bit position indicates an idle state on the input data line (15 or more consecutive 1s).

RNA Receive line Not Active

Indicates whether flags/frames are being received on the line (0) or not (1). RNA takes on the value 1 after seven consecutive ones are received on the line.

VN1–VN0 Version Number of chip

0...A1 version
1...A2 version

Command Register (CMDR) Address: Base + 21/28H Write. Value after reset: 00H.

7							0
RMC	RRES	RMD	X	XHF	FHF	XME	XRES

RMC Receive Message Complete

Reaction to RPF or RME interrupt. The RFIFO pool currently accessible by the microprocessor is released for a subsequent frame (or 32-byte block of data).

RRES Receiver Reset

HDLC receiver is reset, the receive FIFO is cleared of any data.

RMD Receive Message Delete

Reaction to RPF or RME interrupt. The entire frame is to be ignored by the receiver. The part of frame already stored is discarded.

XHF Transmit HDLC Frame

Transmission of an HDLC frame is (or of a block thereof) initiated.

FHF Force HDLC Frame

Used in the Master collision mode (CMS1,0 = 11). When this bit is set and a Transmit HDLC Frame (XHF) command is issued, the controller aborts the frame from CDR (if any) by sending seven 1s on SD0X and then starts transmission. SD2X is set low to indicate that no data will be accepted on CDR input data line.

XME Transmit Message End

Indicates that the current transmit frame is to be closed with CRC and flag.

XRES Transmitter reset

HDLC transmitter is reset, XFIFO is cleared of any data, and the HDLC frame currently being transmitted (if any) is aborted.

Mode Register (MODE) Address: Base + 22/2BH Read/Write. Value after reset: 00H.

7							0
TLP	CMS1	CMS0	ITF	RAC	CAC	CCS1	CCS0

TLP Test Loop

Input and output of HDLC channel are connected together (TLP = 1). The test loop is either transparent (if MDS1,0 = 01, 10) or not (if MDS1,0 = 00, 11).

CMS1,0 Collision Mode Select

CMS1	CMS0	Descriptions
0	0	Unconditional transmission
0	1	Slave Mode
1	0	Multi-master mode
1	1	Master mode

ITF Interframe Time Fill

Idle (ITF = 0) or flags (ITF = 1) are used as interframe time fill.

RAC Receiver Active

Receiver is activated (1) or deactivated (0).

CAC Channel Active

A channel is completely disabled (receiver and transmitter are inactive, transmit line is high impedance, no $\overline{TSC}$ is output) as long as CAC is 0.

CCS1,0 Channel Capacity Select

These bits select the number of bits in the time slot where data are received and transmitted. They have a significance only when MDS1,0 = 00 or 11 (single-connection TS mode and quad-connection TS mode).

The bit rates given below assume a channel repetition rate of 8 kHz.

CCS1	CCS0	Time Slot Width	Channel Data Rate
0	0	2 bits	16 kb/s
0	1	1 bit	8 kb/s
1	0	8 bits	64 kb/s
1	1	7 bits	56 kb/s

Receive Frame Byte Counter (RFBC) Address: Base + 25/2C$_H$ Read. Value after reset: 00$_H$.

7							0
RDC7	RDC6	RDC5	RDC4	RDC3	RDC2	RDC1	RDC0

RDC7–RDC0 Receive Data Count

Total number of bytes of received frame, including the status byte. The contents of the register are valid after an RME interrupt. RDC4–0 indicate the length of the data block currently available in the receive FIFO. RDC7–5 count the number of full 32-byte blocks of a frame which have already been received. If the frame length exceeds 223 bytes, RDC7–5 hold the value 111; only RDC4–0 continue to count modulo 32.

Time Slot Register (TSR) Address: Base + 25/2C$_H$ Write. Value after reset: 00$_H$.

7							0
TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0

TS7-TS0 Time Slot Select

Determine the particular time slot where the HDLC controller is to receive and transmit. This register has a significance only when MDS1,0 = 00, 10 or 11 (single-connection modes and quad-connection TS mode). The register gives the position of a time slot (either 1, 2, 7 or 8 bits wide, cf., CCS1,0) in 2-bit increments (2-bit resolution). The position of the time slot is relative to a Frame Sync signal that marks the beginning of a PCM frame.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias . . . . . 0 to +70°C
Storage temperature . . . . . 65° to +125°C
Voltage on any pin with
respect to ground . . . . . –0.4 to V_{DD} +0.4 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0 to +70°C
Supply Voltage (V_{DD}) . . . . . 5 V ±5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges

T_A = 0 to +70°C; V_{DD} = 5 V ±5%, V_{SS} = 0 V.

Parameter Symbol	Parameter Descriptions		Test Conditions	Limit Values Min	Limit Values Max	Unit
V_{IL}	Input low voltage			–0.4	0.8	V
V_{IH}	Input high voltage			2.0	V_{CC} + 0.4	V
V_{OL}	Output low voltage		I_{OL} = 7 mA (SD3X–SD0X) I_{OL} = 2 mA (all other pins)		0.45	V
V_{OH}	Output high voltage Output high voltage		I_{OH} = –400 µA I_{OH} = –100 µA	2.4 V_{DD} –0.5		V
I_{CC}	Power Supply Current	operational	V_{DD} = 5 V, DCL = 4096 kHz		10	mA
		power-down	Inputs at 0 V/V_{DD} No output loads		1	mA
I_{LI}	Input leakage current		0 V < V_{IN} < V_{DD} to 0 V		+10	µA
I_{LO}	Output leakage current		0 V < V_{OUT} < V_{DD} to 0 V		+10	µA

CAPACITANCES

T_A = 25°C, V_{DD} = 5 V ±5%, V_{SS} = 0 V.

Parameter Symbol	Parameter Descriptions	Test Conditions	Limit Values Min	Limit Values Max	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		10	20	pF

SWITCHING CHARACTERISTICS

T_A = 0 to +70°C, V_{DD} = 5 V ±5%

Inputs are driven to 2.4 V for a logical 1 and to 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input/output waveforms are shown below.

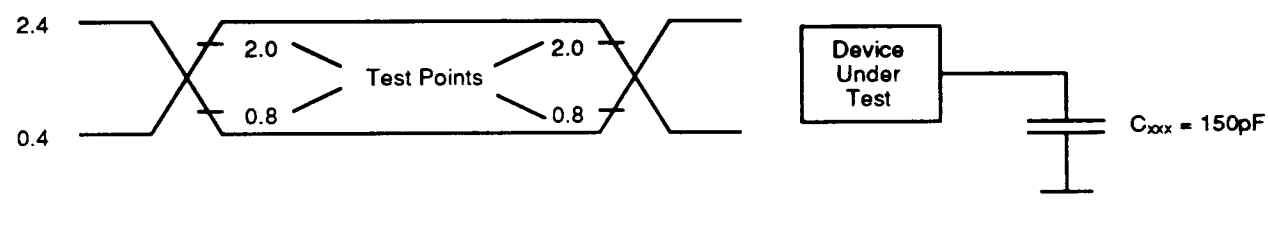


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Figure 22. Input/Output Waveform for AC Tests

MICROCONTROLLER INTERFACE TIMING
Timing Characteristics

Parameter Symbol	Parameter Descriptions	Test Conditions	Min	Max	Unit
t_{AA}	ALE pulse width		50	—	ns
t_{AD}	ALE guard time		15	—	ns
t_{AH}	Address hold time		25	—	ns
t_{AL}	Address setup time to ALE		20	—	ns
t_{ALS}	Address latch setup time to $\overline{WR}$, $\overline{RD}$		35	—	ns
t_{AS}	Address setup time		10	—	ns
t_{DF}	Data float from $\overline{RD}$		—	25	ns
t_{DSD}	$\overline{RD}$ delay after $\overline{WR}$ setup		0	—	ns
t_{DW}	Data setup time to $\overline{WR}$ + $\overline{CS}$		30	—	ns
t_{LA}	Address hold time from ALE		35	—	ns
t_{RD}	Data output delay from $\overline{RD}$		—	120	ns
t_{RI}	$\overline{RD}$ control interval		75	—	ns
t_{RR}	$\overline{RD}$ pulse width		120	—	ns
t_{WD}	Data hold time from $\overline{WR}$ + $\overline{CS}$		10	—	ns
t_{WI}	$\overline{WR}$ control interval		70	—	ns
t_{WW}	$\overline{WR}$ Pulse width		60	—	ns

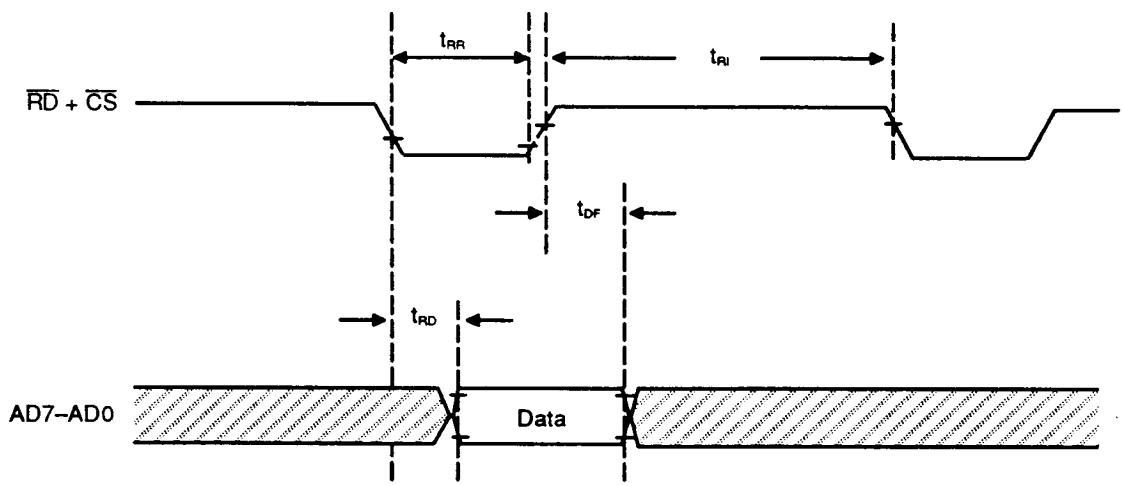

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Figure 23. Microprocessor Read Cycle (Intel Bus Mode)

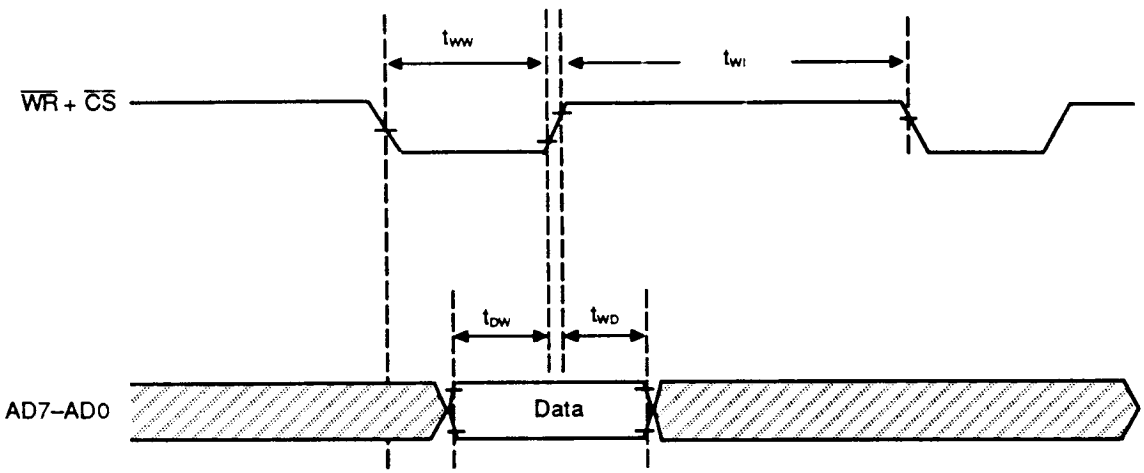

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Figure 24. Microprocessor Write Cycle (Intel Bus Mode)

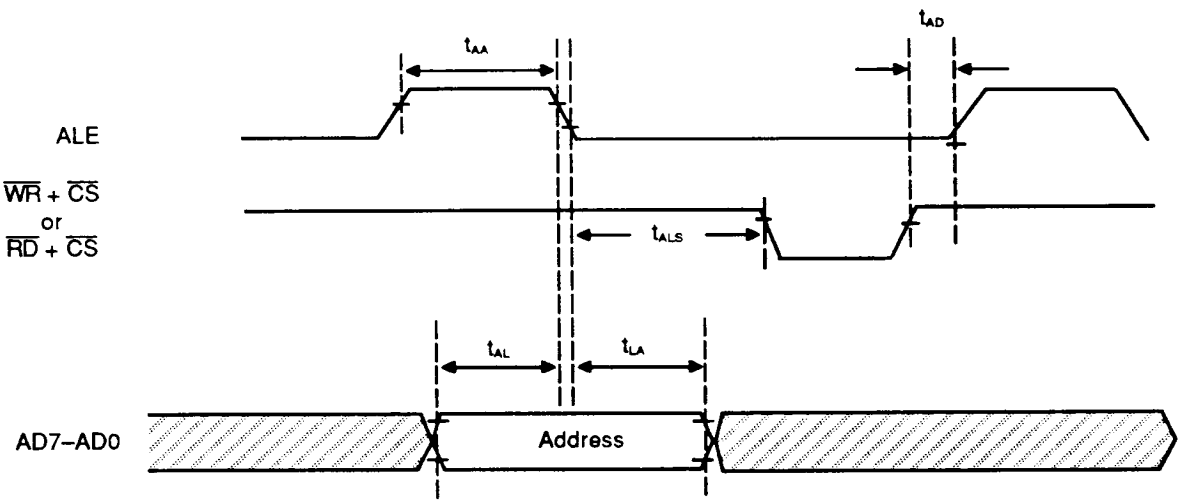

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Figure 25. Multiplexed Address Timing (Intel Bus Mode)

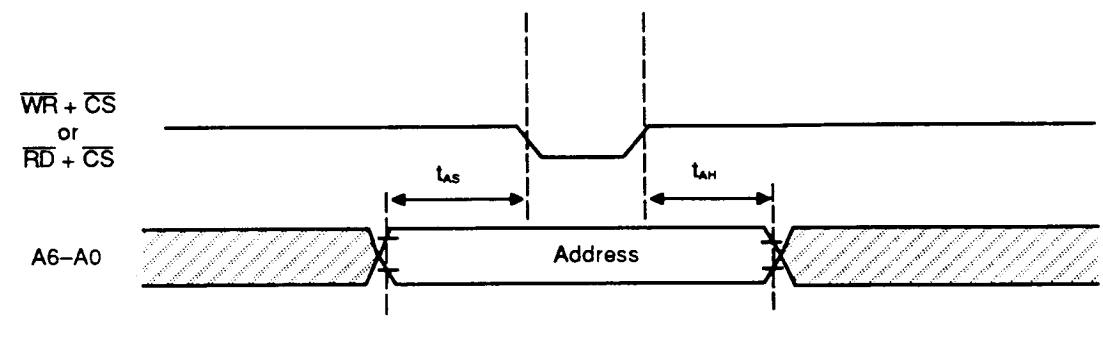

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Figure 26. Non-Multiplexed Address Timing (Intel Bus Mode)

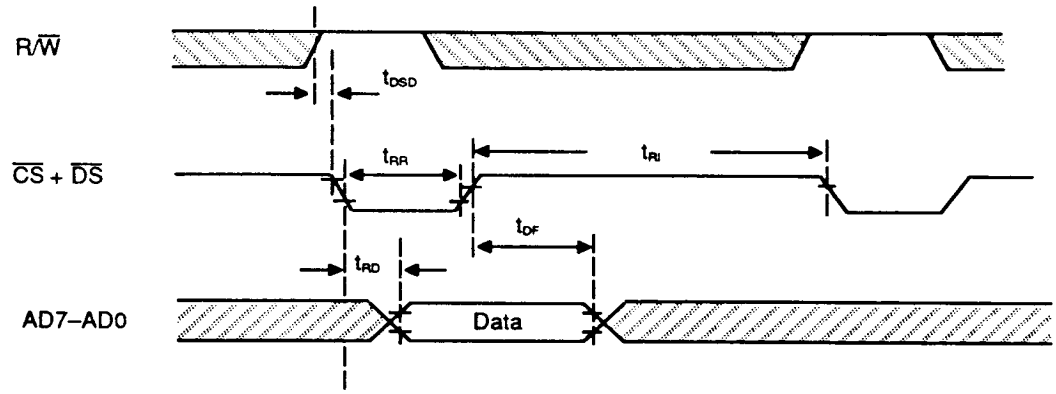

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Figure 27. Microprocessor Read Cycle (Motorola Bus Mode)

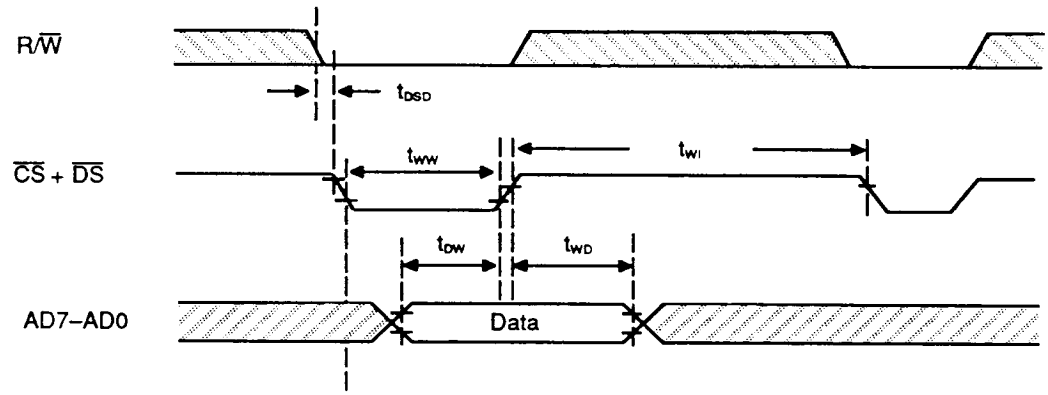

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Figure 28. Microprocessor Write Cycle (Motorola Bus Mode)

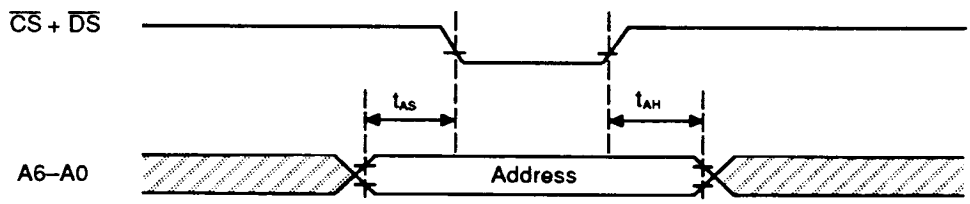

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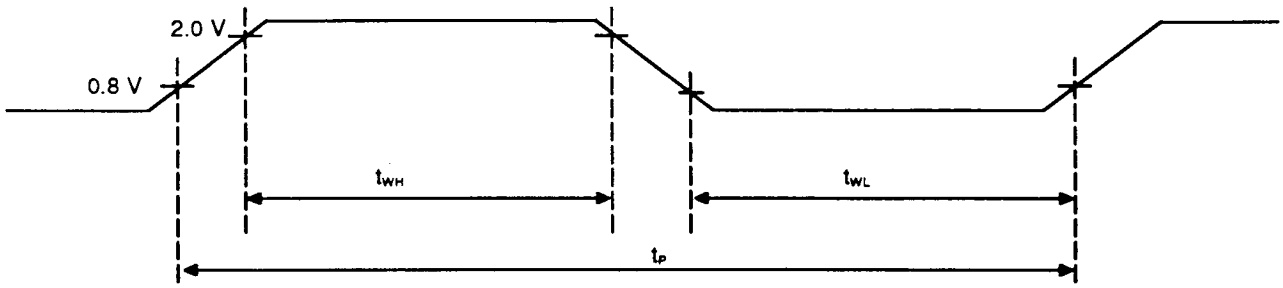
Figure 29. Address Timing (Motorola Bus Mode)



11134C–032

Figure 30. Definition of DCL Period and Width

SERIAL INTERFACE TIMING

DCL Characteristics

Parameter Symbol	Parameter Descriptions	Test Conditions	Min	Typ	Unit
t_P	DCL period	Single clock rate	230	—	ns
		Double clock rate	160	—	ns
t_{WH}	DCL High	Single clock rate	90	—	ns
		Double clock rate	50	—	ns
t_{WL}	DCL Low		70	—	ns

INPUT/OUTPUT CHARACTERISTICS

FSC in Single Connection Modes and Quad Connection TS Mode

FSC Characteristics

Parameter Symbol	Parameter Descriptions	Test Conditions	Min	Typ	Unit
t_{FH}	FSC hold time		30	—	ns
t_{FS}	FSC setup time (See Note)		105	—	ns
t_{IDH}	Input data hold		20	—	ns
t_{IDS}	Input data setup		25	—	ns
t_{ODD}	Output data delay from DCL		—	60	ns
t_{ODF}	Output data delay from FSC	See Note	—	160	ns

Notes: This delay is applicable in two cases only:
1. When FSC appears for the first time (e.g., at system power-up).
2. When the number of bits in the PCM frame is not equal to either 256 or 512.

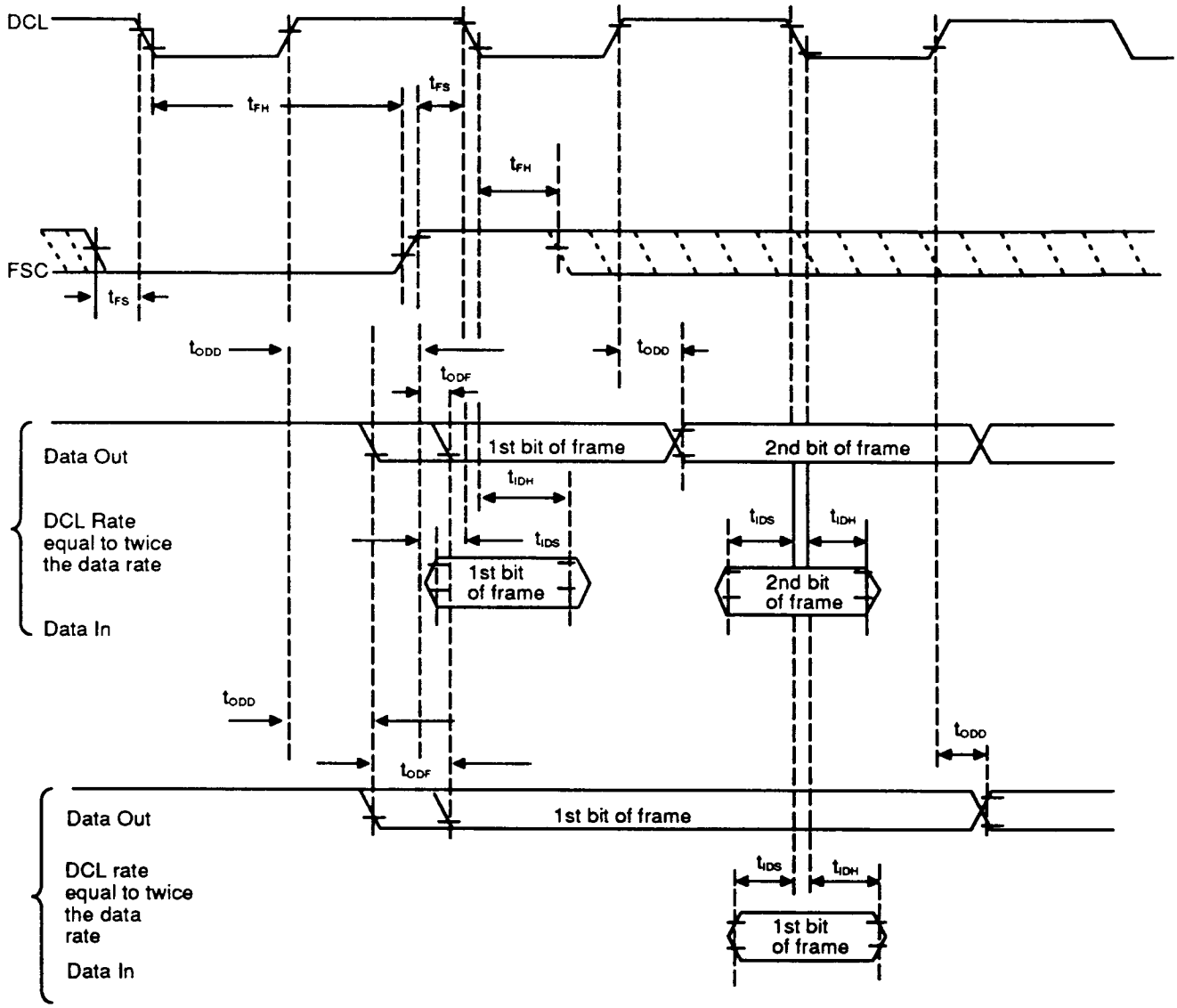


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Figure 31. FSC-Timing Characteristics

FSC in Quad Connection Common Control Mode

Parameter Symbol	Parameter Descriptions	Test Conditions	Min	Typ	Unit
t_{FH1}	FSC hold time		30	—	ns
t_{FS1}	FSC setup time		60	—	ns
t_{IDH}	Input data hold		20	—	ns
t_{IDS}	Input data setup		25	—	ns
t_{ODD}	Output data delay from DCL		—	60	ns
t_{ODZ}	Output data from active to high impedance		—	40	ns
t_{OZD}	Output data from high impedance to active		—	80	ns

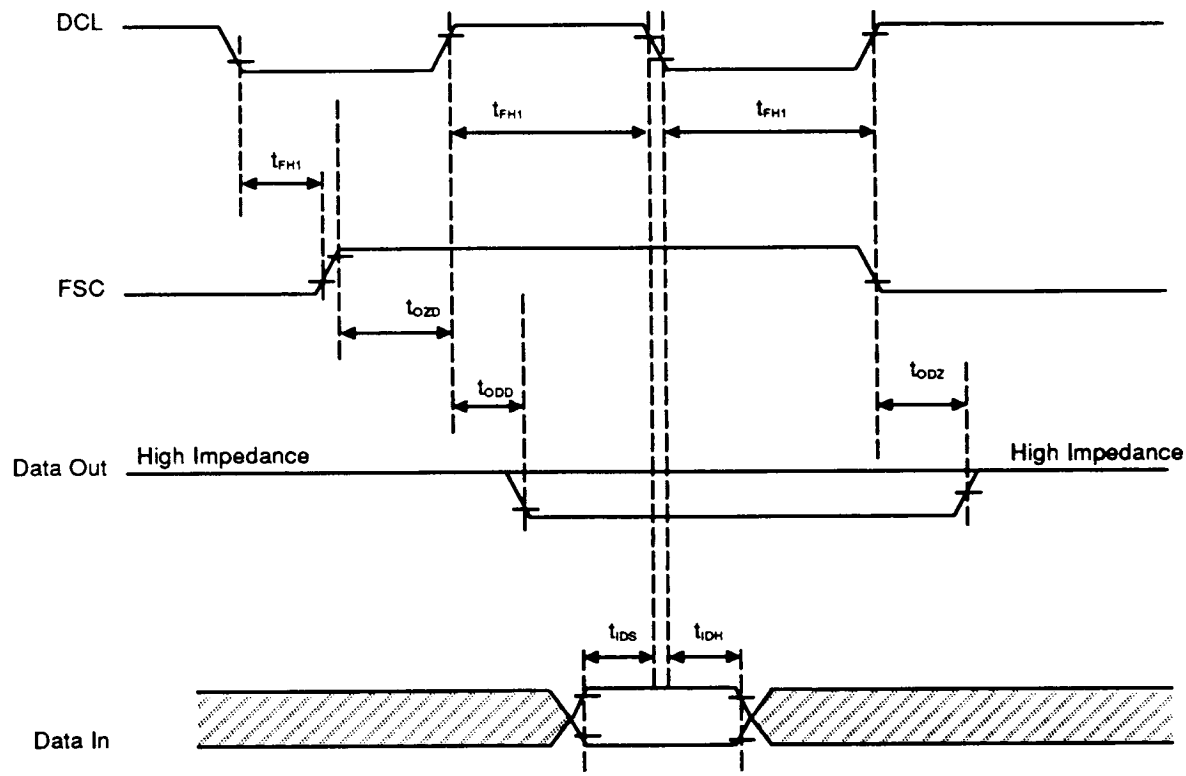

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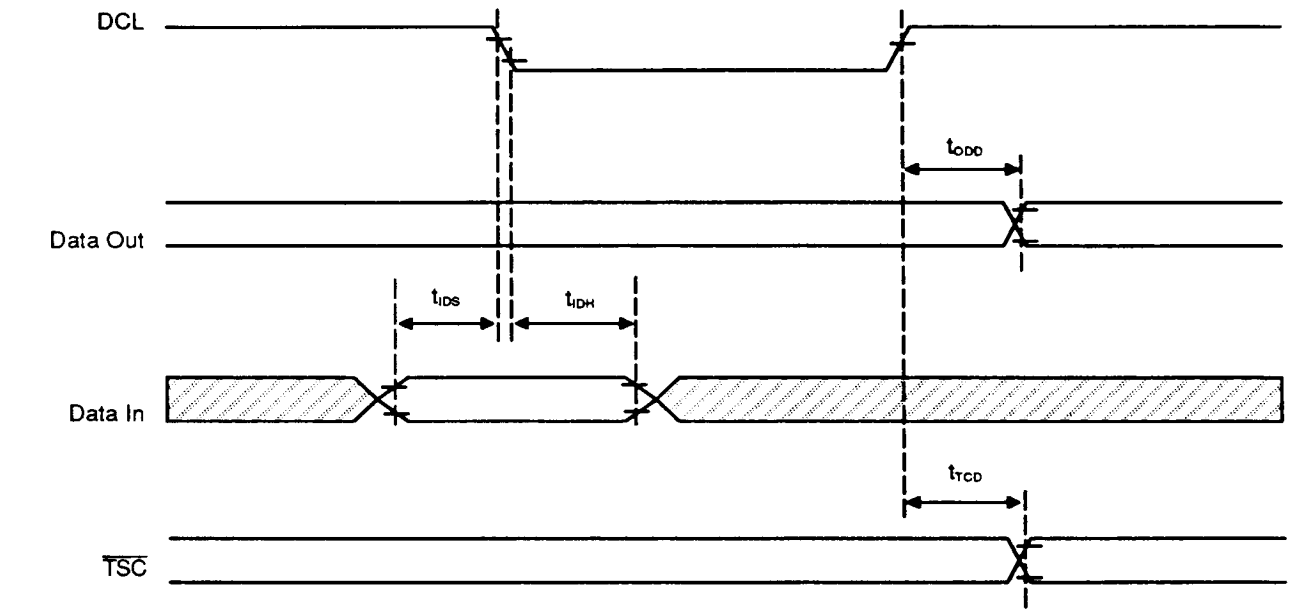
Figure 32. FSC (Strobe) Characteristics

Parameter Symbol	Parameter Descriptions	Test Conditions	Min	Max	Unit
t_{IDH}	Input data hold		20	—	ns
t_{IDS}	Input data setup		25	—	ns
t_{ODD}	Output data delay from DCL		—	60	ns
t_{TCD}	$\overline{TSC}$ delay from DCL		—	60	ns



Data out: SD0X in single-connection modes
SD0X, SD1X, SD2X, SD3X in quad-connection modes
SD1X, SD2X in Master mode

Data in: SD0R in single-connection mode
SD0R, SD1X, SD2R, SD3R in quad-connection modes
CDR in Slave, Multi-master and Master modes

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Figure 33. Data I/O Characteristics

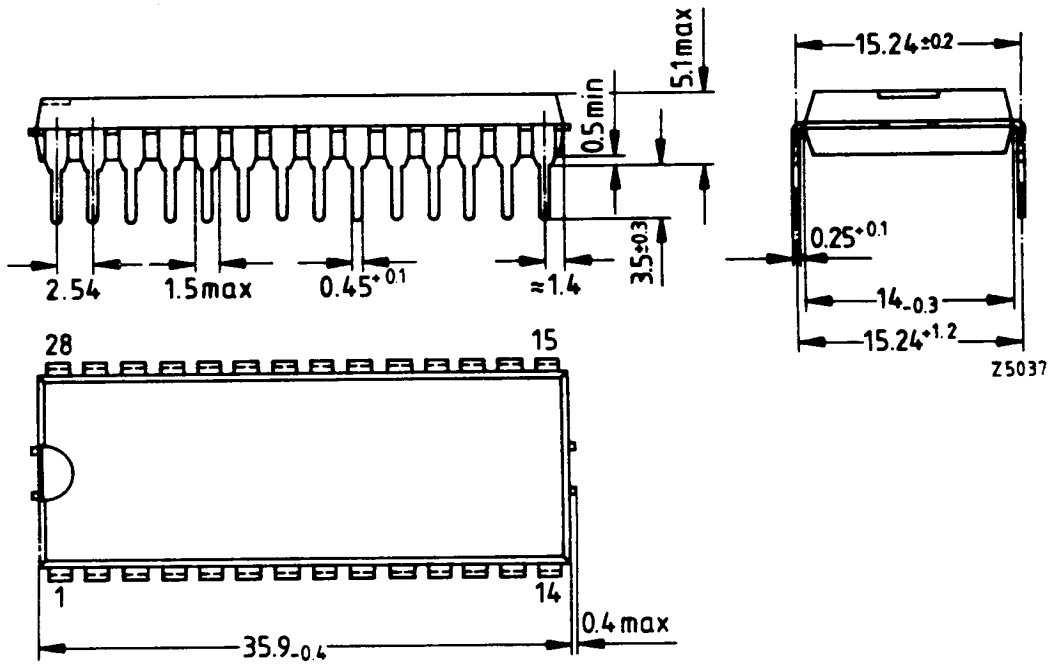
RES Characteristics

Parameter Symbol	Parameter Descriptions	Test Conditions	Min	Typ	Unit
t_{RWH}	RES High		16×T_P	—	ns

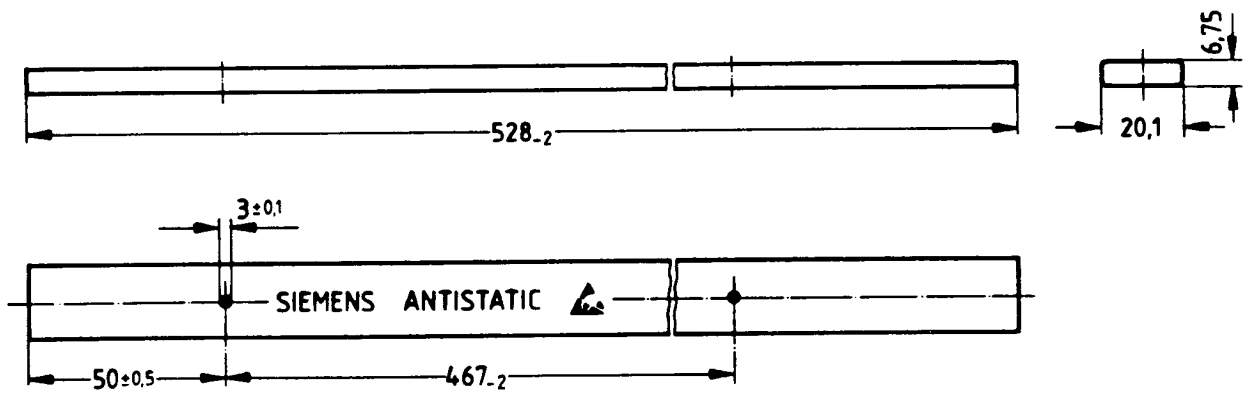
PHYSICAL DIMENSIONS

For reference only. All dimensions measured in millimeters. BSC is an ANSI standard for Basic Space Centering.
Preliminary; package in development.

PD 028



PL 044



Note: Physical Dimensions are in mm.

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