12-Bit High Speed Multiplying D/A Converter

General Description

The Am6012 series of multiplying Digital to Analog Converters (DACs) guarantee differential nonlinearity to better than ±0.5LSB (0.012%) for the 6012A and ±1LSB (0.025%) for the 6012 over the full military and commercial temperature ranges.

The Am6012 combines a 9-bit master DAC with a 3-bit (MSB's) segmented generator to form an accurate 12 D/A converter at low cost. This segmented design technique reduces the requirement for high accuracy thin film resistor ladder networks.

The performance of the DAC is virtually independent of supply voltage and can operate over a power supply range of +4V/-10V to ±18V with minimal effect on full scale current, differential nonlinearity, relative accuracy and settling time of 250ns.

The high compliance voltage, low drift characteristics, guaranteed performance and low cost makes these devices excellent building blocks for A/D converters, data acquisition systems, and video display drivers.

Features

- **Differential Nonlinearity: 0.012% (13 Bits)**
- **Integral Nonlinearity: 0.025%**
- **Guaranteed 12-bit Monotonicity Over Temperature**
- **Fast Settling to 0.01%: 250ns**
- **High Output Compliance: -5V to +10V**
- **Differential Outputs: 0 to 4mA**
- **Low Power Consumption: 225mW**
- **Direct Interface to Major Logic Families**

Applications

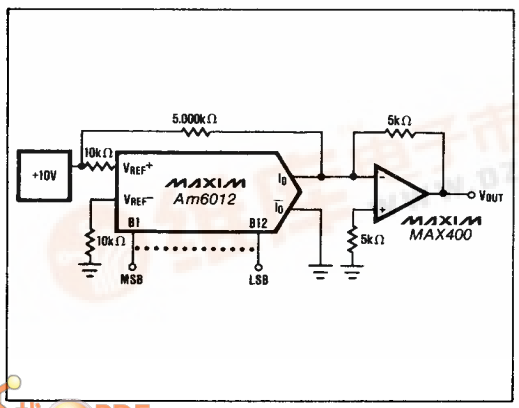
Data Acquisition Systems
Video Display Drivers
Offset DAC Applications
A/D Converters
Test Equipment

Ordering Information

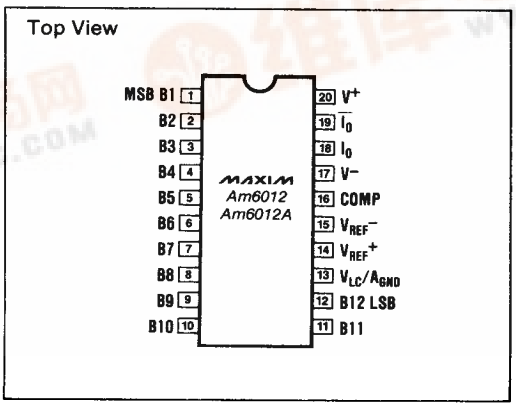
PART	TEMP. RANGE	PACKAGE
Am6012PC	0°C to +70°C	20 Lead Plastic DIP
Am6012DC	0°C to +70°C	20 Lead CERDIP
Am6012CWP	0°C to +70°C	20 Lead Small Outline
Am6012C/D	0°C to +70°C	Dice*
Am6012APC	0°C to +70°C	20 Lead Plastic DIP
Am6012ADC	0°C to +70°C	20 Lead CERDIP
Am6012ACWP	0°C to +70°C	20 Lead Small Outline
Am6012DM	-55°C to +125°C	20 Lead CERDIP
Am6012ADM	-55°C to +125°C	20 Lead CERDIP

** Consult factory for Dice specifications*

Typical Operating Circuit



Pin Configuration



12-Bit High Speed Multiplying D/A Converter

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ..... ±18V
Logic Inputs ..... -5V to +18V
Analog Current Outputs ..... -8V to +12V
Reference Inputs V_{14}, V_{15} ..... V^- to V^+
Reference Input Differential Voltage (V_{14}, V_{15}) ..... ±18V
Reference Input Current 1.25mA
Storage Temperature ..... -65°C to +150°C
Maximum Junction Temperature ..... +160°C

Operating Temperature Range
Am6012APC, ADC, ACWP, PC, DC, CWP ..... 0°to +70°C
Am6012ADM, DM ..... -55°C to +125°C
Package Dissipation
Plastic DIP (derate at 8mW/°C above 70°C) 640mW
Small Outline (derate at 10mW/°C above 70°C) 800mW
CERDIP (derate at 11mW/°C above 70°C) 850mW
Lead Soldering Temperature (60 sec.) ..... +300°

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, I_{REF} = 1.0mA, Over Temperature Range, unless noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

PARAMETER	SYMBOL	CONDITIONS	Am6012A			Am6012			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Resolution			12			12			Bits
Monotonicity			12			12			Bits
Differential Nonlinearity	D.N.L.	Deviation from Ideal Step Size			±0.012 ±0.5			±0.025 ±1	%FS LSB
Nonlinearity	N.L.	Deviation from Ideal Straight Line			±0.05			±0.05	%FS
Full-Scale Current	I_{FS}	V_{REF} = 10.000V; T_A = 25°C R14 = R15 = 10.000kΩ	3.967	3.999	4.031	3.935	3.999	4.063	mA
Full-Scale Tempco	TCI_{FS}			±5.0 ±0.0005	±20 ±0.002		±10 ±0.001	±40 ±0.004	ppm/°C %FS/°C
Output Voltage Compliance	V_{OC}	D.N.L. Specification Guaranteed Over Compliance Range	-5		+10	-5		+10	V
Full-Scale Symmetry	I_{FSS}	$\|I_{FS}\| - \|I_{FS}\|$		±0.02	±1		±0.4	±2	μA
Zero-Scale Current	I_{ZS}				0.10			0.10	μA
Settling Time	t_S	To ±½ LSB, All Bits Switched ON or OFF (Note 1)		250	500		250	500	ns
Propagation Delay — All Bits	t_{PLH} t_{PHL}	All Bits Switched; 50% Point Logic Swing to 50% Point Output (Note 1)		25	50		25	50	ns
Output Resistance	R_O			>10			>10		MΩ
Output Capacitance	C_{OUT}			20			20		pF
Logic Input Levels "0"	V_{IL}	V_{LC} = GND			0.8			0.8	V
Logic Input Levels "1"	V_{IH}	V_{LC} = GND	2			2			V
Logic Input Current	I_{IN}	V_{IN} = -5 to +18V			40			40	μA
Logic Input Swing	V_{IS}		-5		+15	-5		+15	V
Reference Current Range	I_{REF}		0.2	1.0	1.1	0.2	1.0	1.1	mA
Reference Bias Current	I_{15}		0	-0.5	-2	0	-0.5	-2	μA
Reference Input Slew Rate	dI/dt	$R_{14(eq)}$ = 800Ω C_C = 0pF (Note 1)	4	8		4	8		mA/μs
Power Supply Sensitivity	$PSSI_{FS}^+$ $PSSI_{FS}^-$	V^+ = +13.5V to +16.5V; V^- = -15V V^- = -13.5V to -16.5V; V^+ = +15V		±0.0005 ±0.00025	±0.001 ±0.001		±0.0005 ±0.00025	±0.001 ±0.001	V
Power Supply Range	V^+ V^-	V_{OUT} = 0V	4.5 -18		18 -10.8	4.5 -18		18 -10.8	V

ELECTRICAL CHARACTERISTICS (continued)

(V_S = ±15V, I_{REF} = 1.0mA, Over Temperature Range, unless noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

PARAMETER	SYMBOL	CONDITIONS	Am6012A			Am6012			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Power Supply Current	I^+ I^- I^+ I^-	V^+ = +5V, V^- = -15V V^+ = +15V, V^- = -15V		3.3 -13.9 3.9 -13.9	7 -18 7 -18		3.3 -13.9 3.9 -13.9	7 -18 7 -18	mA
Power Dissipation	P_D	V^+ = +5V, V^- = -15V V^+ = +15V, V^- = -15V		225 267	305 375		225 267	305 375	mW

Note 1: Guaranteed by design.

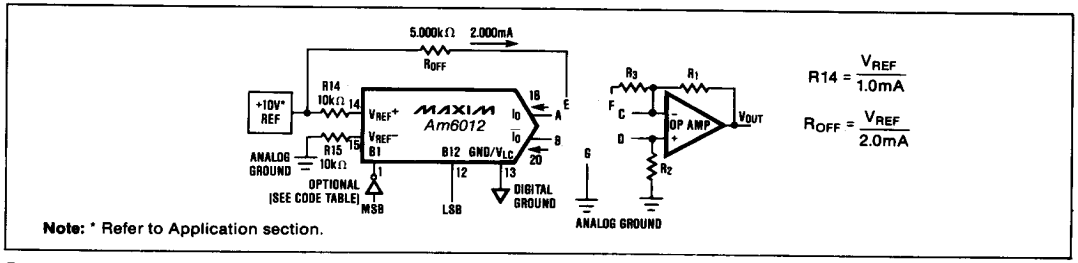


Figure 1. Voltage Output Connections

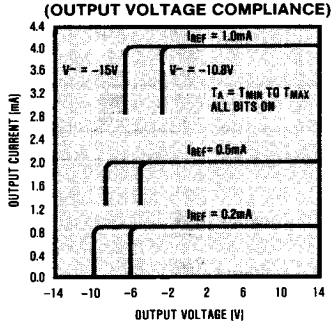
TABLE 1: Input Code Formats

CODE FORMAT		CONNECTIONS	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_0 (mA)	$\overline{I_0}$ (mA)	V_{OUT}
UNIPOLAR	Straight Binary; One Polarity with True Input Code, True Zero Output.	A-C B-G R1 = R2 = 2.5K	Positive Full Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
			Positive Full Scale -1 LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
			Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
	Complementary Binary; One Polarity with Complementary Input Code, True Zero Output.	A-G B-C R1 = R2 = 2.5K	Positive Full Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
			Positive Full Scale -1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
			Zero Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000
SYMMETRICAL OFFSET	Straight Offset Binary; Offset Half Scale, Symmetrical about Zero, No True Zero Output.	A-C B-D F-G R1 = R3 = 2.5K	Positive Full Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
			Positive Full Scale -1 LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
			(+) Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
			(-) Zero Scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0024
			Negative Full Scale -1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9927
			Negative Full Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-9.9976
	1's Complement; Offset Half Scale, Symmetrical About Zero, No True Zero Output MSB Complemented (need Inverter at B1)	A-C B-D F-G R1 = R3 = 2.5K R2 = 1.25K	Positive Full Scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
			Positive Full Scale -1 LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
			(+) Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
			(-) Zero Scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0024
			Negative Full Scale -1 LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9927
			Negative Full Scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-9.9976
OFFSET WITH TRUE ZERO	Offset Binary; Offset Half Scale, True Zero Output	E-A-C B-G R1 = R2 = 5K	Positive Full Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
			Positive Full Scale -1 LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
			+1 LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
			Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
			-1 LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0049
			Negative Full Scale +1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9951
			Negative Full Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-10.000
	2's Complement; Offset Half Scale, True Zero Output MSB Complemented (need Inverter at B1).	E-A-C B-G R1 = R2 = 5K	Positive Full Scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
			Positive Full Scale -1 LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
			+1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
			Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
			-1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.049
			Negative Full Scale	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9951
			Negative Full Scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-10.000

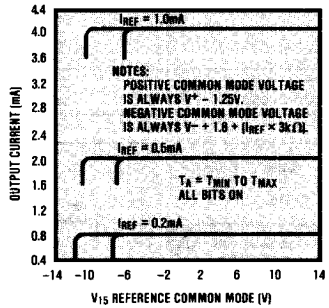
12-Bit High Speed Multiplying D/A Converter

Typical Characteristics

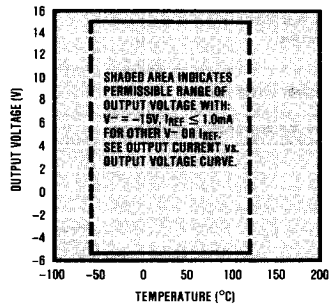
OUTPUT CURRENT vs. OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



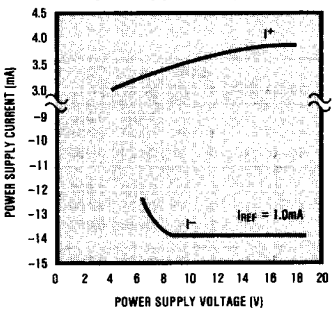
REFERENCE AMPLIFIER COMMON-MODE RANGE



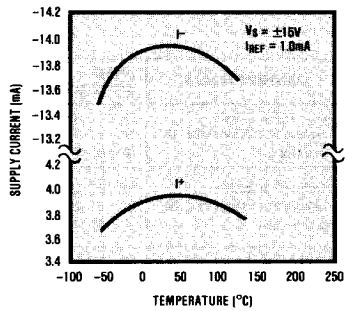
OUTPUT COMPLIANCE vs. TEMPERATURE



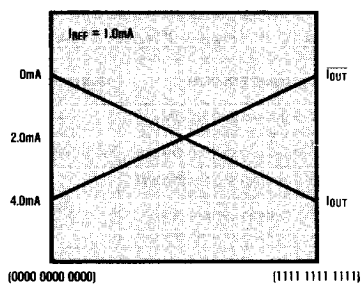
POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE



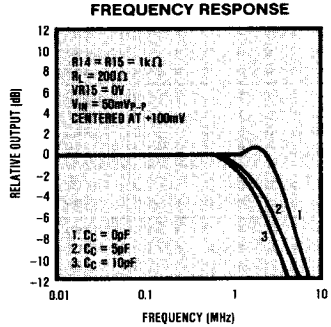
POWER SUPPLY CURRENT vs. TEMPERATURE



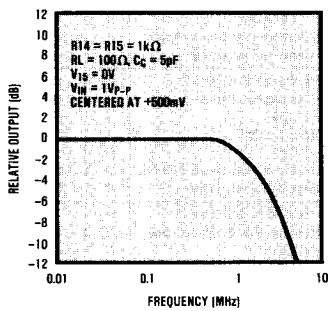
TRUE AND COMPLEMENTARY OUTPUT OPERATION



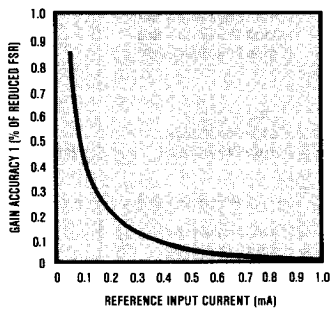
REFERENCE AMPLIFIER SMALL-SIGNAL FREQUENCY RESPONSE



REFERENCE AMPLIFIER LARGE-SIGNAL FREQUENCY RESPONSE



GAIN ACCURACY vs. REFERENCE CURRENT



12-Bit High Speed Multiplying D/A Converter

Detailed Description

The Am6012 DAC has two major sections, an 8 segmented generator and a 9-bit master/slave DAC. Figure 2 shows a simplified schematic, where the 3 most significant bits (MSB's) are inputs to a 3 to 8 line decoder. The selected current source (I_5 in figure 1) is connected to the master/slave 9-bit DAC. The lower currents (I_{1-4}) are summed into the I_0 line whilst the higher order currents (I_{6-8}) are summed into the $\overline{I_0}$ line. The I_5 current supplies 512 steps of current (0 to 0.499mA for a 1mA reference current) which are also summed into either the I_0 or $\overline{I_0}$ lines depending on the bits selected for the 9-bit DAC.

In figure 2, the code selected is 100 110000000, this results in (4 x 0.5mA) segment currents plus (0.375mA) DAC current being summed into I_0 giving a total of 2.375mA. $\overline{I_0}$ has a current of 1.625mA. As the MSB's are incremented, each successive code increases the I_0 output by 0.5mA and subtracts 0.5mA from $\overline{I_0}$. The selected segment current source (I_{1-8}) has its current fed into the 9-bit DAC. The 9-bit DAC's digital code determines how much current is added to the DAC output. The output is therefore a combination of the lower order segment current and the 9-bit DAC. This arrangement guarantees 12-bit monotonicity because the 9-bit DAC is monotonic.

Applications

Logic Inputs

The Am6012 logic input circuitry allows the user to interface with all major logic families. Logic inputs from -5V to +10V can be used with -15V and +5V to +15V supplies. This enables +15V CMOS logic to be interfaced even when the Am6012 is powered with +5V. With V_{LC} tied to ground the internal logic level is set to 1.3V, suitable for TTL and +5V CMOS. The logic threshold can be adjusted over a wide range using the relationship:

$$V_{TH} = V_{LC} + 1.3V$$

Care must be taken when connecting V_{LC} as it typically sinks 3mA and external circuitry should be designed to accommodate this current. When interfacing the Am6012 to ECL, the reference current (I_{REF}) should be limited to ≤1mA.

Power Supplies

The Am6012 operates over a supply range of +5V, -10V to ±18V when using an I_{REF} = 1mA. Operating the Am6012 below -10V reduces the output compliance voltage and below -8V seriously degrades the DAC's overall linearity. The positive supply voltage is not critical for the Am6012, and can be operated from +4V to +18V.

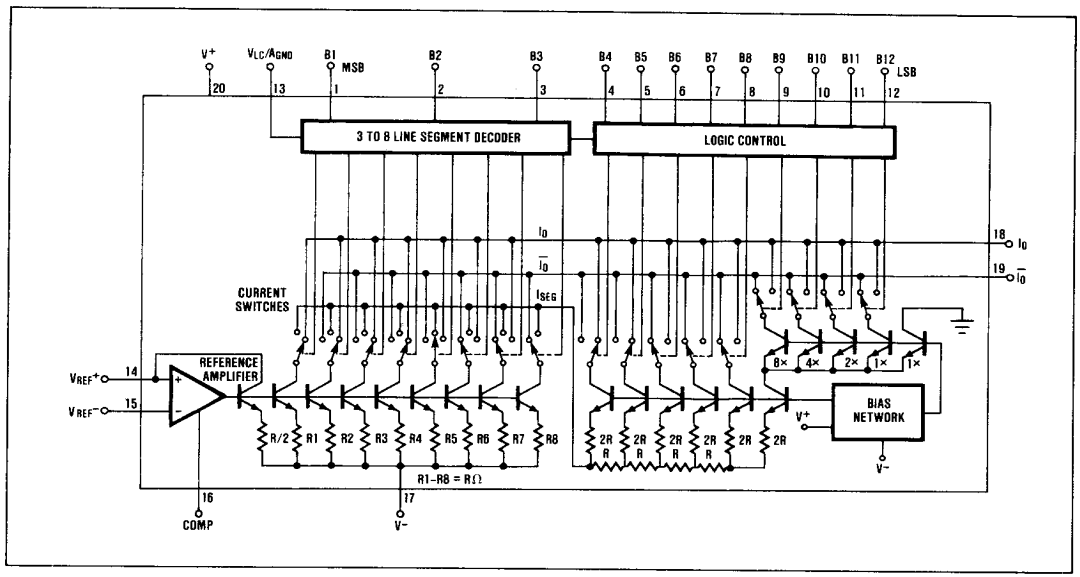


Figure 2. Simplified Schematic

12-Bit High Speed Multiplying D/A Converter

Reference Amplifier

The full scale current (I_{FS}) at the I_0 output is in direct proportion to the reference current (I_{REF}) flowing into pin 14.

$$I_{FS} = \frac{4095}{4096} \times 4 \times (I_{REF})$$

$$= 3.999\text{mA when } I_{REF} = 1\text{mA}$$

The reference current can be varied over a wide range from 1.0μA to 1.1mA.

For high accuracy applications, precision references such as the +10V REF01, AD581, AD584 or +5V REF02 should be used. For the ultimate in performance the +10V MAX670/671 devices should be used as these devices offer kelvin sensed V_{OUT} and ground connections. The temperature coefficient of the Am6012 output current is nearly equal to that of the reference voltage source. Using the +5V logic supply is not recommended as noise can be coupled into the DAC through the reference input. It is also recommended for DC references to split the reference setting resistor and to bypass with a 0.01μF capacitor from the junction of the two resistors and analog ground. To compensate for the input bias current of the Am6012 reference amplifier a resistor with the same value as the reference resistor should be inserted between pin 15 and ground.

A negative reference can also be used with the Am6012 by connecting it to pin 15. The DAC reference current is now established through the resistor from pin 14 to ground. The negative reference connection has the advantage of offering a high input impedance at pin 15.

The reference amplifier of the Am6012 must be compensated with a 0.01μF capacitor from pins 16 to 17 when using a DC reference source. For AC reference applications the value of compensation capacitor C_C depends on the value of the unbypassed source resistor at pin 14. For pulsed reference operation, use minimum value source resistors. Compensation is not required for values less than 800Ω, and offers the fastest slew rate and widest bandwidth.

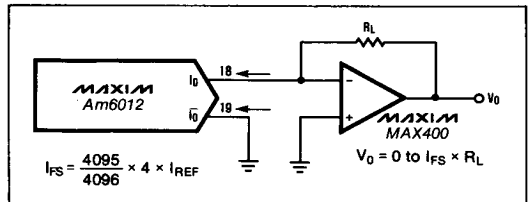
Multiplying Operation

The Am6012 provides excellent performance with an extremely linear relationship between I_{FS} and I_{REF} over a wide range of 1mA to 1μA. Monotonic operation is typically maintained over the 100μA to 1mA range. Gain linearity is slightly degraded at low values of I_{REF}.

Analog Output Currents

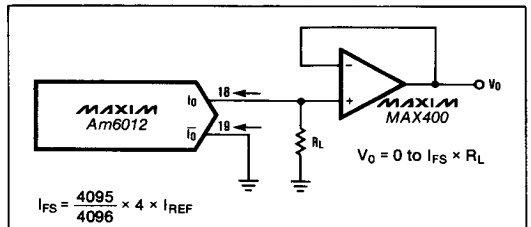
Both the true (I_0) and complemented ($\overline{I_0}$) outputs sink current, and the summation of the two currents equals the full scale current (I_{FS}) for all codes. The current at I_0 increases when a logic 1 is applied to each logic input. Conversely, a logic 0 decreases the current at I_0. Both of the outputs of the DAC can be used simultaneously. If either of the outputs are unused, it must be tied to ground or to a point that can source the I_{FS} current.

The output compliance voltage of the Am6012 is between +10V to +25V above the negative voltage supply. This allows a variety of current to voltage conversion schemers using both load resistors and/or op-amps as shown in figures 1, 3, and 4.



For complementary output (operation as a negative logic DAC), connect inverting input of op-amp to $\overline{I_O}$ (pin 19); connect I_O (pin 18) to GND.

Figure 3. Negative Low Impedance Output Operation



For complementary output (operation as a negative logic DAC), connect inverting input of op-amp to $\overline{I_O}$ (pin 19); connect I_O (pin 18) to GND.

Figure 4. Positive Low Impedance Output Operation

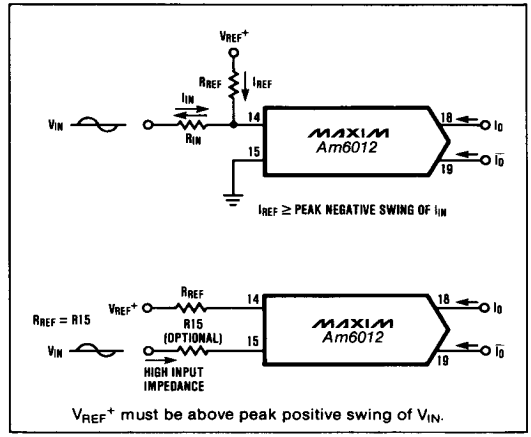


Figure 5. Accommodating Bipolar References

Settling Time

The typical full scale settling time of the Am6012 is 250ns for I_{REF} = 1mA. The full potential of the Am6012 is realized only through careful PC board layout, with particular attention to grounding. Analog ground should not be modulated by digital ground return currents. It is recommended that the digital and analog grounds be connected at one point near to the power supply ground. The fastest operation will be achieved by using short leads, minimizing output capacitance and load resistor values, and by adequate high frequency bypassing of supply, references, and V_{LC} pins. The supplies do not have to be decoupled with large electrolytic bypass capacitors since the Am6012 supply current is independent of input logic codes.

Temperature Performance

The nonlinearity and monotonicity specifications of the Am6012 are guaranteed to apply over the complete temperature range. Full scale output current drift is well controlled at 8ppm/°C, and the zero-scale output current and drift a small fraction of an LSB.

In the majority of situations external components contribute most of the errors due to temperature variations. The external voltage reference temperature coefficient (TC) directly contributes a TC to the output of the DAC. The reference resistor R14 and output scaling resistors also enter into the temperature error budget. The two resistors should track each other and have similar TC's. The reference resistor can have fixed power dissipation (assuming a fixed DC voltage reference), whereas, the scaling resistor has a power dissipation that is proportional to the square of the output voltage. For example at 0V the power dissipation is 0mW but at 10V using a 2.5kΩ resistor the power dissipation is 40mW. If the TCs of the resistors are too high this differential power dissipation can cause errors in the relative accuracy.

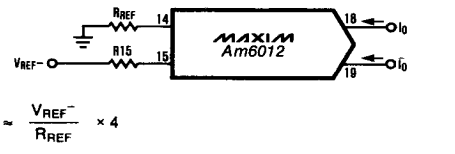


Figure 6. Basic Negative Reference Operation

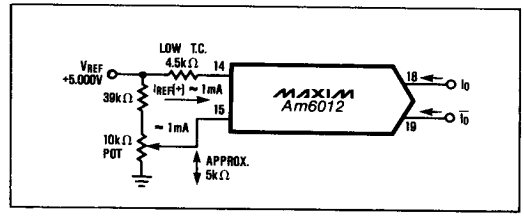


Figure 7. Recommended Full-Scale Adjustment Circuit

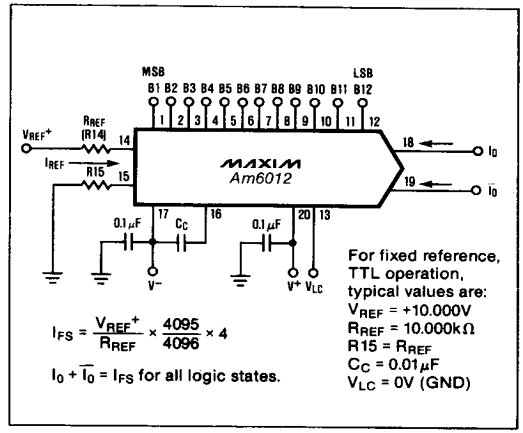


Figure 8. Basic Positive Reference Operation

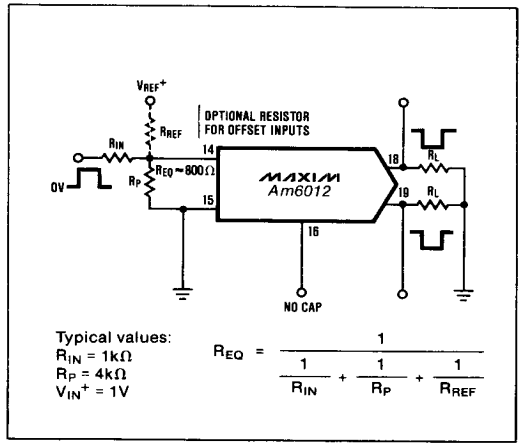
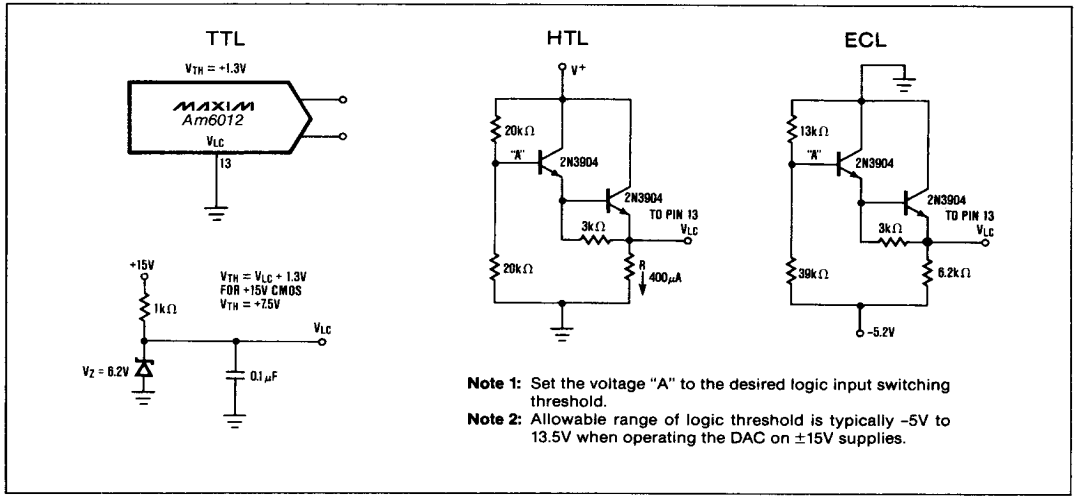


Figure 9. Pulsed Reference Operation

12-Bit High Speed Multiplying D/A Converter

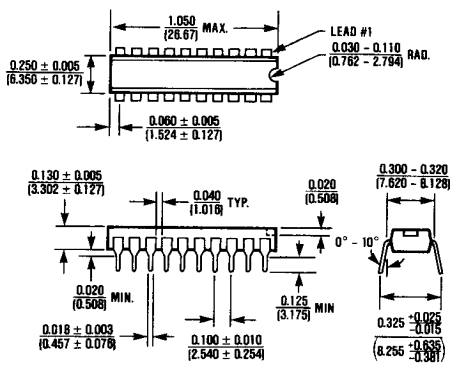


Note 1: Set the voltage "A" to the desired logic input switching threshold.

Note 2: Allowable range of logic threshold is typically -5V to 13.5V when operating the DAC on ±15V supplies.

Figure 10. Interfacing with Various Logic Families

Package Information

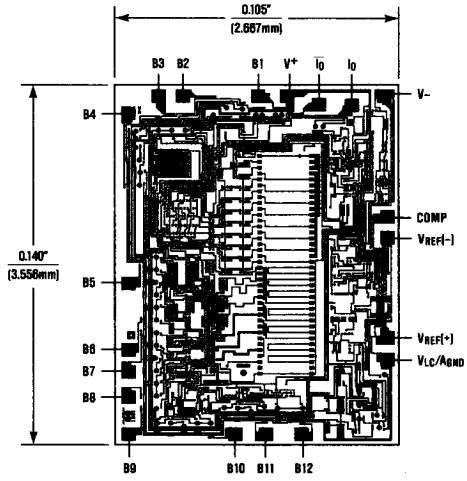


20 Lead Plastic DIP (PP)

θ_{JA} = 125°C/W

θ_{JC} = 60°C/W

Chip Topography



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