



AOD409
P-Channel Enhancement Mode Field Effect Transistor

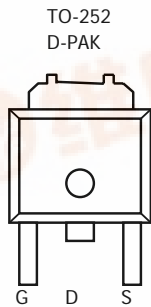


General Description

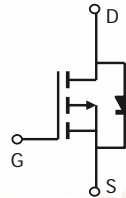
The AOD409 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. With the excellent thermal resistance of the DPAK package, this device is well suited for high current load applications. *Standard Product AOD409 is Pb-free (meets ROHS & Sony 259 specifications). AOD409L is a Green Product ordering option. AOD409 and AOD409L are electrically identical.*

Features

$V_{DS} (V) = -60V$
 $I_D = -26A (V_{GS} = -10V)$
 $R_{DS(ON)} < 40m\Omega (V_{GS} = -10V) @ -20A$
 $R_{DS(ON)} < 55m\Omega (V_{GS} = -4.5V)$



Top View
Drain Connected to Tab



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ C$	-26
		$T_C=100^\circ C$	-18
Pulsed Drain Current ^C	I_{DM}	-60	A
Avalanche Current ^C	I_{AR}	-26	A
Repetitive avalanche energy $L=0.1mH$ ^C	E_{AR}	134	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ C$	60
		$T_C=100^\circ C$	30
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ C$	2.5
		$T_A=70^\circ C$	1.6
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10s$	16.7	$^\circ C/W$
Maximum Junction-to-Ambient ^A		Steady-State	40	$^\circ C/W$
Maximum Junction-to-Case ^C	$R_{\theta JC}$	1.9	2.5	$^\circ C/W$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$	-60			V	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-48\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$		-0.003	-1	μA	
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 100	nA	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1.2	-1.9	-2.4	V	
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}$, $V_{DS}=-5\text{V}$	-60			A	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$, $I_D=-20\text{A}$ $T_J=125^\circ\text{C}$		32	40	$\text{m}\Omega$	
		$V_{GS}=-4.5\text{V}$, $I_D=-20\text{A}$		53		$\text{m}\Omega$	
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-20\text{A}$		32		S	
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.73	-1	V	
I_S	Maximum Body-Diode Continuous Current				-30	A	
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-30\text{V}$, $f=1\text{MHz}$		2977	3600	pF	
C_{oss}	Output Capacitance				241		pF
C_{rss}	Reverse Transfer Capacitance				153		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		2	2.4	Ω	
SWITCHING PARAMETERS							
$Q_g(10\text{V})$	Total Gate Charge (10V)	$V_{GS}=-10\text{V}$, $V_{DS}=-30\text{V}$, $I_D=-20\text{A}$		44	54	nC	
$Q_g(4.5\text{V})$	Total Gate Charge (4.5V)			22.2	28	nC	
Q_{gs}	Gate Source Charge			9		nC	
Q_{gd}	Gate Drain Charge			10		nC	
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-10\text{V}$, $V_{DS}=-30\text{V}$, $R_L=1.5\Omega$, $R_{GEN}=3\Omega$		12		ns	
t_r	Turn-On Rise Time			14.5		ns	
$t_{D(off)}$	Turn-Off DelayTime			38		ns	
t_f	Turn-Off Fall Time			15		ns	
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		40	50	ns	
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		59		nC	

A: The value of R qJA is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation PDSM is based on R qJA and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation PD is based on $T_J(\text{MAX})=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_J(\text{MAX})=175^\circ\text{C}$.

D: The R qJA is the sum of the thermal impedance from junction to case R qJC and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 ms pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_J(\text{MAX})=175^\circ\text{C}$.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

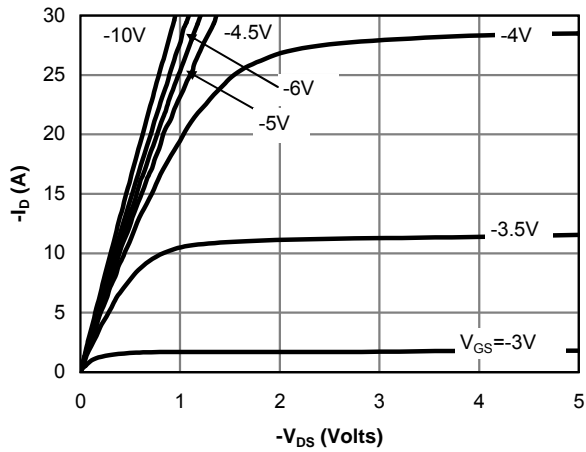


Fig 1: On-Region Characteristics

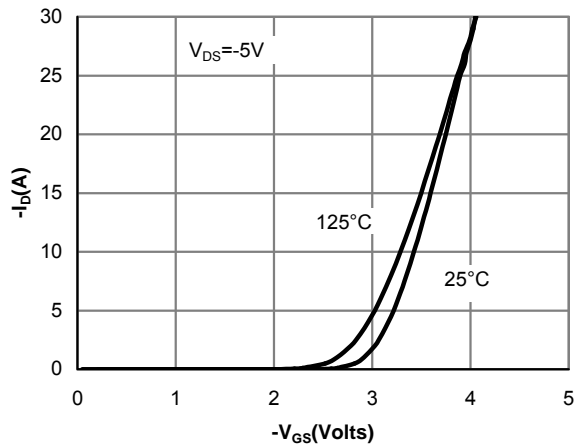


Figure 2: Transfer Characteristics

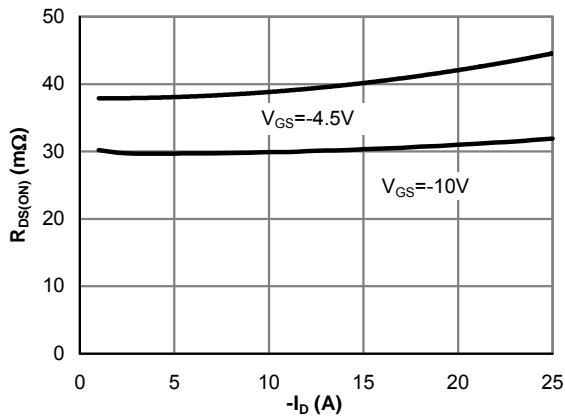


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

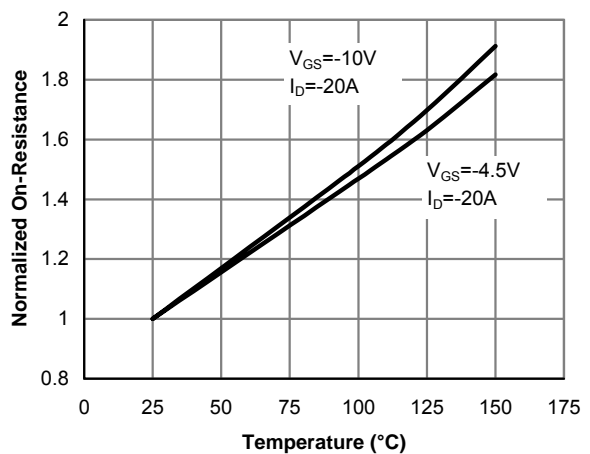


Figure 4: On-Resistance vs. Junction Temperature

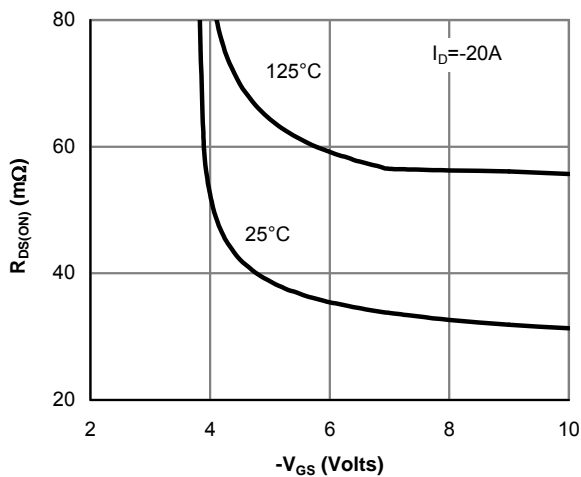


Figure 5: On-Resistance vs. Gate-Source Voltage

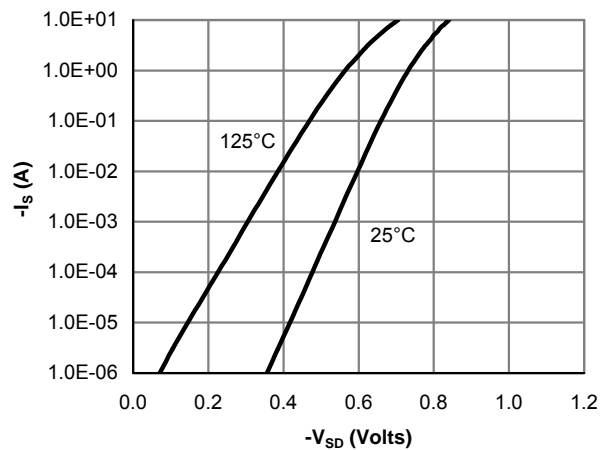


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

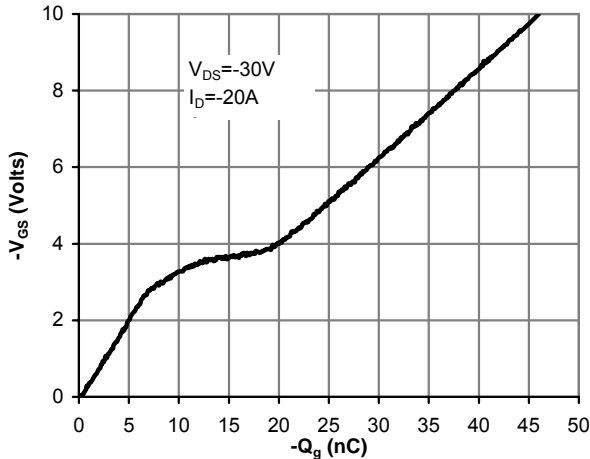


Figure 7: Gate-Charge Characteristics

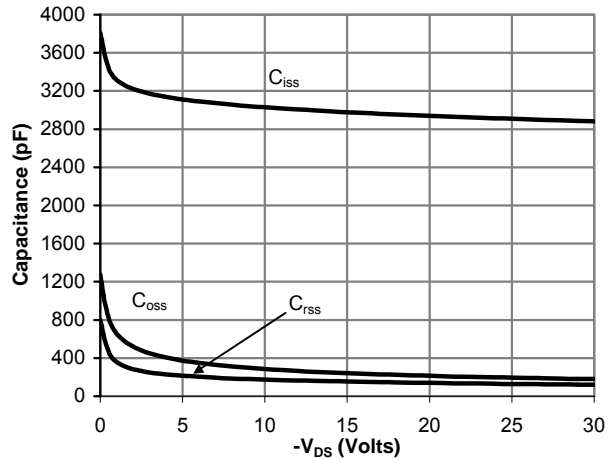


Figure 8: Capacitance Characteristics

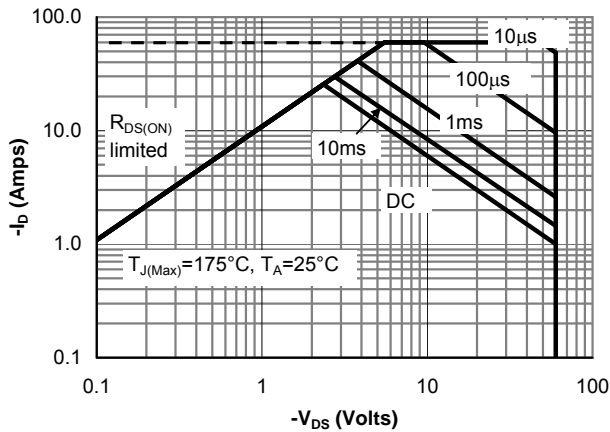


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

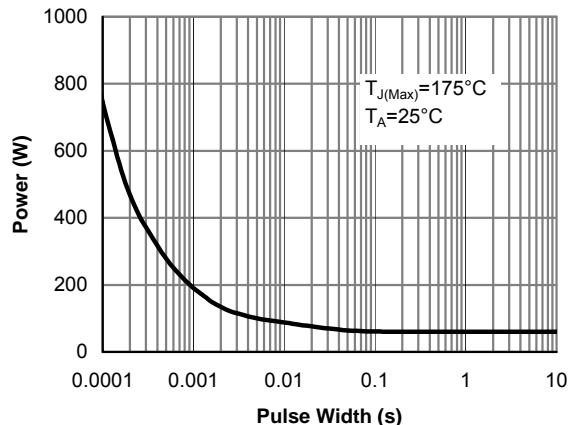


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

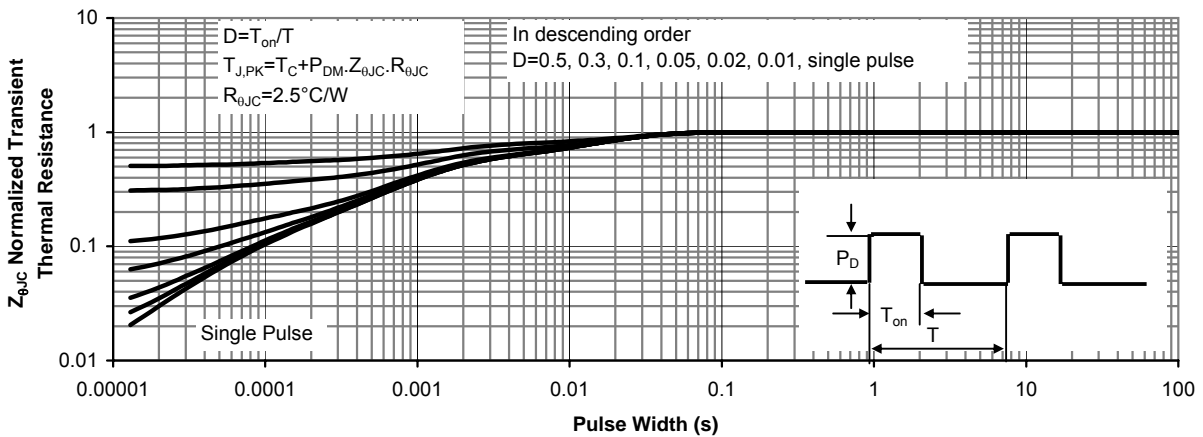


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

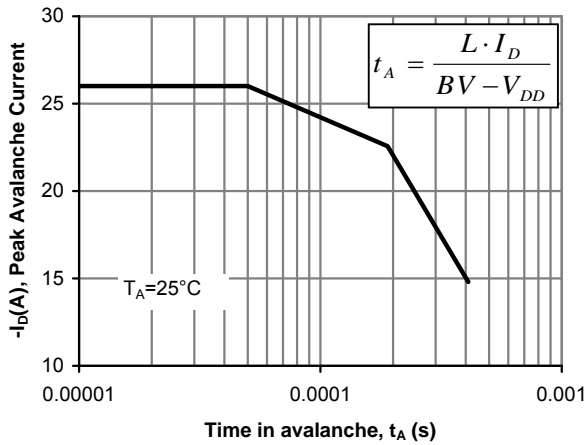


Figure 12: Single Pulse Avalanche capability

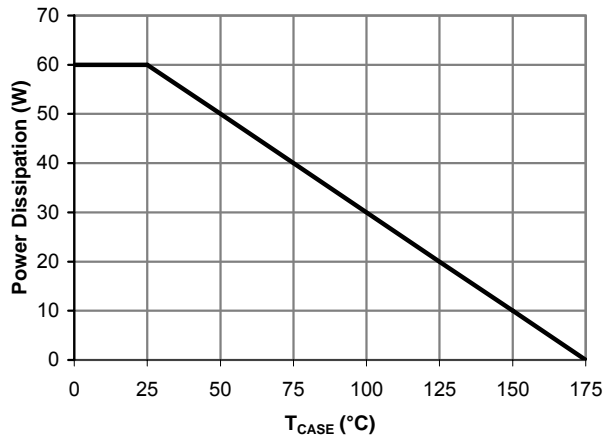


Figure 13: Power De-rating (Note B)

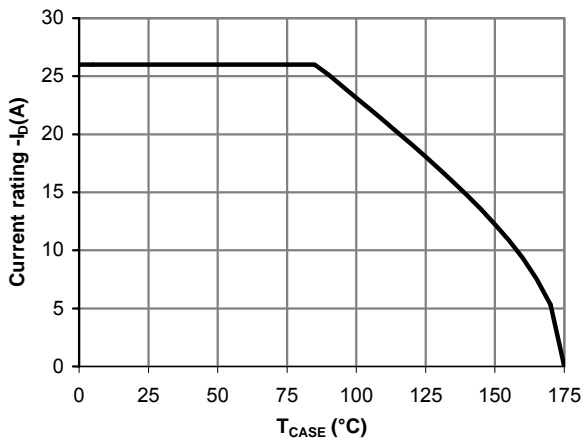


Figure 14: Current De-rating (Note B)

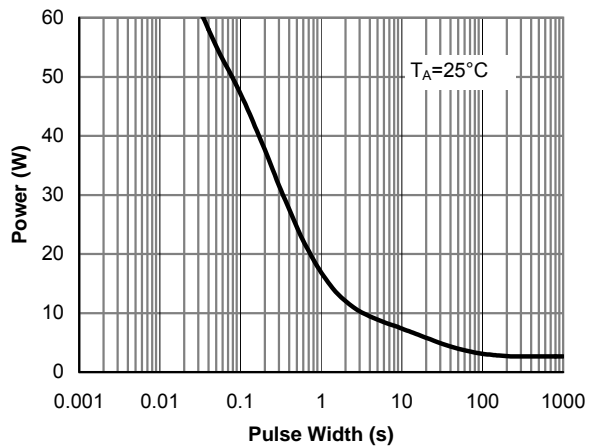


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

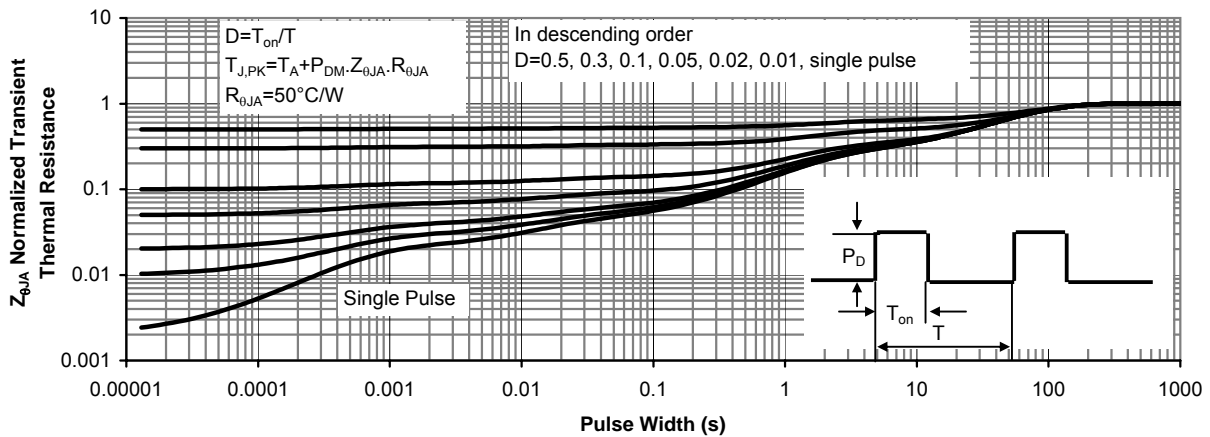


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)