



AON3814

Common-Drain Dual N-Channel Enhancement Mode Field Effect Transistor

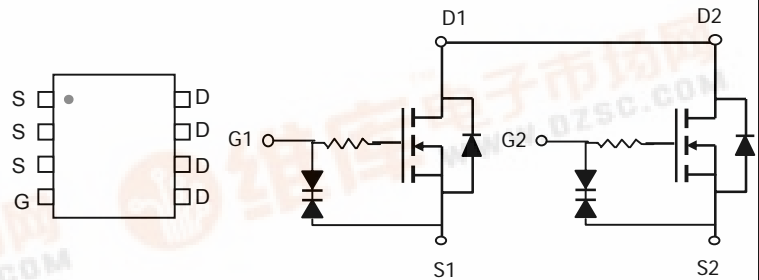
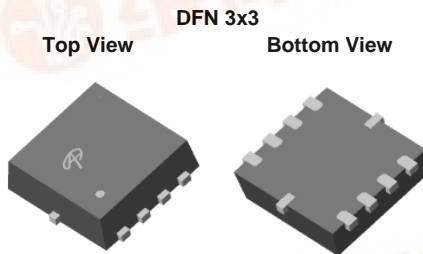


General Description

The AON3814 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V while retaining a 12V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch, facilitated by its common-drain configuration. *Standard Product AON3814 is Pb-free (meets ROHS & Sony 259 specifications).*

Features

- V_{DS} (V) = 20V
- I_D = 6A (V_{GS} = 4.5V)
- $R_{DS(ON)} < 17m\Omega$ (V_{GS} = 4.5V)
- $R_{DS(ON)} < 18.5m\Omega$ (V_{GS} = 4V)
- $R_{DS(ON)} < 24m\Omega$ (V_{GS} = 2.5V)
- $R_{DS(ON)} < 39m\Omega$ (V_{GS} = 1.8V)
- ESD Protected



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ^F	I_D	$T_A=25^\circ C$	6
		$T_A=70^\circ C$	5.3
Pulsed Drain Current ^B	I_{DM}	30	A
Power Dissipation ^F	P_D	$T_A=25^\circ C$	2.4
		$T_A=70^\circ C$	1.5
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	43	52	$^\circ C/W$
Maximum Junction-to-Ambient ^A		Steady-State	75	90
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	36	50	$^\circ C/W$



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Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±10V			10	μA
BV _{GSO}	Gate-Source Breakdown Voltage	V _{DS} =0V, I _G =±250μA	±12			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.4	0.71	1.1	V
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V	30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =4.5V, I _D =6A T _J =125°C	11 15	14 19	17 24	mΩ
		V _{GS} =4V, I _D =6A	11.5	15	18.5	
		V _{GS} =2.5V, I _D =6A	14.5	19	24	
		V _{GS} =1.8V, I _D =6A	23	30	39	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =6A		25		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.75	1	V
I _S	Maximum Body-Diode Continuous Current				3.5	A
DYNAMIC PARAMETERS						
C _{ISS}	Input Capacitance	V _{GS} =0V, V _{DS} =10V, f=1MHz		1315		pF
C _{OSS}	Output Capacitance			219		pF
C _{RSS}	Reverse Transfer Capacitance			183		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		2.1		kΩ
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =4.5V, V _{DS} =10V, I _D =6A		13.1		nC
Q _{gs}	Gate Source Charge			6.7		nC
Q _{gd}	Gate Drain Charge			4.6		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =5V, V _{DS} =10V, R _L =1.7Ω, R _{GEN} =3Ω		1		μS
t _r	Turn-On Rise Time			2.8		μS
t _{D(off)}	Turn-Off DelayTime			5.6		μS
t _f	Turn-Off Fall Time			5.9		μS

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

F: The power dissipation and current rating is based on the t ≤ 10s thermal resistance, and current rating is also limited by wire-bonding.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

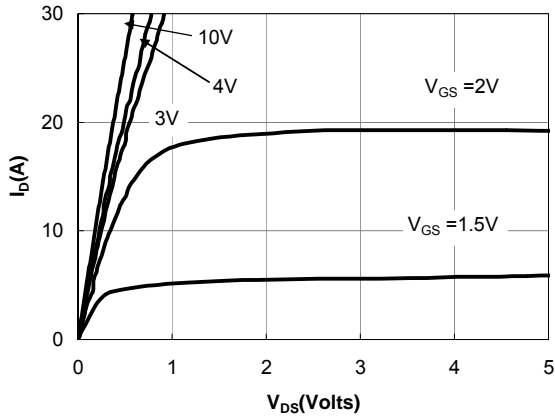


Figure 1: On-Regions Characteristic

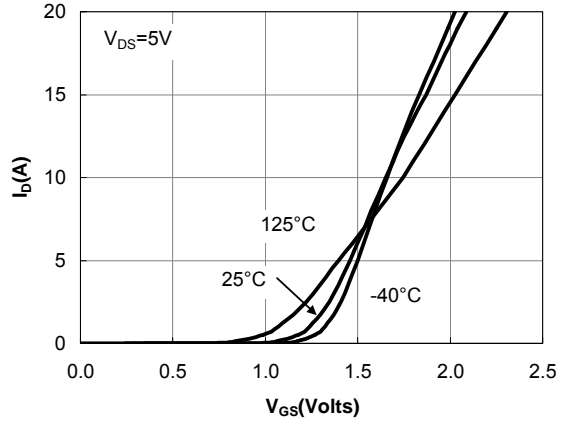


Figure 2: Transfer Characteristics

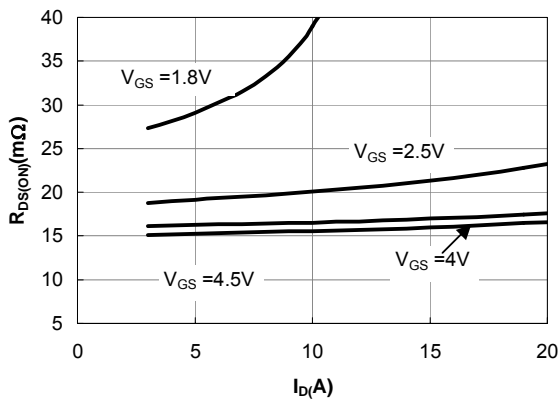


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

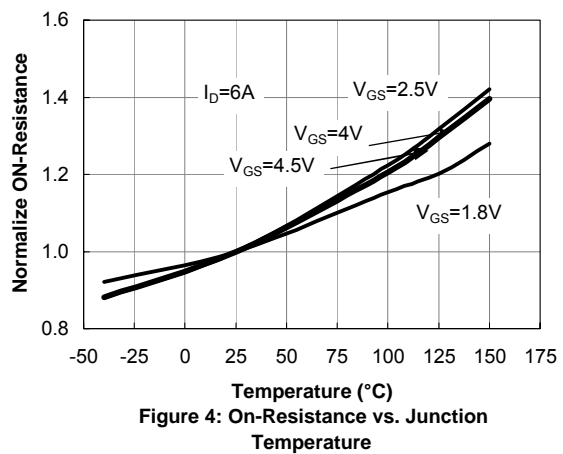


Figure 4: On-Resistance vs. Junction Temperature

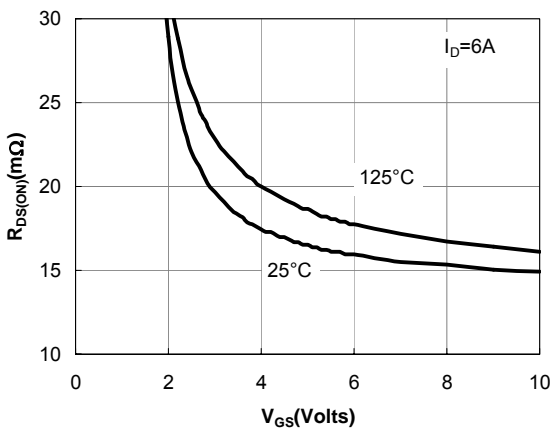


Figure 5: On-Resistance vs. Gate-Source Voltage

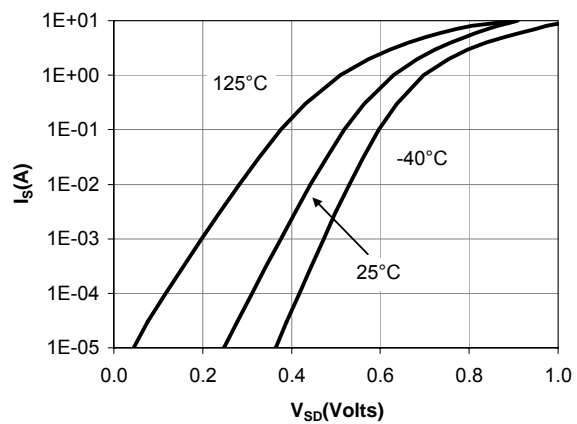


Figure 6: Body-Diode Characteristics

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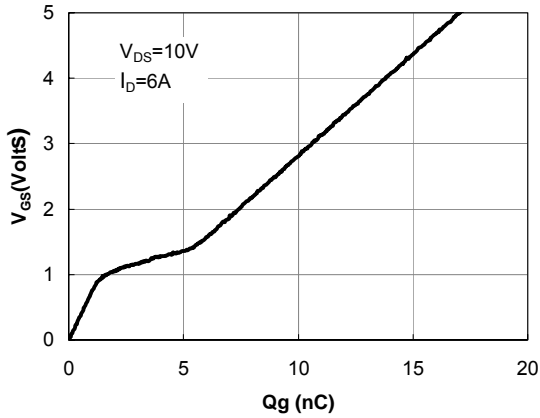


Figure 7: Gate-Charge Characteristics

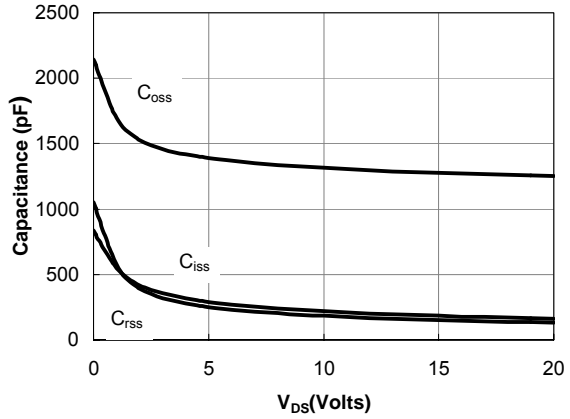


Figure 8: Capacitance Characteristics

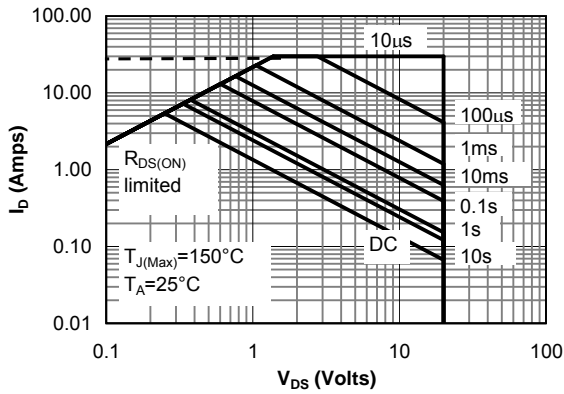


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

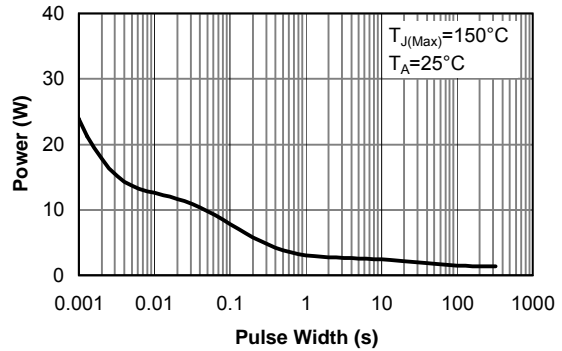


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

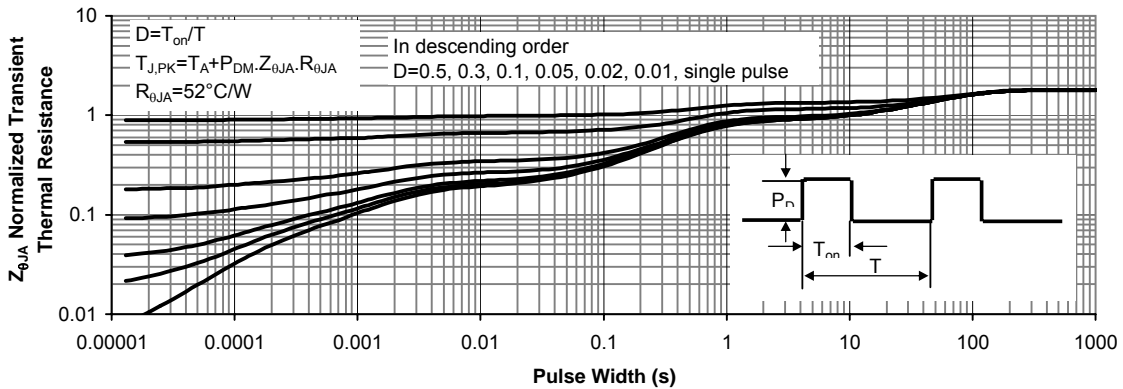


Figure 11: Normalized Maximum Transient Thermal Impedance