APX6219

PWM Stepper Motor Driver

Features

- Able to Drive Both Windings of Bipolar Stepper Motor
- Up to 750 mA Continuous Output Current for Each Winding
- Up to 28V Output Sustaining Voltage
- Internal PWM Current Control
- Built-in Protection Diode
- Low Output Saturation Voltage
- Internal Thermal Shutdown
- Lead Free Available (RoHS Compliant)

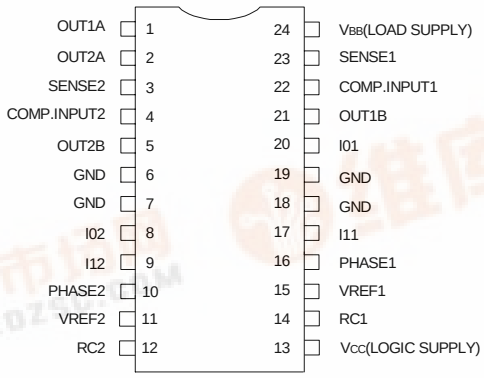
Applications

- Scanner
- Stepping Motor Control
- Thermal Printer

General Description

The APX6219 is designed to drive both winding of a two-phase bipolar stepper motor or bidirectionally control 2 DC motors. APX6219 includes two H-bridges capable of continuous output current of ±750 mA with peak start up to 1A and operating voltages up to 28V. Motor winding current can be controlled by the internal fixed-frequency, pulse-width modulated (PWM), current-control circuitry. Wide range current control is controlled by means of two logic inputs with a external reference voltage for each bridge. The peak load current limit is set by the user's selection of a reference voltage and current-sensing resistor. Two logic-level select output current limits of 0%,33%, 67%, or 100% of the maximum level. A phase input to each bridge determines load current direction. A thermal shutdown protection circuit disables the outputs if the chip temperature over the safe operation limit. The APX6219 come in SOP-24 package.

Pin Configuration



SOP-24 (Top View)

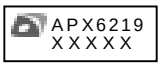
Ordering and Marking Information

APX6219 □□-□□□

- Lead Free Code
- Handling Code
- Temp. Range
- Package Code

Package Code
K : SOP - 24
Temp. Range
I : -40 ~ 85 °C
Handling Code
TU : Tube TR : Tape & Reel
Lead Free Code
L : Lead Free Blank : Original Device

APX6219 K :



XXXXX - Date Code

Notes: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte in plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

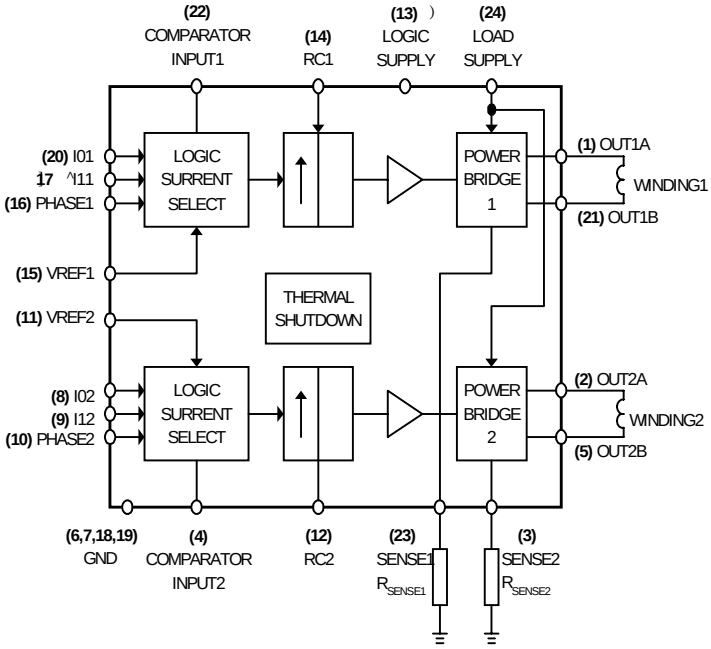
Pin Description

PIN NO.	PIN Name	I/O	Description
1,2	OUTPUT A	O	H- bridge Output connection. The output stage is a "H" bridge formed by four transistors and four-protection diode for switching applications.
3,23	Sense Resistor	O	Connection to lower emitters of output stage for insertion of current sensor resistor to check the peak value of output current
4,22	Comparator Input	I	The voltage across the sense resistor is feedback to this input through the low pass filter R_C C_C. The higher power transistors are disabled when the sense voltage exceeds the reference voltage of selected comparator. The current decays for a time set by R_T C_T when this happen
5,21	OUTPUT B	O	See pins 1,2
6,7,18,19	Ground		Ground connection
8,9	I02/I12	I	These pins are logic inputs which select the outputs of the comparators to set the output current level. Current also depends on the sensing resistor and reference voltage.

I0	I1	Current level
H	H	No current
L	H	Low current 1/3 I_O max
H	L	Medium current 2/3 I_O max
L	L	Maximum current I_O max

20,17	I01/I11	I	See pins 8,9; current level control for channel2
10,16	PHASE	I	This TTL-compatible logic input sets the current flow direction through load. A schmitt trigger with this input provides the noise immunity and a delay circuit prevents output stage short circuits during switching
11,15	Reference Voltage	I	A voltage apply this pin sets the input of a comparator to control the output current
12,14	R_TC_T	O	A R_TC_T connection to this pin sets the off time of higher power transistor
13	V_{CC}		Logic supply voltage
24	V_{BB}		Load supply voltage

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{BB}	Load Supply Voltage	30	V
I_O	Output Current (Peak)	±1	A
I_O	Output Current (Continuous)	±750	mA
V_{CC}	Logic Supply Voltage	7	V
V_{IN}	Logic Input Voltage	-0.3 to V_{CC}+0.3	V
V_{SENSE}	Driver Output Sense Voltage	1.5	V
$R_{TH,JA}$	Thermal Resistance – Junction to Ambient* SOP-24	75	°C/W
$R_{TH,JC}$	Thermal Resistance – Junction to Case SOP-24	15	°C/W
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	0 to 150	°C
T_{OP}	Operating Temperature Range	0 to 70	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (Soldering, 10 second)	260	°C

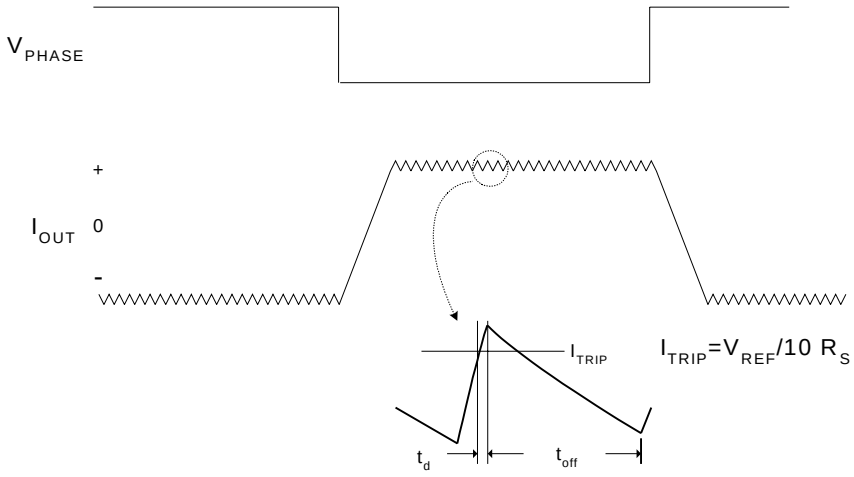
(*) With minimized copper area.

Electrical Characteristics

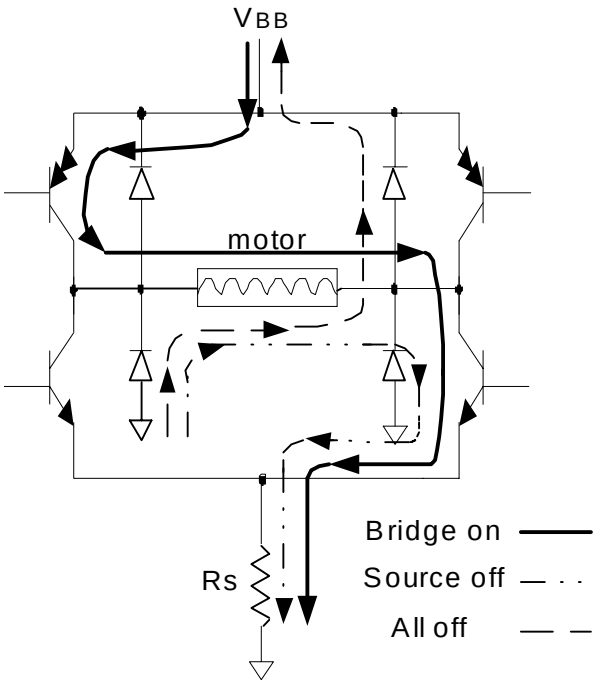
Unless otherwise noted these specifications apply over full temperature, V_{BB}=28V, V_{CC}=4.75 to 5.25V, V_{REF}=5V, T_J=0 to 125°C . Typical values refer to T_J=25°C .

Symbol	Parameter	Test Conditions	APX6219			Unit
			Min.	Typ.	Max.	
Output drivers (OUTA or OUTB)						
V_{BB}	Motor Supply Voltage		10		28	V
I_{LEAK}	Output Leakage Current	$V_{OUT}=V_{BB}$ $V_{OUT}=0$		<1 <-1	50 -50	µA
V_{CE}(sat)	Output Saturation Voltage	Sink driver, I_{OUT}=+500mA Sink driver, I_{OUT}=+750mA Source driver, I_{OUT}=-500mA Source driver, I_{OUT}=-750mA		0.4 0.8 1.1 1.4	0.7 1.1 1.4 1.7	V
I_R	Clamp Diode Leakage Current	V_R=28V		<1	50	µA
V_F	Clamp Diode Forward Voltage	Sink diode Source diode I_F=750mA		1.6 1.6	2 2	V
I_{BB}(on)	Driver Supply Current	Both bridges ON, no load		14	25	mA
I_{BB}(off)	Driver Supply Current	Both bridges OFF		2	10	mA
Control logic						
V_{IH}	Voltage Input	All inputs	2.4			V
V_{IL}	Voltage Input	All inputs			0.8	V
I_{IH}	Input Current	V_{IN}=2.4V		<1	20	µA
I_{IL}	Input Current	V_{IN}=0.8V		-5	-50	µA
V_{REF}	Reference Voltage		1.5		7.5	V
I_{CC} (on)	Logic Supply Current	I0=I1=0.8V, no load		47	57	mA
I_{CC} (off)	Logic Supply Current	I0=I1=2.4V, no load		8	14	mA
V_{REF}/V_{SENSE}	Current Limit Threshold (at trip point)	I0=I1=0.8V I0=2.4V,I1=0.8V I0=0.8V,I1=2.4V	9.5 13.5 25.5	10 15 30	10.5 16.5 34.5	
T_{OFF}	Cutoff Time	R_T=56KΩ, C_T=820pF		45		µs
T_D	Turn off Delay			2		µs
Protection						
OTS	Over Temperature Shutdown			150		°C
	Over Temperature Shutdown Hystersis	Hystersis		20		°C

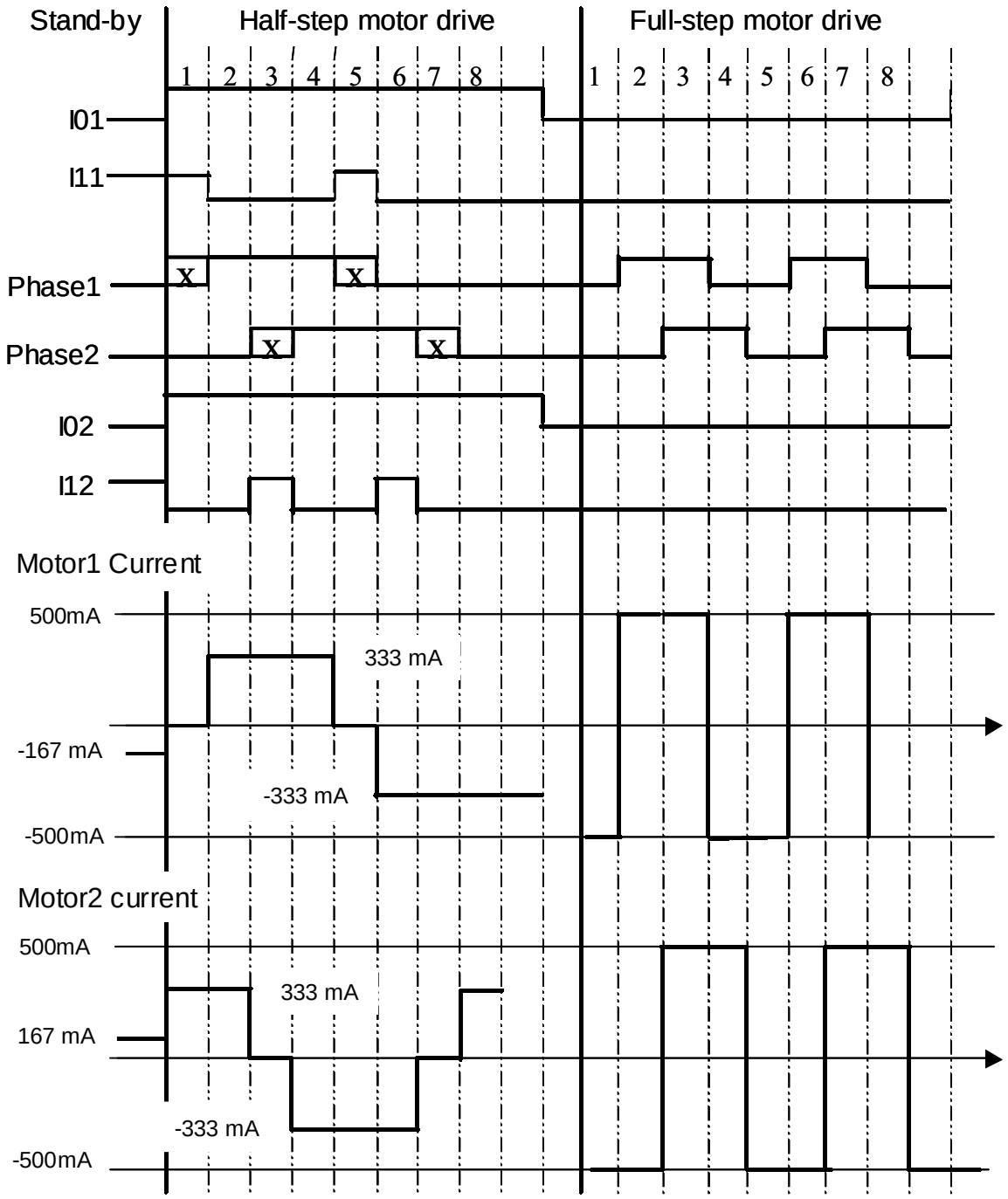
PWM Output Current Waveform



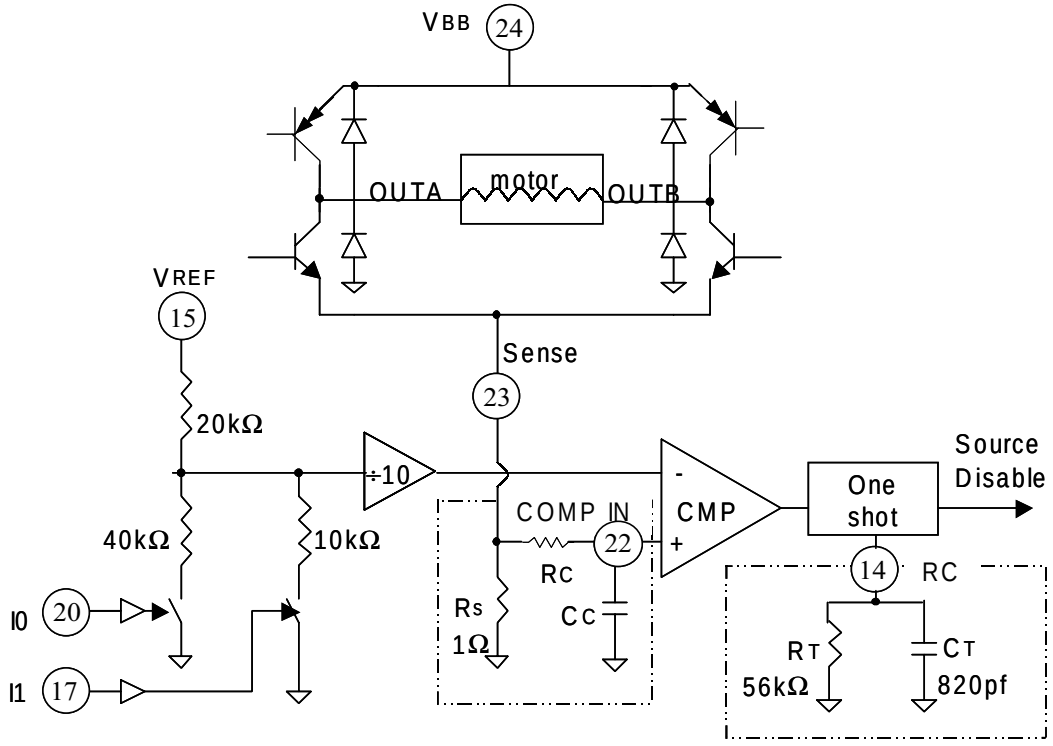
Load Current Paths



Principle Operating Sequence



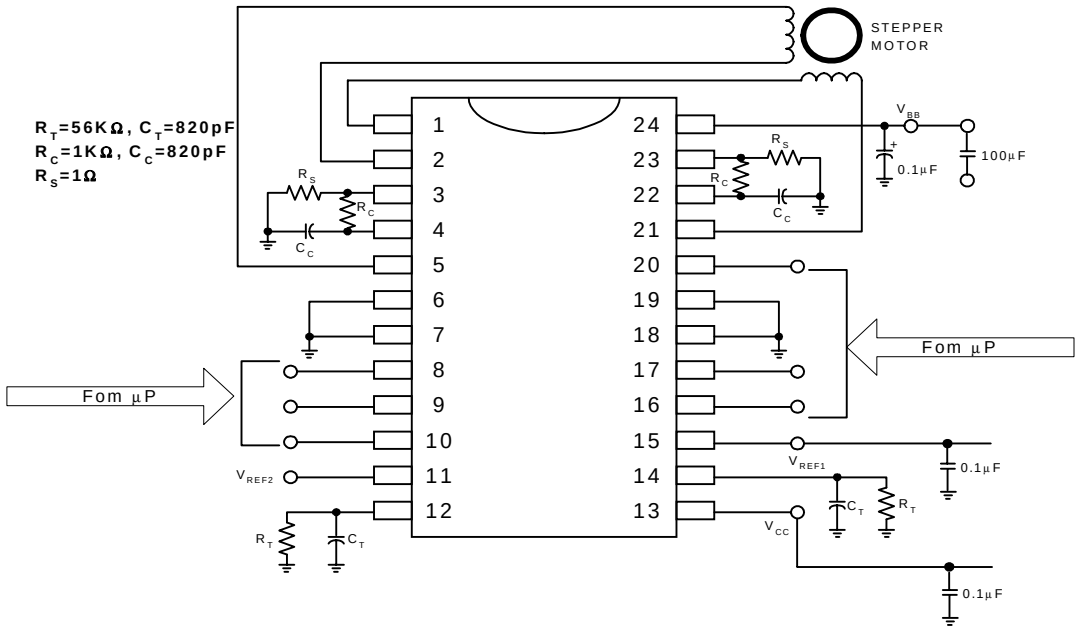
PWM Current-Control Circuitry



True Table

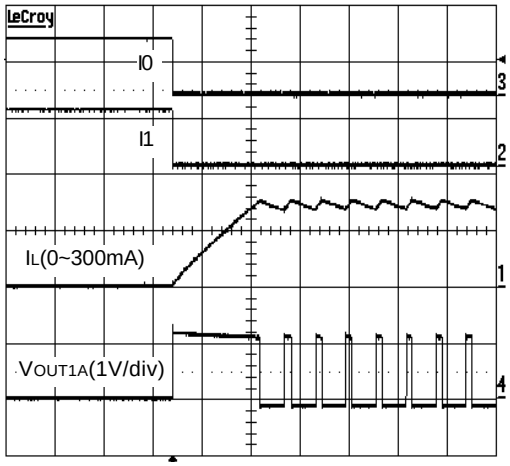
Phase	OUTA	OUTB
H	H	L
L	L	H

Typical Application Circuit

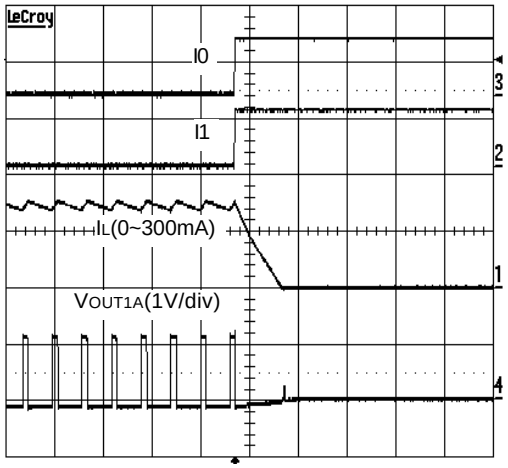


Typical Characteristics

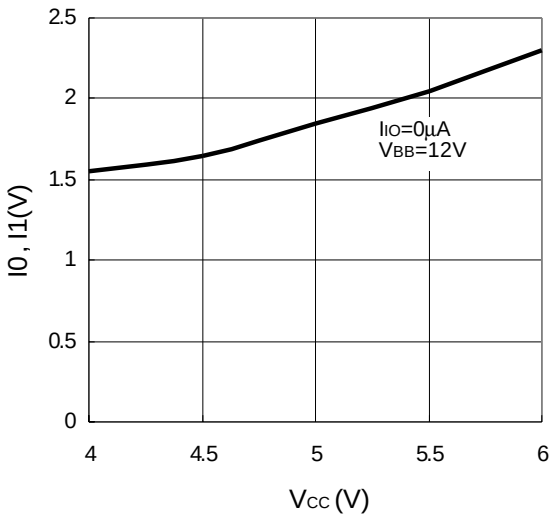
All Bridge Enable



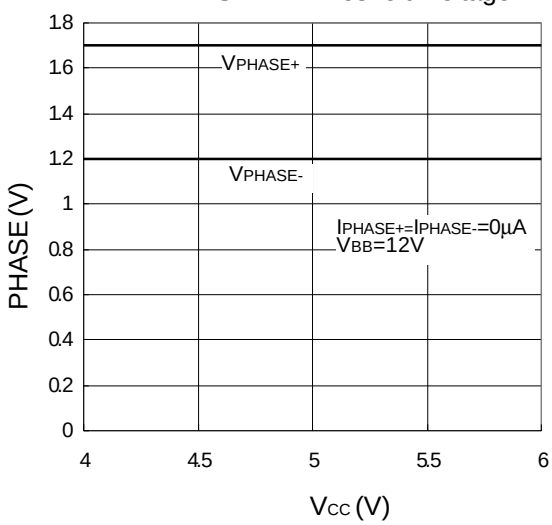
All Bridge Disable



I0, I1 Threshold Voltage

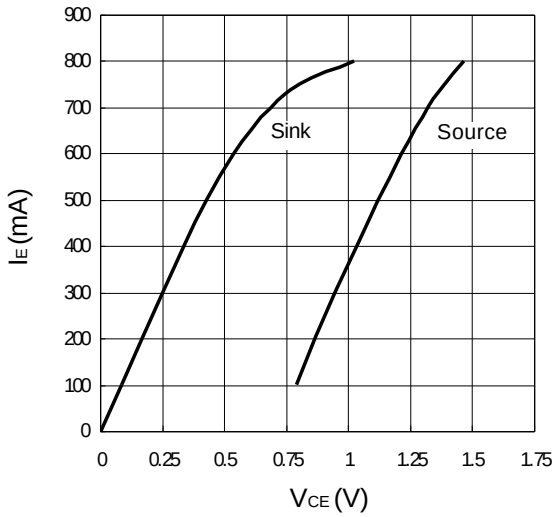


PHASE Pin Threshold Voltage

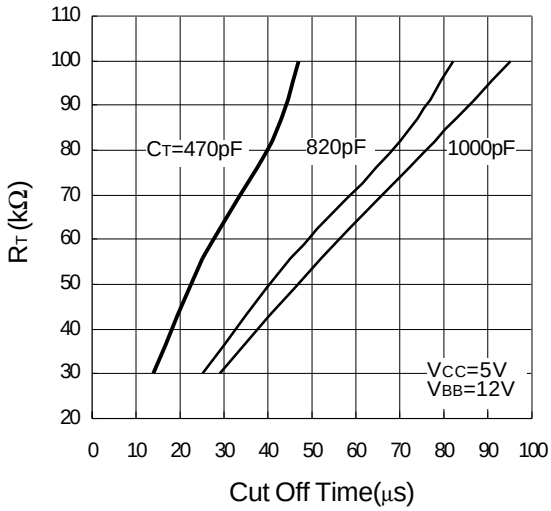


Typical Characteristics

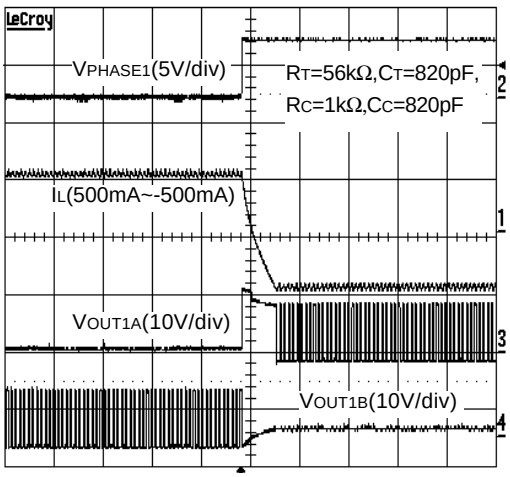
Output Saturation Voltage



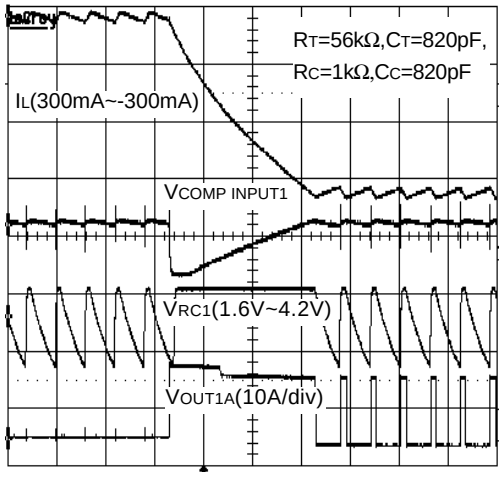
RTCT vs. Cut Off Time



Operating Waveform1

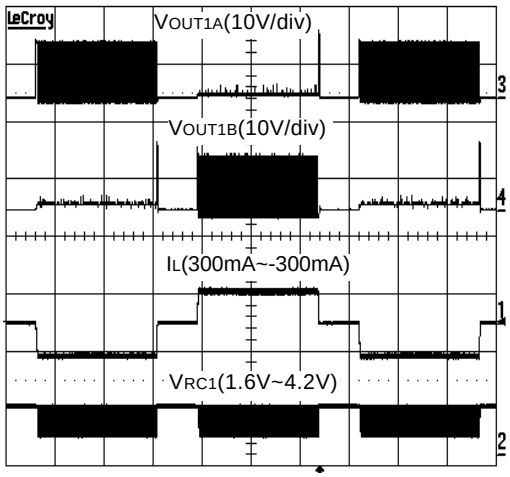


Operating Waveform2



Typical Characteristics

Half Stage Operation



Application Information

PWM Current Control

The APX6219 dual bridge is designed to drive both windings of a bipolar stepper motor. Output current is sensed and controlled independently in each bridge by an external sense resistor (R_S), internal comparator, and monostable multivibrator. When the bridge is turned on, current increases in the motor winding and it is sensed by the external sense resistor until the sense voltage (V_{COMPIN}) reaches the level set at the comparator's input:

$I_{TRIP} = V_{REF}/10\ R_S$

The comparator then triggers the monostable which turns off the source driver of the bridge. The actual load current peak will be slightly higher than the trip point (especially for low-inductance loads) because of the internal logic and switching delays. This delay (T_D) is typically 2μs. After turn-off, the motor current decays, going through the ground-clamp diode and sink transistor (source off). The source driver's off time is determined by the external RC timing components, where $T_{OFF} = R_TC_T$ within the range of 30kΩ to 100kΩ and 470pF to 1000pF.When VRC drop to certain voltage, the source driver will be re-enabled automatically (bridge on), the winding current is again limited at the desired level.

Loads with high V_{BB}, low L , high-frequency and low current will may result in high turn-on current peaks. This peak (appearing across R_S) will attempt to trip the comparator, resulting in erroneous current control or high-frequency oscillations. An external R_CC_C time delay should be used to form low pass filter to reduce noise to avoid the comparator's fault operation. The locations of R_C, C_C, R_C components should be as close to the APX6219 as possible.

Logic Control Of Output Current

Two logic level inputs (I0 and I1) allow digital selection of the motor winding current at 100%, 67%, 33%, or 0% of the maximum level per the table. The 0% output current condition turns off all drivers in the bridge and can be used as an OUTPUT Disable/Enable function.

During half-step operations, the I0 and I1 allow the μP to control the motor at a constant torque between all positions in an eight-step sequence. This is accomplished by digitally selecting 67% drive current when two phases are on. When all drivers are turn off will make rapid current decay when phases be changed. This helps to ensure proper motor operation at high step rates.

The logic control inputs can also be used to select a reduced current level (and reduced power dissipation) for 'hold' conditions and/or increased current (and available torque) for start-up conditions.

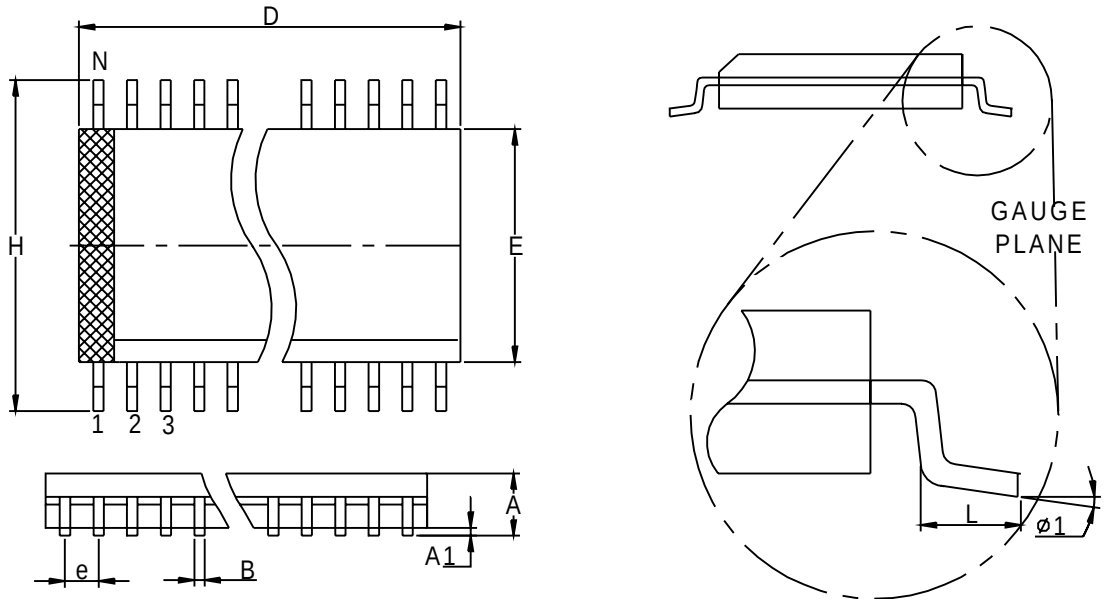
General

The PHASE input to each bridge determines the direction motor winding current flows. An internally generated deadtime (approximately 2μs) prevents shoot through that can occur when switching the PHASE input. Thermal protection circuitry turns off all drivers when the junction temperature reaches +150°C. It is only intended to protect the device from failures due to excessive junction temperature and should not imply that output short circuits are permitted. The output drivers are re-enabled when the junction temperature cools to +130°C.

The APX6219 output drivers are optimized for low output saturation, less than 2V (source plus sink) at loading 500mA.Under normal operating conditions, this allows continuous operation of both bridges simultaneously at 750mA (such as Typical Application).

Package Information

SO – 300mil (Reference JEDEC Registration MS-013)

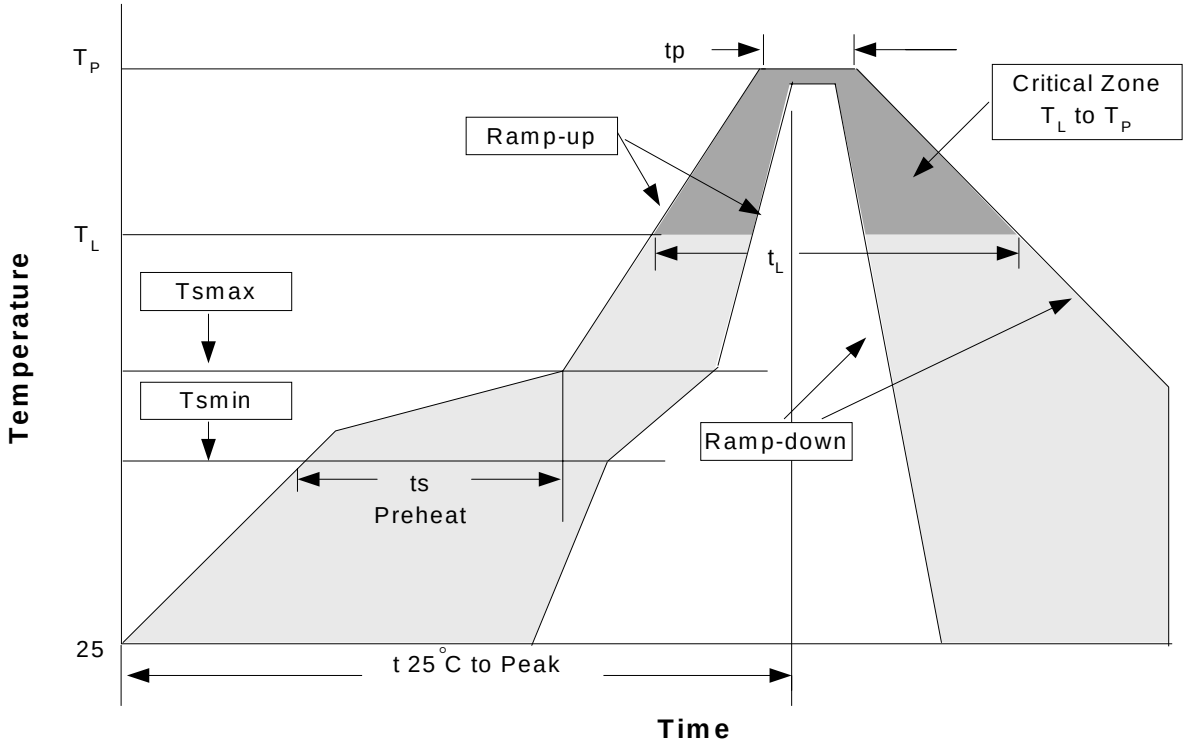


Dim	Millimeters		Variations- D			Dim	Inches		Variations- D		
	Min.	Max.	Variations	Min.	Max.		Min.	Max.	Variations	Min.	Max.
A	2.35	2.65	SO-16	10.10	10.50	A	0.093	0.1043	SO-16	0.398	0.413
A1	0.10	0.30	SO-18	11.35	11.76	A1	0.004	0.0120	SO-18	0.447	0.463
B	0.33	0.51	SO-20	12.60	13	B	0.013	0.020	SO-20	0.496	0.512
D	See variations		SO-24	15.20	15.60	D	See variations		SO-24	0.599	0.614
E	7.40	7.60	SO-28	17.70	18.11	E	0.2914	0.2992	SO-28	0.697	0.713
e	1.27BSC		SO-14	8.80	9.20	e	0.050BSC		SO-14	0.347	0.362
H	10	10.65				H	0.394	0.419			
L	0.40	1.27				L	0.016	0.050			
N	See variations					N	See variations				
ϕ 1	0°	8°				ϕ 1	0°	8°			

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classificatin Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classificatin Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

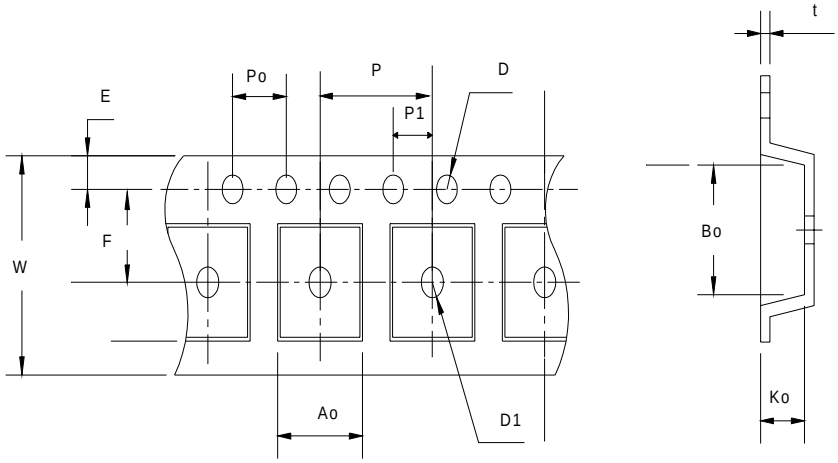
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

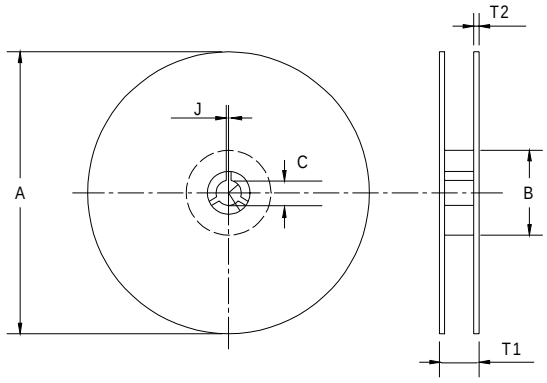
Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Carrier Tape



Carrier Tape(Cont.)



Application	A	B	C	J	T1	T2	W	P	E
SOP- 24	330±1	62 ±1.5	12.75 ± 0.15	2 ± 0.6	24.4 ± 0.2	2± 0.2	24 ± 0.3	12 ± 0.1	.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	11.5 ± 0.1	1.55 +0.1	1.5+ 0.25	4.0 ± 0.1	2.0 ± 0.1	10.9 ± 0.1	15.9± 0.1	3.1± 0.1	.35±0.05

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 24	24	21.3	1000

Customer Service

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