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Oki, Network Solutions for a Global Society

OKI Semiconductor

FEDD51X17400F-03
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MSM51X17400F

4,194,304-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM51X17400F is a 4,194,304-word × 4-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM51X17400F achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM51X17400F is available in a 26/24-pin plastic TSOP.

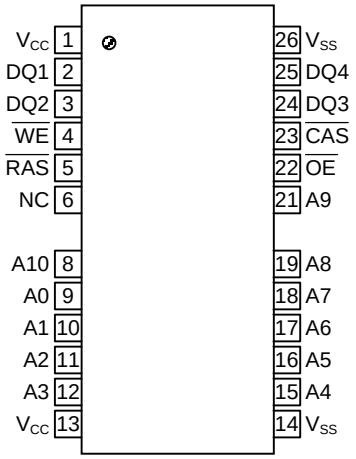
FEATURES

· 4,194,304-word × 4-bit configuration
· Single 2.0V power supply, ±0.15V tolerance
· Input : CMOS Interface, low input capacitance
· Output : CMOS Interface, 3-state
· Refresh : 2048 cycles/32ms
· Fast page mode, read modify write capability
· $\overline{CAS}$ before $\overline{RAS}$ refresh capability
· Packages
26/24-pin 300mil plastic TSOP (TSOPII26/24-P-300-1.27-K) (Product : MSM51X17400F-xxTS-K)
xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM51X17400F-10	100ns	50ns	20ns	20ns	200ns	200mW	1.1mW

PIN CONFIGURATION (TOP VIEW)

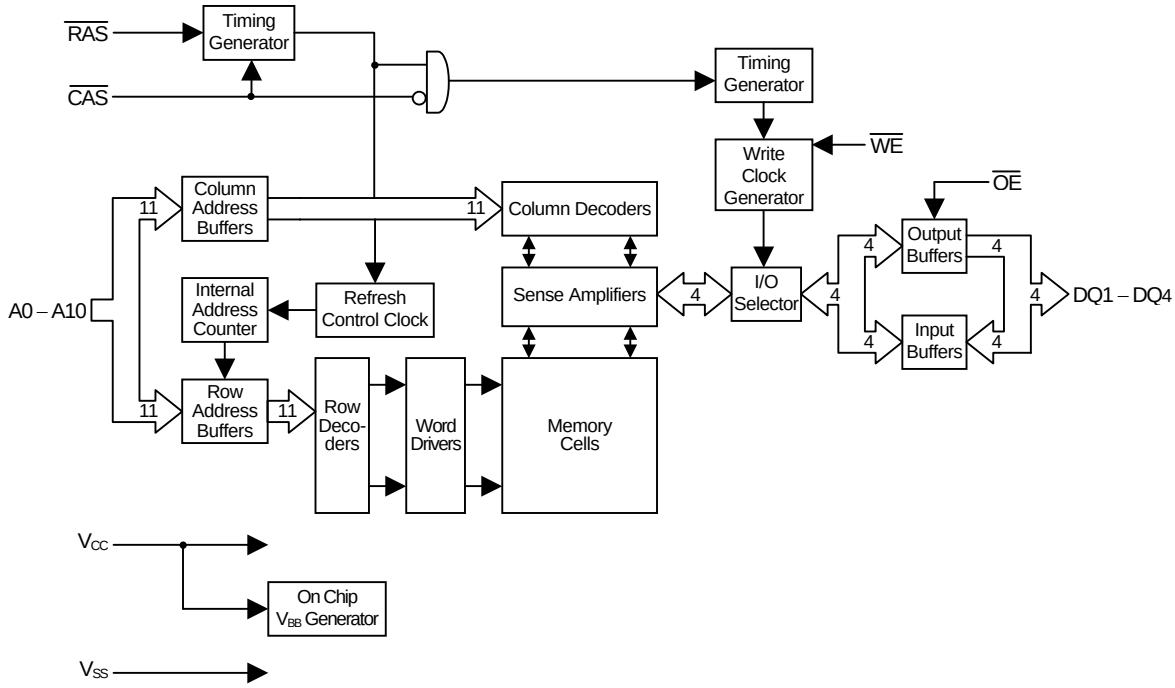


26/24-Pin Plastic TSOP
(K Type)

Pin Name	Function
A0–A10	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQ1–DQ4	Data Input/Data Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground (0V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to V_{CC}+ 0.5	V
Voltage V_{CC} Supply relative to V_{SS}	V_{CC}	–0.5 to 3.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_{D*}	1	W
Operating Temperature	T_{opr}	–10 to 70	°C
Storage Temperature	T_{stg}	–55 to 150	°C

*: Ta = 25°C

RECOMMENDED OPERATING CONDITIONS

(Ta = –10 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	1.85	2.0	2.15	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	0.8 × V_{CC}	—	V_{CC} +0.2	V
Input Low Voltage	V_{IL}	–0.2	—	0.2 × V_{CC}	V

PIN CAPACITANCE

(V_{CC} = 2.0V±0.15V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (A0 – A10)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 – DQ4)	$C_{I/O}$	—	7	pF

DC CHARACTERISTICS

(V_{CC} = 2.0V ± 0.15V, Ta = –10 to 70°C)

Parameter	Symbol	Condition	MSM51X17400 F-10		Unit	Note
			Min.	Max.		
Input High Voltage	V_{IH}		0.8 × V_{CC}	V_{CC} +0.2	V	
Input Low Voltage	V_{IL}		–0.2	0.2 × V_{CC}	V	
Output High Voltage	V_{OH}	I_{OH} = –100μA	0.85 × V_{CC}	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 100μA	0	0.15 × V_{CC}	V	
Input Leakage Current	I_{LI}	0V ≤ V_I ≤ V_{CC}; All other pins not under test = 0V	–10	10	μA	
Output Leakage Current	I_{LO}	DQ disable 0V ≤ V_O ≤ V_{CC}	–10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.	—	90	mA	1,2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	2	mA	1
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2V	—	0.5		
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ = cycling, $\overline{CAS}$ before $\overline{RAS}$	—	90	mA	1,2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min.	—	90	mA	1,3

Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. The address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC CHARACTERISTICS (1/2)

(V_{CC} = 2.0V ± 0.15V, Ta = –10 to 70°C) Note 1,2,3

Parameter	Symbol	MSM51X17400 F-10		Unit	Note
		Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	200	—	ns	
Fast Page Mode Cycle Time	t_{PC}	60	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	100	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	20	ns	4, 5
Access Time from Column Address	t_{AA}	—	50	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	55	ns	4
Access Time from $\overline{OE}$	t_{OEA}	—	20	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	ns	4
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	t_{OFF}	0	25	ns	7
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	25	ns	7
Transition Time	t_T	3	50	ns	3
Refresh Period	t_{REF}	—	32	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t_{ROH}	20	—	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	15	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	ns	

AC CHARACTERISTICS (2/2)

(V_{CC} = 2.0V ± 0.15V, Ta = –10 to 70°C) Note 1,2,3

Parameter	Symbol	MSM51X17400 F-10		Unit	Note
		Min.	Max.		
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	80	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	50	ns	6
Row Address Set-up Time	t_{ASR}	5	—	ns	
Row Address Hold Time	t_{RAH}	15	—	ns	
Column Address Set-up Time	t_{ASC}	5	—	ns	
Column Address Hold Time	t_{CAH}	20	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	50	—	ns	
Read Command Set-up Time	t_{RCS}	5	—	ns	
Read Command Hold Time	t_{RCH}	5	—	ns	8
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	5	—	ns	8
Write Command Set-up Time	t_{WCS}	5	—	ns	
Write Command Hold Time	t_{WCH}	20	—	ns	
Write Command Pulse Width	t_{WP}	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	ns	
Data-in Set-up Time	t_{DS}	5	—	ns	
Data-in Hold Time	t_{DH}	20	—	ns	
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	15	—	ns	

Notes: 1. A start-up delay of 200μs is required after power-up, followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.

2. The AC characteristics assume t_T = 5ns.

3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.

4. This parameter is measured with a load circuit equivalent to 30pF.

5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC}.

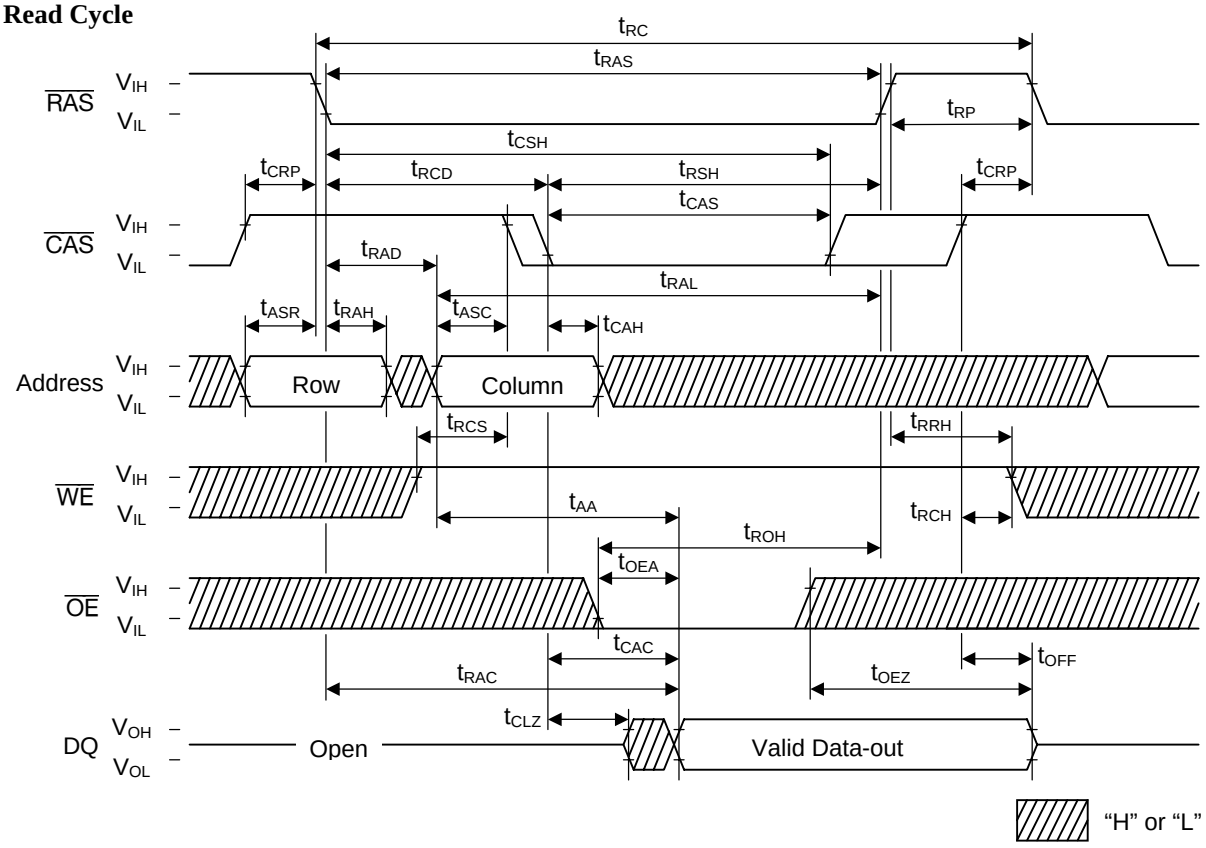
6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA}.

7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.

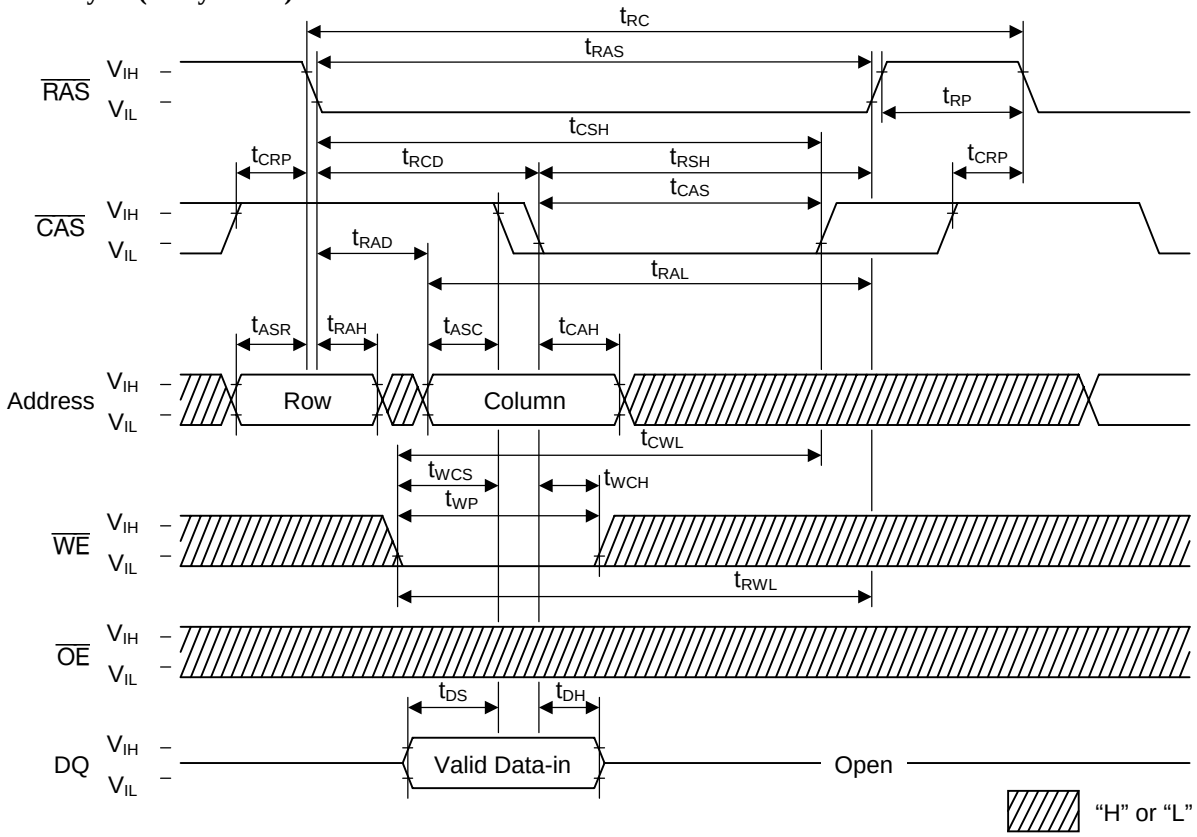
8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

TIMING CHART

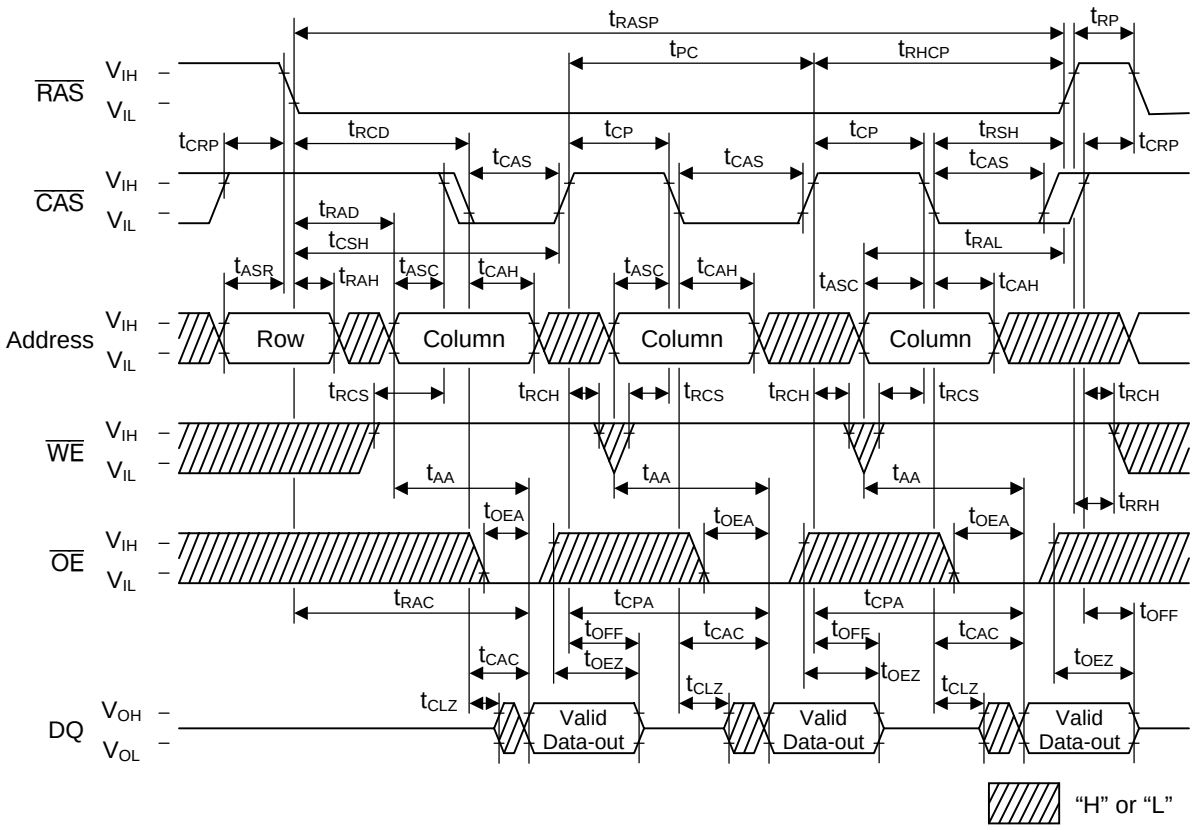
Read Cycle



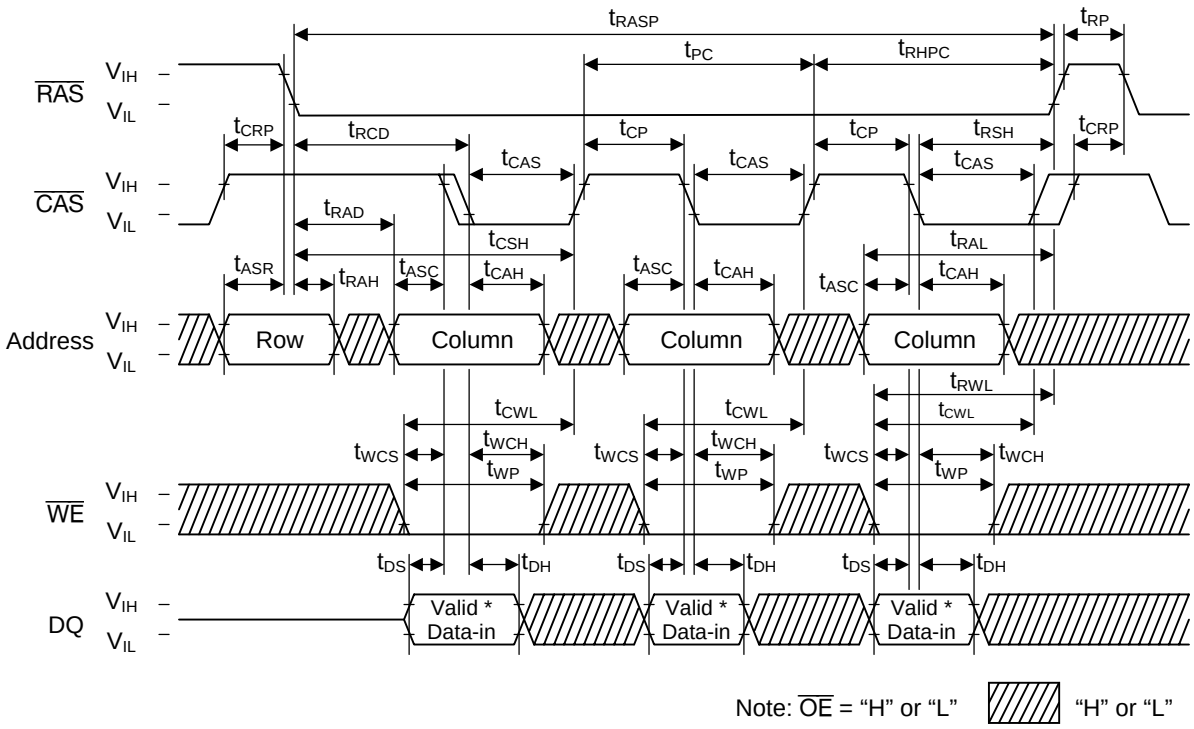
Write Cycle (Early Write)



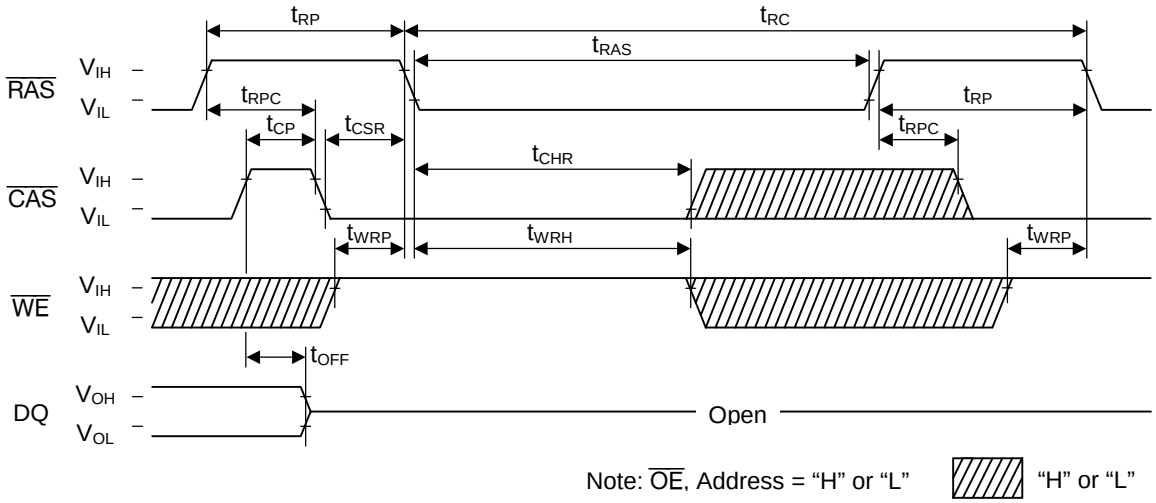
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)



CAS before RAS Refresh Cycle



REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDD51X17400F-01	Aug., 2001	–	–	Final edition 1
FEDD51X17400F-02	Feb., 2002	1, 4, 5, 6, 7	1, 4, 5, 6, 7	Changed VCCmax. from 2.4V to 2.15V
FEDD51X17400F-03	Aug, 2002	1, 2	1, 2	Deleted SOJ package

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