FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12608-2E

8-bit Proprietary Microcontrollers

CMOS

F²MC-8FX MB95140 Series

MB95F146S/F146W/FV100D-101

■ DESCRIPTION

The MB95140 series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURE

- F²MC-8FX CPU core
  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Bit test branch instruction
  - Bit manipulation instructions etc.
- Clock
  - Main clock
  - Main PLL clock
  - Sub clock (for dual clock product)
  - Sub PLL clock (for dual clock product)

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Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

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- Timer
  - 8/16-bit compound timer × 2 channels
  - 8/16-bit PPG × 2 channels
  - 16-bit PPG
  - Timebase timer
  - Watch prescaler (for dual clock product)
- LIN-UART
  - Full duplex double buffer
  - Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
- UART/SIO
  - Full duplex double buffer
  - Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable
- External interrupt
  - Interrupt by edge detection (rising, falling, or both edges can be selected)
  - Can be used to recover from low-power consumption (standby) modes.
- 8/10-bit A/D converter
  8-bit or 10-bit resolution can be selected.
- Low-power consumption (standby) mode
  - Stop mode
  - Sleep mode
  - Watch mode (for dual clock product)
  - Timebase timer mode
- I/O port
  - The number of maximum ports
    - Single clock product : 24 ports
    - Dual clock product : 22 ports
  - Port configuration
    - General-purpose I/O ports (CMOS) : Single-clock product : 24 ports
      : Dual-clock product : 22 ports
- Flash memory security function
  Protects the content of Flash memory (Flash memory device only)

■ PRODUCT LINEUP

Parameter \ Part number*1		MB95F146S	MB95F146W
Type		Flash memory product	
ROM capacity		32K bytes	
RAM capacity		1K byte	
Reset output		No	
Option	Clock system	Single clock	Dual clock
	Low voltage detection reset	No	
CPU functions		Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 61.5 ns (at machine clock frequency 16.25 MHz) Interrupt processing time : 0.6 µs (at machine clock frequency 16.25 MHz)	
Peripheral functions	General purpose I/O ports	Single clock product : 24 ports	Dual clock product : 22 ports
	Timebase timer	Interrupt cycle : 0.5 ms, 2.1 ms, 8.2 ms, 32.8 ms (at 4 MHz main oscillation clock)	
	Watchdog timer	Reset generated cycle At 10 MHz main oscillation clock : Min 105 ms At 32.768 kHz sub oscillation clock (for dual clock product) : Min 250 ms	
	Wild register	Capable of replacing 3 bytes of ROM data	
	UART/SIO	Data transfer capable in UART/SIO Full duplex double buffer, variable data length (5/6/7/8 bits), built-in baud rate generator NRZ type transfer format, error detected function LSB-first or MSB-first can be selected. Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable	
	LIN-UART	Dedicated reload timer allowing a wide range of communication speeds to be set. Full duplex double buffer. Clock asynchronous (UART) or clock synchronous (SIO) serial data transfer capable LIN functions available as the LIN master or LIN slave.	
	8/10-bit A/D converter (8 channels)	8-bit or 10-bit resolution can be selected.	

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Parameter \ Part number*1		MB95F146S	MB95F146W
Peripheral functions	8/16-bit compound timer (2 channels)	Each channel of the timer can be used as “8-bit timer × 2 channels” or “16-bit timer × 1 channel”. Built-in timer function, PWC function, PWM function, capture function and square wave form output Count clock : 7 internal clocks and external clock can be selected.	
	16-bit PPG	PWM mode or one-shot mode can be selected. Counter operating clock : 8 selectable clock sources Support for external trigger start	
	8/16-bit PPG (2 channels)	Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel”. Counter operating clock : 8 selectable clock sources	
	Watch counter (for dual clock product)	Count clock : 4 selectable clock sources (125 ms, 250 ms, 500 ms, or 1 s) Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source 1 second and setting counter value to 60)	
	Watch prescaler (for dual clock product)	4 selectable interval times (125 ms, 250 ms, 500 ms, or 1 s)	
	External interrupt (12 channels)	Interrupt by edge detection (rising, falling, or both edges can be selected.) Can be used to recover from standby modes.	
	Flash memory	Supports automatic programming, Embedded Algorithm™ *2 Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of write/erase cycles (Minimum) : 10000 times Data retention time : 20 years Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash	
Standby mode		Sleep, stop, watch (for dual clock product), and timebase timer	

*1 : MASK ROM products are currently under consideration.

*2 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

Note : Part number of the evaluation device in MB95140 series is MB95FV100D-101. When using it, the MCU board (MB2146-301A) is required.

■ OSCILLATION STABILIZATION WAIT TIME

The initial value of the main clock oscillation stabilization wait time is fixed to the maximum value.

The maximum value is shown as follows.

Oscillation stabilization wait time	Remarks
$(2^{14} - 2) / F_{CH}$	Approx. 4.10 ms (at 4 MHz main oscillation clock)

■ PACKAGES AND CORRESPONDING PRODUCTS

Part number / Package	MB95F146S MB95F146W	MB95FV100D-101
FPT-32P-M21	○	×
BGA-224P-M08	×	○

○ : Available
× : Unavailable

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

- Notes on Using Evaluation Products

  The Evaluation product has not only the functions of the MB95140 series but also those of other products to support software development for multiple series and models of the F²MC-8FX family. The I/O addresses for peripheral resources not used by the MB95140 series are therefore access-barred. Read/write access to these access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

  Particularly, do not use word access to odd numbered byte address in the prohibited areas (If these access are used, the address may be read or written unexpectedly).

  Note that the values read from barred addresses are different between the Evaluation product and the Flash memory product. Therefore, the value must not be used for program.

  The Evaluation product does not support the functions of some bits in single-byte registers. Read/write access to these bits does not cause hardware malfunctions. The Evaluation, and Flash memory products are designed to behave completely the same way in terms of hardware and software.

- Difference of Memory Spaces

  If the amount of memory on the Evaluation product is different from that of the Flash memory product, carefully check the difference in the amount of memory from the model to be actually used when developing software.

  For details of memory space, refer to “■ CPU CORE”.

- Current Consumption

  For details of current consumption, refer to “■ ELECTRICAL CHARACTERISTICS”.

- Package

  For details of information on each package, refer to “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSIONS”.

- Operating voltage

  The operating voltage is different among the Evaluation and Flash memory products.

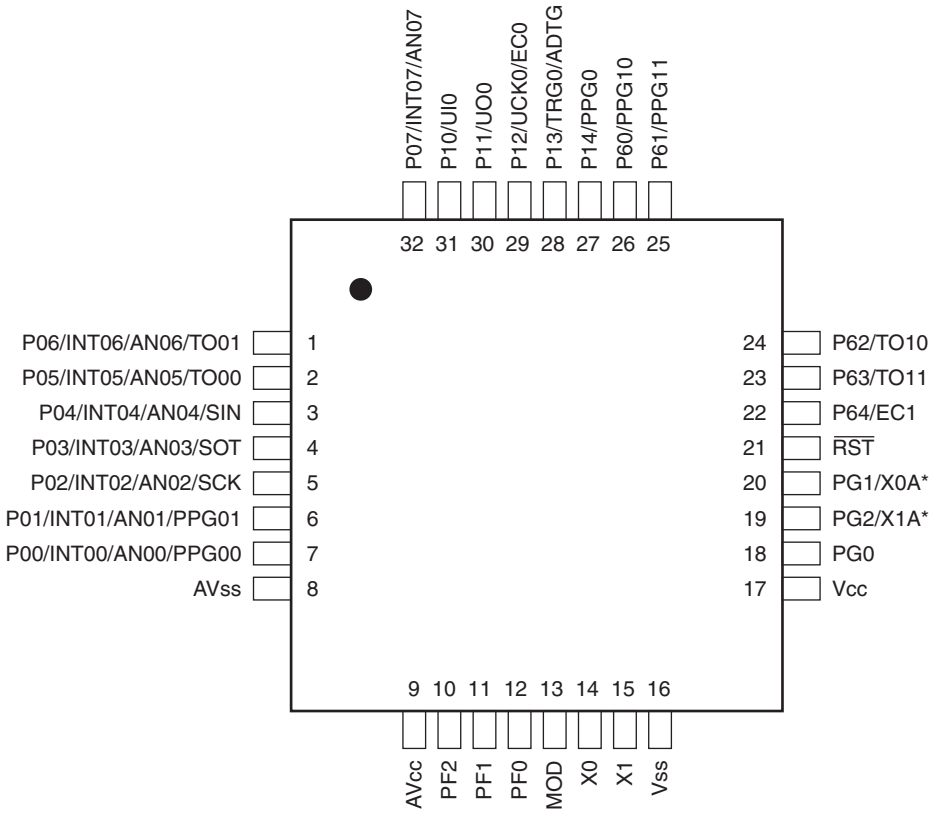
  For details of operating voltage, refer to “■ ELECTRICAL CHARACTERISTICS”

- Difference between $\overline{\text{RST}}$ and MOD pins

  The input type of $\overline{\text{RST}}$ and MOD pins is CMOS input on the Flash memory product.

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-32P-M21)

* : The pins are general-purpose port in single clock product and sub clock oscillation pin in dual clock product.

■ PIN DESCRIPTION

Pin no.	Pin name	I/O circuit type*	Function
1	P06/INT06/ AN06/TO01	D	General-purpose I/O port. Shared with external interrupt input (INT05, INT06), A/D analog input (AN05, AN06) and 8/16-bit compound timer ch.0 output (TO00, TO01).
2	P05/INT05/ AN05/TO00		
3	P04/INT04/ AN04/SIN	E	General-purpose I/O port. Shared with external interrupt input (INT04), A/D converter analog input (AN04) and LIN-UART data input (SIN).
4	P03/INT03/ AN03/SOT	D	General-purpose I/O port. Shared with external interrupt input (INT03), A/D converter analog input (AN03) and LIN-UART data output (SOT).
5	P02/INT02/ AN02/SCK	D	General-purpose I/O port. Shared with external interrupt input (INT02), A/D converter analog input (AN02) and LIN-UART clock I/O (SCK).
6	P01/INT01/ AN01/PPG01	D	General-purpose I/O port. Shared with external interrupt input (INT00, INT01), A/D converter analog input (AN00, AN01) and 8/16-bit PPG ch.0 output (PPG00, PPG01).
7	P00/INT00/ AN00/PPG00		
8	AVss	—	A/D converter power supply pin (GND)
9	AVcc	—	A/D converter power supply pin
10	PF2	K	General-purpose I/O port. Large current port.
11	PF1		
12	PF0		
13	MOD	B	Operating mode designation pin
14	X0	A	Main clock input oscillation pin
15	X1		Main clock I/O oscillation pin
16	Vss	—	Power supply pin (GND)
17	Vcc	—	Power supply pin
18	PG0	H	General-purpose I/O port
19	PG2/X1A	H/A	This pin is general-purpose port in single clock product (PG2) . This pin is sub clock oscillation pin in dual clock product (32 kHz) .
20	PG1/X0A		This pin is general-purpose port in single clock product (PG1) . This pin is sub clock oscillation pin in dual clock product (32 kHz) .
21	RST	B’	Reset pin

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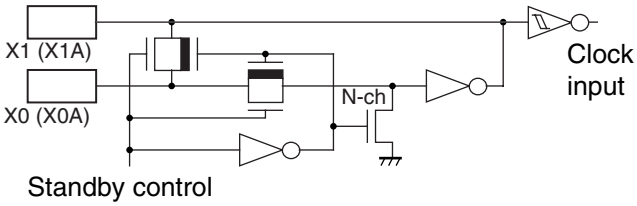
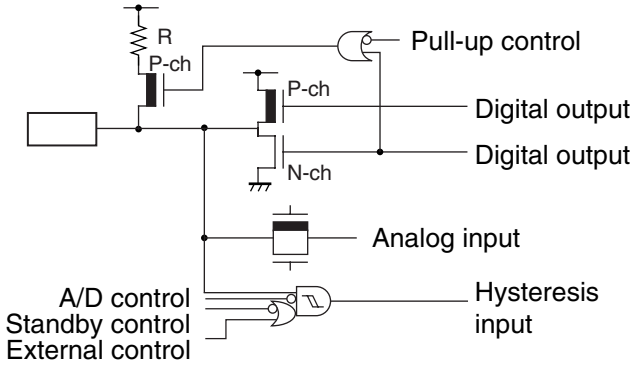
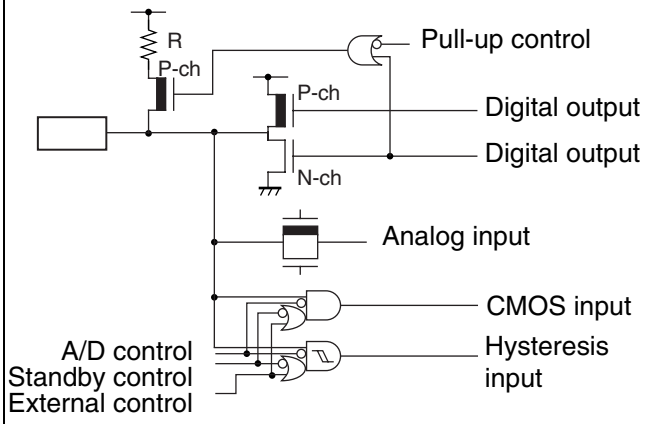
Pin no.	Pin name	I/O circuit type*	Function
22	P64/EC1	K	General-purpose I/O port. Shared with 8/16-bit compound timer ch.1 clock input.
23	P63/TO11		General-purpose I/O port. Shared with 8/16-bit compound timer ch.1 output.
24	P62/TO10		
25	P61/PPG11		General-purpose I/O port. Shared with 8/16-bit PPG ch.1 output.
26	P60/PPG10	K	General-purpose I/O port. Shared with 8/16-bit PPG ch.1 output.
27	P14/PPG0	H	General-purpose I/O port. Shared with 16-bit PPG ch.0 output.
28	P13/TRG0/ ADTG	H	General-purpose I/O port. Shared with 16-bit PPG ch.0 trigger input (TRG0) and A/D trigger input (ADTG).
29	P12/UCK0/EC0	H	General-purpose I/O port. Shared with UART/SIO ch.0 clock I/O (UCK0) and 8/16-bit compound timer ch.0 clock input (EC0).
30	P11/UO0	H	General-purpose I/O port. Shared with UART/SIO ch.0 data output.
31	P10/UI0	G	General-purpose I/O port. Shared with UART/SIO ch.0 data input.
32	P07/INT07/ AN07	D	General-purpose I/O port. Shared with external interrupt input (INT07) and A/D converter analog input (AN07).

* : For the I/O circuit type, refer to “■ I/O CIRCUIT TYPE”.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation circuit • High-speed side Feedback resistance : approx. 1 MΩ • Low-speed side Feedback resistance : approx. 24 MΩ (Evaluation product : approx. 10 MΩ) Dumping resistance : approx. 144 kΩ (Evaluation product : without dumping resistance)
B		• Only for input • Hysteresis input
B’		Hysteresis input
D		• CMOS output • Hysteresis input • Analog input • With pull - up control
E		• CMOS output • CMOS input • Hysteresis input • Analog input • With pull - up control

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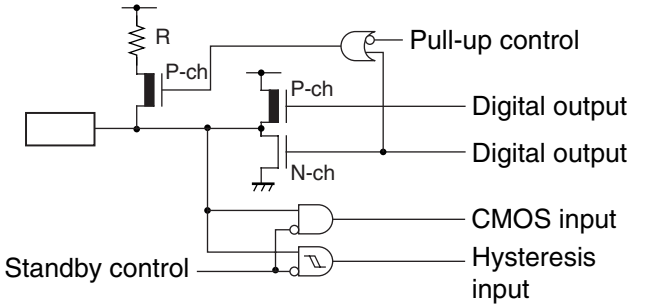
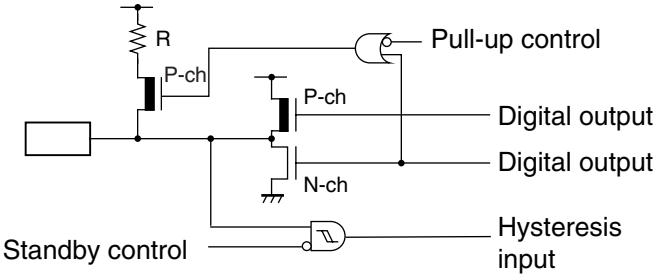
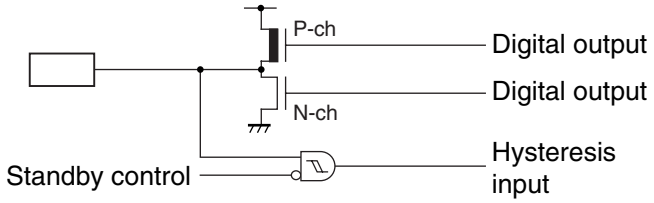
Type	Circuit	Remarks
G		• CMOS output • CMOS input • Hysteresis input • With pull - up control
H		• CMOS output • Hysteresis input • With pull - up control
K		• CMOS output • Hysteresis input

■ HANDLING DEVICES

• Preventing Latch-up

Care must be taken to ensure that maximum voltage ratings are not exceeded when they are used.

Latch-up may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between V_{CC} pin and V_{SS} pin.

When latch-up occurs, power supply current increases rapidly and might thermally damage elements.

Also, take care to prevent the analog power supply voltage (AV_{CC}) and analog input voltage from exceeding the digital power supply voltage (V_{CC}) when the analog system power supply is turned on or off.

• Stable Supply Voltage

Supply voltage should be stabilized.

A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the V_{CC} power-supply voltage.

For stabilization, in principle, keep the variation in V_{CC} ripple (p-p value) in a commercial frequency range (50/60 Hz) not to exceed 10% of the standard V_{CC} value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

• Precautions for Use of External Clock

Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub clock mode or stop mode.

■ PIN CONNECTION

• Treatment of Unused Pin

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leaving to permanent damage.

Unused input pins should always be pulled up or down through resistance of at least 2 kΩ. Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it to open.

• Treatment of Power Supply Pins on A/D Converter

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$ even if the A/D converter is not in use.

Noise riding on the AV_{CC} pin may cause accuracy degradation. So, connect approx. 0.1 μF ceramic capacitor as a bypass capacitor between AV_{CC} and AV_{SS} pins in the vicinity of this device.

• Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 μF between V_{CC} and V_{SS} pins near this device.

- Mode Pin (MOD)

  Connect the MOD pin directly to V_{CC} or V_{SS} pins.

  To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the MOD pin to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

- Analog Power Supply

  Always set the same potential to AV_{CC} and V_{CC} pins. When $V_{CC} > AV_{CC}$, the current may flow through the AN00 to AN07 pins.

■ PROGRAMMING FLASH MEMORY MICROCONTROLLERS USING PARALLEL PROGRAMMER

• Supported Parallel Programmers and Adapters

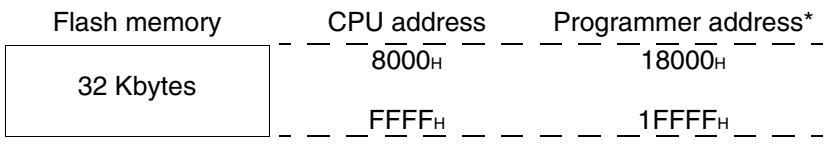
The following table lists supported parallel programmers and adapters.

Package	Applicable adapter model	Parallel programmers
FPT-32P-M21	TEF110-95F146	AF9708 (Ver 02.35G or more) AF9709/B (Ver 02.35G or more)

Note : For information on applicable adapter models and parallel programmers, contact the following:
Flash Support Group, Inc. TEL: +81-53-428-8380

• Sector Configuration

The individual sectors of Flash memory correspond to addresses used for CPU access and programming by the parallel programmer as follows:



*: Programmer addresses are corresponding to CPU addresses, used when the parallel programmer programs data into Flash memory.
These programmer addresses are used for the parallel programmer to program or erase data in Flash memory.

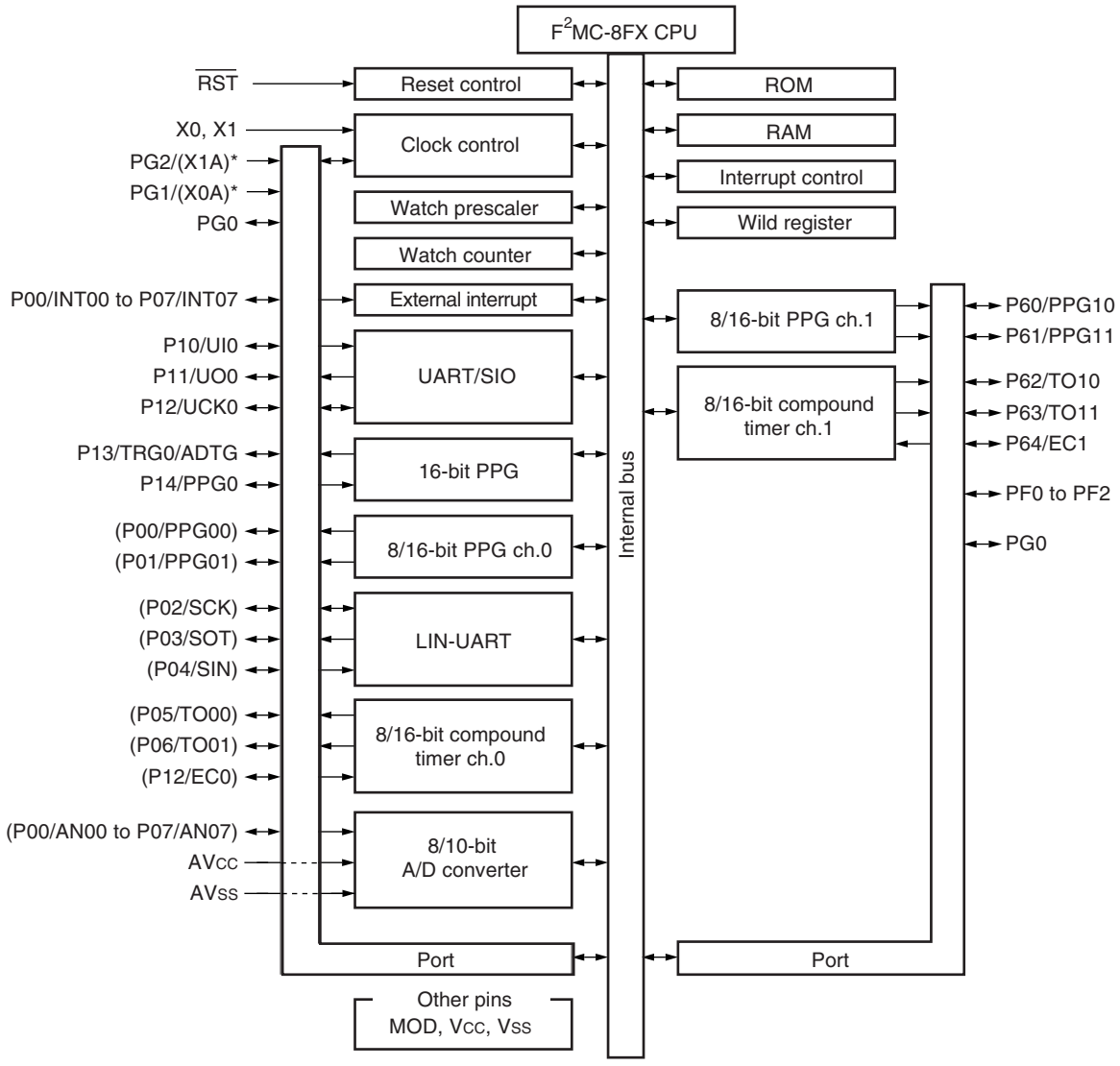
• Programming Method

1) Set the type code of the parallel programmer to “1723E”.

2) Load program data to programmer addresses 18000_H to $1FFFF_H$.

3) Programmed by parallel programmer

■ BLOCK DIAGRAM



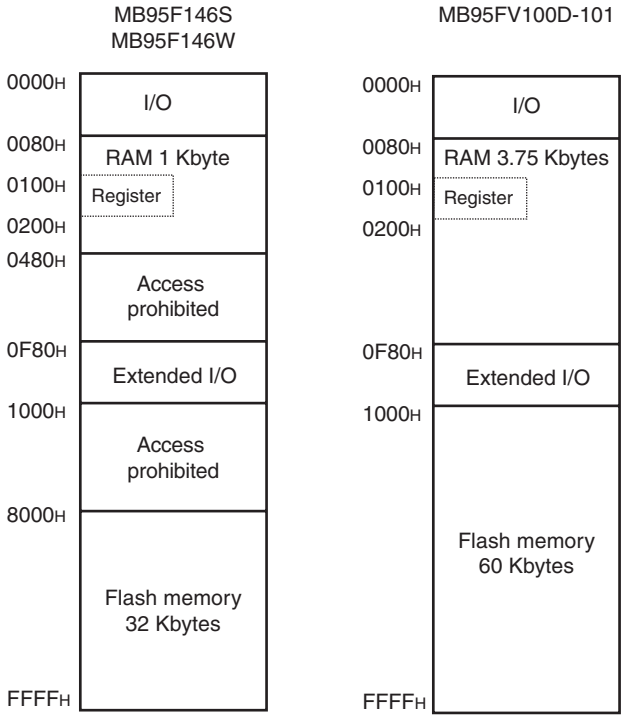
* : The pins are general-purpose port in single clock product and sub clock oscillation pin in dual clock product.

■ CPU CORE

1. Memory space

Memory space of the MB95140 series is 64K bytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose 7 registers and vector table. Memory map of the MB95140 series is shown below.

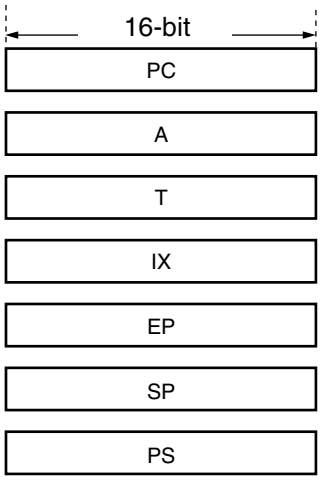
- Memory Map



2. Register

The MB95140 series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The dedicated registers are as follows:

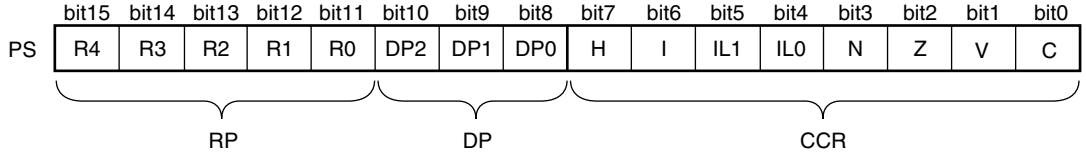
Program counter (PC)	:	A 16-bit register to indicate locations where instructions are stored.
Accumulator (A)	:	A 16-bit register for temporary storage of arithmetic operations. In the case of an 8-bit data processing instruction, the lower 1 byte is used.
Temporary accumulator (T)	:	A 16-bit register which performs arithmetic operations with the accumulator. In the case of an 8-bit data processing instruction, the lower 1 byte is used.
Index register (IX)	:	A 16-bit register for index modification
Extra pointer (EP)	:	A 16-bit pointer to point to a memory address.
Stack pointer (SP)	:	A 16-bit register to indicate a stack area.
Program status (PS)	:	A 16-bit register for storing a register bank pointer, a direct bank pointer, and a condition code register



	Initial Value
: Program counter	$FFFD_H$
: Accumulator	0000_H
: Temporary accumulator	0000_H
: Index register	0000_H
: Extra pointer	0000_H
: Stack pointer	0000_H
: Program status	0030_H

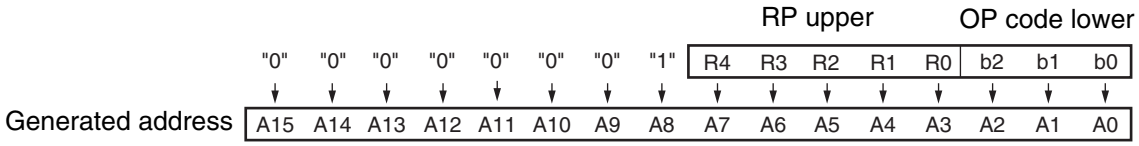
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and a direct bank pointer (DP) and the lower 8 bits for use as a condition code register (CCR) . (Refer to the diagram below.)

• Structure of the Program Status



The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:

- Rule for Conversion of Actual Addresses in the General-purpose Register Area



The DP specifies the area for mapping instructions (16 different instructions such as MOV A, dir) using direct addresses to 0080_H to $00FF_H$.

Direct bank pointer (DP2 to DP0)	Specified address area	Mapping area
XXX_B (no effect to mapping)	0000_H to $007F_H$	0000_H to $007F_H$ (without mapping)
000_B (initial value)	0080_H to $00FF_H$	0080_H to $00FF_H$ (without mapping)
001_B		0100_H to $017F_H$
010_B		0180_H to $01FF_H$
011_B		0200_H to $027F_H$
100_B		0280_H to $02FF_H$
101_B		0300_H to $037F_H$
110_B		0380_H to $03FF_H$
111_B		0400_H to $047F_H$

The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at interrupt.

H flag : Set to “1” when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. This flag is for decimal adjustment instructions.

I flag : Interrupt is enabled when this flag is set to “1”. Interrupt is disabled when this flag is set to “0”. The flag is cleared to “0” when reset.

IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by these bits.

IL1	IL0	Interrupt level	Priority
0	0	0	High
0	1	1	↕
1	0	2	
1	1	3	Low = no interruption

N flag : Set to “1” if the MSB is set to “1” as the result of an arithmetic operation. Cleared to “0” when the bit is set to “0”.

Z flag : Set to “1” when an arithmetic operation results in “0”. Cleared to “0” otherwise.

V flag : Set to “1” if the complement on 2 overflows as a result of an arithmetic operation. Cleared to “0” otherwise.

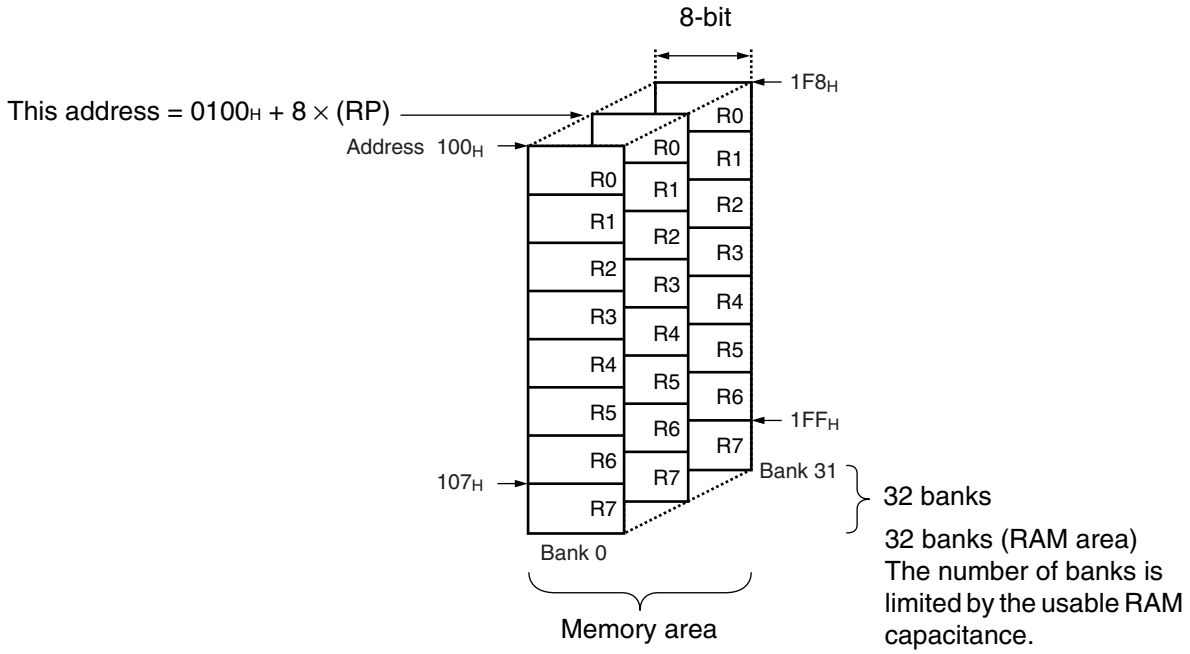
C flag : Set to “1” when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. 1-bank contains 8-register. Up to a total of 32 banks can be used on the MB95140 series. The bank currently in use is specified by the register bank pointer (RP), and the lower 3 bits of OP code indicates the general-purpose register 0 (R0) to general-purpose register 7 (R7).

- Register Bank Configuration



■ I/O MAP

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	PLLC	PLL control register	R/W	00000000_B
0007_H	SYCC	System clock control register	R/W	$1010X011_B$
0008_H	STBC	Standby control register	R/W	00000000_B
0009_H	RSRR	Reset source register	R	$XXXXXXXX_B$
$000A_H$	TBTC	Timebase timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	00000000_B
$000D_H$ to 0015_H	—	(Disabled)	—	—
0016_H	PDR6	Port 6 data register	R/W	00000000_B
0017_H	DDR6	Port 6 direction register	R/W	00000000_B
0018_H to 0027_H	—	(Disabled)	—	—
0028_H	PDRF	Port F data register	R/W	00000000_B
0029_H	DDRF	Port F direction register	R/W	00000000_B
$002A_H$	PDRG	Port G data register	R/W	00000000_B
$002B_H$	DDRG	Port G direction register	R/W	00000000_B
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$	PUL1	Port 1 pull-up register	R/W	00000000_B
$002E_H$ to 0034_H	—	(Disabled)	—	—
0035_H	PULG	Port G pull-up register	R/W	00000000_B
0036_H	T01CR1	8/16-bit compound timer 01 control status register 1 ch.0	R/W	00000000_B
0037_H	T00CR1	8/16-bit compound timer 00 control status register 1 ch.0	R/W	00000000_B
0038_H	T11CR1	8/16-bit compound timer 11 control status register 1 ch.1	R/W	00000000_B
0039_H	T10CR1	8/16-bit compound timer 10 control status register 1 ch.1	R/W	00000000_B
$003A_H$	PC01	8/16-bit PPG1 control register ch.0	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
003B$_H$	PC00	8/16-bit PPG0 control register ch.0	R/W	00000000$_B$
003C$_H$	PC11	8/16-bit PPG1 control register ch.1	R/W	00000000$_B$
003D$_H$	PC10	8/16-bit PPG0 control register ch.1	R/W	00000000$_B$
003E$_H$ to 0041$_H$	—	(Disabled)	—	—
0042$_H$	PCNTH0	16-bit PPG control status register (Upper byte) ch.0	R/W	00000000$_B$
0043$_H$	PCNTL0	16-bit PPG control status register (Lower byte) ch.0	R/W	00000000$_B$
0044$_H$ to 0047$_H$	—	(Disabled)	—	—
0048$_H$	EIC00	External interrupt circuit control register ch.0/ch.1	R/W	00000000$_B$
0049$_H$	EIC10	External interrupt circuit control register ch.2/ch.3	R/W	00000000$_B$
004A$_H$	EIC20	External interrupt circuit control register ch.4/ch.5	R/W	00000000$_B$
004B$_H$	EIC30	External interrupt circuit control register ch.6/ch.7	R/W	00000000$_B$
004C$_H$ to 004F$_H$	—	(Disabled)	—	—
0050$_H$	SCR	LIN-UART serial control register	R/W	00000000$_B$
0051$_H$	SMR	LIN-UART serial mode register	R/W	00000000$_B$
0052$_H$	SSR	LIN-UART serial status register	R/W	00001000$_B$
0053$_H$	RDR/TDR	LIN-UART reception/transmission data register	R/W	00000000$_B$
0054$_H$	ESCR	LIN-UART extended status control register	R/W	00000100$_B$
0055$_H$	ECCR	LIN-UART extended communication control register	R/W	000000XX$_B$
0056$_H$	SMC10	UART/SIO serial mode control register 1 ch.0	R/W	00000000$_B$
0057$_H$	SMC20	UART/SIO serial mode control register 2 ch.0	R/W	00100000$_B$
0058$_H$	SSR0	UART/SIO serial status register ch.0	R/W	00000001$_B$
0059$_H$	TDR0	UART/SIO serial output data register ch.0	R/W	00000000$_B$
005A$_H$	RDR0	UART/SIO serial input data register ch.0	R	00000000$_B$
005B$_H$ to 006B$_H$	—	(Disabled)	—	—
006C$_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000$_B$
006D$_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000$_B$
006E$_H$	ADDH	8/10-bit A/D converter data register (Upper byte)	R/W	00000000$_B$
006F$_H$	ADDL	8/10-bit A/D converter data register (Lower byte)	R/W	00000000$_B$

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0070H	WCSR	Watch counter status register	R/W	00000000B
0071H	—	(Disabled)	—	—
0072H	FSR	Flash memory status register	R/W	000X0000B
0073H	SWRE0	Flash memory sector writing control register 0	R/W	00000000B
0074H	SWRE1	Flash memory sector writing control register 1	R/W	00000000B
0075H	—	(Disabled)	—	—
0076H	WREN	Wild register address compare enable register	R/W	00000000B
0077H	WROR	Wild register data test setting register	R/W	00000000B
0078H	—	(Mirror of register bank pointer (RP) and direct bank pointer (DP))	—	—
0079H	ILR0	Interrupt level setting register 0	R/W	11111111B
007AH	ILR1	Interrupt level setting register 1	R/W	11111111B
007BH	ILR2	Interrupt level setting register 2	R/W	11111111B
007CH	ILR3	Interrupt level setting register 3	R/W	11111111B
007DH	ILR4	Interrupt level setting register 4	R/W	11111111B
007EH	ILR5	Interrupt level setting register 5	R/W	11111111B
007FH	—	(Disabled)	—	—
0F80H	WRARH0	Wild register address setting register (Upper byte) ch.0	R/W	00000000B
0F81H	WRARL0	Wild register address setting register (Lower byte) ch.0	R/W	00000000B
0F82H	WRDR0	Wild register data setting register ch.0	R/W	00000000B
0F83H	WRARH1	Wild register address setting register (Upper byte) ch.1	R/W	00000000B
0F84H	WRARL1	Wild register address setting register (Lower byte) ch.1	R/W	00000000B
0F85H	WRDR1	Wild register data setting register ch.1	R/W	00000000B
0F86H	WRARH2	Wild register address setting register (Upper byte) ch.2	R/W	00000000B
0F87H	WRARL2	Wild register address setting register (Lower byte) ch.2	R/W	00000000B
0F88H	WRDR2	Wild register data setting register ch.2	R/W	00000000B
0F89H to 0F91H	—	(Disabled)	—	—
0F92H	T01CR0	8/16-bit compound timer 01 control status register 0 ch.0	R/W	00000000B
0F93H	T00CR0	8/16-bit compound timer 00 control status register 0 ch.0	R/W	00000000B
0F94H	T01DR	8/16-bit compound timer 01 data register ch.0	R/W	00000000B
0F95H	T00DR	8/16-bit compound timer 00 data register ch.0	R/W	00000000B
0F96H	TMCR0	8/16-bit compound timer 00/01 timer mode control register ch.0	R/W	00000000B
0F97H	T11CR0	8/16-bit compound timer 11 control status register 0 ch.1	R/W	00000000B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0F98H	T10CR0	8/16-bit compound timer 10 control status register 0 ch.1	R/W	00000000B
0F99H	T11DR	8/16-bit compound timer 11 data register ch.1	R/W	00000000B
0F9AH	T10DR	8/16-bit compound timer 10 data register ch.1	R/W	00000000B
0F9BH	TMCR1	8/16-bit compound timer 10/11 timer mode control register ch.1	R/W	00000000B
0F9CH	PPS01	8/16-bit PPG1 cycle setting buffer register ch.0	R/W	11111111B
0F9DH	PPS00	8/16-bit PPG0 cycle setting buffer register ch.0	R/W	11111111B
0F9EH	PDS01	8/16-bit PPG1 duty setting buffer register ch.0	R/W	11111111B
0F9FH	PDS00	8/16-bit PPG0 duty setting buffer register ch.0	R/W	11111111B
0FA0H	PPS11	8/16-bit PPG1 cycle setting buffer register ch.1	R/W	11111111B
0FA1H	PPS10	8/16-bit PPG0 cycle setting buffer register ch.1	R/W	11111111B
0FA2H	PDS11	8/16-bit PPG1 duty setting buffer register ch.1	R/W	11111111B
0FA3H	PDS10	8/16-bit PPG0 duty setting buffer register ch.1	R/W	11111111B
0FA4H	PPGS	8/16-bit PPG start register	R/W	00000000B
0FA5H	REVC	8/16-bit PPG output inversion register	R/W	00000000B
0FA6H to 0FA9H	—	(Disabled)	—	—
0FAAH	PDCRH0	16-bit PPG down counter register (Upper byte) ch.0	R	00000000B
0FABH	PDCRL0	16-bit PPG down counter register (Lower byte) ch.0	R	00000000B
0FACH	PCSRH0	16-bit PPG cycle setting buffer register (Upper byte) ch.0	R/W	11111111B
0FADH	PCSRL0	16-bit PPG cycle setting buffer register (Lower byte) ch.0	R/W	11111111B
0FAEH	PDUTH0	16-bit PPG duty setting buffer register (Upper byte) ch.0	R/W	11111111B
0FAFH	PDUTL0	16-bit PPG duty setting buffer register (Lower byte) ch.0	R/W	11111111B
0FB0H to 0FBBH	—	(Disabled)	—	—
0FBCH	BGR1	LIN-UART baud rate generator register 1	R/W	00000000B
0FBDH	BGR0	LIN-UART baud rate generator register 0	R/W	00000000B
0FBEH	PSSR0	UART/SIO dedicated baud rate generator prescaler selection register ch.0	R/W	00000000B
0FBFH	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch.0	R/W	00000000B
0FC0H to 0FC2H	—	(Disabled)	—	—
0FC3H	AIDRL	A/D input disable register (Lower byte)	R/W	00000000B
0FC4H to 0FE2H	—	(Disabled)	—	—

(Continued)

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Address	Register abbreviation	Register name	R/W	Initial value
0FE3H	WCDR	Watch counter data register	R/W	00111111B
0FE4H to 0FEDH	—	(Disabled)	—	—
0FEEH	ILSR	Input level select register	R/W	00000000B
0FEFH	WICR	Interrupt pin control register	R/W	01000000B
0FF0H to 0FFFH	—	(Disabled)	—	—

• R/W access symbols
  R/W : Readable/Writable
  R : Read only
  W : Write only

• Initial value symbols
  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is undefined.

Note : Do not write to the “ (Disabled) ”. Reading the “ (Disabled) ” returns an undefined value.

■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Same level priority order (at simultaneous occurrence)
		Upper	Lower		
External interrupt ch.0	IRQ0	FFFA$_H$	FFFB$_H$	L00 [1 : 0]	High
External interrupt ch.4					
External interrupt ch.1	IRQ1	FFF8$_H$	FFF9$_H$	L01 [1 : 0]	
External interrupt ch.5					
External interrupt ch.2	IRQ2	FFF6$_H$	FFF7$_H$	L02 [1 : 0]	
External interrupt ch.6					
External interrupt ch.3	IRQ3	FFF4$_H$	FFF5$_H$	L03 [1 : 0]	
External interrupt ch.7					
UART/SIO ch.0	IRQ4	FFF2$_H$	FFF3$_H$	L04 [1 : 0]	
8/16-bit compound timer ch.0 (Lower)	IRQ5	FFF0$_H$	FFF1$_H$	L05 [1 : 0]	
8/16-bit compound timer ch.0 (Upper)	IRQ6	FFEE$_H$	FFEF$_H$	L06 [1 : 0]	
LIN-UART (reception)	IRQ7	FFEC$_H$	FFED$_H$	L07 [1 : 0]	
LIN-UART (transmission)	IRQ8	FFEA$_H$	FFEB$_H$	L08 [1 : 0]	
8/16-bit PPG ch.1 (Lower)	IRQ9	FFE8$_H$	FFE9$_H$	L09 [1 : 0]	
8/16-bit PPG ch.1 (Upper)	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1 : 0]	
(Unused)	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1 : 0]	
8/16-bit PPG ch.0 (Upper)	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1 : 0]	
8/16-bit PPG ch.0 (Lower)	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1 : 0]	
8/16-bit compound timer ch.1 (Upper)	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1 : 0]	
16-bit PPG ch.0	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1 : 0]	
(Unused)	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1 : 0]	
(Unused)	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1 : 0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1 : 0]	
Timebase timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1 : 0]	
Watch timer/Watch counter	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1 : 0]	
(Unused)	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1 : 0]	
8/16-bit compound timer ch.1 (Lower)	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1 : 0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1 : 0]	Low

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC} AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 4.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*3
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	Applicable to pins*4
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to pins*4
"L" level maximum output current	I_{OL1}	—	15	mA	Other than PF0 to PF2
	I_{OL2}		15		PF0 to PF2
"L" level average current	I_{OLAV1}	—	4	mA	Other than PF0 to PF2 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		PF0 to PF2 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total of pins)
"H" level maximum output current	I_{OH1}	—	– 15	mA	Other than PF0 to PF2
	I_{OH2}		– 15		PF0 to PF2
"H" level average current	I_{OHAV1}	—	– 4	mA	Other than PF0 to PF2 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		– 8		PF0 to PF2 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	– 100	mA	
"H" level total average output current	ΣI_{OHAV}	—	– 50	mA	Total average output current = operating current × operating ratio (Total of pins)

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Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	− 40	+ 85	°C	
Storage temperature	Tstg	− 55	+ 150	°C	

*1 : The parameter is based on $AV_{SS} = V_{SS} = 0.0$ V.

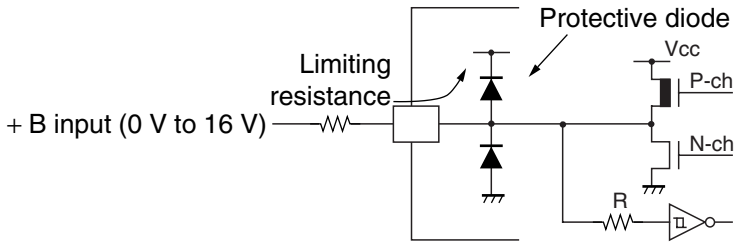
*2 : Apply equal potential to AV_{CC} and V_{CC}.

*3 : V_I and Vo should not exceed V_{CC} + 0.3 V. V_I must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4 : Applicable to pins : P00 to P07, P10 to P14, P60 to P64, PF0 to PF2, PG0

- Use within recommended operating conditions.
- Use at DC voltage (current).
- The + B signal is an input signal that exceeds V_{CC} voltage. The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this affects other devices.
- Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the + B input pin open.
- Sample recommended circuits :

- Input/Output Equivalent Circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply voltage	V_{CC}, AV_{CC}	—	—	2.3*	3.3	V	At normal operating, T_A = –10 °C to +85 °C
		—	—	2.4*	3.3		At normal operating, T_A = –40 °C to +85 °C
		—	—	2.6	3.6		MB95FV100D-101 T_A = +5 to +35
		—	—	1.5	3.3		Retain status in stop mode
Operating temperature	T_A	—	—	– 40	+ 85	°C	

* : The values vary with the operating frequency.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = AV_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	P04, P10	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	At selecting CMOS input level
	V_{IHS}	P00 to P07, P10 to P14, P60 to P64, PF0 to PF2, PG0, PG1*2, PG2*2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	$\overline{RST}$, MOD	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P04, P10	*1	V_{SS} − 0.3	—	0.3 V_{CC}	V	At selecting CMOS input level (Hysteresis input)
	V_{ILS}	P00 to P07, P10 to P14, P60 to P64, PF0 to PF2, PG0, PG1*2, PG2*2	*1	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	$\overline{RST}$, MOD	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
"H" level output voltage	V_{OH1}	Output pin other than PF0 to PF2	I_{OH} = − 4.0 mA	2.4	—	—	V	
	V_{OH2}	PF0 to PF2	I_{OH} = − 8.0 mA	2.4	—	—	V	
"L" level output voltage	V_{OL1}	Output pin other than PF0 to PF2	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	PF0 to PF2	I_{OL} = 12 mA	—	—	0.4	V	
Input leakage current (Hi-Z output leakage current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	− 5	—	+ 5	µA	When the pull-up is prohibition setting
Pull-up resistor	R_{PULL}	P00 to P07, P10 to P14, PG0, PG1*2, PG2*2	V_I = 0.0 V	25	50	100	kΩ	When the pull-up is permission setting
Power supply current*3	I_{CC}	V_{CC} (External clock operation)	F_{CH} = 20 MHz F_{MP} = 10 MHz Main clock mode (divided by 2)	—	11.0	14.0	mA	At other than Flash memory writing and erasing
				—	30.0	35.0	mA	At Flash memory writing and erasing
			F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	17.6	22.4	mA	At other than Flash memory writing and erasing
				—	38.1	44.9	mA	At Flash memory writing and erasing

(Continued)

(V_{CC} = AV_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*3	I_{CCS}	V_{CC} (External clock operation)	F_{CH} = 20 MHz F_{MP} = 10 MHz Main Sleep mode (divided by 2)	—	4.5	6.0	mA	
			F_{CH} = 32 MHz F_{MP} = 16 MHz Main Sleep mode (divided by 2)	—	7.2	9.6	mA	
	I_{CCL}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Sub clock mode (divided by 2) , T_A = + 25 °C	—	25	35	µA	
	I_{CCLS}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Sub sleep mode (divided by 2) , T_A = + 25 °C	—	7	15	µA	
	I_{CCT}		F_{CL} = 32 kHz Watch mode Main stop mode T_A = + 25 °C	—	2	10	µA	
	I_{CCMPLL}		F_{CH} = 4 MHz F_{MP} = 10 MHz Main PLL mode (multiplied by 2.5)	—	10	14	mA	
			F_{CH} = 6.4 MHz F_{MP} = 16 MHz Main PLL mode (multiplied by 2.5)	—	16.0	22.4	mA	
	I_{CCSPLL}		F_{CL} = 32 kHz F_{MPL} = 128 kHz Sub PLL mode (multiplied by 4) , T_A = + 25 °C	—	190	250	µA	
	I_{CTS}		F_{CH} = 10 MHz Timebase timer mode T_A = + 25 °C	—	0.64	0.80	mA	
	I_{CCH}		Sub stop mode T_A = + 25 °C	—	1	5	µA	

(Continued)

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(V_{CC} = AV_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*3	I_A	AV_{CC}	F_{CH} = 10 MHz At operating of A/D conversion	—	1.3	2.2	mA	
	I_{AH}		F_{CH} = 10 MHz At stopping of A/D conversion T_A = + 25 °C	—	1	5	μA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, V_{SS}	f = 1 MHz	—	5	15	pF	

*1 : P04, P10 can switch the input level to either the “CMOS input level” or “hysteresis input level”. The switching of the input level can be set by the input level selection register (ILSR).

*2 : Single clock product only

*3 : Power supply current is regulated by external clock.

- Refer to “4. AC Characteristics (1) Clock Timing” for F_{CH} and F_{CL}.
- Refer to “4. AC Characteristics (2) Source Clock/Machine Clock” for F_{MP} and F_{MPL}.

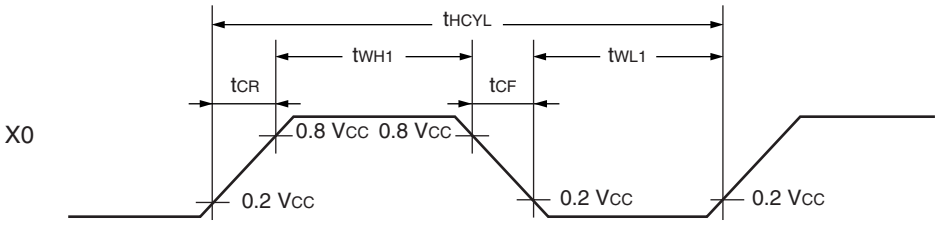
4. AC Characteristics

(1) Clock Timing

(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

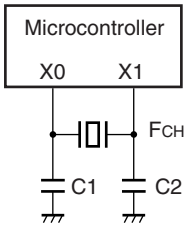
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1.00	—	16.25	MHz	When using main oscillation circuit
				1.00	—	32.50	MHz	When using external clock
				3.00	—	10.00	MHz	Main PLL multiplied by 1
				3.00	—	8.13	MHz	Main PLL multiplied by 2
				3.00	—	6.50	MHz	Main PLL multiplied by 2.5
				3.00	—	4.06	MHz	Main PLL multiplied by 4
	F_{CL}	X0A, X1A		—	32.768	—	kHz	When using sub oscillation circuit
				—	32.768	—	kHz	When using sub PLL Flash memory product : V_{CC} = 2.3 V to 3.3 V
Clock cycle time	t_{HCYL}	X0, X1		100	—	1000	ns	When using main oscillation circuit
				50	—	1000	ns	When using external clock
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	When using sub oscillation circuit, When using external clock
Input clock pulse width	t_{WH1} t_{WL1}	X0		10	—	—	ns	When using external clock Duty ratio is about 30% to 70%.
	t_{WH2} t_{WL2}	X0A		—	15.2	—	µs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0, X0A		—	—	10	ns	When using external clock

• Input wave form for using external clock (main clock)

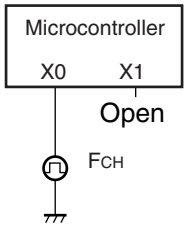


• Figure of main clock input port external connection

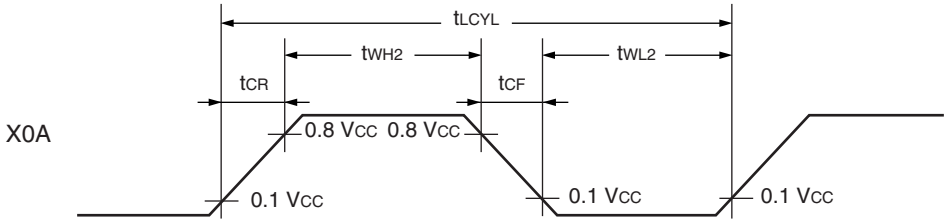
When using a crystal or ceramic oscillator



When using external clock

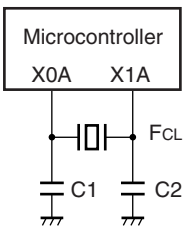


• Input wave form for using external clock (sub clock)

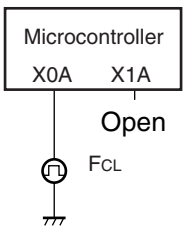


• Figure of sub clock input port external connection

When using a crystal or ceramic oscillator



When using external clock



(2) Source Clock/Machine Clock

(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1 (Clock before setting division)	t_{SCLK}	—	61.5	—	2000	ns	When using main clock Min : F_{CH} = 8.125 MHz, PLL multiplied by 2 Max : F_{CH} = 1 MHz, divided by 2
			7.6	—	61.0	µs	When using sub clock Min : F_{CL} = 32 kHz, PLL multiplied by 4 Max : F_{CL} = 32 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	16.25	MHz	When using main clock
	F_{SPL}	—	16.384	—	131.072	kHz	When using sub clock
Machine clock cycle time*2 (Minimum instruction execution time)	t_{MCLK}	—	100	—	32000	ns	When using main clock Min : F_{SP} = 16.25 MHz, no division Max : F_{SP} = 0.5 MHz, divided by 16
			7.6	—	976.5	µs	When using sub clock Min : F_{SPL} = 131 kHz, no division Max : F_{SPL} = 16 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.250	MHz	When using main clock
	F_{MPL}		1.024	—	131.072	kHz	When using sub clock

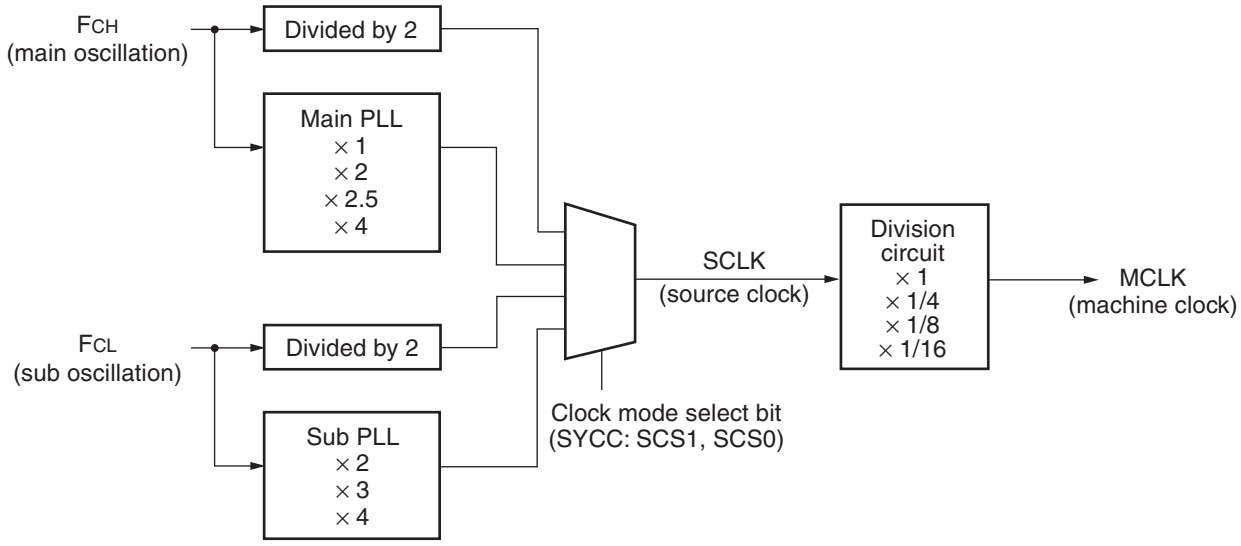
*1 : Clock before setting division due to machine clock division ratio selection bits (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bits (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follows.

- Main clock divided by 2
- PLL multiplication of main clock (select from 1, 2, 2.5, 4 multiplication)
- Sub clock divided by 2
- PLL multiplication of sub clock (select from 2, 3, 4 multiplication)

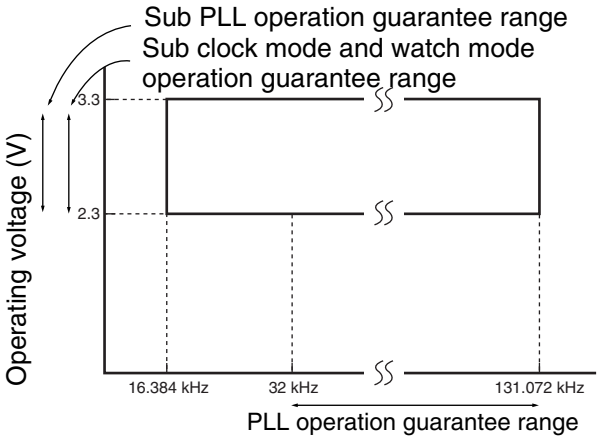
*2 : Operation clock of the microcontroller. Machine clock can be selected as follows.

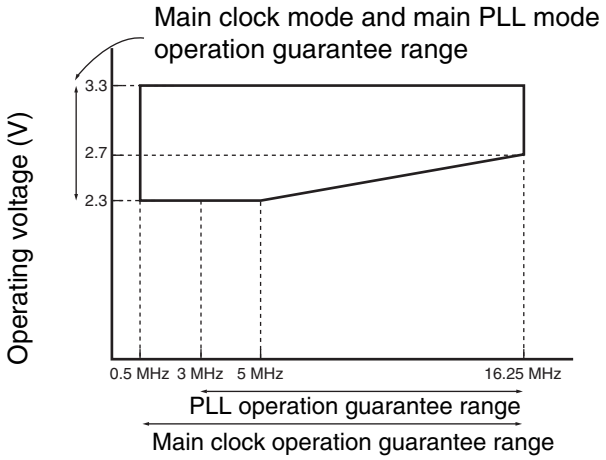
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

• Outline of Clock Generation Block

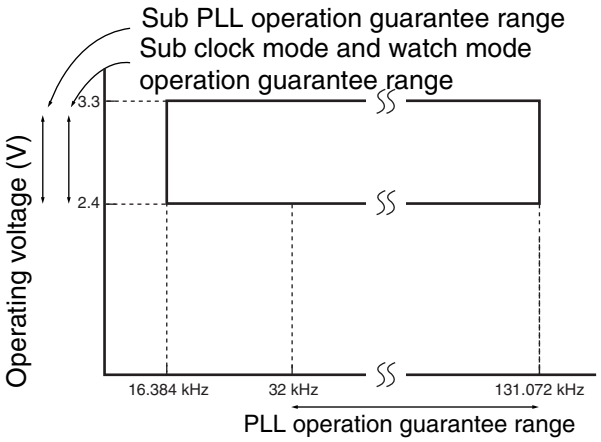


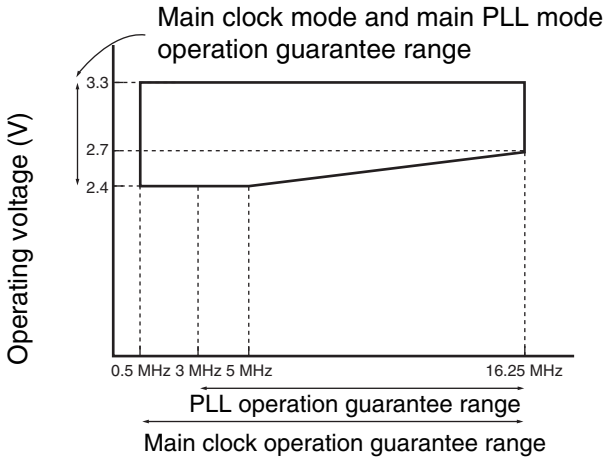
- Operating Voltage - Operating Frequency (When T_A = − 10 °C to + 85 °C)
  - MB95F146S, MB95F146W



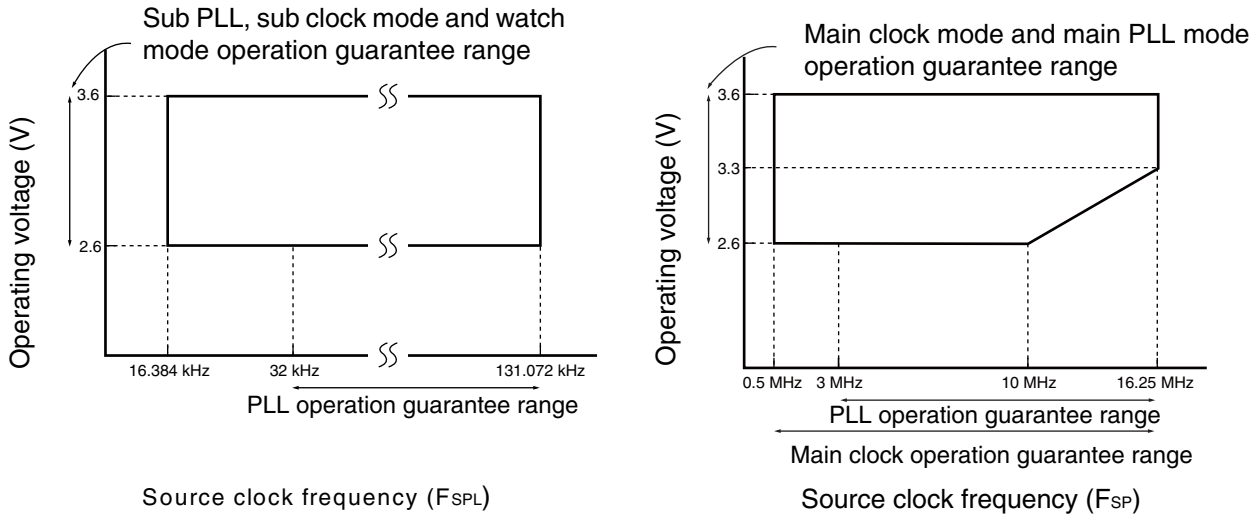


- Operating Voltage - Operating Frequency (When T_A = − 40 °C to + 85 °C)
  - MB95F146S, MB95F146W

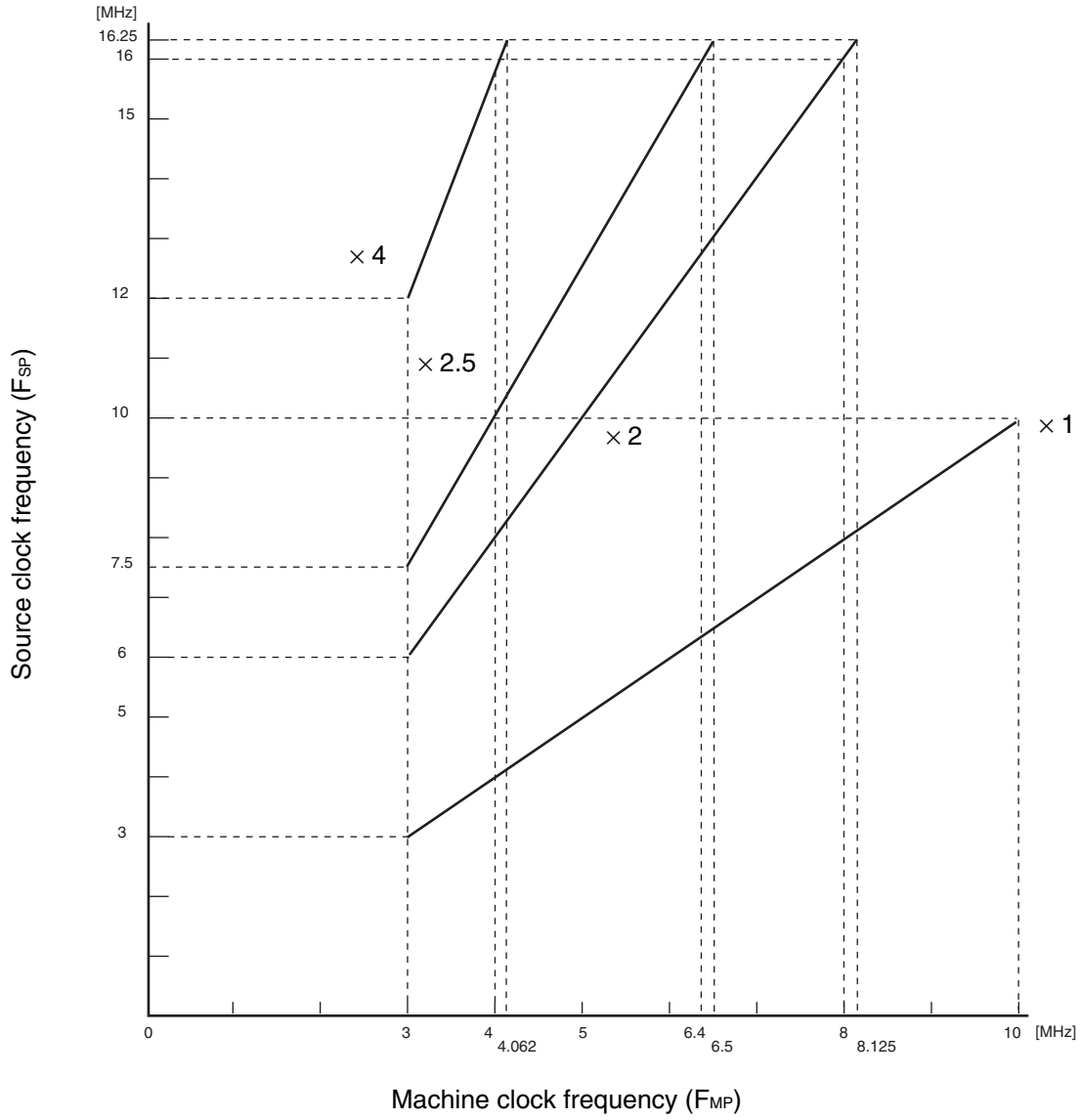




• Operating voltage – Operating frequency (T_A = + 5 °C to + 35 °C)
  • MB95FV100D-101



• Main PLL Operation Frequency



(3) External Reset

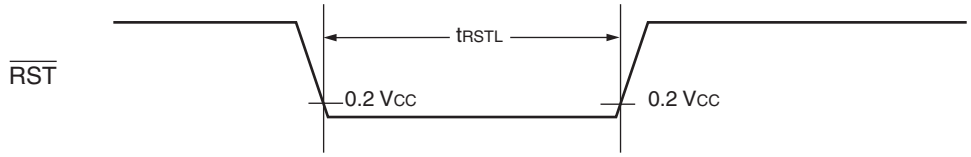
(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	At normal operating
		Oscillation time of oscillator*2 + 2 t_{MCLK}*1	—	ns	At stop mode, sub clock mode, sub sleep mode, and watch mode

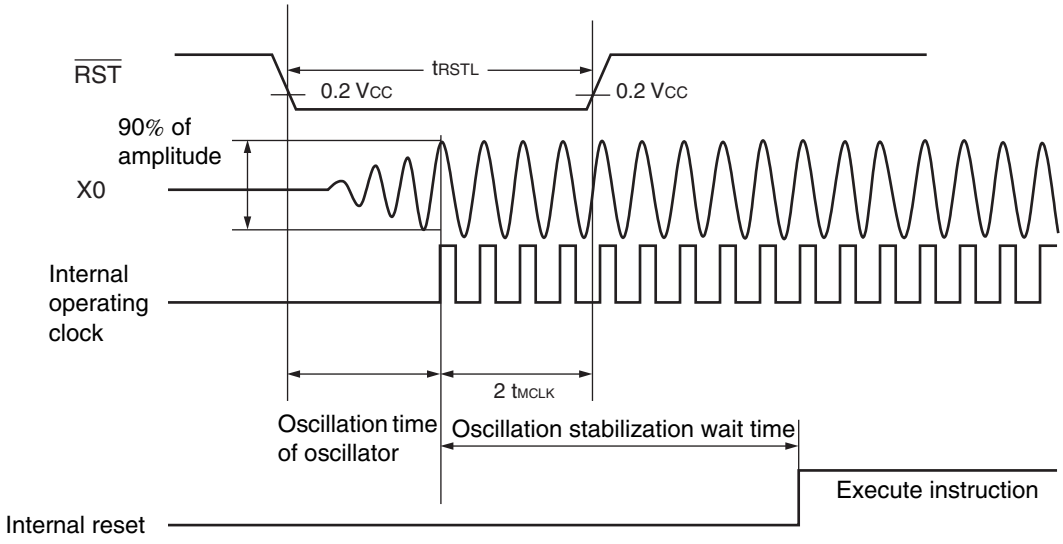
*1 : Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.

*2 : Oscillation start time of oscillator is the time that the amplitude reaches 90 %. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In ceramic oscillators, the oscillation time is between hundreds of μs and several ms. In the external clock, the oscillation time is 0 ms.

• At Normal Operating



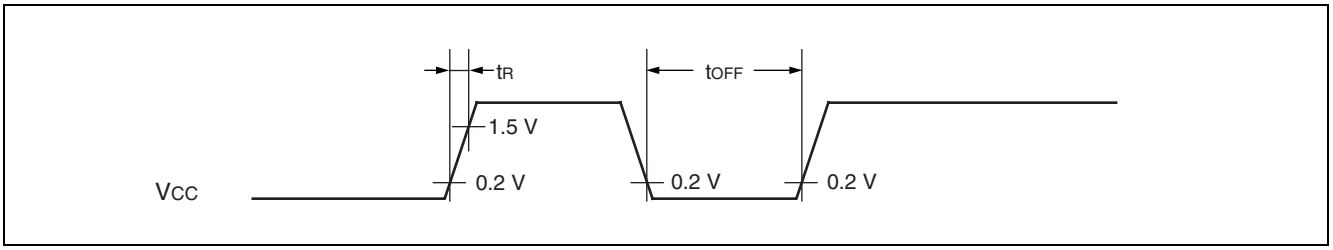
• At Stop Mode, Sub clock Mode, Sub Sleep Mode, Watch Mode, and Power-on



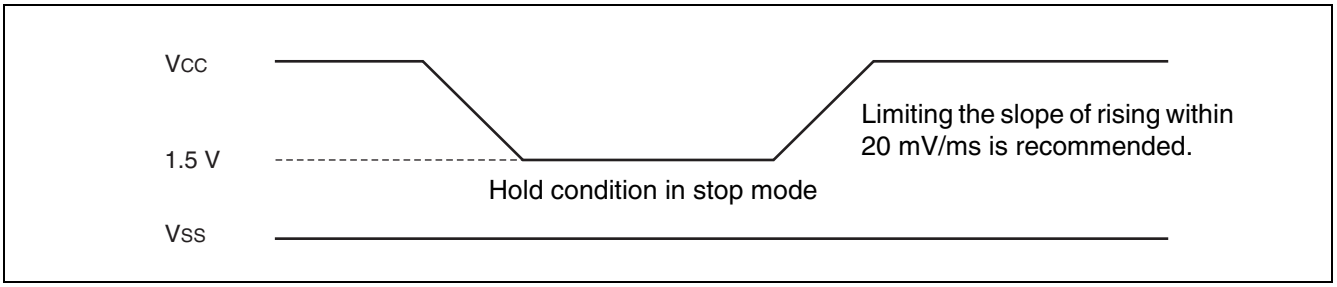
(4) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	36	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Waiting time until power-on



Note : Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 20 mV/ms as shown below.

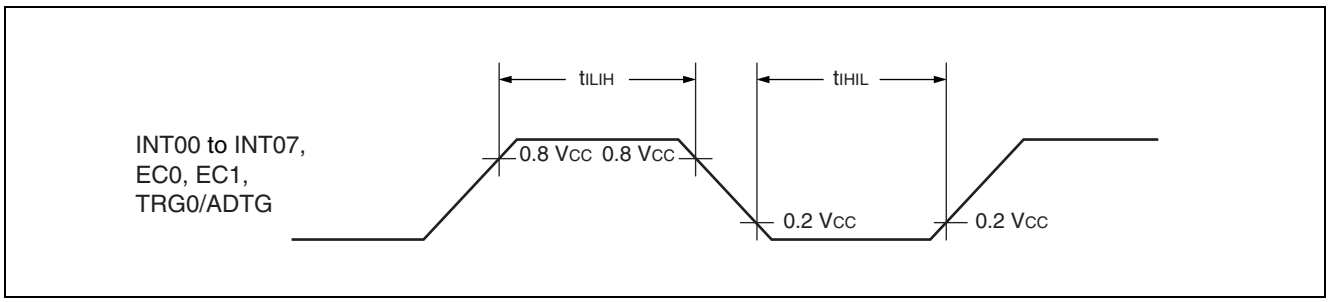


(5) Peripheral Input Timing

(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, EC0, EC1, TRG0/ADTG	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

* : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.



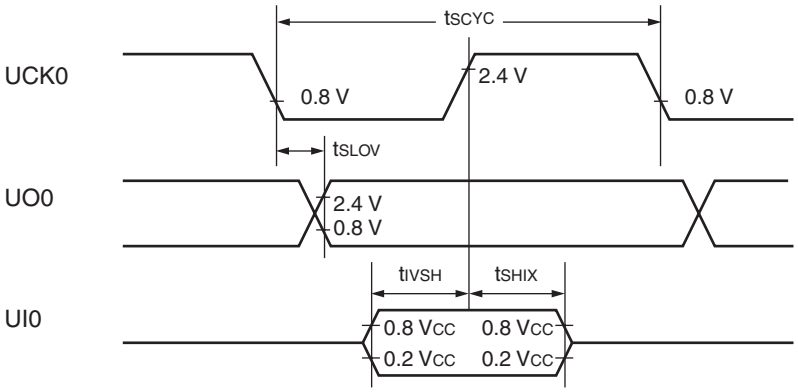
(6) UART/SIO, Serial I/O Timing

(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = − 40 °C to + 85 °C)

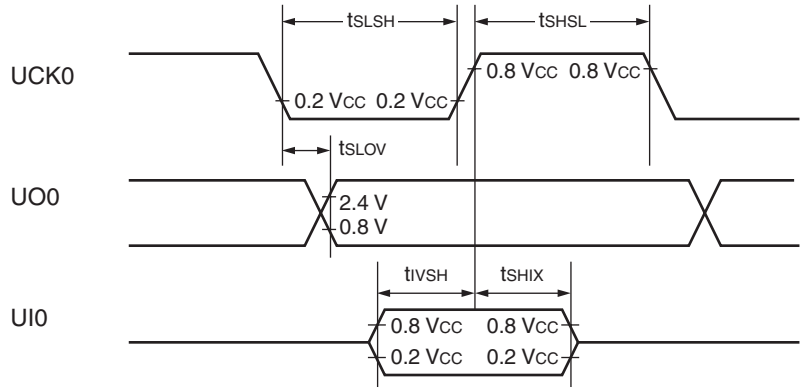
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0	Internal clock operation output pin : C_L = 80 pF + 1TTL.	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		− 190	+ 190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK0	External clock operation output pin : C_L = 80 pF + 1TTL.	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK0		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		0	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns

* : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



(7) LIN-UART Timing

Sampling at the rising edge of sampling clock*1 and prohibited serial clock delay*2
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to + 85 °C)

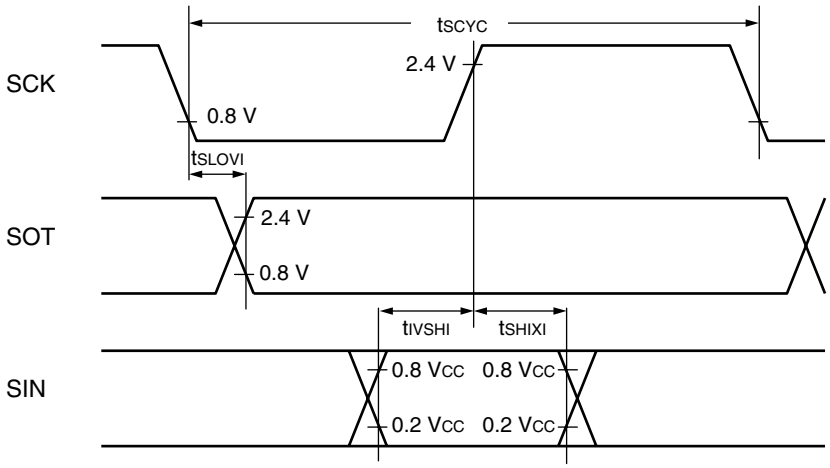
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–95	+ 95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	3 t_{MCLK}*3 – t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

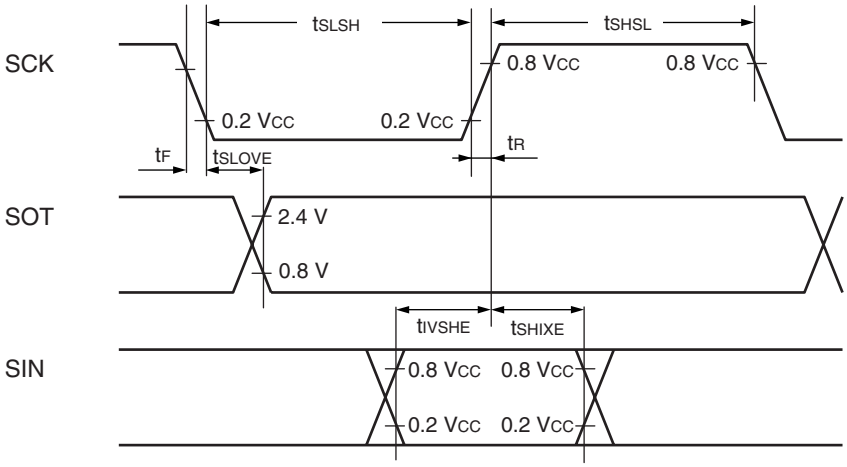
*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



Sampling at the falling edge of sampling clock*1 and prohibited serial clock delay*2
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)

(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to + 85 °C)

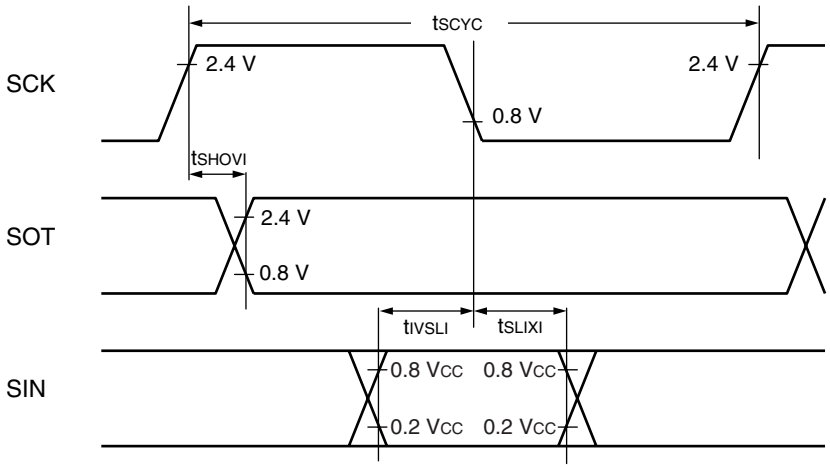
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–95	+ 95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin : C_L = 80 pF + 1 TTL.	3 t_{MCLK}*3 – t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

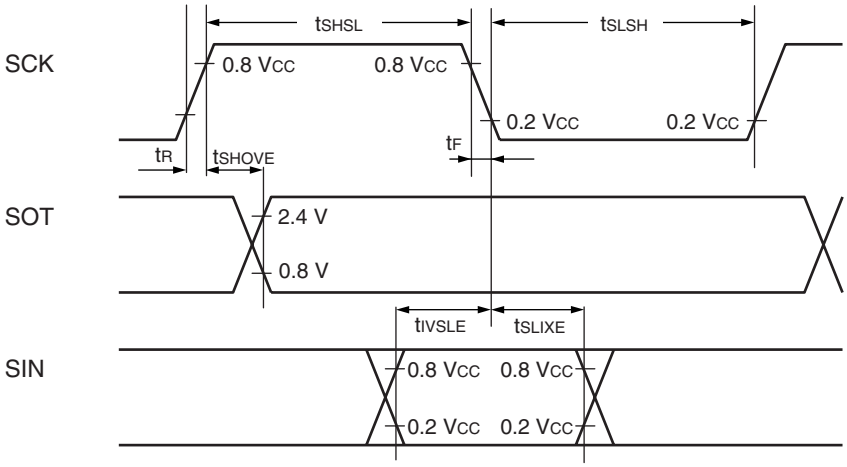
*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to “ (2) Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



Sampling at the rising edge of sampling clock*1 and enabled serial clock delay*2
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)

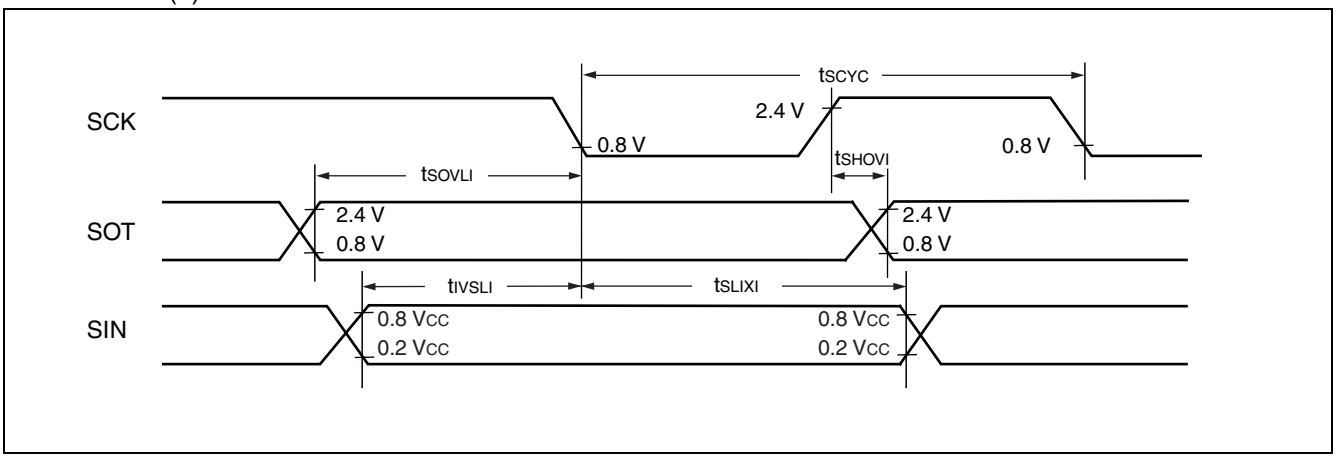
(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–95	+ 95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.



Sampling at the falling edge of sampling clock*1 and enabled serial clock delay*2
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)

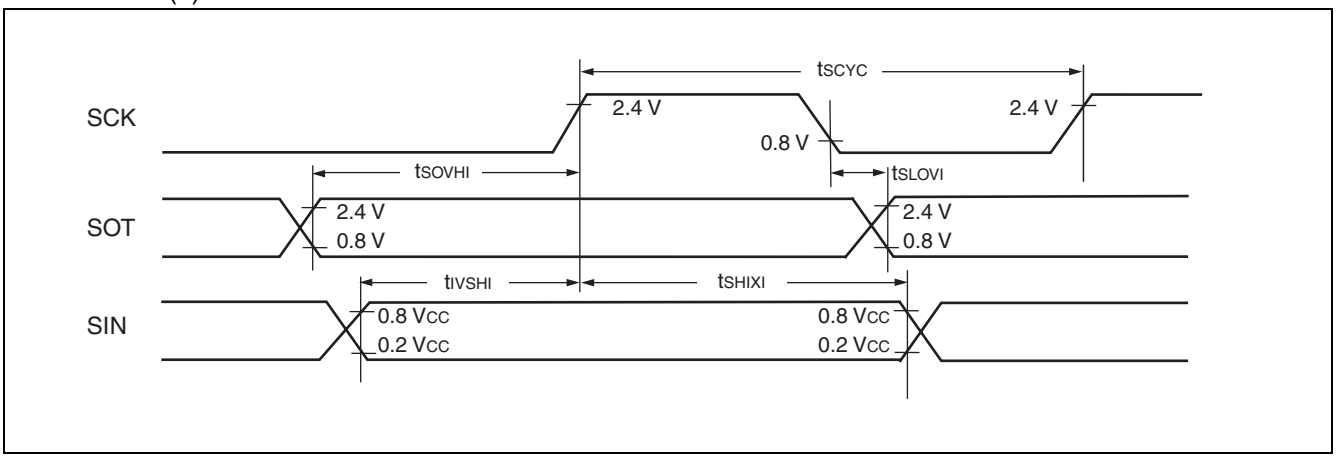
(V_{CC} = 3.3 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to + 85 °C)

Parameter	Sym-bol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operating output pin : C_L = 80 pF + 1 TTL.	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–95	+ 95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1 : Provide switch function whether sampling of reception data is performed at rising edge or falling edge of the serial clock.

*2 : Serial clock delay function is used to delay half clock for the output signal of serial clock.

*3 : Refer to " (2) Source Clock/Machine Clock" for t_{MCLK}.



5. A/D Converter

(1) A/D Converter Electrical Characteristics

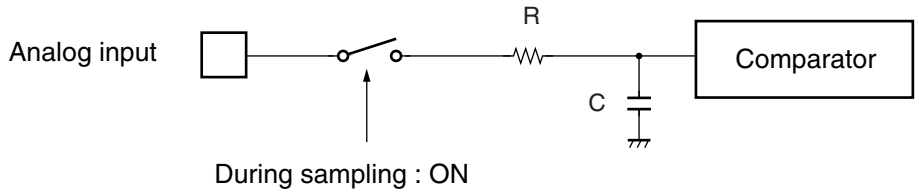
($AV_{CC} = V_{CC}$ = 1.8 V to 3.3 V, $AV_{SS} = V_{SS}$ = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		− 3.0	—	+ 3.0	LSB	
Linearity error		− 2.5	—	+ 2.5	LSB	
Differential linear error		− 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	AV_{SS} − 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	2.7 V ≤ AV_{CC} ≤ 3.3 V
		AV_{SS} − 0.5 LSB	AV_{SS} + 1.5 LSB	AV_{SS} + 3.5 LSB	V	1.8 V ≤ AV_{CC} < 2.7 V
Full-scale transition voltage	V_{FST}	AV_{CC} − 3.5 LSB	AV_{CC} − 1.5 LSB	AV_{CC} + 0.5 LSB	V	2.7 V ≤ AV_{CC} ≤ 3.3 V
		AV_{CC} − 2.5 LSB	AV_{CC} − 0.5 LSB	AV_{CC} + 1.5 LSB	V	1.8 V ≤ AV_{CC} < 2.7 V
Compare time	—	0.6	—	140	µs	2.7 V ≤ AV_{CC} ≤ 3.3 V
		20	—	140	µs	1.8 V ≤ AV_{CC} < 2.7 V
Sampling time	—	0.4	—	∞	µs	2.7 V ≤ AV_{CC} ≤ 3.3 V external impedance < at 1.8 kΩ
		30	—	∞	µs	1.8 V ≤ AV_{CC} < 2.7 V external impedance < at 14.8 kΩ
Analog input current	I_{AIN}	−0.3	—	+ 0.3	µA	
Analog input voltage	V_{AIN}	AV_{SS}	—	AV_{CC}	V	
Reference voltage	—	AV_{SS} + 1.8	—	AV_{CC}	V	AV_{CC} pin
Reference voltage supply current	I_R	—	400	600	µA	AV_{CC} pin, During A/D operation
	I_{RH}	—	—	5	µA	AV_{CC} pin, At stop mode

(2) Notes on Using A/D Converter

- **About the external impedance of analog input and its sampling time**
  - A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

• Analog input equivalent circuit

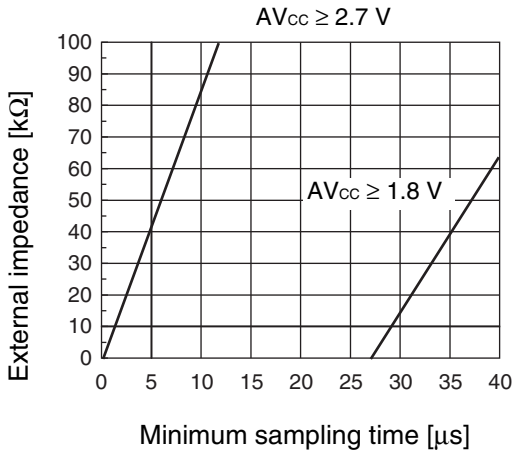


	R	C
2.7 V ≤ AV_{CC} ≤ 3.6 V	1.7 kΩ (Max)	14.5 pF (Max)
1.8 V ≤ AV_{CC} < 2.7 V	84 kΩ (Max)	25.2 pF (Max)

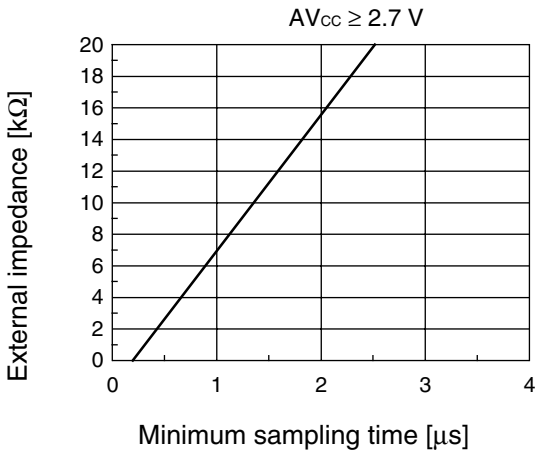
Note : The values are reference values.

• The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)

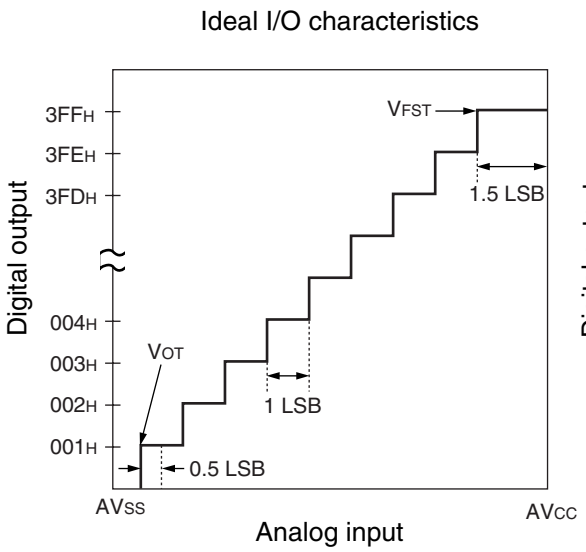


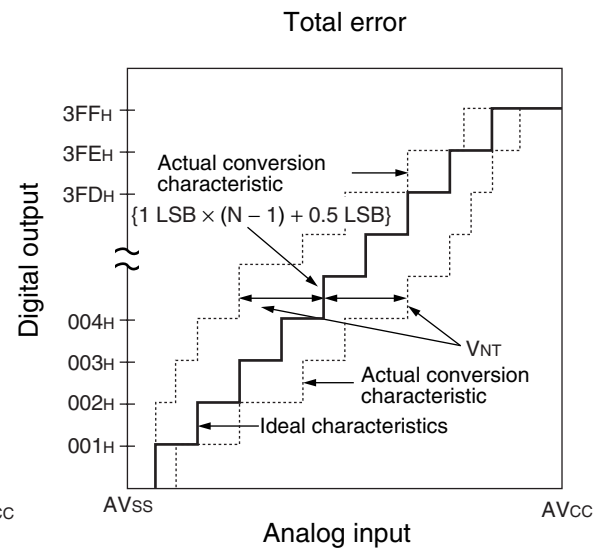
- **About errors**

As |AV_{CC} – AV_{SS}| becomes smaller, values of relative errors grow larger.

(3) Definition of A/D Converter Terms

- Resolution
  The level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit : LSB)
  The deviation between the value along a straight line connecting the zero transition point ("00 0000 0000" ← → "00 0000 0001") of a device and the full-scale transition point ("11 1111 1111" ← → "11 1111 1110") compared with the actual conversion values obtained.
- Differential linear error (Unit : LSB)
  Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error (unit: LSB)
  Difference between actual and theoretical values, caused by a zero transition error, full-scale transition error, linearity error, quantum error, and noise.





$$1\ \text{LSB} = \frac{AV_{CC} - AV_{SS}}{1024}\ \text{(V)}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

N : A/D converter digital output value
V_{NT} : A voltage at which digital output transits from (N – 1) to N.

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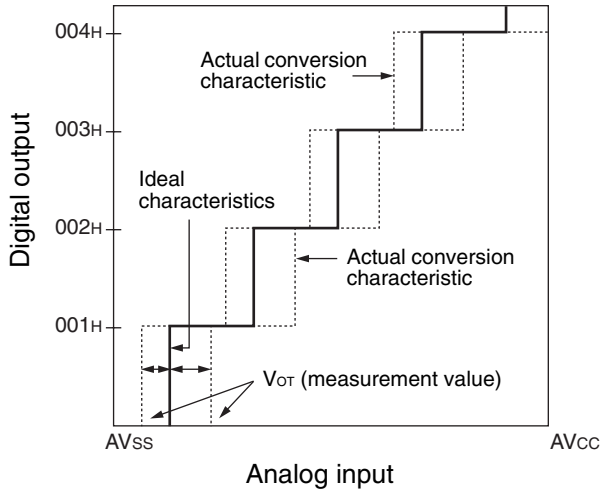
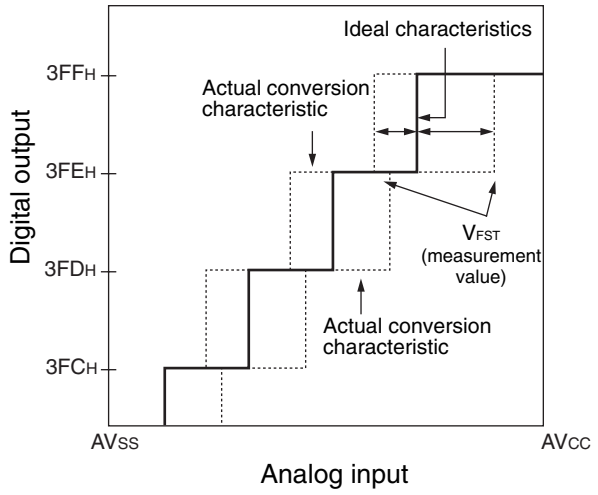
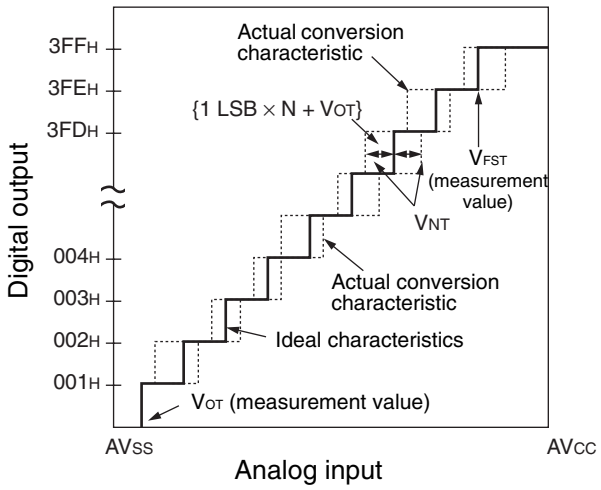
Zero transition error



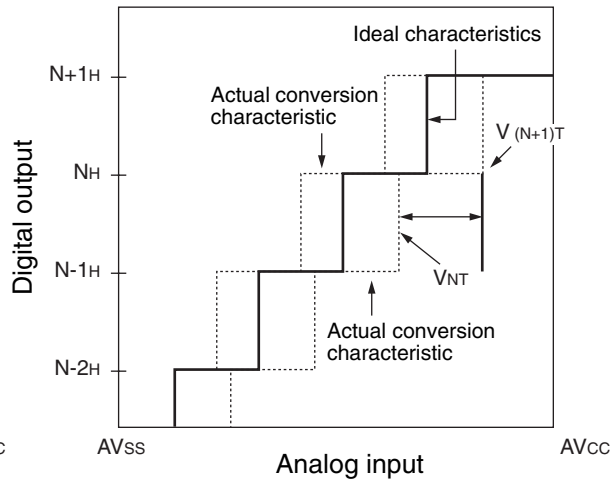
Full-scale transition error



Linearity error



Differential linear error



$$\text{Linear error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value
V_{NT} : A voltage at which digital output transits from (N – 1) to N.
V_{OT} (Ideal value) = AV_{SS} + 0.5 LSB [V]
V_{FST} (Ideal value) = AV_{CC} – 1.5 LSB [V]

6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Chip erase time	—	1*1	1.5*2	s	Excludes 00_H programming prior erasure.
Byte programming time	—	32	3600*2	µs	Excludes system-level overhead time.
Program/erase cycle	10000	—	—	cycle	
Power supply voltage at program/erase	2.7	—	3.3	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85 °C

*1 : T_A = + 25 °C, V_{CC} = 3.0 V, 10000 cycles

*2 : T_A = + 85 °C, V_{CC} = 2.7 V, 10000 cycles

*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

■ MASK OPTION

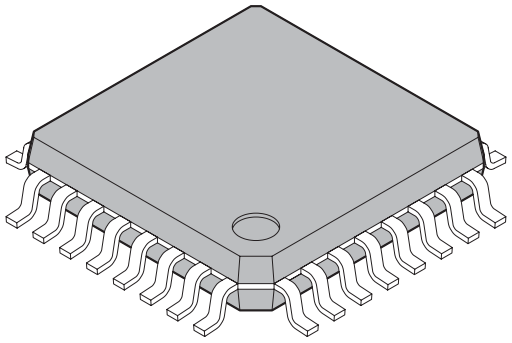
No.	Part number	MB95F146S	MB95F146W	MB95FV100D-101
	Specifying procedure	**Setting disabled**	**Setting disabled**	**Setting disabled**
1	Clock mode select* • Single-system clock mode • Dual-system clock mode	Single-system clock mode	Dual-system clock mode	Changing by the switch on MCU board
2	Low voltage detection reset* • With low voltage detection reset • Without low voltage detection reset	No	No	No
3	Clock supervisor* • With clock supervisor • Without clock supervisor	No	No	No
4	Selection of oscillation stabilization wait time • Selectable the initial value of main clock oscillation stabilization wait time	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14} - 2) / F_{CH}$

* : Low voltage detection reset and clock supervisor are options of 5-V products.

■ ORDERING INFORMATION

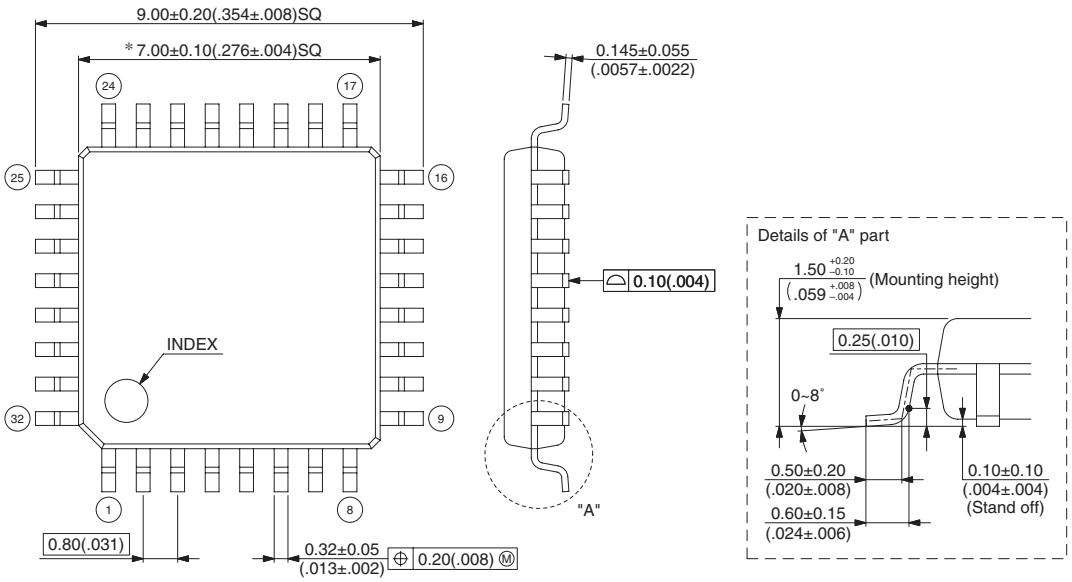
Part number	Package
MB95F146SPFM MB95F146WPFM	32-pin plastic LQFP (FPT-32P-M21)
MB2146-301A (MB95FV100D-101PBT)	MCU board (224-pin plastic PFBGA (BGA-224P-M08))

■ PACKAGE DIMENSIONS

32-pin plastic LQFP		
 (FPT-32P-M21)	Lead pitch	0.80 mm
	Package width × package length	7 × 7 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LQFP32-7×7-0.80

32-pin plastic LQFP
(FPT-32P-M21)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Preliminary Data Sheet→Data Sheet
—	—	Changed the part number MB95FV100B-101→MB95FV100D-101
3	■ PRODUCT LINEUP	CPU functions Minimum instruction execution time : 0.1 µs (at machine clock frequency 10 MHz) →Minimum instruction execution time : 61.5 ns (at machine clock frequency 16.25 MHz) Interrupt processing time : 0.9 µs (at machine clock frequency 10 MHz) →Interrupt processing time : 0.6 µs (at machine clock frequency 16.25 MHz)
4		Added the description Flash memory
27	■ ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Changed under the table*3; V_{I1}→V_I
28	2. Recommended Operating Conditions	Changed the Min value of power supply voltage V_{CC}, AV_{CC}. T_A = − 10 °C to + 85 °C 1.8→2.3 T_A = − 40 °C to + 85 °C 2.0→2.4
29, 30	3. DC Characteristics	Moved “H” level input voltage and “L” level input voltage from the section "2. Recommended Operating Conditions".
		Added to F_{MP} = 16 MHz in the section of I_{CC}, I_{CCS}, I_{CCMPLL} of power supply voltage.
		Changed the Typ and Max values of I_{CTS} 0.4 → 0.64 (Typ value) 0.5 → 0.80 (Max value)
32	4. AC Characteristics (1) Clock Timing	Changed the Max values of clock frequency X0, X1. When using main oscillation circuit 10→16.25 When using external clock 20→32.50 Main PLL multiplied by 2 : 5→8.13 Main PLL multiplied by 2.5 : 4 →6.50
		Added the Main PLL multiplied by 4
34	(2) Source Clock/Machine Clock	Changed source clock cycle time (when using main clock) Min : F_{CH} = 10 MHz, PLL multiplied by 1 →Min : F_{CH} = 8.125 MHz, PLL multiplied by 2
		Changed the Max value of source clock frequency F_{SP}. 10→16.25
		Changed machine clock cycle time (when using main clock) Min : F_{SP} = 10 MHz→Min : F_{SP} = 16.25 MHz
		Changed the Max value of machine clock frequency F_{MP}. 10 .000→16.250

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Page	Section	Change Results
35	4. AC Characteristics (2) Source Clock/Machine Clock	Changed the diagram of • Outline of Clock Generation Block
36, 37		Changed the diagram of • Operating voltage - Operating frequency
38		Changed the diagram of • Main PLL operation frequency range.
49	5. A/D Converter (1) A/D Converter Electrical Characteristics	Changed the pin name in the value section of full-scale transition voltage; AVR→AV_{CC}
55	■ ORDERING INFORMATION	The part number is revised as follows; MB2146-301 MB2146-301A

The vertical lines marked in the left side of the page show the changes.

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

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