

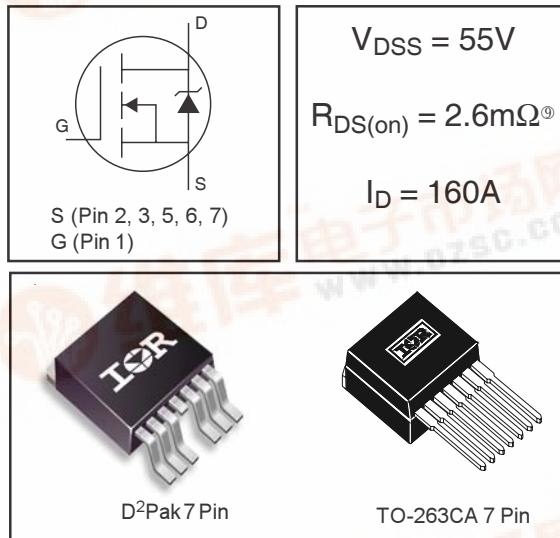
International
IR Rectifier

AUTOMOTIVE MOSFET

PD - 97205A

IRF3805S-7PPbF
IRF3805L-7PPbF

HEXFET® Power MOSFET



Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	240	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (See Fig. 9)	170	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	160	
I_{DM}	Pulsed Drain Current ①	1000	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	440	mJ
E_{AS} (tested)	Single Pulse Avalanche Energy Tested Value ⑥	680	
I_{AR}	Avalanche Current ①	See Fig.12a,12b,15,16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	300 (1.6mm from case)	
		10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	0.50	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑨	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑩⑪	—	40	

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
$\Delta V_{\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.05	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$ SMD	Static Drain-to-Source On-Resistance	—	2.0	2.6	$\text{m}\Omega$	$V_{GS} = 10V, I_D = 140\text{A}$ ③
$V_{GS(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
g_{fs}	Forward Transconductance	110	—	—	S	$V_{DS} = 25V, I_D = 140\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250	μA	$V_{DS} = 55V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200	nA	$V_{GS} = -20V$
Q_g	Total Gate Charge	—	130	200	nC	$I_D = 140\text{A}$
Q_{gs}	Gate-to-Source Charge	—	53	—	nC	$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	49	—	nC	$V_{GS} = 10V$ ③
$t_{d(on)}$	Turn-On Delay Time	—	23	—	ns	$V_{DD} = 28V$
t_r	Rise Time	—	130	—	ns	$I_D = 140\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	80	—	ns	$R_G = 2.4\Omega$
t_f	Fall Time	—	52	—	ns	$V_{GS} = 10V$ ②
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—	nH	
C_{iss}	Input Capacitance	—	7820	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1260	—	pF	$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	610	—	pF	$f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	4310	—	pF	$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	980	—	pF	$V_{GS} = 0V, V_{DS} = 44V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	1540	—	pF	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 44V$

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	240	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	1000	A	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 140\text{A}, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	45	68	ns	$T_J = 25^\circ\text{C}, I_F = 140\text{A}, V_{DD} = 28V$
Q_{rr}	Reverse Recovery Charge	—	35	53	nC	$dI/dt = 100\text{A}/\mu\text{s}$ ③

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by $T_{J\text{max}}$, starting $T_J = 25^\circ\text{C}$, $L=0.043\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 140\text{A}$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ③ Pulse width $\leq 1.0\text{ms}$; duty cycle $\leq 2\%$.
- ④ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑤ Limited by $T_{J\text{max}}$, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R_θ is measured at T_J of approximately 90°C .
- ⑨ Solder mounted on IMS substrate.

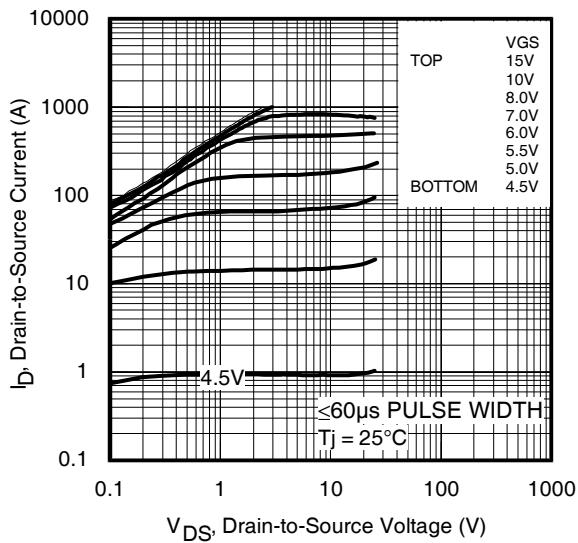


Fig 1. Typical Output Characteristics

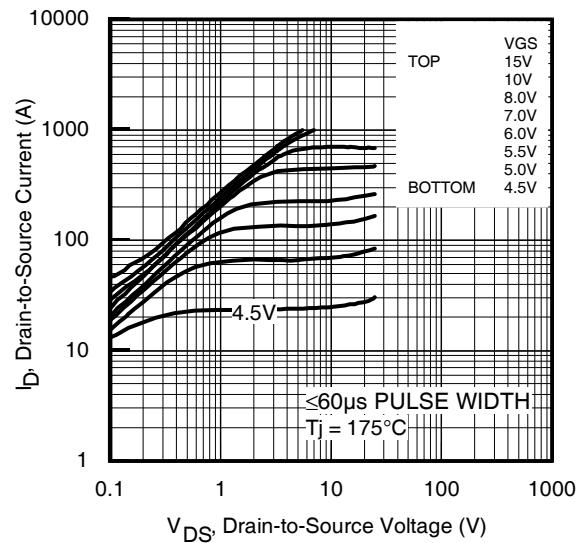


Fig 2. Typical Output Characteristics

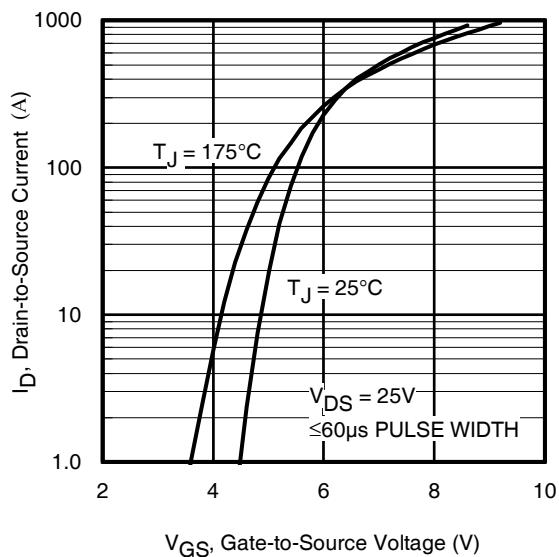


Fig 3. Typical Transfer Characteristics

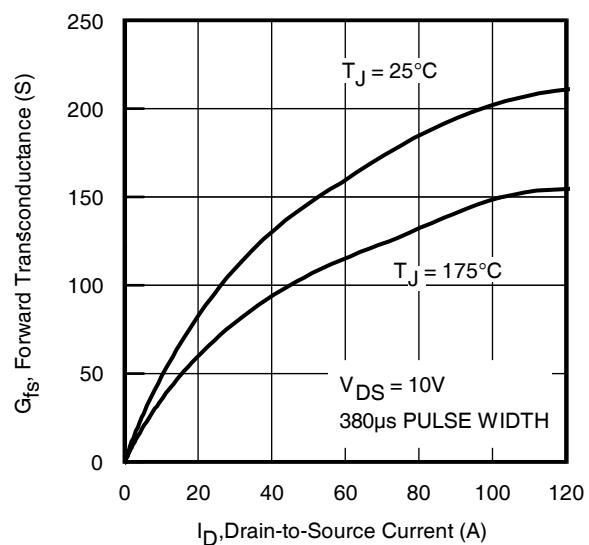


Fig 4. Typical Forward Transconductance vs. Drain Current

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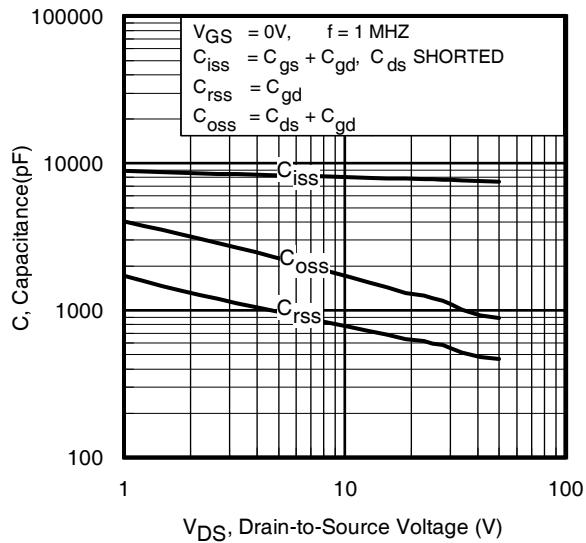


Fig 5. Typical Capacitance vs.
Drain-to-Source Voltage

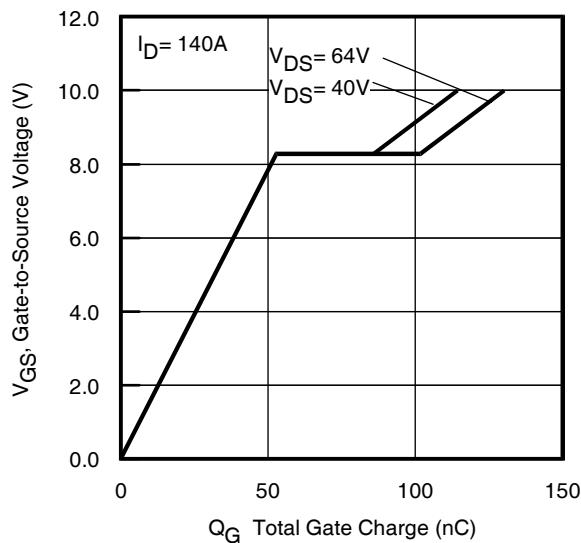


Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage

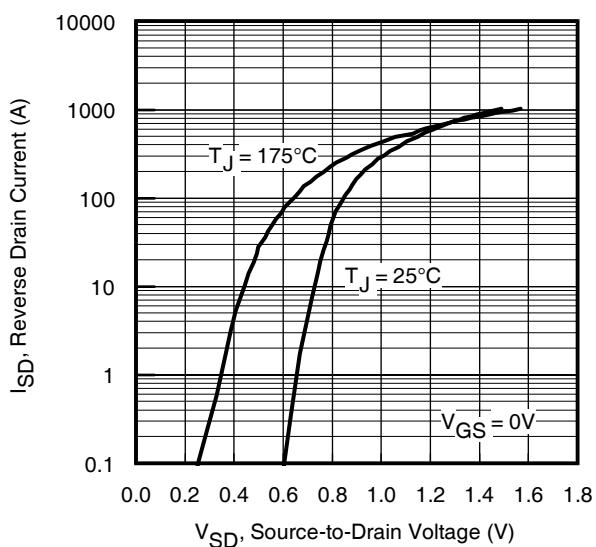


Fig 7. Typical Source-Drain Diode
Forward Voltage

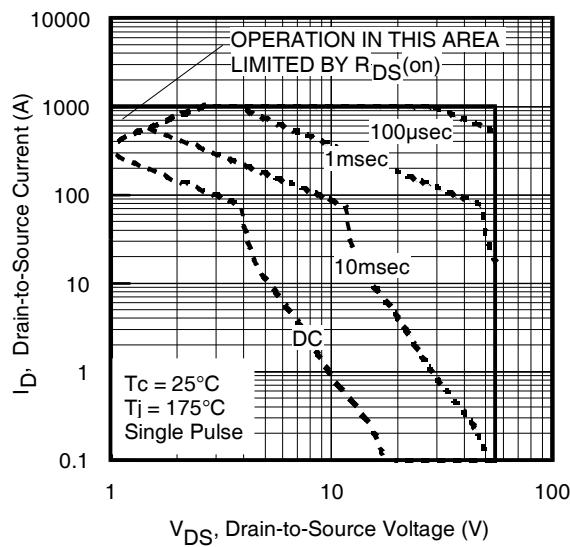


Fig 8. Maximum Safe Operating Area

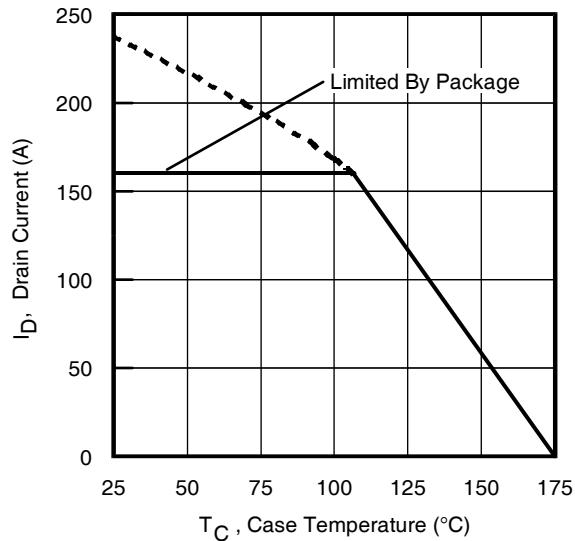


Fig 9. Maximum Drain Current vs.
Case Temperature

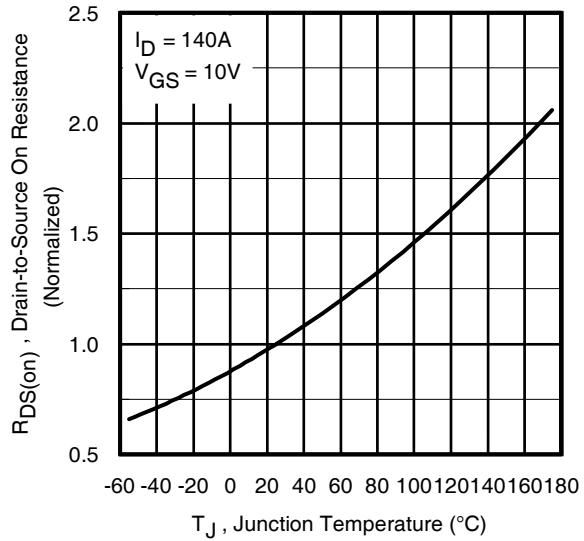


Fig 10. Normalized On-Resistance
vs. Temperature

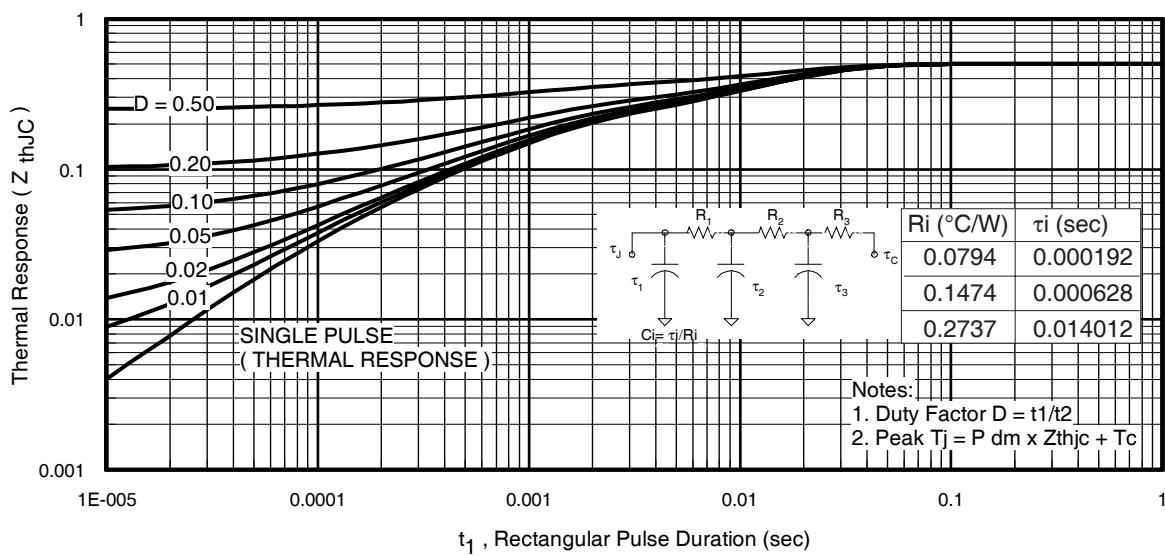


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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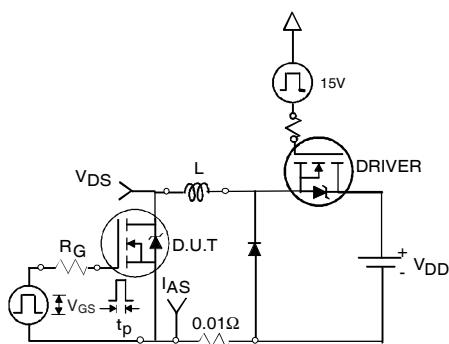


Fig 12a. Unclamped Inductive Test Circuit

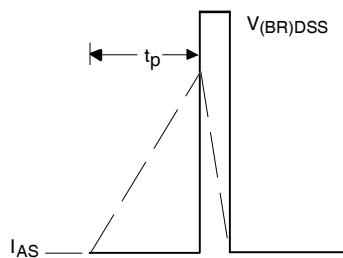


Fig 12b. Unclamped Inductive Waveforms

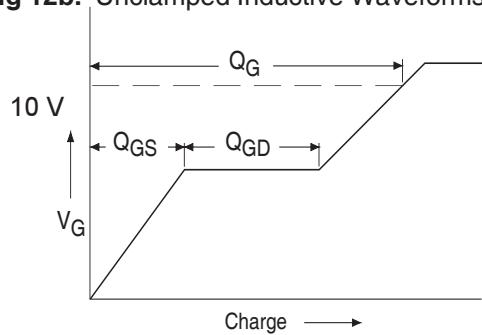


Fig 13a. Basic Gate Charge Waveform

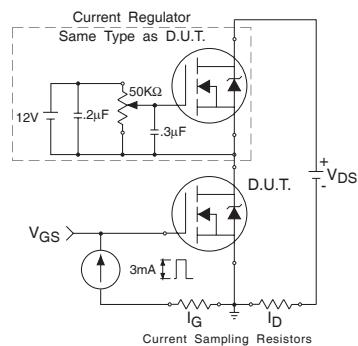


Fig 13b. Gate Charge Test Circuit

6

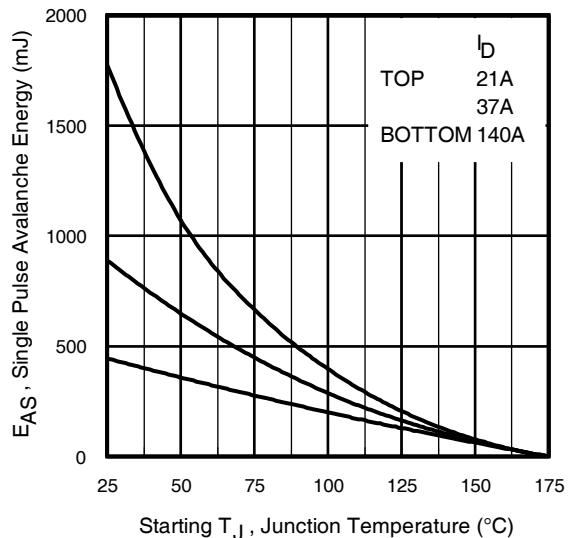


Fig 12c. Maximum Avalanche Energy vs. Drain Current

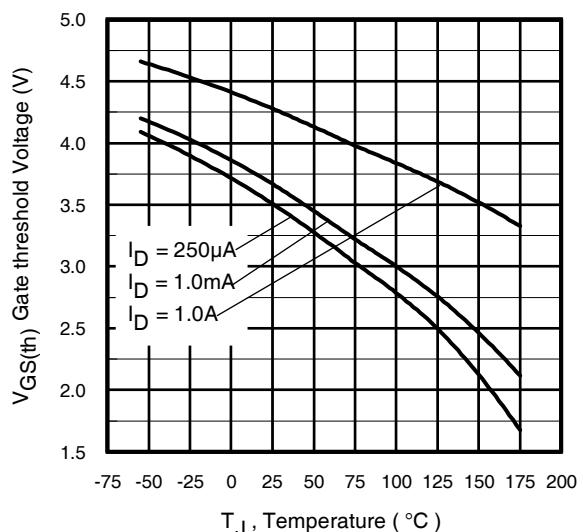


Fig 14. Threshold Voltage vs. Temperature

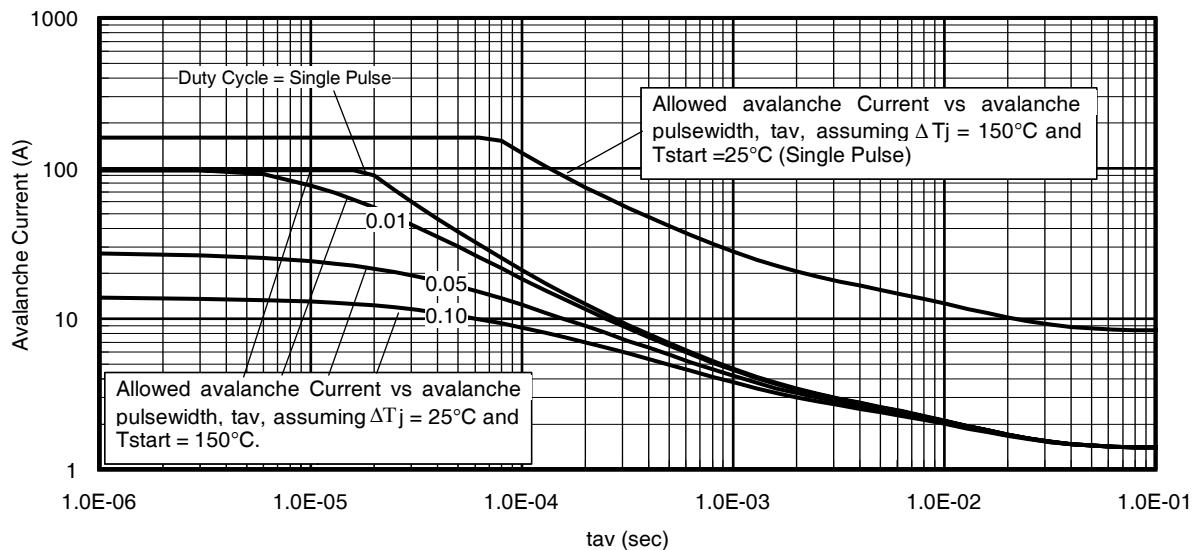


Fig 15. Typical Avalanche Current vs.Pulsewidth

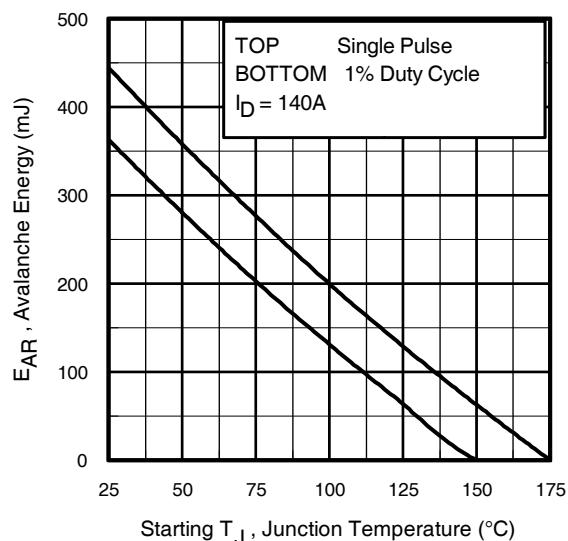


Fig 16. Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
 2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
 3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
 4. $P_D(\text{ave})$ = Average power dissipation per single avalanche pulse.
 5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
 6. I_{av} = Allowable avalanche current.
 7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
- t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_D(\text{ave}) = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_D(\text{ave}) \cdot t_{av}$$

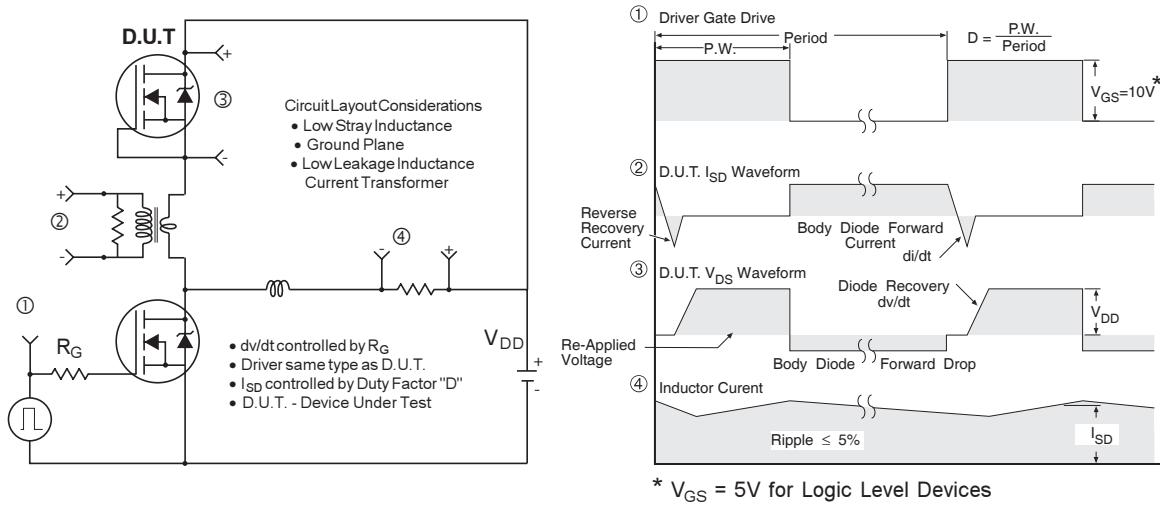


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

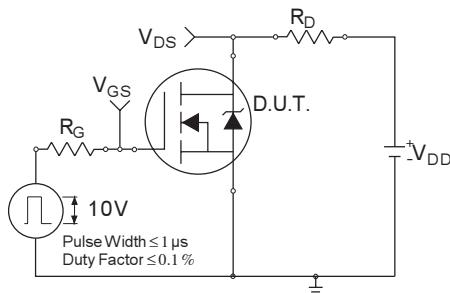


Fig 18a. Switching Time Test Circuit

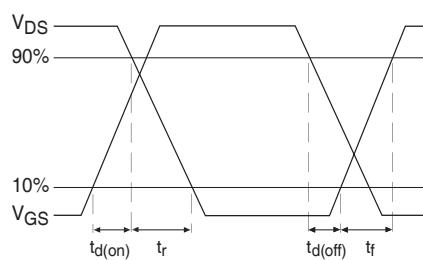
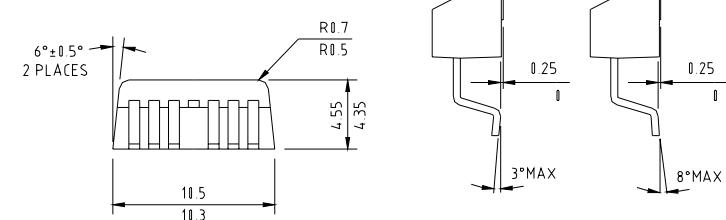
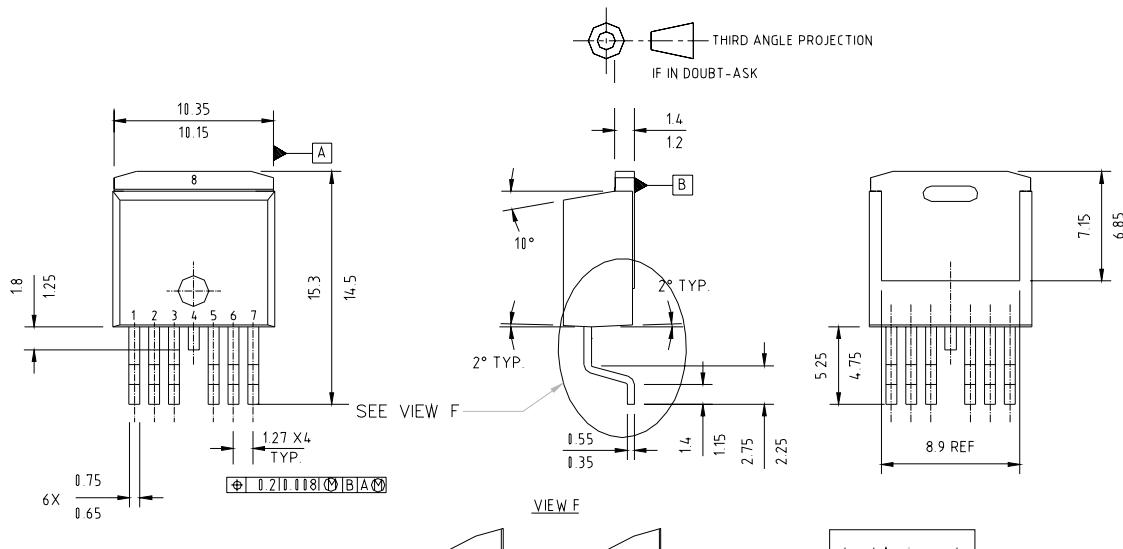


Fig 18b. Switching Time Waveforms

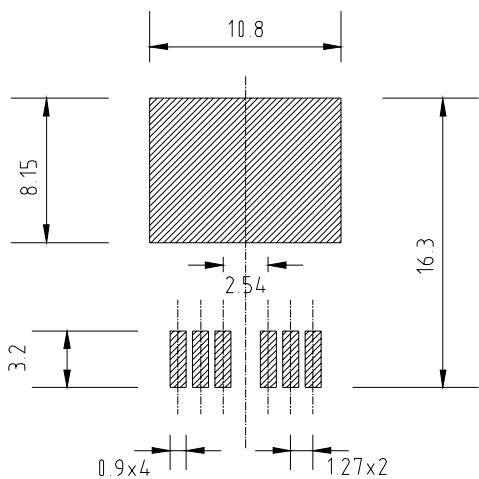
D²Pak - 7 Pin Package Outline

Dimensions are shown in millimeters (inches)



Lead Assignment	
1	Gate
2	Source
3	Source
4	Drain
5	Source
6	Source
7	Source
8	Drain

RECOMMENDED FOOTPRINT



REV	DATE	MODIFICATION
-	18/03/03	RAISED IAW ECN 3426
Rev1	07/04/03	CHANGED IAW ECN 3438
A	23/04/04	ADD LEAD ASSIGNMENT

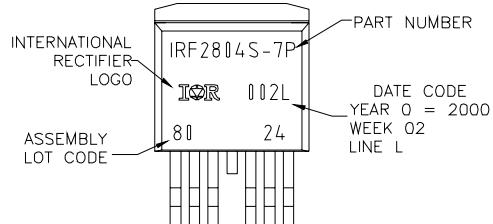
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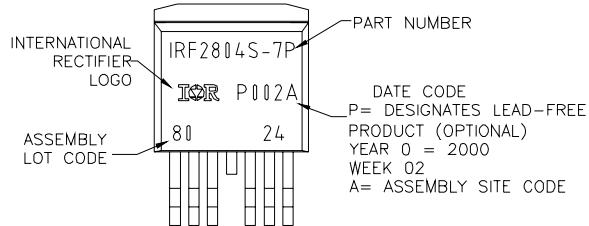
D²Pak - 7 Pin Part Marking Information

EXAMPLE: THIS IS AN IRF2804S-7P WITH
LOT CODE 8024
ASSEMBLED ON WW02,2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead Free"



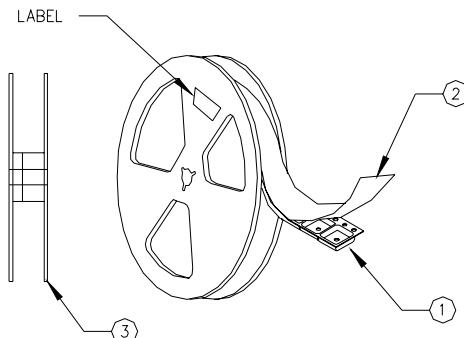
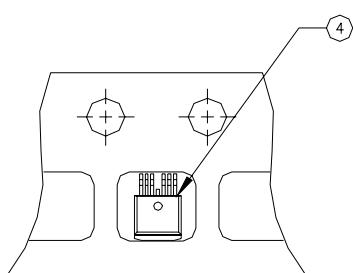
OR



D²Pak - 7 Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.
 - 1.1 REEL SIZE 13 INCH DIAMETER.
 - 1.2 EACH REEL CONTAINING 800 DEVICES.
 - 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
 - 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
 - 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
 - 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.

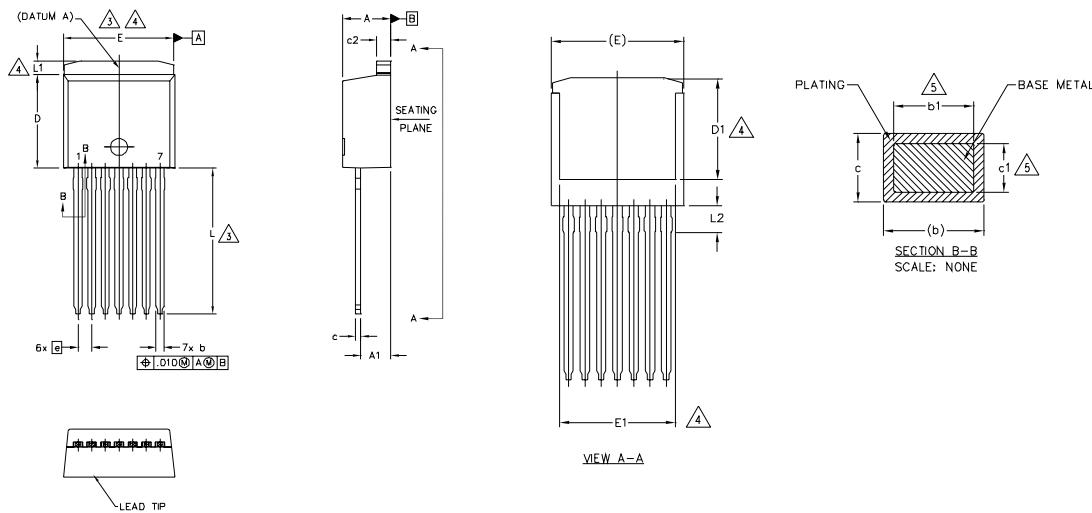


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IRF3805S/L-7PPbF

TO-263CA 7 Pin Long Leads Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-263 CA

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190		
A1	2.03	3.02	.080	.119		
b	0.51	0.91	.020	.036		
b1	0.51	0.81	.020	.032	5	
c	0.38	0.74	.015	.029		
c1	0.38	0.58	.015	.023	5	
c2	1.14	1.65	.045	.065		
D	8.51	9.65	.335	.380	3	
D1	6.86	—	.270	—	4	
E	9.65	10.67	.380	.420	3,4	
E1	6.22	—	.245	—	4	
e	1.27	BSC	.050	BSC		
L	13.46	14.10	.530	.555		
L1	—	1.65	—	.065	4	
L2	—	6.35	—	.250		

LEAD ASSIGNMENTS

HEXFET

1. GATE
2. SOURCE
3. SOURCE
4. DRAIN
5. SOURCE
6. SOURCE
7. SOURCE

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information. 12/06

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>