



## W29C102

# 64K × 16 CMOS FLASH MEMORY

### GENERAL DESCRIPTION

The W29C102 is a 1-megabit, 5-volt only CMOS flash memory organized as 64K × 16 bits. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt VPP is not required. The unique cell architecture of the W29C102 results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

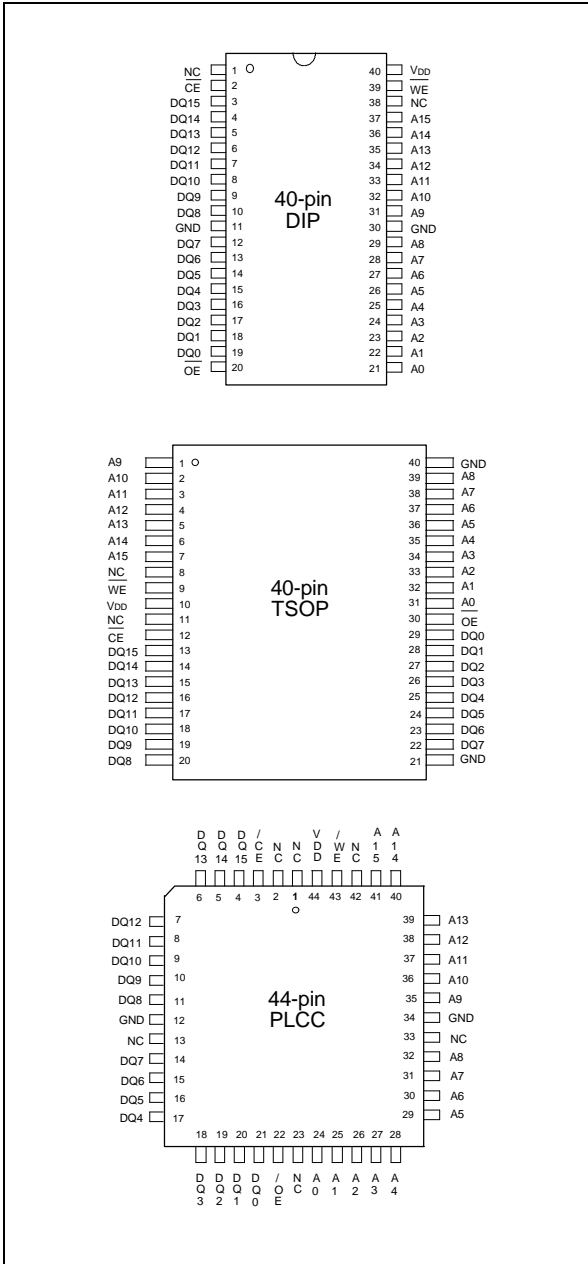
### FEATURES

- Single 5-volt program and erase operations
- Fast page-write operations
  - 128 words per page
  - Page program cycle: 10 mS (max.)
  - Effective word-program cycle time: 39 μS
  - Optional software-protected data write
- Fast chip-erase operation: 50 mS
- Read access time: 70/90/120 nS
- Typical page program/erase cycles: 1K/10K
- Ten-year data retention
- Software and hardware data protection
- Low power consumption
  - Active current: 25 mA (typ.)
  - Standby current: 20 μA (typ.)
- Automatic program timing with internal VPP generation
- End of program detection
  - Toggle bit
  - Data polling
- Latched address and data
- TTL compatible I/O
- JEDEC standard word-wide pinouts
- Available packages: 40-pin 600 mil DIP, TSOP and 44-pin PLCC

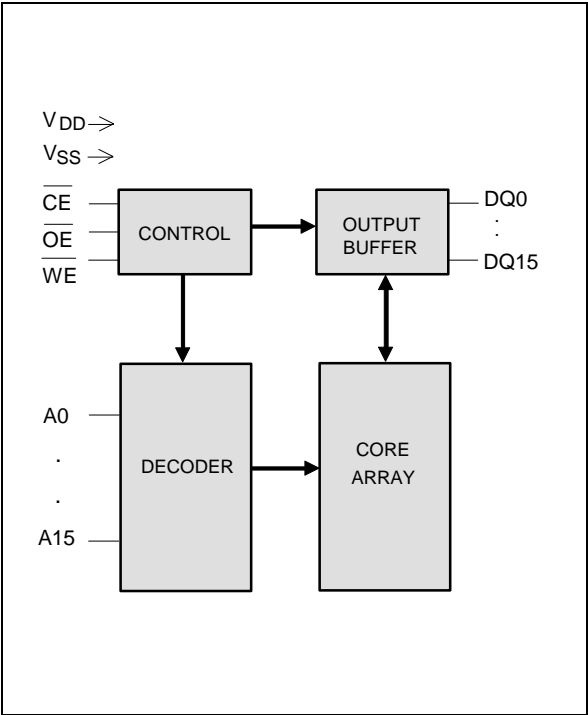




## PIN CONFIGURATIONS



## BLOCK DIAGRAM



## PIN DESCRIPTION

SYMBOL	PIN NAME
A0–A15	Address Inputs
DQ0–DQ15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
VDD	Power Supply
GND	Ground
NC	No Connection



## FUNCTIONAL DESCRIPTION

### Read Mode

The read operation of the W29C102 is controlled by  $\overline{CE}$  and  $\overline{OE}$ , both of which have to be low for the host to obtain data from the outputs.  $\overline{CE}$  is used for device selection. When  $\overline{CE}$  is high, the chip is de-selected and only standby power will be consumed.  $\overline{OE}$  is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either  $\overline{CE}$  or  $\overline{OE}$  is high. Refer to the timing waveforms for further details.

### Page Write Mode

The W29C102 is programmed on a page basis. Every page contains 128 words of data. If a word of data within a page is to be changed, data for the entire page must be loaded into the device. Any word that is not loaded will be erased to "FFh" during programming of the page.

The write operation is initiated by forcing  $\overline{CE}$  and  $\overline{WE}$  low and  $\overline{OE}$  high. The write procedure consists of two steps. Step 1 is the word-load cycle, in which the host writes to the page buffer of the device. Step 2 is an internal programming cycle, during which the data in the page buffers are simultaneously written into the memory array for non-volatile storage.

During the word-load cycle, the addresses are latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. The data are latched by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. If the host loads a second word into the page buffer within a word-load cycle time ( $T_{BLC}$ ) of 200  $\mu$ S, after the initial word-load cycle, the W29C102 will stay in the page load cycle. Additional words can then be loaded consecutively. The page load cycle will be terminated and the internal programming cycle will start if no additional word is loaded into the page buffer. A7 to A15 specify the page address. All words that are loaded into the page buffer must have the same page address. A0 to A6 specify the word address within the page. The words may be loaded in any order; sequential loading is not required.

In the internal programming cycle, all data in the page buffers, i.e., 128 words of data, are written simultaneously into the memory array. The typical programming time is 5 mS. The entire memory array can be written in 2.6 seconds. Before the completion of the internal programming cycle, the host is free to perform other tasks such as fetching data from other locations in the system to prepare to write the next page.

### Software-protected Data Write

The device provides a JEDEC-approved optional software-protected data write. Once this scheme is enabled, any write operation requires a series of three-word program commands (with specific data to a specific address) to be performed before the data load operation. The three-word load command sequence begins the page load cycle, without which the write operation will not be activated. This write scheme provides optimal protection against inadvertent write cycles, such as cycles triggered by noise during system power-up and power-down.

The W29C102 is shipped with the software data protection enabled. To enable the software data protection scheme, perform the three-word command cycle at the beginning of a page load cycle. The device will then enter the software data protection mode, and any subsequent write operation must be preceded by the three-word program command cycle. Once enabled, the software data protection will remain enabled unless the disable commands are issued. A power transition will not reset the



software data protection feature. To reset the device to unprotected mode, a six-word command sequence is required. See Table 3 for specific codes and Figure 10 for the timing diagram.

## Hardware Data Protection

The integrity of the data stored in the W29C102 is also hardware protected in the following ways:

- (1) Noise/Glitch Protection: A  $\overline{WE}$  pulse of less than 15 nS in duration will not initiate a write cycle.
- (2) VDD Power Up/Down Detection: The programming operation is inhibited when VDD is less than 2.5V.
- (3) Write Inhibit Mode: Forcing  $\overline{OE}$  low,  $\overline{CE}$  high, or  $\overline{WE}$  high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.
- (4) VDD power-on delay: When VDD has reached its sense level, the device will automatically time-out 5 mS before any write (erase/program) operation.

## Data Polling (DQ7 & DQ15)- Write Status Detection

The W29C102 includes a data polling feature to indicate the end of a programming cycle. When the W29C102 is in the internal programming cycle, any attempt to read DQ7 and/or DQ15 of the last word loaded during the page/word-load cycle will receive the complement of the true data. Once the programming cycle is completed, DQ7 will show the true data.

## Toggle Bit (DQ6 & DQ14)- Write Status Detection

In addition to data polling, the W29C102 provides another method for determining the end of a program cycle. During the internal programming cycle, any consecutive attempts to read DQ6 and/or DQ14 will produce alternating 0's and 1's. When the programming cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

## 5-Volt-only Software Chip Erase

The chip-erase mode can be initiated by a six-word command sequence. After the command loading cycles, the device enters the internal chip erase mode, which is automatically timed and will be completed in 50 mS. The host system is not required to provide any control or timing during this operation.

## Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-word command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code (00DAh). A read from address 0001H outputs the device code (004Fh). The product ID operation can be terminated by a three-word command sequence.

In the hardware access mode, access to the product ID is activated by forcing  $\overline{CE}$  and  $\overline{OE}$  low,  $\overline{WE}$  high, and raising A9 to 12 volts.



## TABLE OF OPERATING MODES

### Operating Mode Selection

(V<sub>HH</sub> = 12V)

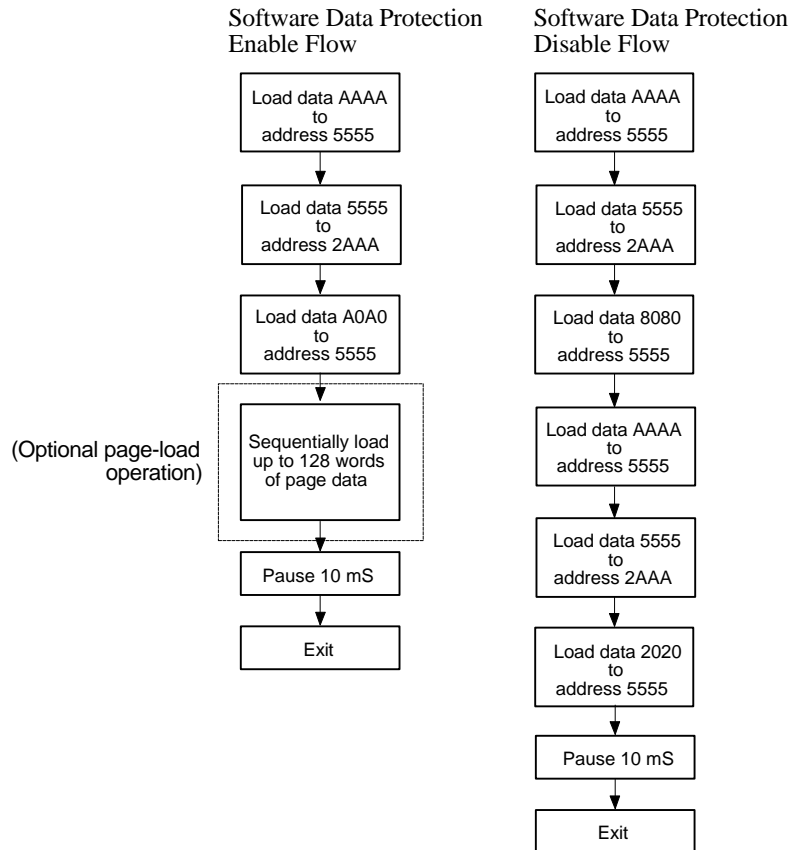
MODE	PINS				
	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	ADDRESS	DQ.
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	A <sub>IN</sub>	Dout
Write	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	A <sub>IN</sub>	Din
Standby	V <sub>IH</sub>	X	X	X	High Z
Write Inhibit	X	V <sub>IL</sub>	X	X	High Z/DOUT
	X	X	V <sub>IH</sub>	X	High Z/DOUT
Output Disable	X	V <sub>IH</sub>	X	X	High Z
5-Volt Software Chip Erase	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	A <sub>IN</sub>	Din
Product ID	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	A <sub>0</sub> = V <sub>IL</sub> ; A <sub>1</sub> –A <sub>15</sub> = V <sub>IL</sub> ; A <sub>9</sub> = V <sub>HH</sub>	Manufacturer Code 00DA (Hex)
	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	A <sub>0</sub> = V <sub>IH</sub> ; A <sub>1</sub> –A <sub>15</sub> = V <sub>IL</sub> ; A <sub>9</sub> = V <sub>HH</sub>	Device Code 004F (Hex)



## Command Codes for Software Data Protection

BYTE SEQUENCE	TO ENABLE PROTECTION		TO DISABLE PROTECTION	
	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555H	AAAAH	5555H	AAAAH
1 Write	2AAAH	5555H	2AAAH	5555H
2 Write	5555H	A0A0H	5555H	8080H
3 Write	-	-	5555H	AAAAH
4 Write	-	-	2AAAH	5555H
5 Write	-	-	5555H	2020H

## Software Data Protection Acquisition Flow



Notes for software program code:

Data Format: DQ15–DQ0 (Hex)

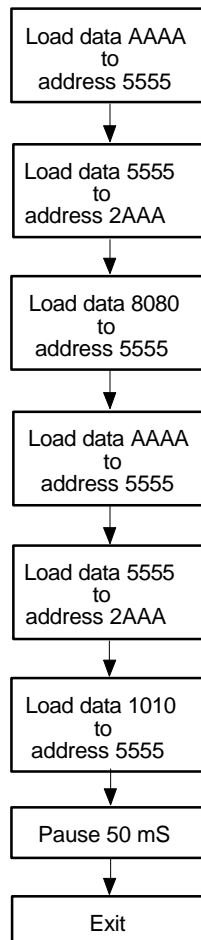
Address Format: A14–A0 (Hex)



## Command Codes for Software Chip Erase

BYTE SEQUENCE	ADDRESS	DATA
0 Write	5555H	AAAAH
1 Write	2AAAH	5555H
2 Write	5555H	8080H
3 Write	5555H	AAAAH
4 Write	2AAAH	5555H
5 Write	5555H	1010H

## Software Chip Erase Acquisition Flow



Notes for software chip erase:  
 Data Format: DQ15–DQ0 (Hex)  
 Address Format: A14–A0 (Hex)

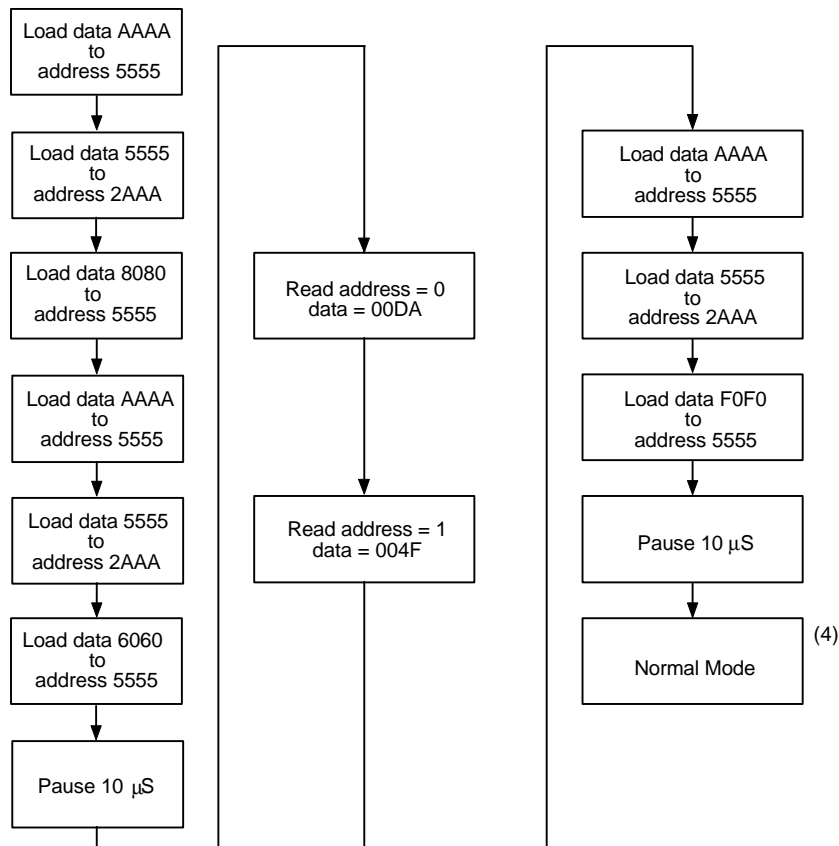


## Command Codes for Product Identification

BYTE SEQUENCE	ALTERNATE SOFTWARE (5) PRODUCT IDENTIFICATION ENTRY		SOFTWARE PRODUCT IDENTIFICATION ENTRY		SOFTWARE PRODUCT IDENTIFICATION EXIT	
	ADDRESS	DATA	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555H	AAH	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H	2AAAH	55H
2 Write	5555H	90H	5555H	80H	5555H	F0H
3 Write	-	-	5555H	AAH	-	-
4 Write	-	-	2AAAH	55H	-	-
5 Write	-	-	5555H	60H	-	-
Pause 10 μS			Pause 10 μS		Pause 10 μS	

## Software Product Identification Acquisition Flow

Product Identification Entry (1) Product Identification Mode (2, 3) Product Identification Exit (1)



Notes for software product identification:

- (1) Data format: DQ15–DQ0 (Hex); address format: A14–A0 (Hex).
- (2) A1–A15 = V<sub>IL</sub>; manufacture code is read for A0 = V<sub>IL</sub>; device code is read for A0 = V<sub>IH</sub>.
- (3) The device does not remain in identification mode if power down.
- (4) The device returns to standard operation mode.
- (5) This product supports both the JEDEC standard 3 byte command code sequence and original 6 byte command code sequence. For new designs, Winbond recommends that the 3 byte command code sequence be used.





## DC CHARACTERISTICS

### Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V <sub>SS</sub> Potential	-0.5 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential except $\overline{OE}$	-0.5 to V <sub>DD</sub> +1.0	V
Transient Voltage (<20 nS ) on Any Pin to Ground Potential	-1.0 to V <sub>DD</sub> +1.0	V
Voltage on A9 and $\overline{OE}$ Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### DC Operating Characteristics

(V<sub>DD</sub> = 5.0V ±10%, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I <sub>CC</sub>	$\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ , all I/Os open Address inputs = V <sub>IL</sub> /V <sub>IH</sub> , at f = 5 MHz	-	25	60	mA
Standby V <sub>DD</sub> Current (TTL input)	I <sub>SB1</sub>	$\overline{CE} = V_{IH}$ , all I/Os open Other inputs = V <sub>IL</sub> /V <sub>IH</sub>	-	2	3	mA
Standby V <sub>DD</sub> Current (CMOS input)	I <sub>SB2</sub>	$\overline{CE} = V_{DD} - 0.3V$ , all I/Os open Other inputs = V <sub>DD</sub> - 0.3V/GND	-	20	200	μA
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>DD</sub>	-	-	10	μA
Output Leakage Current	I <sub>LO</sub>	V <sub>OUT</sub> = GND to V <sub>DD</sub>	-	-	10	μA
Input Low Voltage	V <sub>IL</sub>	-	-	-	0.8	V
Input High Voltage	V <sub>IH</sub>	-	2.0	-	-	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA	-	-	0.45	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -0.4 mA	2.4	-	-	V
Output High Voltage CMOS	V <sub>OH2</sub>	I <sub>OH</sub> = -100 μA; V <sub>CC</sub> = 4.5V	4.2	-	-	V



## Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	TPU. READ	100	$\mu$ S
Power-up to Write Operation	TPU. WRITE	5	mS

## CAPACITANCE

(V<sub>DD</sub> = 5.0V, T<sub>A</sub> = 25° C, f = 1 MHz)

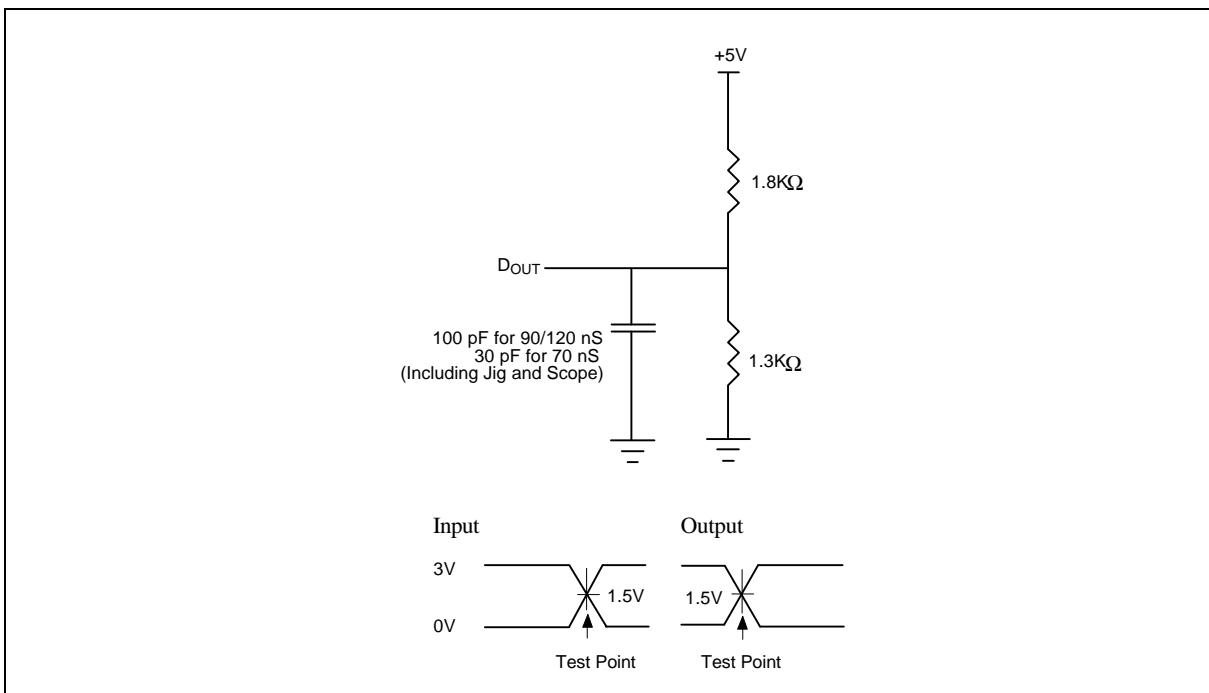
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	12	pf
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	6	pf

## AC CHARACTERISTICS

### AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise/Fall Time	<5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C <sub>L</sub> = 100 pF for 90/120 nS C <sub>L</sub> = 30 pF for 70 nS

### AC Test Load and Waveform





AC Characteristics, continued

## Read Cycle Timing Parameters

(V<sub>DD</sub> = 5.0V ±10%, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to 70° C)

PARAMETER	SYM.	W29C102-70		W29C102-90		W29C102-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	70	-	90	-	120	-	nS
Chip Enable Access Time	TCE	-	70	-	90	-	120	nS
Address Access Time	TAA	-	70	-	90	-	120	nS
Output Enable Access Time	TOE	-	35	-	45	-	60	nS
$\overline{\text{CE}}$ High to High-Z Output	TCHZ	-	25	-	25	-	30	nS
$\overline{\text{OE}}$ High to High-Z Output	TOHZ	-	25	-	25	-	30	nS
Output Hold from Address Change	TOH	0	-	0	-	0	-	nS

## Byte/Page-write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Write Cycle (erase and program)	TWC	-	-	10	mS
Address Setup Time	TAS	0	-	-	nS
Address Hold Time	TAH	50	-	-	nS
$\overline{\text{WE}}$ and $\overline{\text{CE}}$ Setup Time	TCS	0	-	-	nS
$\overline{\text{WE}}$ and $\overline{\text{CE}}$ Hold Time	TCH	0	-	-	nS
$\overline{\text{OE}}$ High Setup Time	TOES	0	-	-	nS
$\overline{\text{OE}}$ High Hold Time	TOEH	0	-	-	nS
$\overline{\text{CE}}$ Pulse Width	TC <sub>P</sub>	70	-	-	nS
$\overline{\text{WE}}$ Pulse Width	TW <sub>P</sub>	70	-	-	nS
$\overline{\text{WE}}$ High Width	TW <sub>PH</sub>	100	-	-	nS
Data Setup Time	T <sub>DS</sub>	50	-	-	nS
Data Hold Time	T <sub>DH</sub>	0	-	-	nS
Byte Load Cycle Time	T <sub>BLC</sub>	-	-	150	μS

Notes:

All AC timing signals observe the following guidelines for determining setup and hold times:

- (a) High level signal's reference level is V<sub>IH</sub>.
- (b) Low level signal's reference level is V<sub>IL</sub>.



AC Characteristics, continued

**DATA Polling Characteristics (1)**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Data Hold Time	T <sub>DH</sub>	10	-	-	nS
$\overline{\text{OE}}$ Hold Time	T <sub>OE<math>\overline{\text{H}}</math></sub>	10	-	-	nS
$\overline{\text{OE}}$ to Output Delay (2)	T <sub>OE</sub>	-	-	-	nS
Write Recovery Time	T <sub>WR</sub>	0	-	-	nS

Notes:

- (1) These parameters are characterized and not 100% tested.  
 (2) See T<sub>OE</sub> spec in A.C. Read Cycle Timing Parameters.

**Toggle Bit Characteristics (1)**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Data Hold Time	T <sub>DH</sub>	10	-	-	nS
$\overline{\text{OE}}$ Hold Time	T <sub>OE<math>\overline{\text{H}}</math></sub>	10	-	-	nS
$\overline{\text{OE}}$ to Output Delay (2)	T <sub>OE</sub>	-	-	-	nS
$\overline{\text{OE}}$ High Pulse	T <sub>OEHP</sub>	150	-	-	nS
Write Recovery Time	T <sub>WR</sub>	0	-	-	nS

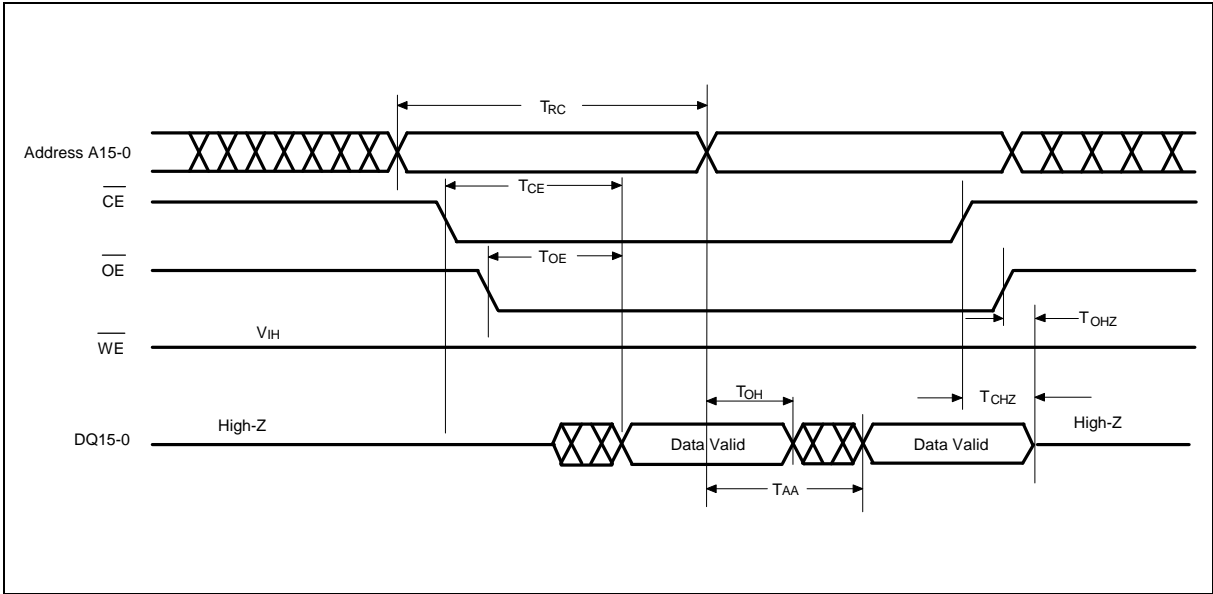
Notes:

- (1) These parameters are characterized and not 100% tested.  
 (2) See T<sub>OE</sub> spec in A.C. Read Cycle Timing Parameters.

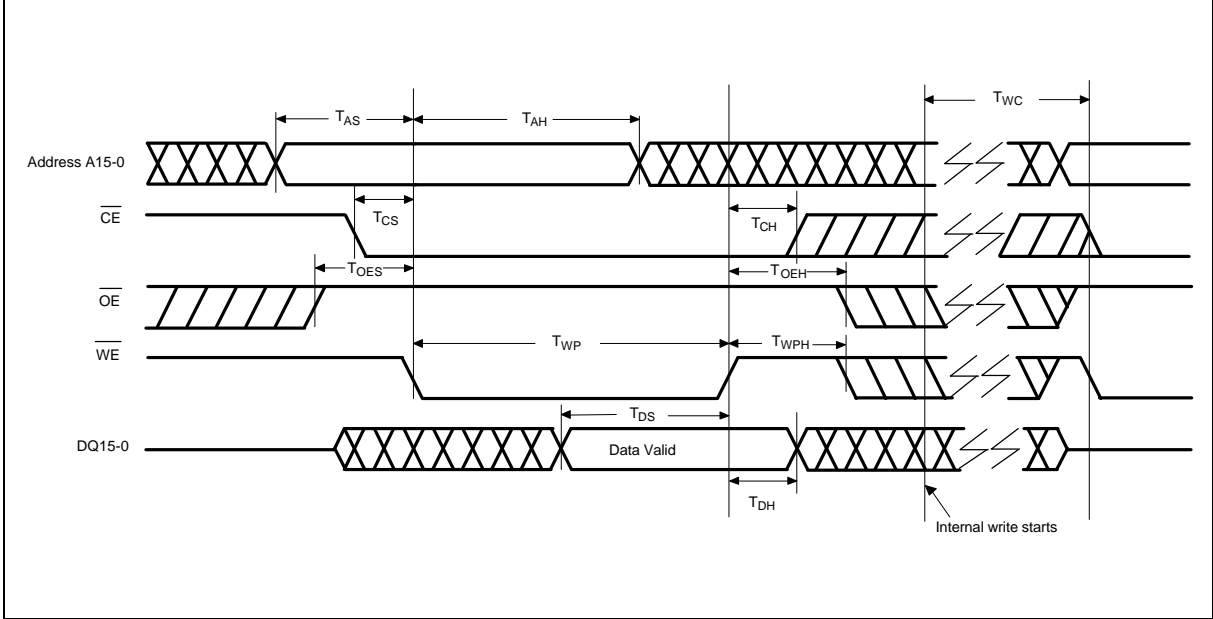


TIMING WAVEFORMS

Read Cycle Timing Diagram



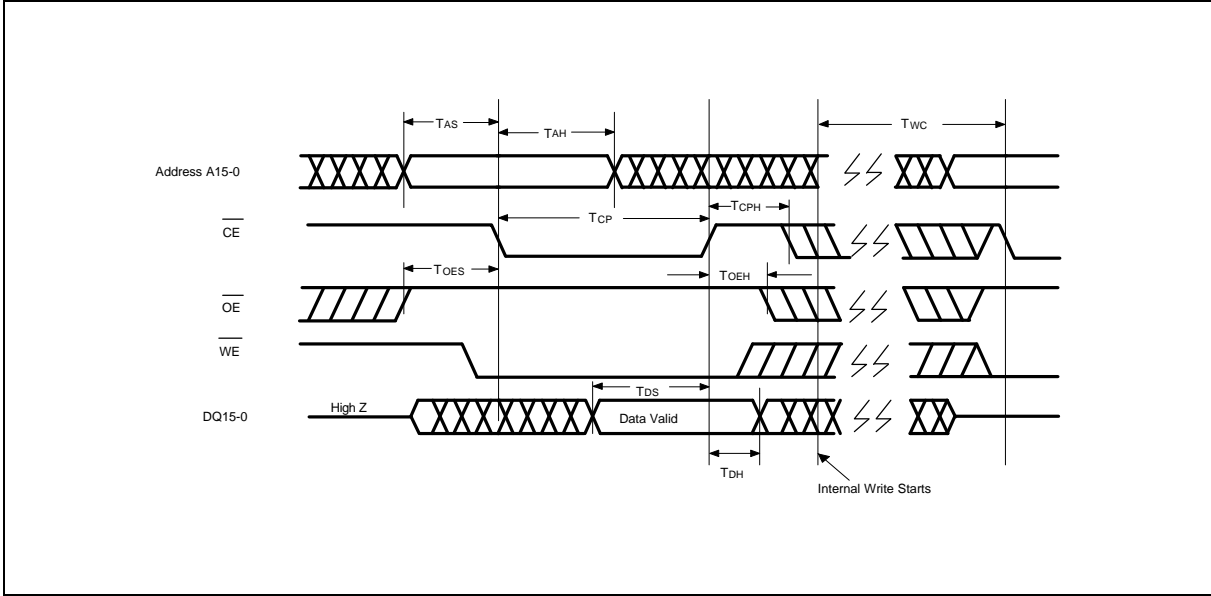
WE Controlled Write Cycle Timing Diagram



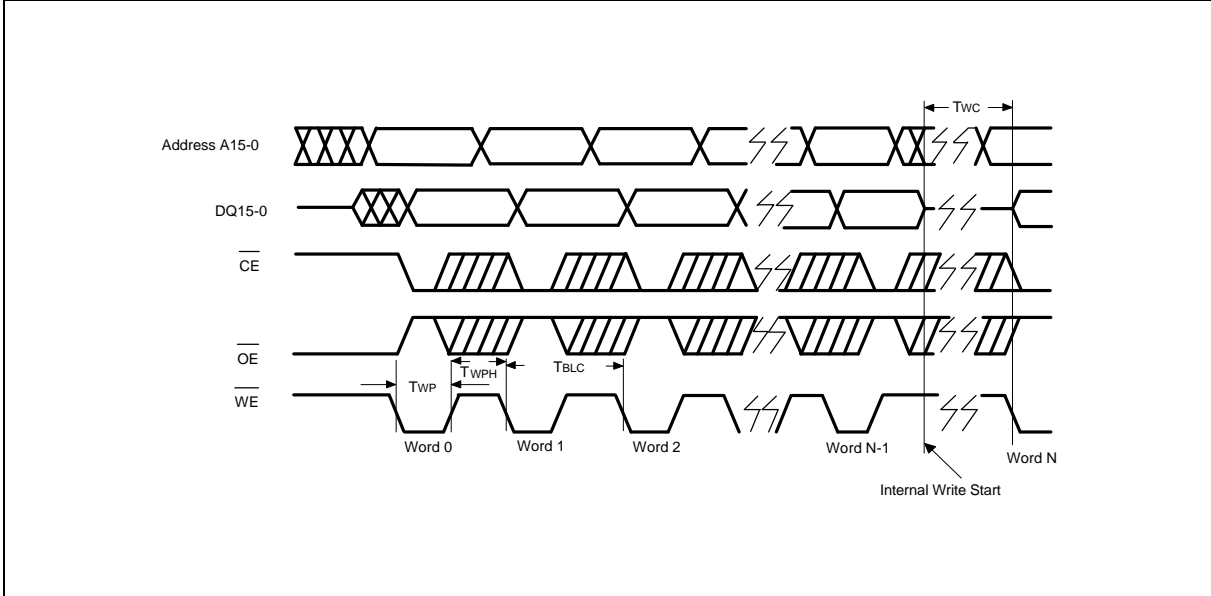


Timing Waveforms, continued

**CE Controlled Write Cycle Timing Diagram**



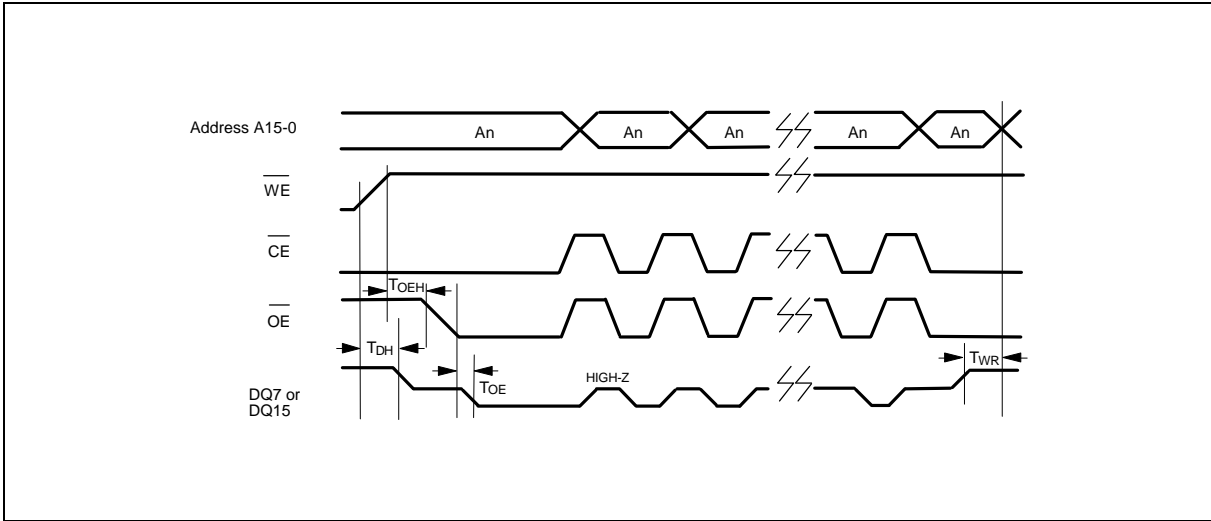
**Page Write Cycle Timing Diagram**



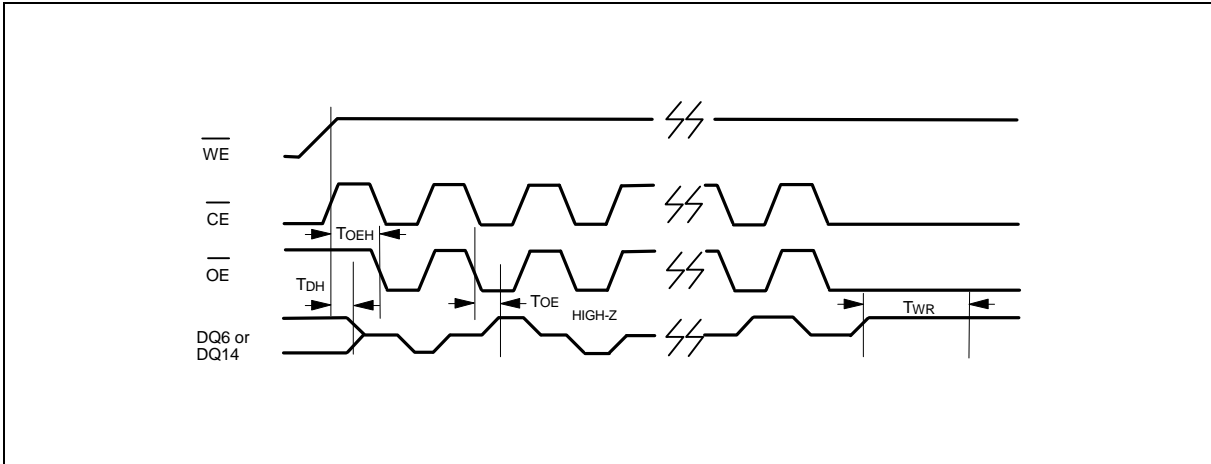


Timing Waveforms, continued

**DATA Polling Timing Diagram**



**Toggle Bit Timing Diagram**



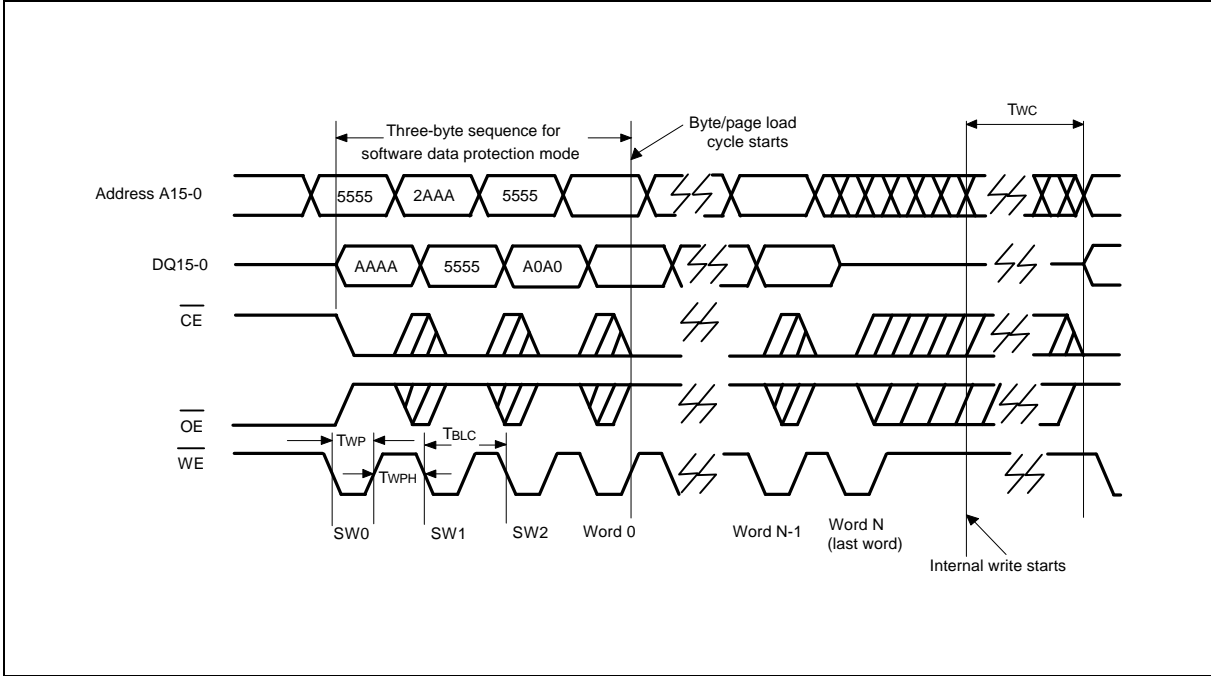
Notes:

- 1. Toggling either  $\overline{OE}$  or  $\overline{CE}$  or both  $\overline{OE}$  and  $\overline{CE}$  will operate toggle bit.
- 2. Beginning and ending state of DQ6 and DQ14 may vary.
- 3. Any address location may be used but the address should not vary.

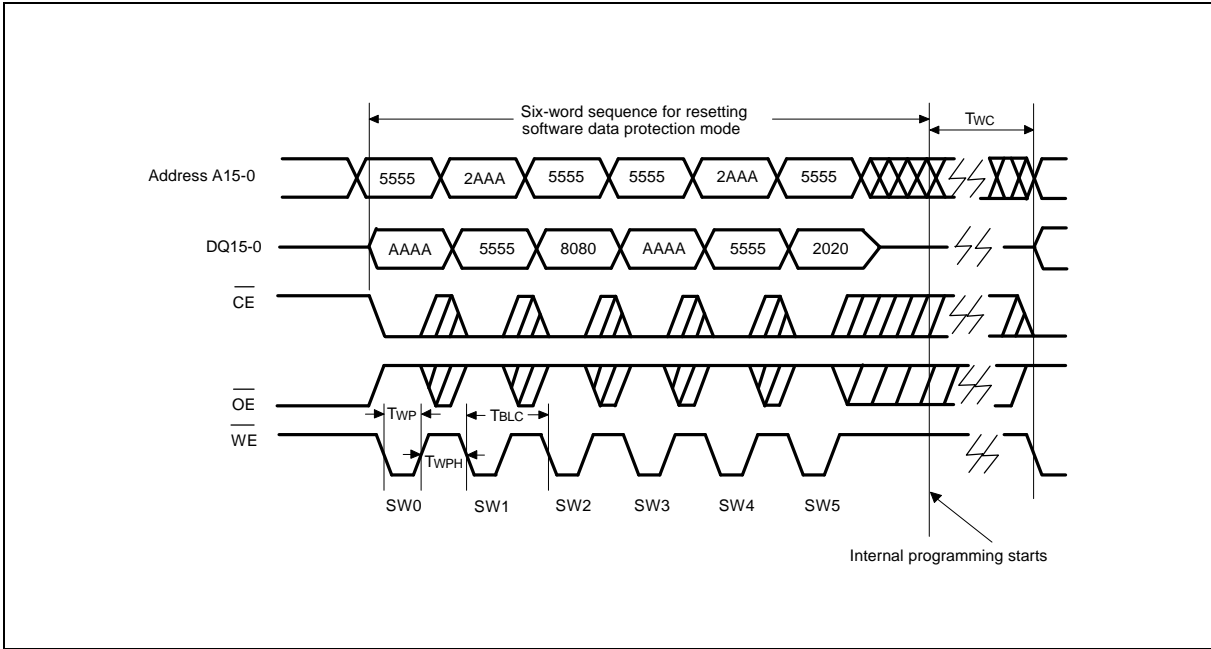


Timing Waveforms, continued

Page Write Timing Diagram Software Data Protection Mode



Reset Software Data Protection Timing Diagram

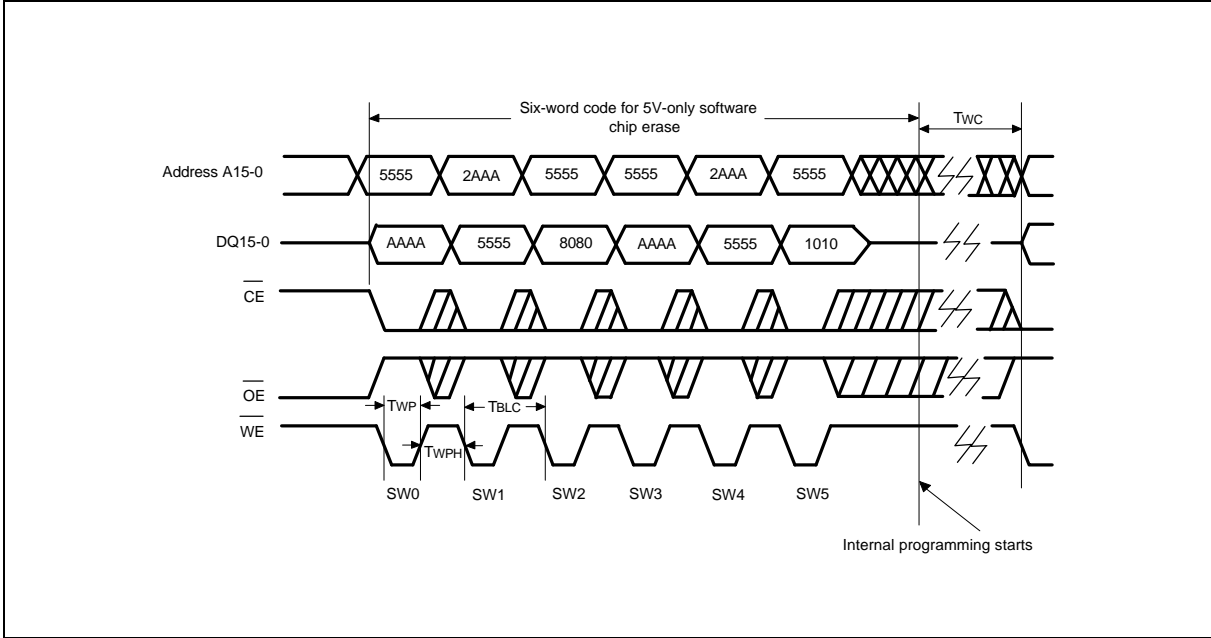






Timing Waveforms, continued

5-Volt-only Software Chip Erase Timing Diagram



# W29C102



## ORDERING INFORMATION

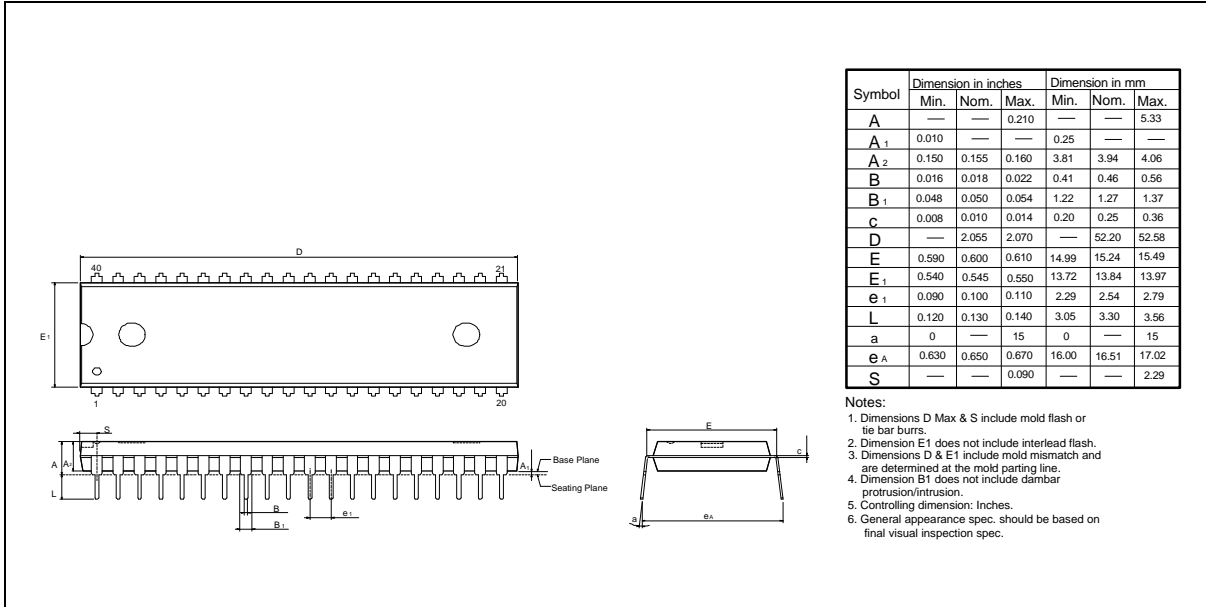
PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY VDD CURRENT MAX. ( $\mu$ A)	PACKAGE	CYCLE
W29C102-70	70	60	200	600 mil DIP	1K
W29C102-90	90	60	200	600 mil DIP	1K
W29C102-12	120	60	200	600 mil DIP	1K
W29C102Q-70	70	60	200	40-pin TSOP (10 mm $\times$ 14 mm)	1K
W29C102Q-90	90	60	200	40-pin TSOP (10 mm $\times$ 14 mm)	1K
W29C102Q-12	120	60	200	40-pin TSOP (10 mm $\times$ 14 mm)	1K
W29C102T-70	70	60	200	40-pin TSOP (10 mm $\times$ 20 mm)	1K
W29C102T-90	90	60	200	40-pin TSOP (10 mm $\times$ 20 mm)	1K
W29C102T-12	120	60	200	40-pin TSOP (10 mm $\times$ 20 mm)	1K
W29C102P-70	70	60	200	44-pin PLCC	1K
W29C102P-90	90	60	200	44-pin PLCC	1K
W29C102P-12	120	60	200	44-pin PLCC	1K
W29C102-70B	70	60	200	600 mil DIP	10K
W29C102-90B	90	60	200	600 mil DIP	10K
W29C102-12B	120	60	200	600 mil DIP	10K
W29C102Q-70B	70	60	200	40-pin TSOP (10 mm $\times$ 14 mm)	10K
W29C102Q-90B	90	60	200	40-pin TSOP (10 mm $\times$ 14 mm)	10K
W29C102Q-12B	120	60	200	40-pin TSOP (10 mm $\times$ 14 mm)	10K
W29C102T-70B	70	60	200	40-pin TSOP (10 mm $\times$ 20 mm)	10K
W29C102T-90B	90	60	200	40-pin TSOP (10 mm $\times$ 20 mm)	10K
W29C102T-12B	120	60	200	40-pin TSOP (10 mm $\times$ 20 mm)	10K
W29C102P-70B	70	60	200	44-pin PLCC	10K
W29C102P-90B	90	60	200	44-pin PLCC	10K
W29C102P-12B	120	60	200	44-pin PLCC	10K

### Notes:

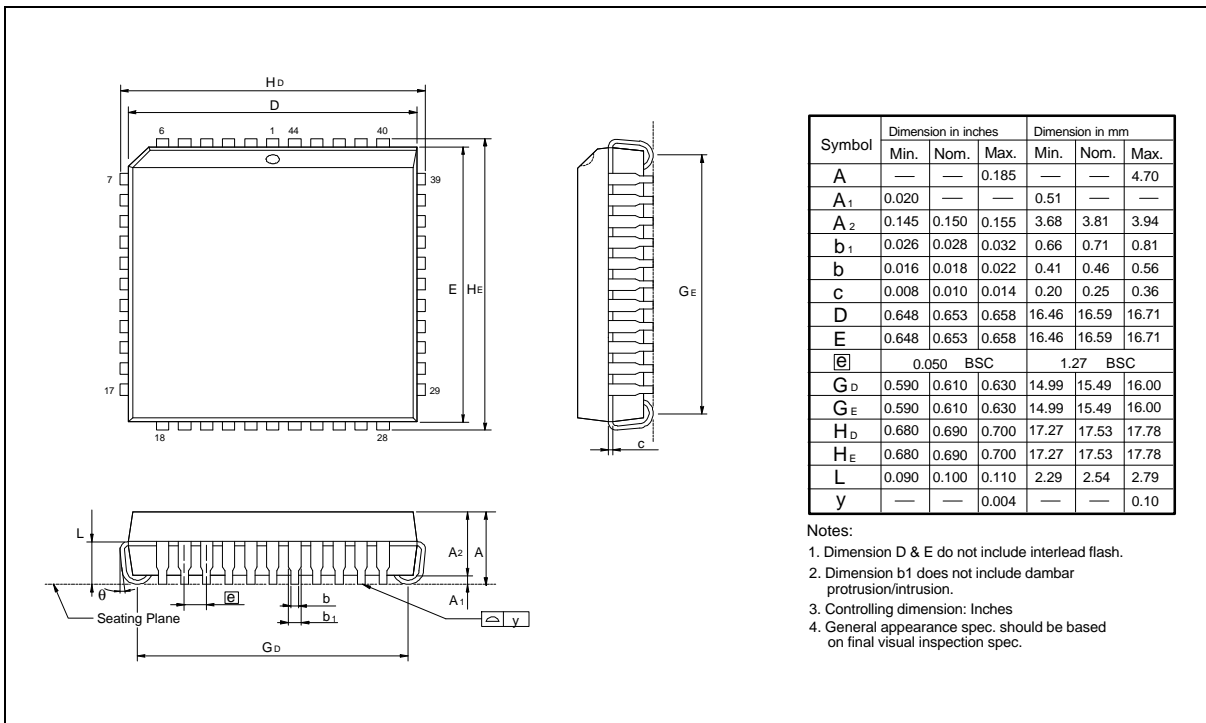
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

## PACKAGE DIMENSIONS

### 40-pin PDIP



### 44-pin PLCC

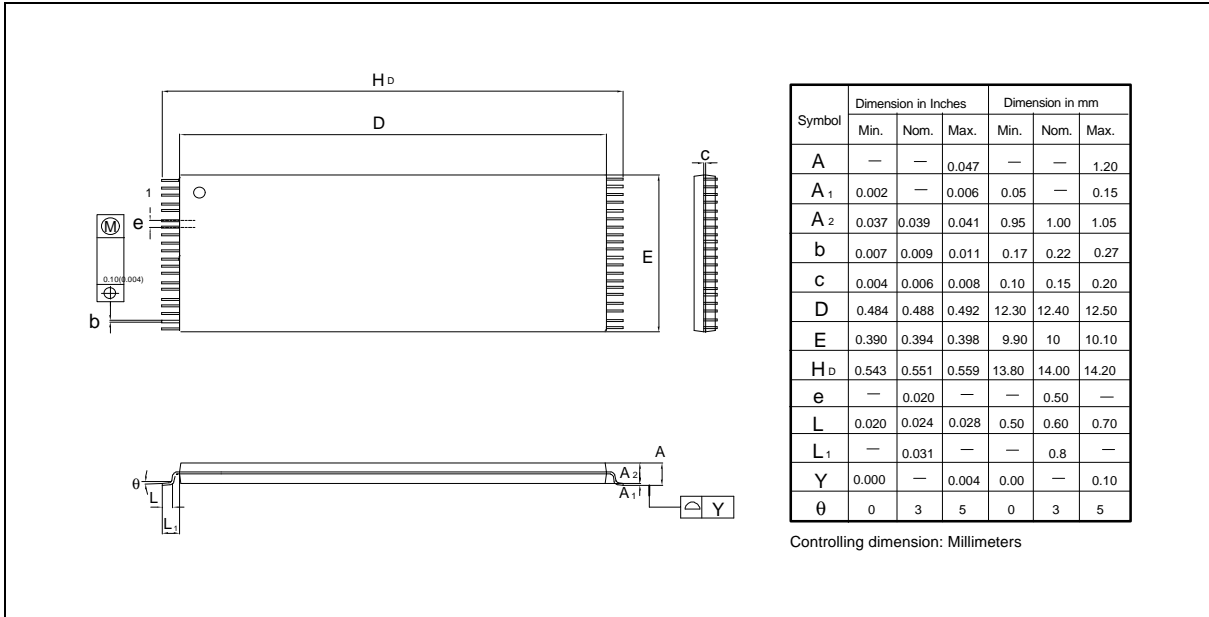


# W29C102

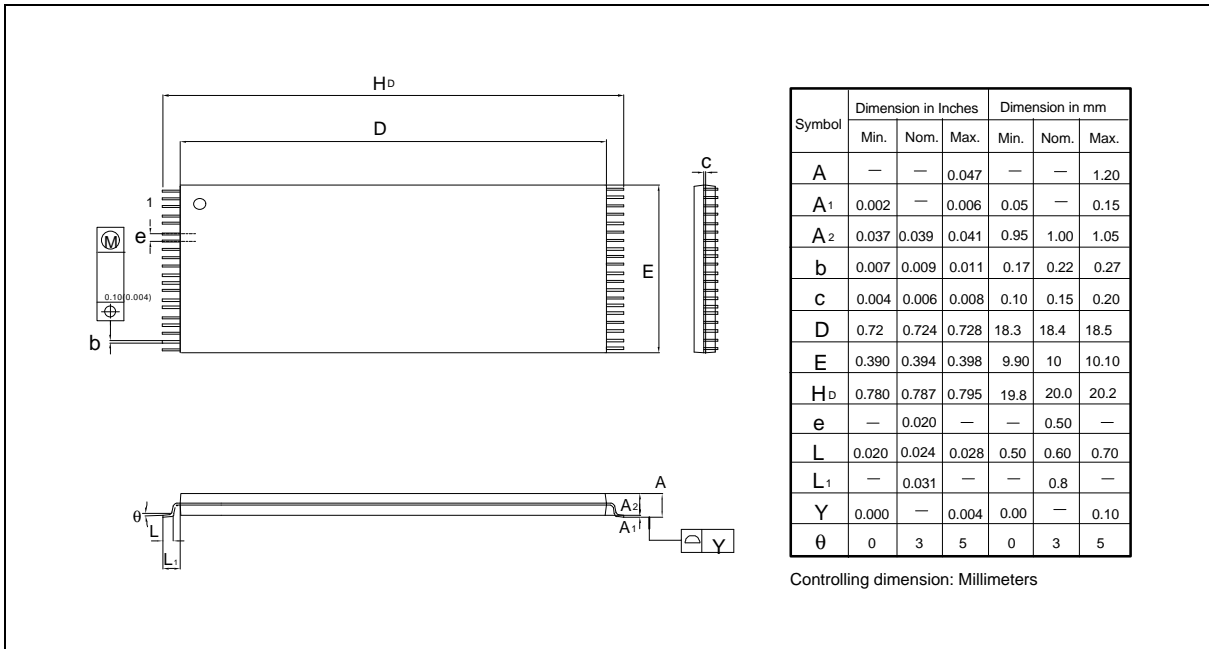


Package Dimensions, continued

## 40-pin TSOP (10 mm × 14 mm)



## 40-pin TSOP (10 mm × 20 mm)





## VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A3	Mar. 1998	6	Add. pause 10 mS
		7	Add. pause 50 mS
		8	Correct the time from 10 mS to 10 $\mu$ S
		11	Change V <sub>DD</sub> from 5% to 10% for 70 nS



### Headquarters

No. 4, Creation Rd. III,  
Science-Based Industrial Park,  
Hsinchu, Taiwan  
TEL: 886-3-5770066  
FAX: 886-3-5796096  
<http://www.winbond.com.tw/>  
Voice & Fax-on-demand: 886-2-27197006

### Taipei Office

11F, No. 115, Sec. 3, Min-Sheng East Rd.,  
Taipei, Taiwan  
TEL: 886-2-27190505  
FAX: 886-2-27197502

### Winbond Electronics (H.K.) Ltd.

Rm. 803, World Trade Square, Tower II,  
123 Hoi Bun Rd., Kwun Tong,  
Kowloon, Hong Kong  
TEL: 852-27513100  
FAX: 852-27552064

### Winbond Electronics North America Corp.

Winbond Memory Lab.  
Winbond Microelectronics Corp.  
Winbond Systems Lab.  
2727 N. First Street, San Jose,  
CA 95134, U.S.A.  
TEL: 408-9436666  
FAX: 408-5441798

Note: All data and specifications are subject to change without notice.