



OKI Semiconductor

MR27T802F

512k-Word × 16-Bit or 1M-Word × 8-Bit P2ROM

FEDR27T802F-02-05

Issue Date: Dec. 28, 2004

FEATURES

- 512k-word × 16-bit / 1M-word × 8-bit electrically switchable configuration
- +2.7 V to 3.6 V power supply
- Access time 80 ns MAX
- Operating current 18 mA MAX(5MHz)
- Standby current 5 μ A MAX
- Input/Output TTL compatible
- Three-state output

PACKAGES

- MR27T802F-xxxTN
48-pin plastic TSOP (TSOP I 48-P-1220-0.50-1K)
- MR27T802F-xxxMA
44-pin plastic SOP (SOP44-P-600-1.27-K)
- MR27T802F-xxxTP
44-pin plastic TSOP (TSOP II 44-P-400-0.80-K)

P2ROM ADVANCED TECHNOLOGY

P2ROM stands for Production Programmed ROM. This exclusive Oki technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing. Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

- **Short lead time**, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
- **No mask charge**, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
- **No additional programming charge**, unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
- **Custom Marking** is available at no additional charge.
- **Pin Compatible with Mask ROM** and some FLASH products.

PIN CONFIGURATION (TOP VIEW)

NC	1	44	NC
A18	2	43	NC
A17	3	42	A8
A7	4	41	A9
A6	5	40	A10
A5	6	39	A11
A4	7	38	A12
A3	8	37	A13
A2	9	36	A14
A1	10	35	A15
A0	11	34	A16
CE#	12	33	BYTE#
Vss	13	32	Vss
OE#	14	31	D15/A-1
D0	15	30	D7
D8	16	29	D14
D1	17	28	D6
D9	18	27	D13
D2	19	26	D5
D10	20	25	D12
D3	21	24	D4
D11	22	23	Vcc

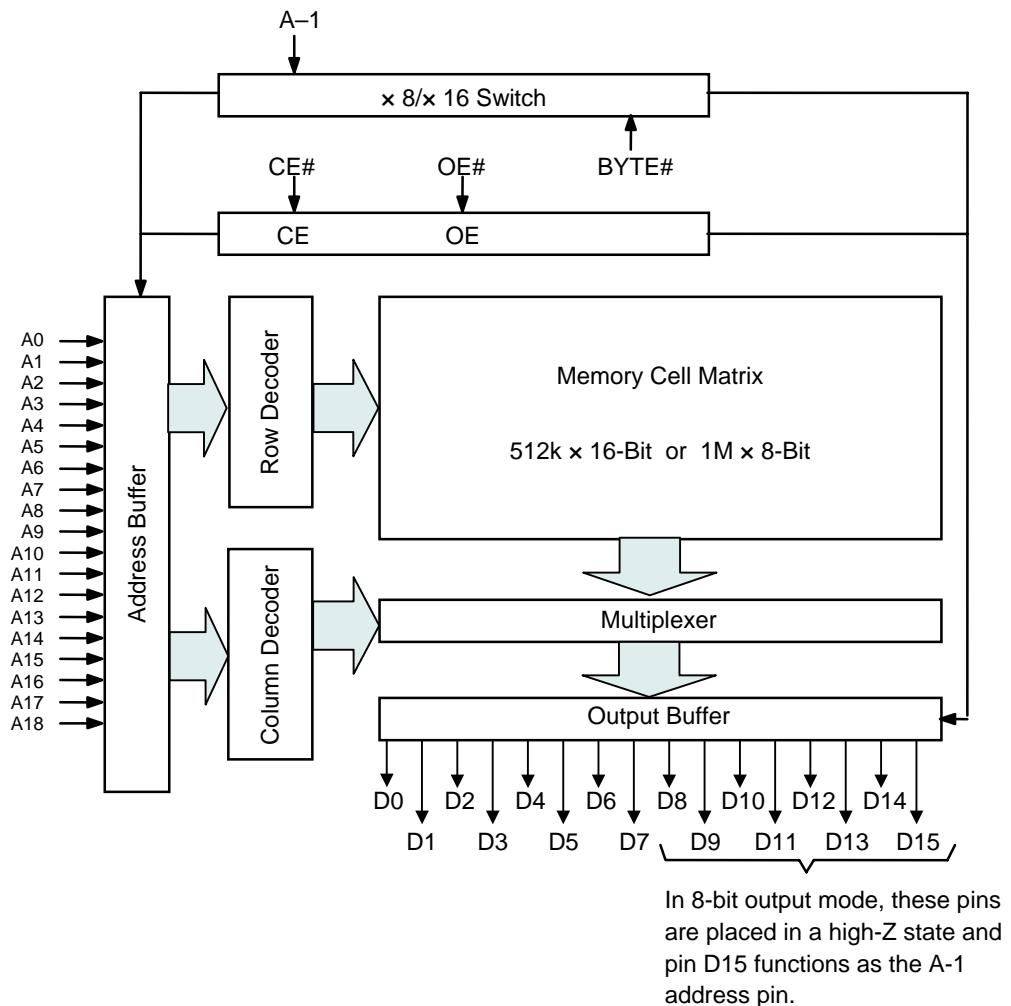
44SOP,
44TSOP(Type-II)

A15	1	48	A16
A14	2	47	BYTE#
A13	3	46	Vss
A12	4	45	D15/A-1
A11	5	44	D7
A10	6	43	D14
A9	7	42	D6
A8	8	41	D13
NC	9	40	D5
NC	10	39	D12
NC	11	38	D4
NC	12	37	Vcc
NC	13	36	D11
NC	14	35	D3
NC	15	34	D10
A18	16	33	D2
A17	17	32	D9
A7	18	31	D1
A6	19	30	D8
A5	20	29	D0
A4	21	28	OE#
A3	22	27	Vss
A2	23	26	CE#
A1	24	25	A0

48TSOP(Type-I)



BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin name	Functions
D15 / A-1	Data output / Address input
A0 to A18	Address inputs
D0 to D14	Data outputs
CE#	Chip enable input
OE#	Output enable input
BYTE#	Word / Byte select input
V _{CC}	Power supply voltage
V _{SS}	Ground
NC	No connect

FUNCTION TABLE

Mode	CE#	OE#	BYTE#	V _{CC}	D0 to D7	D8 to D14	D15/A-1
Read (16-Bit)	L	L	H	3.0V	D _{OUT}		
Read (8-Bit)	L	L	L		D _{OUT}	Hi-Z	L/H
Output disable	L	H	H		Hi-Z	*	
			L				
Standby	H	*	H		Hi-Z	*	
			L				

*: Don't Care (H or L)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T _a	—	0 to 70	°C
Storage temperature	T _{stg}		-55 to 125	°C
Input voltage	V _I	relative to V _{SS}	-0.5 to V _{CC} +0.5	V
Output voltage	V _O		-0.5 to V _{CC} +0.5	V
Power supply voltage	V _{CC}		-0.5 to 5	V
Power dissipation per package	P _D	T _a = 25°C	1.0	W
Output short circuit current	I _{OS}	—	10	mA

RECOMMENDED OPERATING CONDITIONS

(T_a = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V _{CC} power supply voltage	V _{CC}	V _{CC} = 2.7 to 3.6 V	2.7	—	3.6	V
Input "H" level	V _{IH}		2.2	—	V _{CC} +0.5*	V
Input "L" level	V _{IL}		-0.5**	—	0.6	V

Voltage is relative to V_{SS}.*: V_{CC}+1.5V(Max.) when pulse width of overshoot is less than 10ns.

**: -1.5V(Min.) when pulse width of undershoot is less than 10ns.

PIN CAPACITANCE

(V_{CC} = 3.3 V, T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C _{IN1}	V _I = 0 V	—	—	8	pF
BYTE#	C _{IN2}		—	—	100	
Output	C _{OUT}	V _O = 0 V	—	—	10	

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V _{CC} = 2.7 V to 3.6 V, Ta = 0 to 70°C)						
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I _{LI}	V _I = 0 to V _{CC}	—	—	5	μA
Output leakage current	I _{LO}	V _O = 0 to V _{CC}	—	—	5	μA
V _{CC} power supply current (Standby)	I _{CCSC}	CE# = V _{CC}	—	—	5	μA
	I _{CCST}	CE# = V _{IH}	—	—	1	mA
V _{CC} power supply current (Read)	I _{CCA}	CE# = V _{IL} , OE# = V _{IH} tc = 200 ns	—	—	18	mA
Input "H" level	V _{IH}	—	2.2	—	V _{CC} +0.5*	V
Input "L" level	V _{IL}	—	-0.5**	—	0.6	V
Output "H" level	V _{OH}	I _{OH} = -1 mA	2.4	—	—	V
Output "L" level	V _{OL}	I _{OL} = 2 mA	—	—	0.4	V

Voltage is relative to VSS.

* : V_{CC}+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

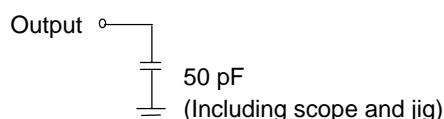
AC Characteristics

(V _{CC} = 2.7 V to 3.6 V, Ta = 0 to 70°C)					
Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	t _C	—	80	—	ns
Address access time	t _{ACC}	CE# = OE# = V _{IL}	—	80	ns
CE# access time	t _{CE}	OE# = V _{IL}	—	80	ns
OE# access time	t _{OE}	CE# = V _{IL}	—	30	ns
Output disable time	t _{CHZ}	OE# = V _{IL}	0	20	ns
	t _{TOHZ}	CE# = V _{IL}	0	20	ns
Output hold time	t _{OH}	CE# = OE# = V _{IL}	0	—	ns

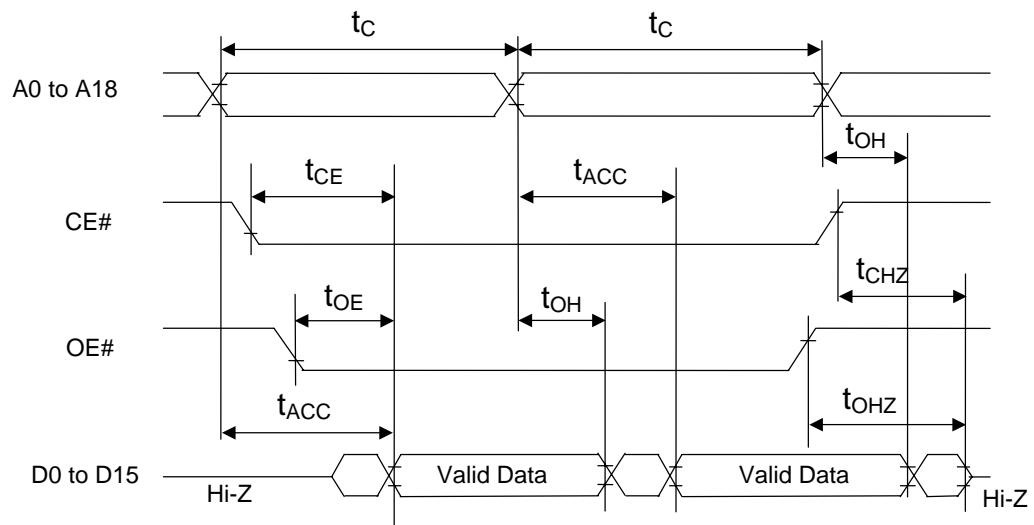
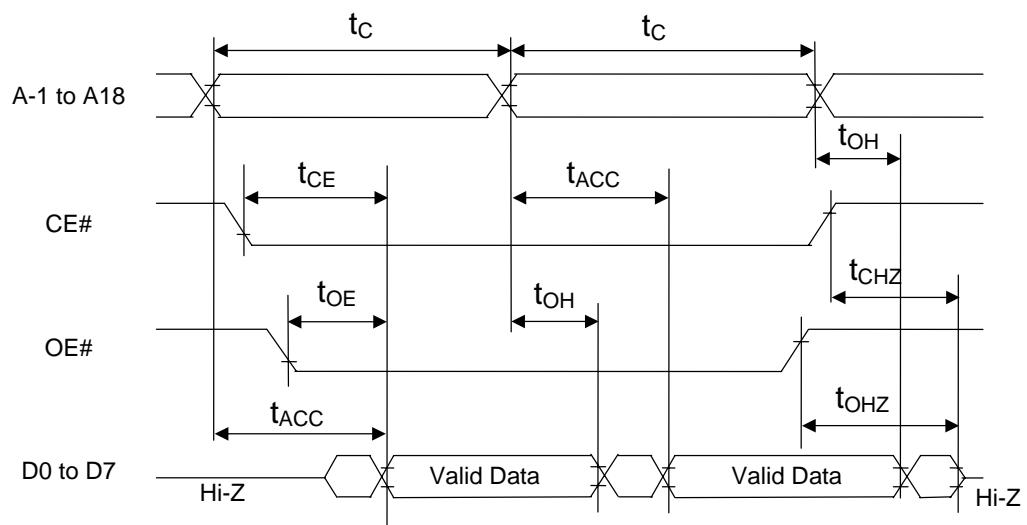
Measurement conditions

Input signal level ----- 0 V/3 V
 Input timing reference level ----- 1/2V_{CC}
 Output load ----- 50 pF
 Output timing reference level ----- 1/2V_{CC}

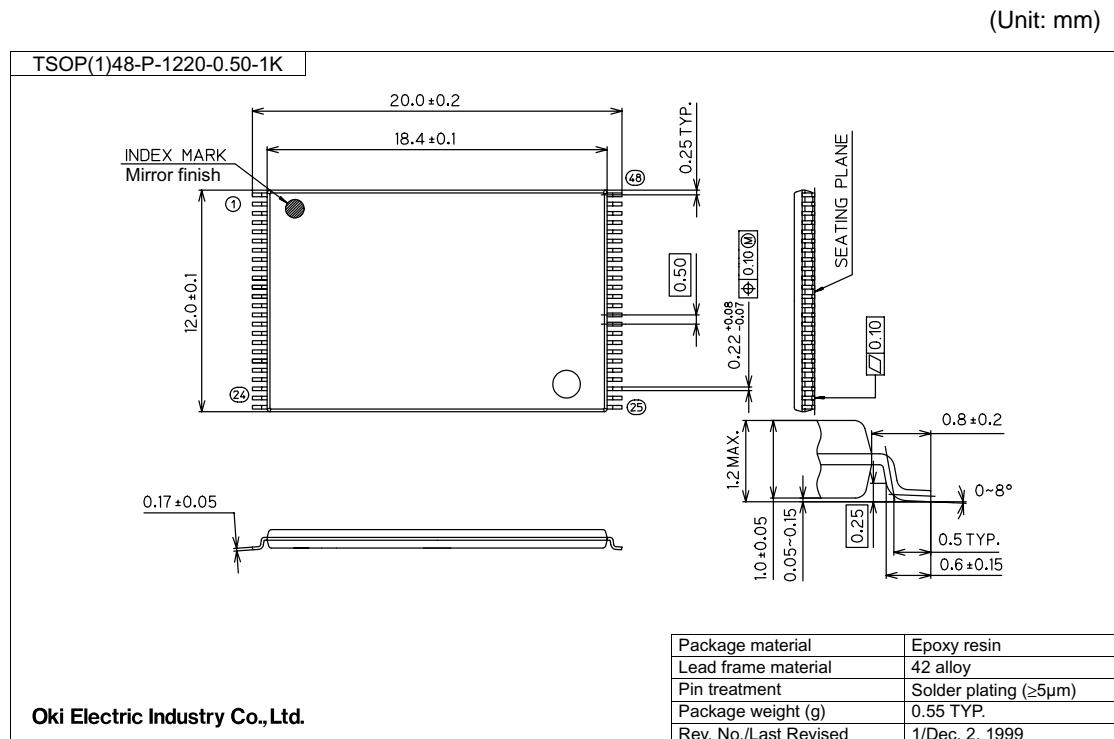
Output load



TIMING CHART (READ CYCLE)

16-Bit Read Mode (BYTE# = V_{IL})8-Bit Read Mode (BYTE# = V_{IL})

PACKAGE DIMENSIONS

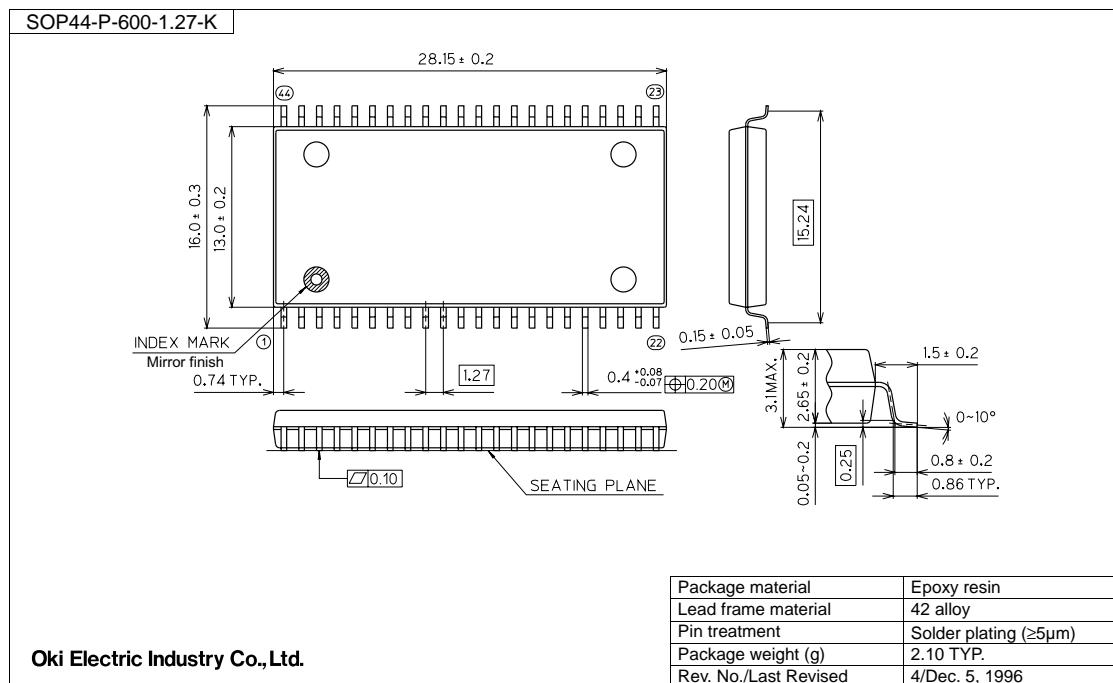


Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit: mm)

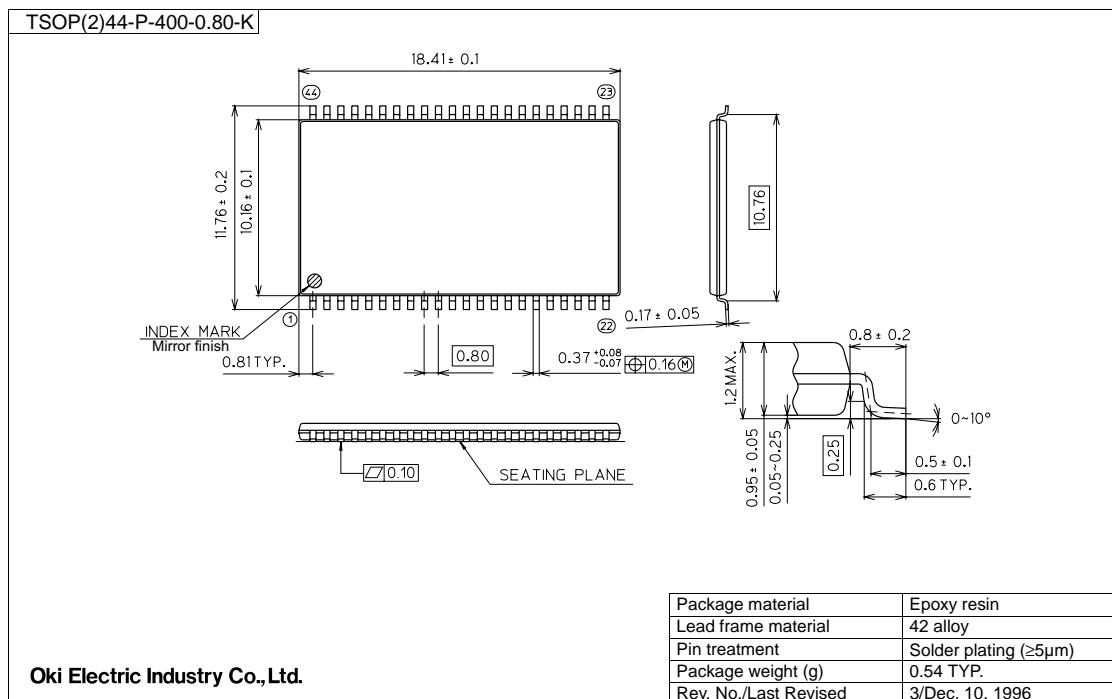


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REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR27T802F-02-01	Dec., 2002	–	–	Final edition 1
FEDR27T802F-02-02	Jun. 17, 2003	3, 4	3, 4	Change Operating temperature under bias (Ta) to 0 to 70°C.
FEDR27T802F-02-03	Jul. 9, 2004	3	3	Add P_D condition and $I_{OS} = 10mA$
FEDR27T802F-02-04	Sep. 3, 2004	1	1, 7	Add MR27T802F-xxxMA
FEDR27T802F-02-05	Dec. 28, 2004	1	1, 8	Add MR27T802F-xxxTP

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