



Integrated
Circuit
Systems, Inc.

ICS843001I-22

FEMTOCLOCKS™ CRYSTAL/LVCMOS-TO-3.3V, 2.5V LVPECL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The ICS843001I-22 is a highly versatile, low phase noise LVPECL/LVCMOS Synthesizer which can generate low jitter reference clocks for a variety of communications applications and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. The dual crystal interface allows the synthesizer to support up to two communications standards in a given application (i.e. 1Gb Ethernet with a 25MHz crystal and 1Gb Fibre Channel using a 25.5625MHz crystal). The rms phase jitter performance is typically less than 1ps, thus making the device acceptable for use in demanding applications such as OC48 SONET and 10Gb Ethernet. The ICS843001I-22 is packaged in a small 24-pin TSSOP package.

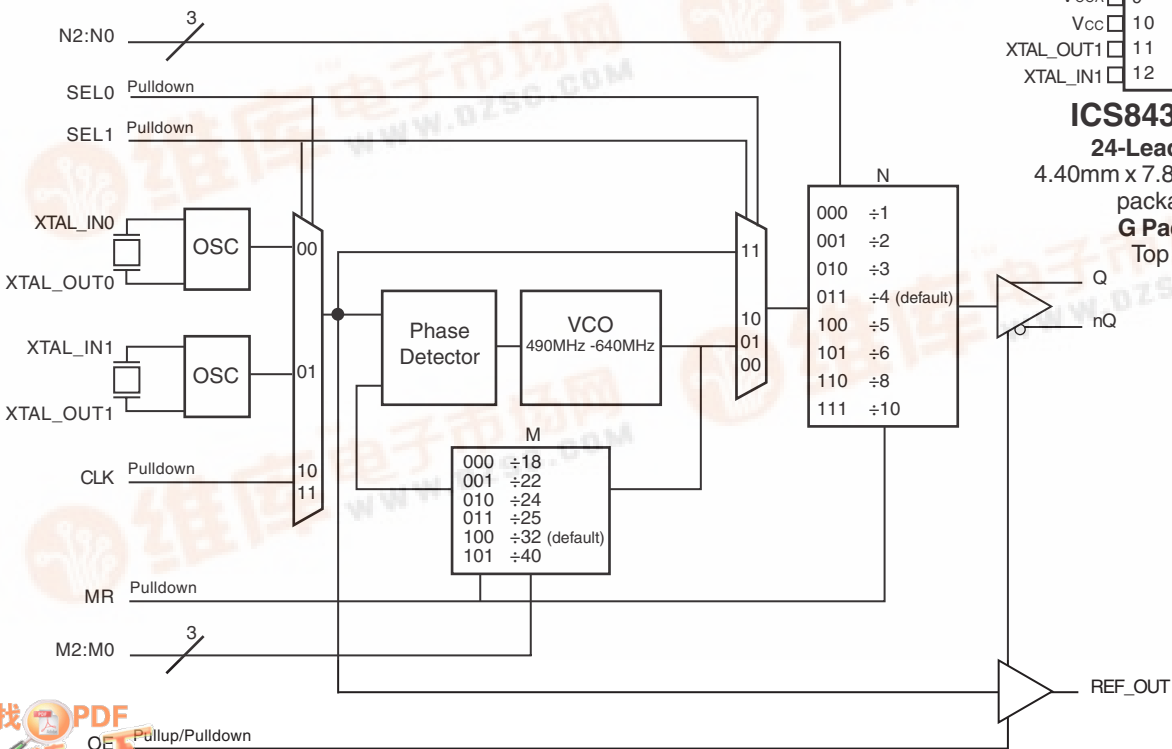
FEATURES

- One 3.3V or 2.5V LVPECL output pair and one LVCMOS/LVTTL output
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 490MHz - 640MHz
- Output frequency range: 490MHz - 640MHz
- Supports the following applications: SONET, Ethernet, Fibre Channel, Serial ATA, and HDTV
- RMS phase jitter @ 125MHz (1.875MHz - 20MHz): 0.5ps (typical)
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in both, Standard and RoHS/Lead-Free compliant packages

CONTROL INPUT FUNCTION TABLE

Control Input	Outputs	
OE	Q/nQ	REF_OUT
0	High-Z	High-Z
1	High-Z	Active
FLOAT	Active	High-Z

BLOCK DIAGRAM



PIN ASSIGNMENT

VCCO_LVCMOS	1	24	REF_OUT
N0	2	23	VEE
N1	3	22	OE
N2	4	21	M2
VCCO_LVPECL	5	20	M1
Q	6	19	M0
nQ	7	18	MR
VEE	8	17	SEL1
VCCA	9	16	SEL0
VCC	10	15	CLK
XTAL_OUT1	11	14	XTAL_IN0
XTAL_IN1	12	13	XTAL_OUT0

ICS843001I-22

24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View

000	÷1
001	÷2
010	÷3
011	÷4 (default)
100	÷5
101	÷6
110	÷8
111	÷10



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TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 5	V_{CC0_LVCMOS} , V_{CC0_LVPECL}	Power		Output supply pins.
2, 3	N0, N1	Input	Pullup	Output divider select pins. Default value = ÷4. LVCMOS/LVTTL interface levels. See Table 3C.
4	N2	Input	Pulldown	
6, 7	Q, nQ	Output		Differential output pair. LVPECL interface levels.
8, 23	V_{EE}	Power		Negative supply pin.
9	V_{CCA}	Power		Analog supply pin.
10	V_{CC}	Power		Core supply pin.
11 12	XTAL_OUT1, XTAL_IN1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
13 14	XTAL_OUT0, XTAL_IN0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
15	CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
16, 17	SEL0, SEL1	Input	Pulldown	Input MUX select pins. LVCMOS/LVTTL interface levels. See Table 3D.
18	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q to go low and the inverted output nQ to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
19, 20	M0, M1	Input	Pulldown	Feedback divider select pins. Default value = ÷32. LVCMOS/LVTTL interface levels. See Table 3B.
21	M2	Input	Pullup	
22	OE	Input		3-State clock output enable, (High/Low/Float). See page 1, Control Input Function Table.
24	REF_OUT	Output		Reference clock output. LVCMOS/LVTTL interface levels.

NOTE: *Pulldown and Pullup* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULDDOWN}$	Input Pulldown Resistor			51		k Ω
R_{PULLUP}	Input Pullup Resistor			51		k Ω
R_{out}	Output Impedance	REF_CLK		15		Ω



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TABLE 3A. COMMON CONFIGURATIONS TABLE

Input Reference Clock (MHz)	M Divider Value	N Divider Value	VCO (MHz)	Output Frequency (MHz)	Application
27	22	8	594	74.25	HDTV
22.4	25	8	560	70	
24.75	24	8	594	74.25	HDTV
25	24	3	600	200	Processor
14.8351649	40	8	593.4066	74.1758245	HDTV
19.44	32	4	622.08	155.52	SONET
19.44	32	8	622.08	77.76	SONET
19.44	32	1	622.08	622.08	SONET
19.44	32	2	622.08	311.04	SONET
19.53125	32	4	625	156.25	10 GigE
20	25	2	500	250	Ethernet
25	25	5	625	125	1 GigE
25	25	10	625	62.5	1 GigE
25	24	6	600	100	PCI Express
25	24	4	600	150	SATA
25	24	8	600	75	SATA
26.5625	24	6	637.5	106.25	Fibre Channel 1
26.5625	24	3	637.5	212.5	4 Gig Fibre Channel
26.5625	24	4	637.5	159.375	10 Gig Fibre Channel
31.25	18	3	562.5	187.5	12 Gig Ethernet

TABLE 3B. PROGRAMMABLE M OUTPUT DIVIDER
FUNCTION TABLE

Inputs			M Divider Value	Input Frequency (MHz)	
M2	M1	M0		Minimum	Maximum
0	0	0	18	27.22	35.56
0	0	1	22	22.27	29.09
0	1	0	24	20.41	26.67
0	1	1	25	19.6	25.6
1	0	0	32	15.31	20
1	0	1	40	12.25	16

TABLE 3C. PROGRAMMABLE N OUTPUT DIVIDER
FUNCTION TABLE

Inputs			N Divide Value
N2	N1	N0	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4 (default)
1	0	0	5
1	0	1	6
1	1	0	8
1	1	1	10

TABLE 3D. BYPASS MODE FUNCTION TABLE

Inputs		Reference Input	PLL Mode
SEL1	SEL0		
0	0	XTAL0	Active
0	1	XTAL1	Active
1	0	CLK	Active
1	1	CLK	Bypass



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_i	-0.5V to $V_{CC} + 0.5V$
Outputs, I_o (LVPECL)	
Continuous Current	50mA
Surge Current	100mA
Outputs, V_o (LVCMOS)	-0.5V to $V_{CCO} + 0.5V$
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO_LVCMOS}, V_{CCO_LVPECL} = 3.3V \pm 10\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.97	3.3	3.63	V
V_{CCA}	Analog Supply Voltage		2.97	3.3	3.63	V
$V_{CCO_LVPECL},$ V_{CCO_LVCMOS}	Output Supply Voltage		2.97	3.3	3.63	V
I_{EE}	Power Supply Current				160	mA
I_{CCO}	Output Supply Current				8	mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO_LVCMOS}, V_{CCO_LVPECL} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		2.375	2.5	2.625	V
$V_{CCO_LVPECL},$ V_{CCO_LVCMOS}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				155	mA
I_{CCO}	Output Supply Current				8	mA



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TABLE 4C. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO_LVCMOS} = 3.3V \pm 10\%$ OR $2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	$V_{CC} = 3.3V \pm 10\%$	2		$V_{CC} + 0.3$	V
		$V_{CC} = 2.5V \pm 5\%$	1.7		$V_{CC} + 0.3$	V
V_{IM}	Input Medium Voltage					V
						V
V_{IL}	Input Low Voltage	$V_{CC} = 3.3V \pm 10\%$	-0.3		0.8	V
		$V_{CC} = 2.5V \pm 5\%$	-0.3		0.7	V
I_{IH}	Input High Current	CLK, SEL0, SEL1, MR, M0, M1, N2, OE $V_{CC} = V_{IN} = 3.63V$ or 2.625V			150	μA
		M2, N0, N1 $V_{CC} = V_{IN} = 3.63V$ or 2.625V			5	μA
I_{IM}	Input Medium Current					μA
I_{IL}	Input Low Current	CLK, SEL0, SEL1, MR, M0, M1, N2, OE $V_{CC} = 3.63V$ or 2.625V, $V_{IN} = 0V$	-5			μA
		M2, N0, N1, OE $V_{CC} = 3.63V$ or 2.625V, $V_{IN} = 0V$	-150			μA
V_{OH}	Output High Voltage; NOTE 1	$V_{CCO_LVCMOS} = 3.63V$	2.6			V
		$V_{CCO_LVCMOS} = 2.625V$	1.8			V
V_{OL}	Output Low Voltage: Note 1	$V_{CCO_LVCMOS} = 3.63V$ or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO_LVCMOS}/2$. See Parameter Measurement Information Section, "Output Load Test Circuit Diagram".

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO_LVPECL} = 3.3V \pm 10\%$ OR $2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

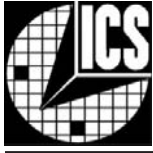
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO_LVPECL} - 2V$.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			MHz
Frequency		14		35.55	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.



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TABLE 6. INPUT FREQUENCY CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO_LVCMOS}, V_{CCO_LVPECL} = 3.3V \pm 10\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
f_{IN}	Input Frequency	CLK	SEL1 = 1, SEL0 = 0	14		35.55	MHz
			SEL1 = 1, SEL0 = 0	DC		250	MHz

TABLE 7A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO_LVCMOS}, V_{CCO_LVPECL} = 3.3V \pm 10\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
f_{OUT}	Output Frequency		49		640	MHz	
$f_{jit}(\emptyset)$	RMS Phase Jitter, (Random); NOTE 1	125MHz (1.875MHz - 20MHz)		0.5		ps	
f_{VCO}	PLL VCO Lock Range		490		640	MHz	
t_R / t_F	Output Rise/Fall Time	Q/nQ	20% to 80%		200	500	ps
		REF_OUT		200	700	ps	
odc	Output Duty Cycle	Q/nQ			45	55	%
		REF_OUT	$f \leq 250\text{MHz}$		44	56	%

NOTE 1: Phase jitter using a crystal interface.

TABLE 7B. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO_LVCMOS}, V_{CCO_LVPECL} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
f_{OUT}	Output Frequency		49		640	MHz	
$f_{jit}(\emptyset)$	RMS Phase Jitter, (Random); NOTE 1	125MHz (1.875MHz - 20MHz)		0.5		ps	
f_{VCO}	PLL VCO Lock Range		490		640	MHz	
t_R / t_F	Output Rise/Fall Time	Q/nQ	20% to 80%		200	500	ps
		REF_OUT		300	800	ps	
odc	Output Duty Cycle	Q/nQ			45	55	%
		REF_OUT	$f \leq 250\text{MHz}$		44	56	%

NOTE 1: Phase jitter using a crystal interface.

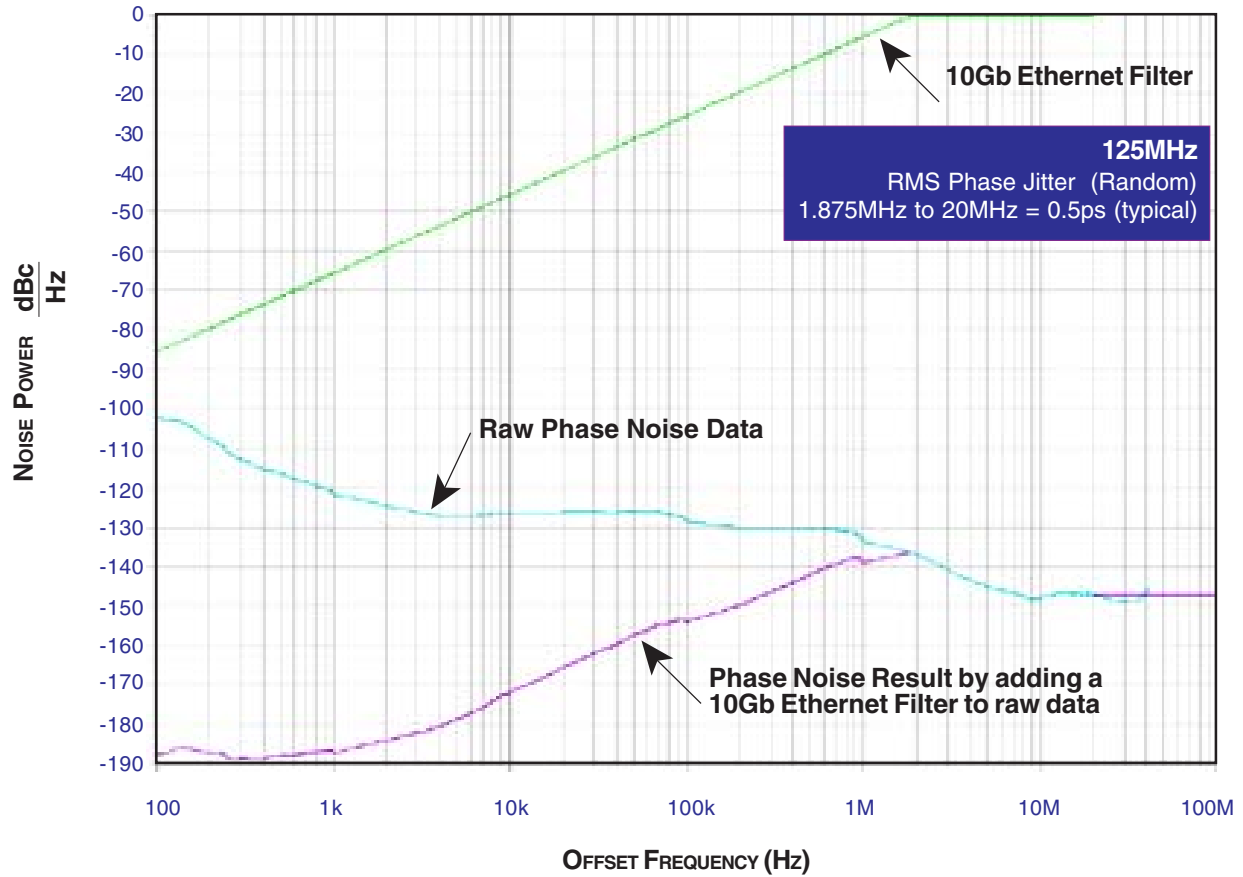


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3.3V, 2.5V LVPECL FREQUENCY SYNTHESIZER

TYPICAL PHASE NOISE AT 125MHz



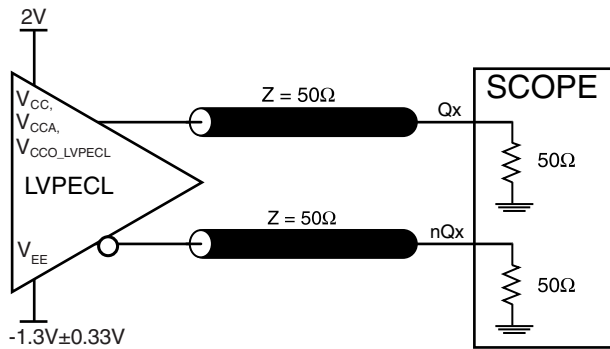


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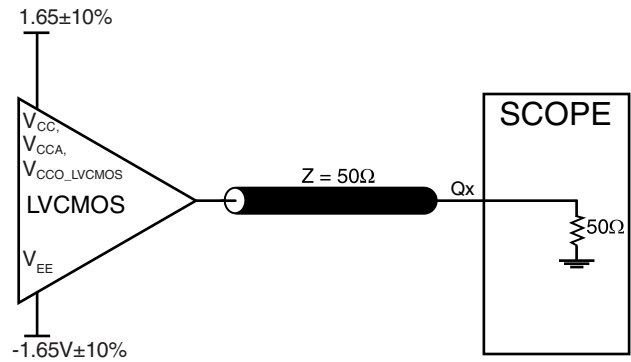
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FEMTOCLOCKS™ CRYSTAL/LVCMOS-TO-3.3V, 2.5V LVPECL FREQUENCY SYNTHESIZER

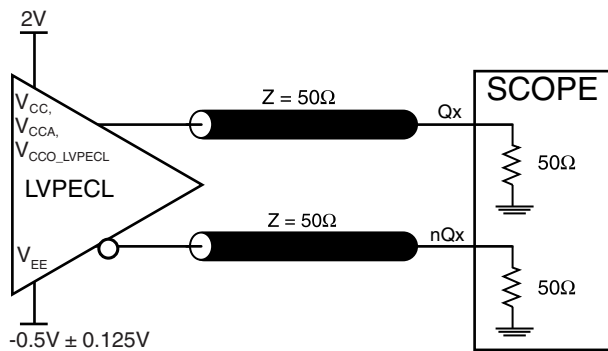
PARAMETER MEASUREMENT INFORMATION



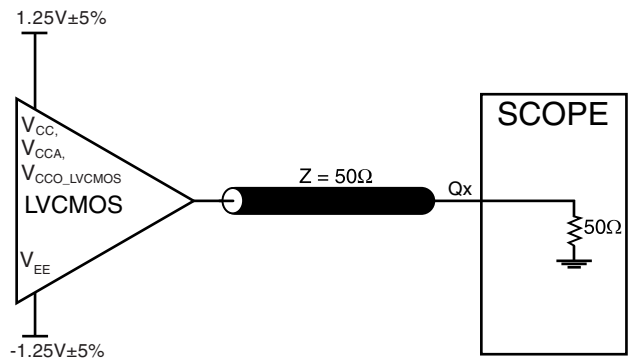
3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT



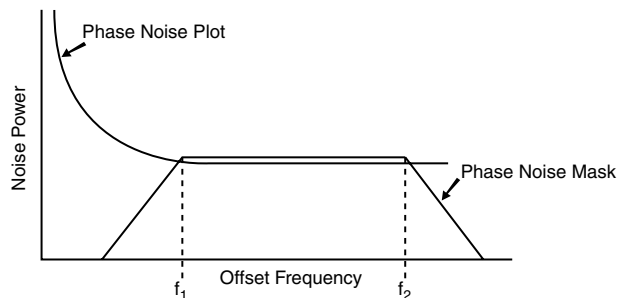
3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



2.5V LVPECL OUTPUT LOAD AC TEST CIRCUIT

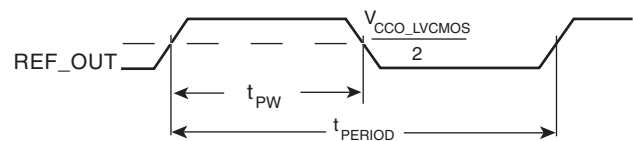


2.5V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



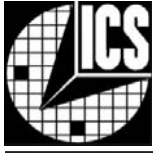
$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

RMS PHASE JITTER



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

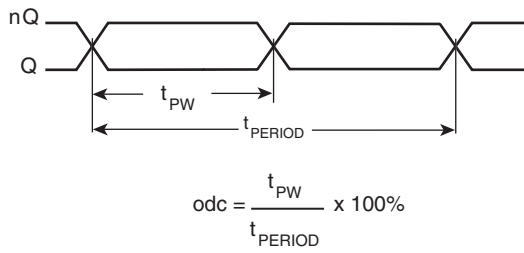
LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



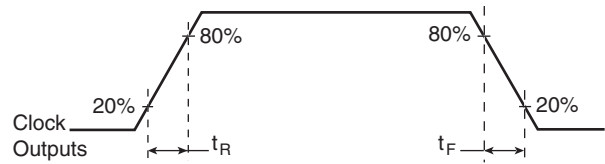
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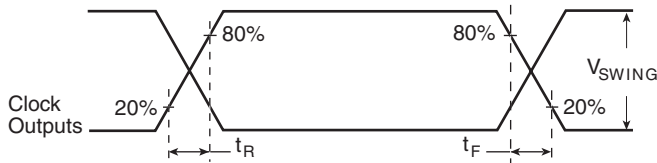
FEMTOCLOCKS™ CRYSTAL/LVCMOS-TO-
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LVPECL OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



LVCMOS OUTPUT RISE/FALL TIME



LVPECL OUTPUT RISE/FALL TIME



APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843001I-22 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} , V_{CCA} , and V_{CCO_x} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu F$ and a $.01\mu F$ bypass capacitor should be connected to each V_{CCA} .

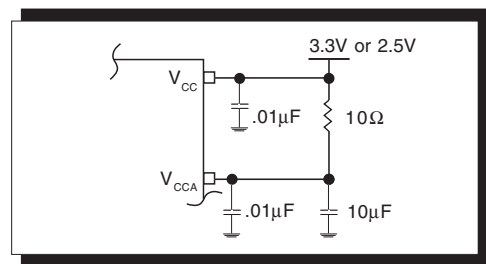


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843001I-22 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2*

below were determined using a 26.5625MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

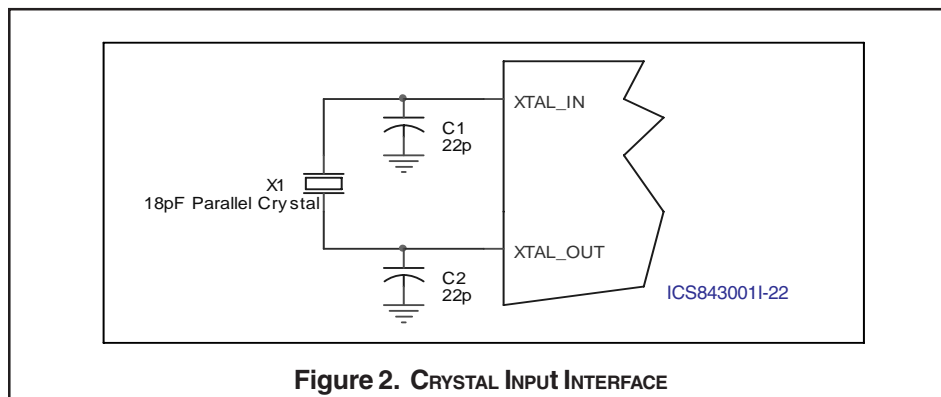


Figure 2. CRYSTAL INPUT INTERFACE



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RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK INPUT:

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

LVPEECL OUTPUT

All unused LVPEECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPEECL OUTPUT

The clock layout topology shown below is a typical termination for LVPEECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPEECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These

outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

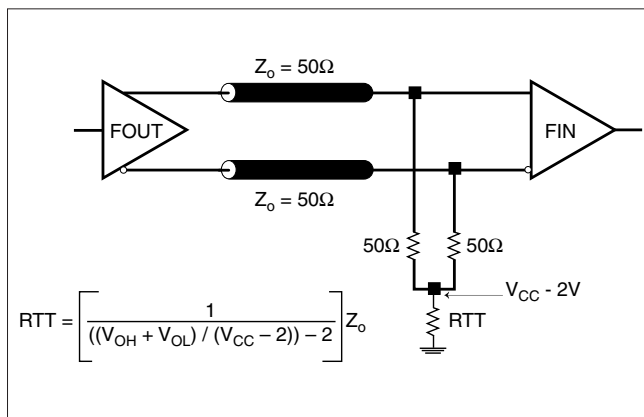


FIGURE 3A. LVPEECL OUTPUT TERMINATION

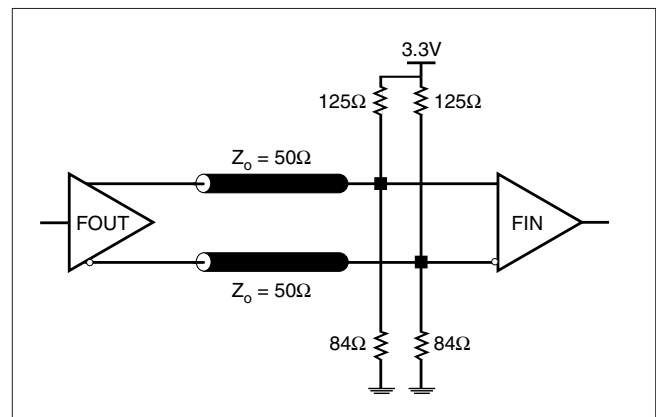
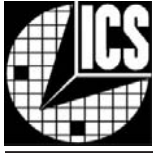


FIGURE 3B. LVPEECL OUTPUT TERMINATION



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843001I-22. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843001I-22 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 160mA = 554.4mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 554.4mW + 30mW = \mathbf{584.4mW}$$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 8 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.584W * 65^\circ C/W = 123^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 8. THERMAL RESISTANCE θ_{JA} FOR 24-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W



3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5*.

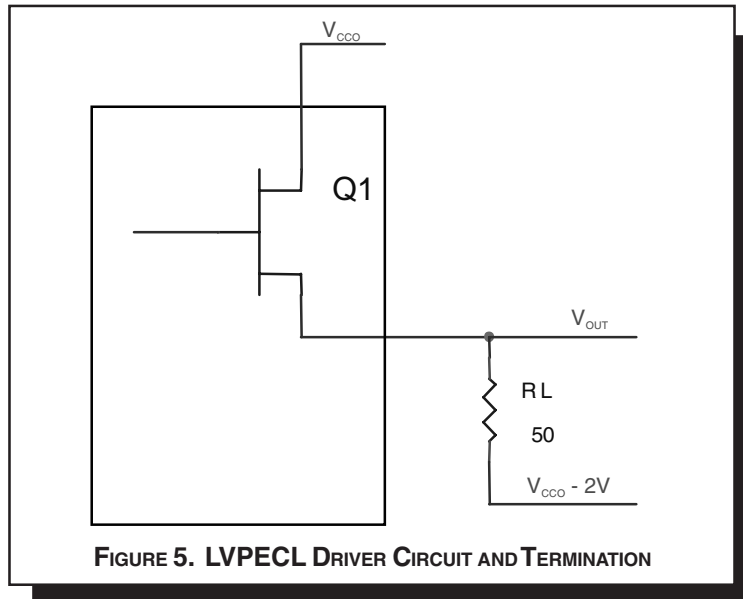


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 0.9V$

$$(V_{CCO_MAX} - V_{OH_MAX}) = 0.9V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.7V$

$$(V_{CCO_MAX} - V_{OL_MAX}) = 1.7V$$

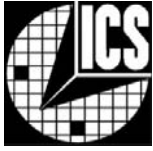
Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = $Pd_H + Pd_L = 30mW$



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RELIABILITY INFORMATION

TABLE 9. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS843001I-22 is: 3881



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PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

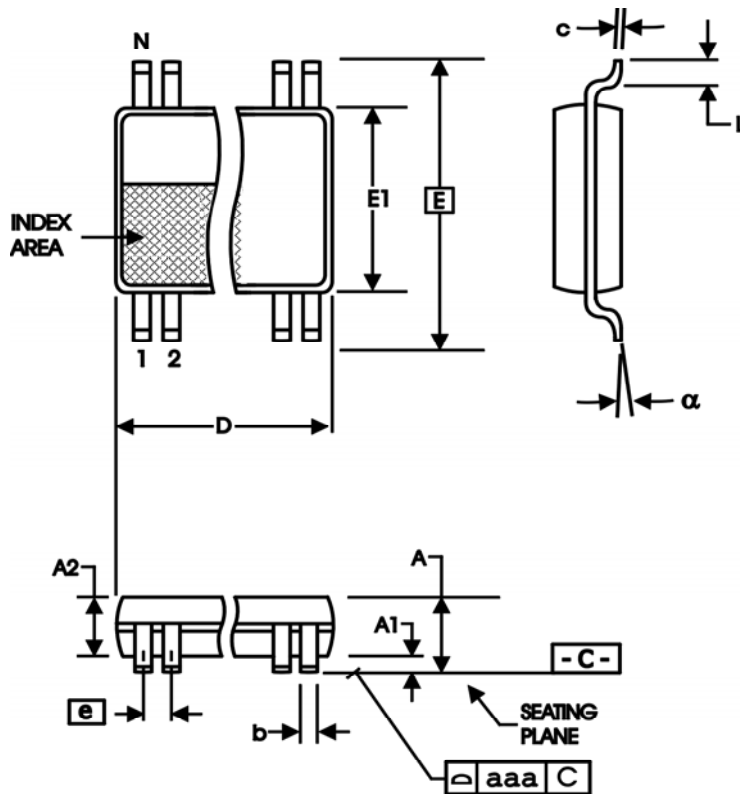
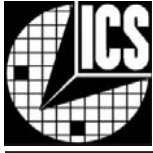


TABLE 10. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
alpha	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153



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TABLE 11. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843001AGI-22	ICS843001AI22	24 Lead TSSOP	tube	-40°C to 85°C
ICS843001AGI-22T	ICS843001AI22	24 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS843001AGI-22LF	ICS43001AI22L	24 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS843001AGI-22LFT	ICS43001AI22L	24 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.