XCR3128: 128 Macrocell CPLD

DS034 (v1.2) August 10, 2000 **Product Specification**

Introduction

- Industry's first TotalCMOS™ PLD - both CMOS design and process technologies
- Fast Zero Power (FZP™) design technique provides ultra-low power and very high speed
- IEEE 1149.1-compliant, JTAG Testing Capability
  - Four pin JTAG interface (TCK, TMS, TDI, TDO)
  - IEEE 1149.1 TAP Controller
  - JTAG commands include: Bypass, Sample/Preload, Extest, Usercode, Idcode, HighZ
- 3.3V, In-System Programmable (ISP) using the JTAG interface
  - On-chip supervoltage generation
  - ISP commands include: Enable, Erase, Program, Verify
  - Supported by multiple ISP programming platforms
- High speed pin-to-pin delays of 10 ns
- Ultra-low static power of less than 100 µA
- 100% routable with 100% utilization while all pins and all macrocells are fixed
- Deterministic timing model that is extremely simple to use
- Four clocks available
- Programmable clock polarity at every macrocell
- Support for asynchronous clocking
- Innovative XPLA™ architecture combines high-speed with extreme flexibility
- 1000 erase/program cycles guaranteed
- 20 years data retention guaranteed
- Logic expandable to 37 product terms
- PCI compliant
- Advanced 0.5µ E^2CMOS process
- Security bit prevents unauthorized access
- Design entry and verification using industry standard and Xilinx CAE tools
- Reprogrammable using industry standard device programmers
- Innovative control term structure provides either sum terms or product terms in each logic block for:
  - Programmable 3-state buffer
  - Asynchronous macrocell register preset/reset
  - Programmable global 3-state pin facilitates "bed of nails" testing without using logic resources
  - Available in PLCC, VQFP, and PQFP packages
  - Available in both commercial and industrial grades

Description

The XCR3128 CPLD (Complex Programmable Logic Device) is the third in a family of CoolRunner® CPLDs from Xilinx. These devices combine high speed and zero power in a 128 macrocell CPLD. With the FZP design technique, the XCR3128 offers true pin-to-pin speeds of 10 ns, while simultaneously delivering power that is less than 100 µA at standby without the need for 'turbo-bits' or other power-down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any competing CPLD. These devices are the first TotalCMOS PLDs, as they use both a CMOS process technology **and** the patented full CMOS FZP design technique. For 5V applications, Xilinx also offers the high speed XCR5128 CPLD that offers these features in a full 5V implementation.

The Xilinx FZP CPLDs utilize the patented XPLA (eXtended Programmable Logic Array) architecture. The XPLA architecture combines the best features of both PLA and PAL type structures to deliver high speed and flexible logic allocation that results in superior ability to make design changes with fixed pinouts. The XPLA structure in each logic block provides a fast 10 ns PAL path with five dedicated product terms per output. This PAL path is joined by an additional PLA structure that deploys a pool of 32 product terms to a fully programmable OR array that can allocate the PLA product terms to any output in the logic block. This combination allows logic to be allocated efficiently throughout the logic block and supports as many as 37 product terms on an output. The speed with which logic is allocated from the PLA array to an output is only 2.5 ns, regardless of the number of PLA product terms used, which results in worst case t_{PD}'s of only 12.5 ns from any pin to any other pin. In addition, logic that is common to multiple outputs can be placed on a single PLA product term and shared across multiple outputs via the OR array, effectively increasing design density.

The XCR3128 CPLDs are supported by industry standard CAE tools (CadencE/OrCAD, Exemplar Logic, Mentor, Synopsys, Synario, Viewlogic, and Synplicity), using text (ABEL, VHDL, Verilog) and/or schematic entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms. Device fitting uses a Xilinx developed tool, XPLA Professional (available on the Xilinx web site).

The XCR3128 CPLD is electrically reprogrammable using industry standard device programmers from vendors such as Data I/O, BP Microsystems, SMS, and others. The XCR3128 also includes an industry-standard, IEEE 1149.1, JTAG interface through which in-system programming (ISP) and reprogramming of the device is supported.

XPLA Architecture

Figure 1 shows a high level block diagram of a 128 macrocell device implementing the XPLA architecture. The XPLA architecture consists of logic blocks that are interconnected by a Zero-power Interconnect Array (ZIA). The ZIA is a virtual crosspoint switch. Each logic block is essentially a 36V16 device with 36 inputs from the ZIA and 16 macrocells. Each logic block also provides 32 ZIA feedback paths from the macrocells and I/O pins.

From this point of view, this architecture looks like many other CPLD architectures. What makes the CoolRunner family unique is what is inside each logic block and the design technique used to implement these logic blocks. The contents of the logic block will be described next.

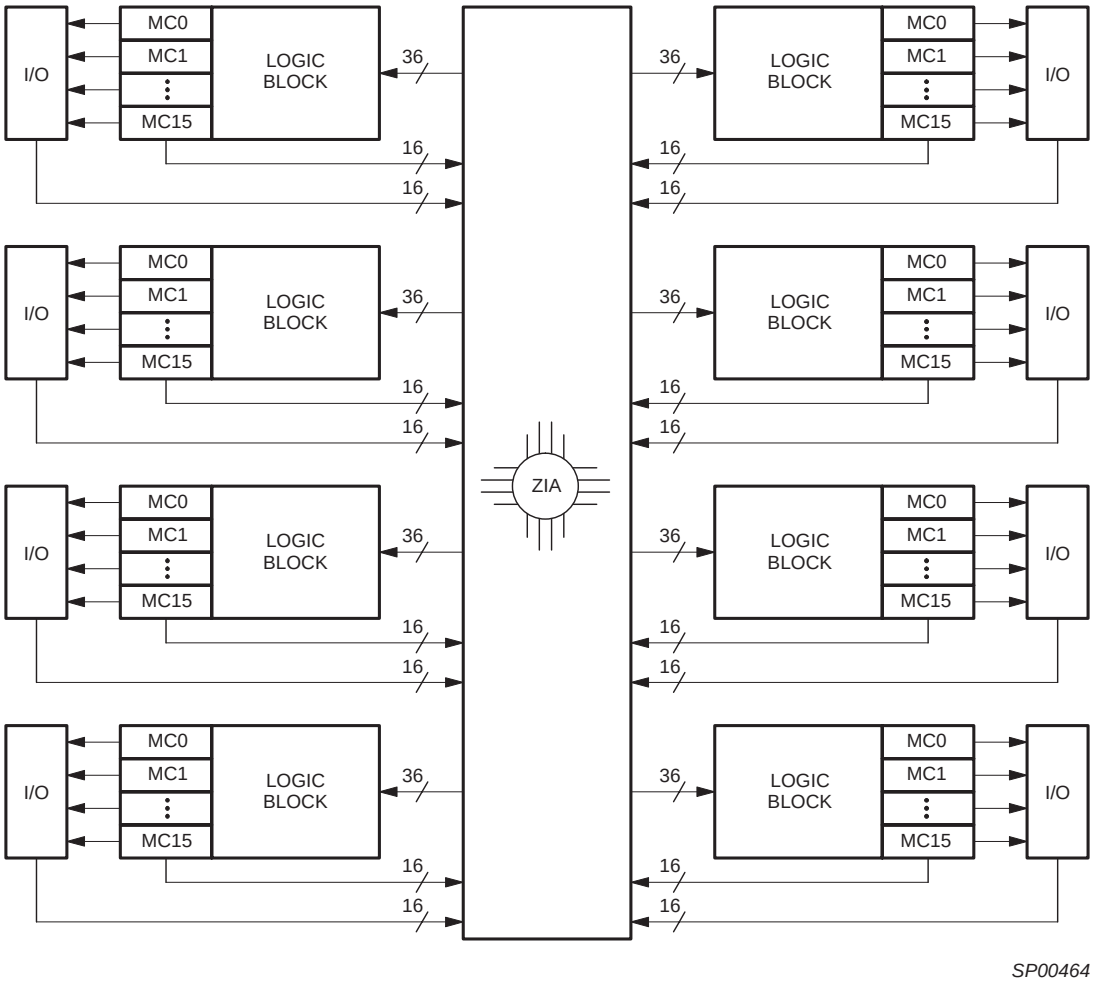


Figure 1: Xilinx XPLA Architecture

Logic Block Architecture

Figure 2 illustrates the logic block architecture. Each logic block contains control terms, a PAL array, a PLA array, and 16 macrocells. the six control terms can individually be configured as either SUM or PRODUCT terms, and are used to control the preset/reset and output enables of the 16 macrocells' flip-flops. The PAL array consists of a programmable AND array with a fixed OR array, while the PLA array consists of a programmable AND array with a programmable OR array. The PAL array provides a high speed path through the array, while the PLA array provides increased product term density.

Each macrocell has five dedicated product terms from the PAL array. The pin-to-pin t_{PD} of the XCR3128 device through the PAL array is 10 ns. If a macrocell needs more than five product terms, it simply gets the additional product terms from the PLA array. The PLA array consists of 32 product terms, which are available for use by all 16 macrocells. The additional propagation delay incurred by a macrocell using one or all 32 PLA product terms is just 2.5 ns. So the total pin-to-pin t_{PD} for the XCR3128 using six to 37 product terms is 12.5 ns (10 ns for the PAL + 2.5 ns for the PLA).

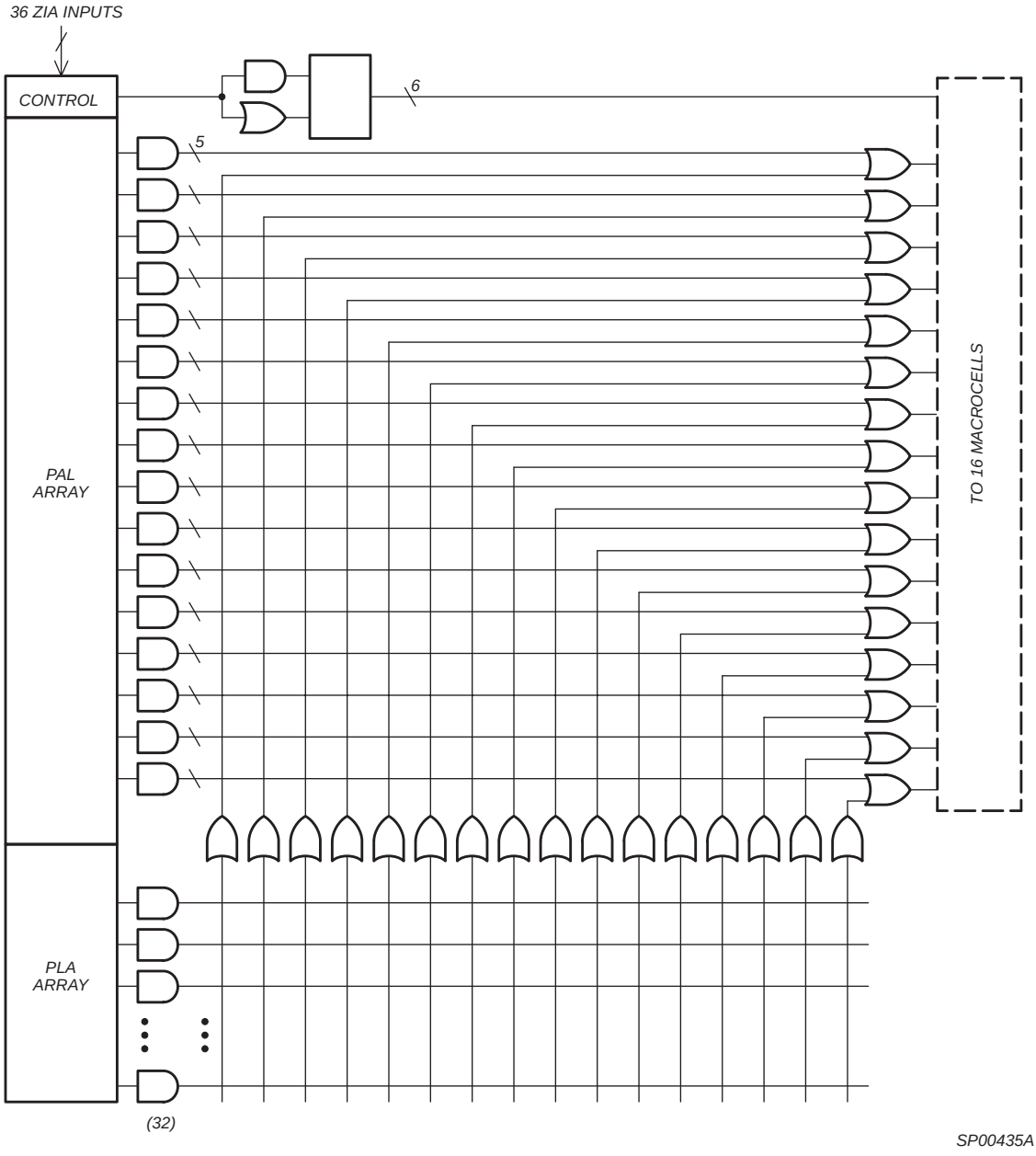


Figure 2: Xilinx XPLA Logic Block Architecture

Macrocell Architecture

Figure 3 shows the architecture of the macrocell used in the CoolRunner family. The macrocell consists of a flip-flop that can be configured as either a D- or T-type. A D-type flip-flop is generally more useful for implementing state machines and data buffering. A T-type flip-flop is generally more useful in implementing counters. All CoolRunner family members provide both synchronous and asynchronous clocking and provide the ability to clock off either the falling or rising edges of these clocks. These devices are designed such that the skew between the rising and falling edges of a clock are minimized for clocking integrity. There are four clocks available on the XCR3128 device. Clock 0 (CLK0) is designated as the "synchronous" clock and must be driven by an external source. Clock 1 (CLK1), Clock 2 (CLK2), and Clock 3 (CLK3) can either be used as a synchronous clock (driven by an external source) or as an asynchronous clock (driven by a macrocell equation). The timing for asynchronous clocks is different in that the t_{CO} time is extended by the amount of time that it takes for the signal to propagate through the array and reach the clock network, and the t_{SU} time is reduced.

Two of the control terms (CT0 and CT1) are used to control the Preset/Reset of the macrocell's flip-flop. The Preset/Reset feature for each macrocell can also be disabled. Note that the Power-on Reset leaves all macrocells in the "zero" state when power is properly applied. The other four control terms (CT2-CT5) can be used to control the Output Enable of the macrocell's output buffers. The reason there are as many control terms dedicated for the Output Enable of the macrocell is to insure that all CoolRunner devices are PCI compliant. The macrocell's output buffers can also be always enabled or disabled. All CoolRunner devices also provide a Global 3-state (GTS) pin, which, when enabled and pulled Low, will 3-state all the outputs of the device. This pin is provided to support "In-circuit Testing" or "Bed-of-nails" testing.

There are two feedback paths to the ZIA: one from the macrocell, and one from the I/O pin. The ZIA feedback path before the output buffer is the macrocell feedback path, while the ZIA feedback path after the output buffer is the I/O pin ZIA path. When the macrocell is used as an output, the output buffer is enabled, and the macrocell feedback path can be used to feedback the logic implemented in the macrocell. When the I/O pin is used as an input, the output buffer will be 3-stated and the input signal will be fed into the ZIA via the I/O feedback path, and the logic implemented in the buried macrocell can be fed back to the ZIA via the macrocell feedback path. It should be noted that unused inputs or I/Os should be properly terminated (see the section on "Terminations" on page 9 in this data sheet and the application note *Terminating Unused I/O Pins in Xilinx XPLA1 and XPLA2 CoolRunner™ CPLDs*).

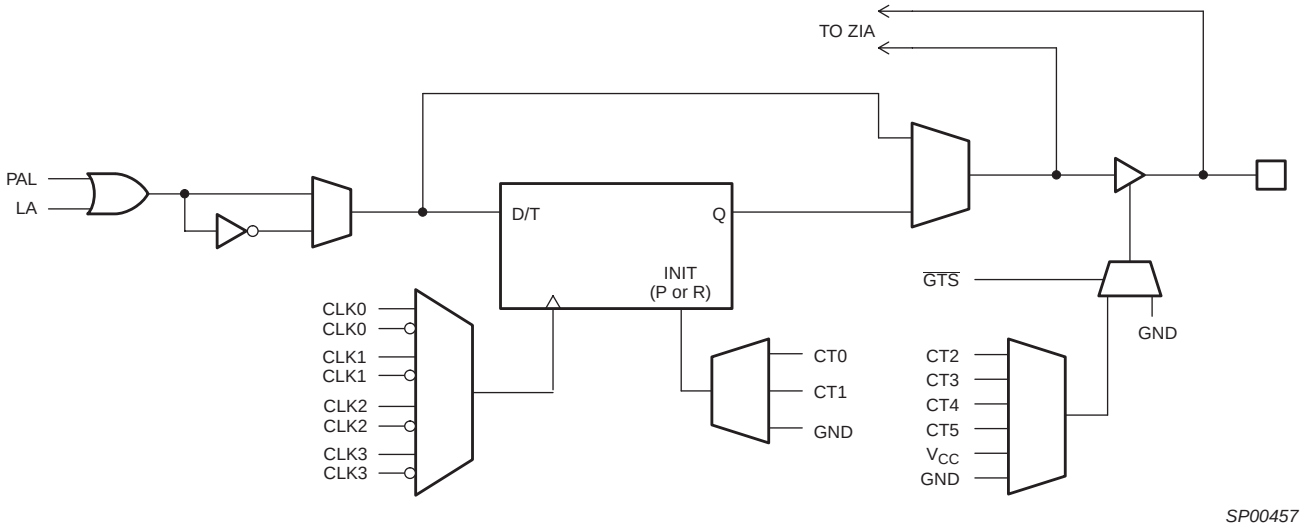


Figure 3: XCR3128 Macrocell Architecture

Simple Timing Model

Figure 4 shows the CoolRunner Timing Model. The CoolRunner timing model looks very much like a 22V10 timing model in that there are three main timing parameters, including t_{PD}, t_{SU}, and t_{CO}. In other competing architectures, the user may be able to fit the design into the CPLD, but is not sure whether system timing requirements can be met until after the design has been fit into the device. This is because the timing models of competing architectures are very complex and include such things as timing dependencies on the number of parallel expanders borrowed, sharable expanders, varying number of X and Y routing channels used, etc. In the XPLA architecture, the user knows up front whether the design will meet system timing requirements. This is due to the simplicity of the timing model.

TotalCMOS Design Technique for Fast Zero Power

Xilinx is the first to offer a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs which are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 5 and Table 1 showing the I_{CC} vs. Frequency of our XCR3128 TotalCMOS CPLD (data taken w/eight up/down, loadable 16 bit counters at 3.3V, 25°C).

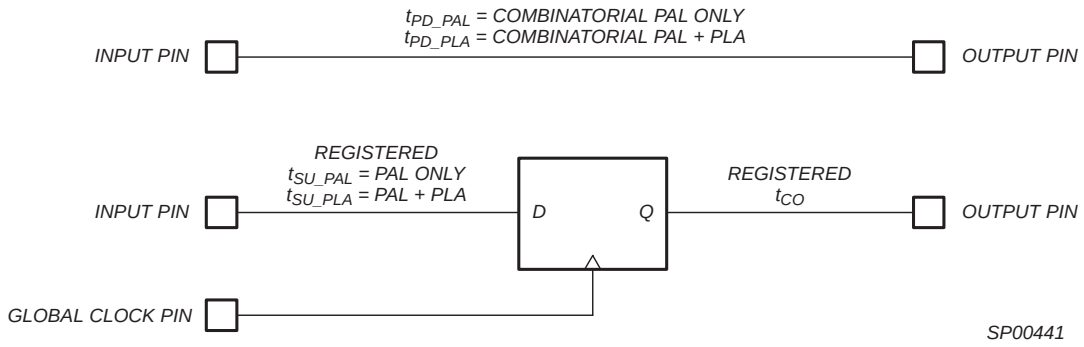


Figure 4: CoolRunner Timing Model

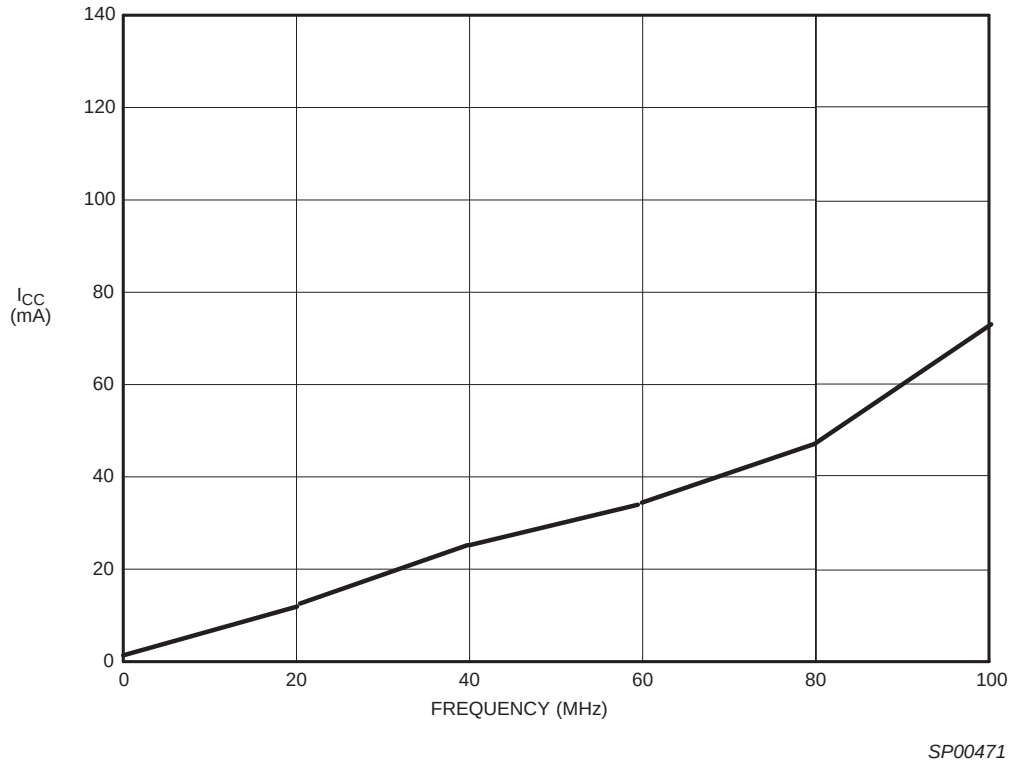


Figure 5: I_{CC} vs. Frequency @ V_{CC} = 3.3V, 25°C

Table 1: I_{CC} vs. Frequency (V_{CC} = 3.3V, 25°C)

Frequency (MHz)	0	1	20	40	60	80	100
Typical I_{CC} (mA)	.03	.06	12	24	35	46	63

JTAG Testing Capability

JTAG is the commonly-used acronym for the Boundary Scan Test (BST) feature defined for integrated circuits by IEEE Standard 1149.1. This standard defines input/output pins, logic control functions, and commands which facilitate both board and device level testing without the use of specialized test equipment. BST provides the ability to test the external connections of a device, test the internal logic of the device, and capture data from the device during normal operation. BST provides a number of benefits in each of the following areas:

- Testability
  - Allows testing of an unlimited number of interconnects on the printed circuit board
  - Testability is designed in at the component level
  - Enables desired signal levels to be set at specific pins (Preload)
  - Data from pin or core logic signals can be examined during normal operation
- Reliability
  - Eliminates physical contacts common to existing test fixtures (e.g., "bed-of-nails")
  - Degradation of test equipment is no longer a concern
  - Facilitates the handling of smaller, surface-mount components
  - Allows for testing when components exist on both sides of the printed circuit board
- Cost
  - Reduces/eliminates the need for expensive test equipment
  - Reduces test preparation time
  - Reduces spare board inventories

The Xilinx XCR3128's JTAG interface includes a TAP Port and a TAP Controller, both of which are defined by the IEEE 1149.1 JTAG Specification. As implemented in the Xilinx

XCR3128, the TAP Port includes four of the five pins (refer to Table 2) described in the JTAG specification: TCK, TMS, TDI, and TDO. The fifth signal defined by the JTAG specification is TRST* (Test Reset). TRST* is considered an optional signal, since it is not actually required to perform BST or ISP. The Xilinx XCR3128 saves an I/O pin for general purpose use by not implementing the optional TRST* signal in the JTAG interface. Instead, the Xilinx XCR3128 supports the test reset functionality through the use of its power up reset circuit, which is included in all Xilinx CPLDs. The pins associated with the power up reset circuit should connect to an external pull-up resistor to keep the JTAG signals from floating when they are not being used.

In the Xilinx XCR3128, the four mandatory JTAG pins each require a unique, dedicated pin on the device. However, if JTAG and ISP are not desired in the end-application, these pins may instead be used as additional general I/O pins. The decision as to whether these pins are used for JTAG/ISP or as general I/O is made when the JEDEC file is generated. If the use of JTAG/ISP is selected, the dedicated pins are not available for general purpose use. However, unlike competing CPLD's, the Xilinx XCR3128 does allow the macrocell logic associated with these dedicated pins to be used as buried logic even when JTAG/ISP is selected. Table 3 defines the dedicated pins used by the four mandatory JTAG signals for each of the XCR3128 package types.

The JTAG specifications defines two sets of commands to support boundary-scan testing: high-level commands and low-level commands. High-level commands are executed via board test software on an a user test station such as automated test equipment, a PC, or an engineering workstation (EWS). Each high-level command comprises a sequence of low level commands. These low-level commands are executed within the component under test, and therefore must be implemented as part of the TAP Controller design. The set of low-level boundary-scan commands implemented in the Xilinx XCR3128 is defined in Table 4. By supporting this set of low-level commands, the XCR3128 allows execution of all high-level boundary-scan commands.

Table 2: JTAG Pin Description

PIN	NAME	DESCRIPTION
TCK	Test Clock Output	Clock pin to shift the serial data and instructions in and out of the TDI and TDO pins, respectively. TCK is also used to clock the TAP Controller state machine.
TMS	Test Mode Select	Serial input pin selects the JTAG instruction mode. TMS should be driven high during user mode operation.
TDI	Test Data Input	Serial input pin for instructions and test data. Data is shifted in on the rising edge of TCK.
TDO	Test Data Output	Serial output pin for instructions and test data. Data is shifted out on the falling edge of TCK. The signal is tri-stated if data is not being shifted out of the device.

Table 3: XCR3128 JTAG Pinout by Package Type

Device XCR3128	(Pin Number / Macrocell #)			
	TCK	TMS	TDI	TDO
84-pin PLCC	62 / 96 (F15)	23 / 48 (C15)	14 / 32 (B15)	71 / 112 (G15)
100-pin PQFP	64 / 96 (F15)	17 / 48 (C15)	6 / 32 (B15)	75 / 112 (G15)
100-pin VQFP	62 / 96 (F15)	15 / 48 (C15)	4 / 32 (B15)	73 / 112 (G15)
128-pin TQFP	82 / 96 (F15)	21 / 48 (C15)	8 / 32 (B15)	95 / 112 (G15)
160-pin PQFP	99 / 96 (F15)	22 / 48 (C15)	9 / 32 (B15)	112/ 112 (G15)

Table 4: XCR3128 Low-Level JTAG Boundary-Scan Commands

Instruction (Instruction Code) Register Used	Description
Sample/Preload (0010) Boundary-Scan Register	The mandatory SAMPLE/PRELOAD instruction allows a snapshot of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the Boundary-Scan Shift-Register prior to selection of the other boundary-scan test instructions.
Extest (0000) Boundary-Scan Register	The mandatory EXTEST instruction allows testing of off-chip circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of Boundary-Scan Shift-Register using the Sample/Preload instruction prior to selection of the EXTEST instruction.
Bypass (1111) Bypass Register	Places the 1 bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. The Bypass instruction can be entered by holding TDI at a constant high value and completing an Instruction-Scan cycle.
Idcode (0001) Boundary-Scan Register	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. The IDCODE instruction permits blind interrogation of the components assembled onto a printed circuit board. Thus, in circumstances where the component population may vary, it is possible to determine what components exist in a product.
HighZ (0101) Bypass Register	The HIGHZ instruction places the component in a state in which all of its system logic outputs are placed in an inactive drive state (e.g., high impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component. The HighZ instruction also forces the Bypass Register between TDI and TDO.

3.3V In-System Programming (ISP)

ISP is the ability to reconfigure the logic and functionality of a device, printed circuit board, or complete electronic system before, during, and after its manufacture and shipment to the end customer. ISP provides substantial benefits in each of the following areas:

- Design
  - Faster time-to-market
  - Debug partitioning and simplified prototyping
  - Printed circuit board reconfiguration during debug
  - Better device and board level testing
- Manufacturing
  - Multi-Functional hardware
  - Reconfigurability for test
  - Eliminates handling of "fine lead-pitch" components for programming
  - Reduced Inventory and manufacturing costs
  - Improved quality and reliability
- Field Support
  - Easy remote upgrades and repair
  - Support for field configuration, re-configuration, and customization

The Xilinx XCR3128 allows for 3.3V, in-system programming/reprogramming of its EEPROM cells via its JTAG interface. An on-chip charge pump eliminates the need for externally-provided supervoltages, so that the XCR3128 may be easily programmed on the circuit board using only the 3.3-volt supply required by the device for normal operation. A set of low-level ISP basic commands implemented in the XCR3128 enable this feature. The ISP commands implemented in the Xilinx XCR3128 are specified in Table 5 Please note that an ENABLE command must precede all ISP commands **unless** an ENABLE command has already been given for a preceding ISP command **and** the device has not gone through a Test-Logic/Rest TAP Controller State. See also Table 5 Programming Specifications.

Table 5: Programming Specifications

Symbol	Parameter	Min.	Max.	Unit
DC Parameters				
V_{CCP}	V_{CC} supply program/verify	3.0	3.6	V
I_{CCP}	I_{CC} limit program/verify		200	mA
V_{IH}	Input voltage (High)	2.0		V
V_{IL}	Input voltage (Low)		0.8	V
V_{SOL}	Output voltage (Low)		0.5	V
V_{SOH}	Output voltage (High)	2.4		V
TDO_I_{OL}	Output current (Low)	8		mA
TDO_I_{OH}	Output current (High)	-8		mA
AC Parameters				
f_{MAX}	CLK maximum frequency	10		MHz
PWE	Pulse width erase	100		ms
PWP	Pulse width program	10		ms
PWV	Pulse width verify	10		µs
INIT	Initialization time	100		µs
TMS_SU	TMS setup time before TCK =	10		ns
TDI_SU	TDI setup time before TCK =	10		ns
TMS_H	TMS hold time after TCK =	25		ns
TDI_H	TDI hold time after TCK =	25		ns
TDO_CO	TDO valid after TCK O		40	ns

Terminations

The CoolRunner XCR3128 CPLDs are TotalCMOS devices. As with other CMOS devices, it is important to consider how to properly terminate unused inputs and I/O pins when fabricating a PC board. Allowing unused inputs and I/O pins to float can cause the voltage to be in the linear region of the CMOS input structures, which can increase the power consumption of the device. The XCR3128 CPLDs have programmable on-chip pull-down resistors on each I/O pin. These pull-downs are automatically activated by the fitter software for all unused I/O pins. Note that an I/O macrocell used as buried logic that does not have the I/O pin used for input is considered to be unused, and the pull-down resistors will be turned on. We recommend that any unused I/O pins on the XCR3128 device be left unconnected.

There are no on-chip pull-down structures associated with the dedicated input pins. Xilinx recommends that any unused dedicated inputs be terminated with external 10kΩ pull-up resistors. These pins can be directly connected to V_{CC} or GND, but using the external pull-up resistors maintains maximum design flexibility should one of the unused dedicated inputs be needed due to future design changes.

When using the JTAG/ISP functions, it is also recommended that 10kΩ pull-up resistors be used on each of the pins associated with the four mandatory JTAG signals. Letting these signals float can cause the voltage on TMS to come close to ground, which could cause the device to enter JTAG/ISP mode at unspecified times. See the application notes *JTAG and ISP Overview for Xilinx XPLA1 and XPLA2 CPLDs* and *Terminating Unused I/O Pins in Xilinx XPLA1 and XPLA2 CoolRunner CPLDs* for more information.

JTAG and ISP Interfacing

A number of industry-established methods exist for JTAG/ISP interfacing with CPLD's and other integrated circuits. The Xilinx XCR3128 supports the following methods:

- PC parallel port
- Workstation or PC serial port
- Embedded processor
- Automated test equipment
- Third party programmers
- High-End JTAG and ISP tools

A Boundary-Scan Description Language (BSDL) description of the XCR3128 is also available from Xilinx for use in test program development. For more details on JTAG and ISP for the XCR3128, refer to the related application note: *JTAG and ISP Overview for Xilinx XPLA1 and XPLA2 CPLDs*.

Absolute Maximum Ratings[1]

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage[2]	-0.5	7.0	V
V_I	Input voltage	-1.2	V_{CC} + 0.5	V
V_{OUT}	Output voltage	-0.5	V_{CC} + 0.5	V
I_{IN}	Input current	-30	30	mA
I_{OUT}	Output current	-100	100	mA
T_J	Maximum junction temperature	-40	150	°C
T_{str}	Storage temperature	-65	150	°C

Notes:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage must rise monotonically.

Operating Range

Product Grade	Temperature	Voltage
Commercial	0 to +70°C	3.3V ± 10%
Industrial	-40 to +85°C	3.3V ± 10%

DC Electrical Characteristics For Commercial Grade Devices

Commercial: 0°C ≤ T_{AMB} ≤ +70°C; 3.0V ≤ V_{CC} ≤ 3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IL}	Input voltage low	V_{CC} = 3.0V		0.8	V
V_{IH}	Input voltage high	V_{CC} = 3.6V	2.0		V
V_I	Input clamp voltage	V_{CC} = 3.0V, I_{IN} = -18 mA		-1.2	V
V_{OL}	Output voltage low	V_{CC} = 3.0V, I_{OL} = 8 mA		0.5	V
V_{OH}	Output voltage high	V_{CC} = 3.0V, I_{OH} = -8 mA	2.4		V
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	-10	10	µA
I_{OZ}	3-stated output leakage current	V_{IN} = 0 to V_{CC}	-10	10	µA
I_{CCQ}[1]	Standby current	V_{CC} = 3.6V, T_{AMB} = 0°C		60	µA
I_{CCD}[1, 2]	Dynamic current	V_{CC} = 3.6V, T_{AMB} = 0°C at 1 MHz		2	mA
		V_{CC} = 3.6V, T_{AMB} = 0°C at 50 MHz		50	mA
I_{OS}	Short circuit output current[3]	One pin at a time for no longer than 1 second	-50	-100	mA
C_{IN}	Input pin capacitance[3]	T_{AMB} = 25°C, f = 1 MHz		8	pF
C_{CLK}	Clock input capacitance[3]	T_{AMB} = 25°C, f = 1MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance[3]	T_{AMB} = 25°C, f = 1MHz		10	pF

Notes:
1. See Table 1 on page 6 for typical values.
2. This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
3. Typical values, not tested.

AC Electrical Characteristics[1] For Commercial Grade Devices

Commercial: 0°C ≤ T_{AMB} ≤ +70°C; 3.0V ≤ V_{CC} ≤ 3.6V

Symbol	Parameter	10		12		15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD_PAL}	Propagation delay time, input (or feedback node) to output through PAL	2	10	2	12	2	15	ns
t_{PD_PLA}	Propagation delay time, input (or feedback node) to output through PAL + PLA	3	12.5	3	14.5	3	17.5	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	7	2	8	2	9	ns
t_{SU_PAL}	Setup time (from input or feedback node) through PAL	6		7		8		ns
t_{SU_PLA}	Setup time (from input or feedback node) through PAL + PLA	8.5		9.5		10.5		ns
t_H	Hold time		0		0		0	ns
t_{CH}	Clock High time	3		4		4		ns
t_{CL}	Clock Low time	3		4		4		ns
t_R	Input Rise time		20		20		20	ns
t_F	Input Fall time		20		20		20	ns
f_{MAX1}	Maximum FF toggle rate [2] $1/(t_{CH} + t_{CL})$	167		125		125		MHz
f_{MAX2}	Maximum internal frequency [2] $1/(t_{SUPAL} + t_{CF})$	87		74		65		MHz
f_{MAX3}	Maximum external frequency [2] $1/(t_{SUPAL} + t_{CO})$	77		66		59		MHz
t_{BUF}	Output buffer delay time		1.5		1.5		1.5	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL	2	0.5	2	10.5	2	13.5	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PAL+PLA	3	11	3	13	3	16	ns
t_{CF}	Clock to internal feedback node delay time		5.5		6.5		7.5	ns
t_{INIT}	Delay from valid V_{DD} to valid reset		50		50		50	µs
t_{ER}	Input to output disable [3]		12.5		14		17	ns
t_{EA}	Input to output valid		12.5		14		17	ns
t_{RP}	Input to register preset		14		16		19	ns
t_{RR}	Input to register reset		14		16		19	ns

Notes:

1. Specifications measured with one output switching. See Figure 6 and Table 6 for derating.
2. This parameter guaranteed by design and characterization, not by test.
3. Output C_L = 5 pF.

DC Electrical Characteristics For Industrial Grade Devices

Industrial: -40°C ≤ T_{AMB} ≤ +85°C; 3.0V ≤ V_{CC} ≤ 3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IL}	Input voltage Low	V_{CC} = 3.0V		0.8	V
V_{IH}	Input voltage High	V_{CC} = 3.6V	2.0		V
V_I	Input clamp voltage	V_{CC} = 3.0V, I_{IN} = -18 mA		-1.2	V
V_{OL}	Output voltage Low	V_{CC} = 3.0V, I_{OL} = 8 mA		0.5	V
V_{OH}	Output voltage High	V_{CC} = 3.0V, I_{OH} = -8 mA	2.4		V
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	-10	10	µA
I_{OZ}	3-stated output leakage current	V_{IN} = 0 to V_{CC}	-10	10	µA
I_{CCQ}[1]	Standby current	V_{CC} = 3.6V, T_{AMB} = -40°C		75	µA
I_{CCD}[1, 2]	Dynamic current	V_{CC} = 3.6V, T_{AMB} = -40°C at 1 MHz		2	mA
		V_{CC} = 3.6V, T_{AMB} = -40°C at 50 MHz		50	mA
I_{OS}	Short circuit output current[3]	One pin at a time for no longer than 1 second	-50	-130	mA
C_{IN}	Input pin capacitance[3]	T_{AMB} = 25°C, f = 1 MHz		8	pF
C_{CLK}	Clock input capacitance[3]	T_{AMB} = 25°C, f = 1MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance[3]	T_{AMB} = 25°C, f = 1MHz		10	pF

Notes:

1. See Table 1 on page 6 for typical values.
2. This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs DISabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
3. Typical values, not tested.

AC Electrical Characteristics[1] For Industrial Grade Devices

Industrial: -40°C ≤ T_{AMB} ≤ +85°C; 3.0V ≤ V_{CC} ≤ 3.6V

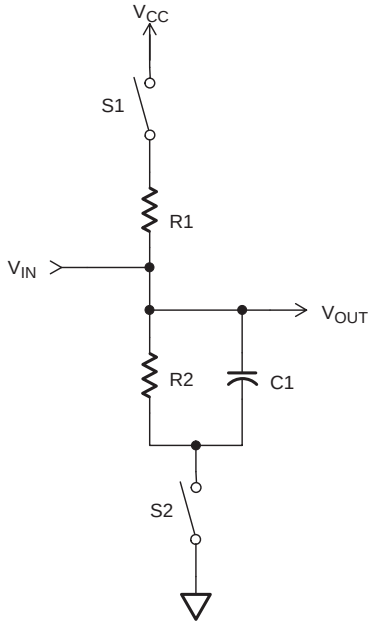
Symbol	Parameter	12		15		Unit
		Min.	Max.	Min.	Max.	
t_{PD_PAL}	Propagation delay time, input (or feedback node) to output through PAL	2	12	2	15	ns
t_{PD_PLA}	Propagation delay time, input (or feedback node) to output through PAL + PLA	3	14.5	3	17.5	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	7.5	2	9	ns
t_{SU_PAL}	Setup time (from input or feedback node) through PAL	7		8		ns
t_{SU_PLA}	Setup time (from input or feedback node) through PAL + PLA	9.5		10.5		ns
t_H	Hold time		0		0	ns
t_{CH}	Clock High time	3		4		ns
t_{CL}	Clock Low time	3		4		ns
t_R	Input Rise time		20		20	ns
t_F	Input Fall time		20		20	ns
f_{MAX1}	Maximum FF toggle rate[2] $1/(t_{CH} + t_{CL})$	167		125		MHz
f_{MAX2}	Maximum internal frequency[2] $1/(t_{SUPAL} + t_{CF})$	77		65		MHz
f_{MAX3}	Maximum external frequency[2] $1/(t_{SUPAL} + t_{CO})$	69		59		MHz
t_{BUF}	Output buffer delay time		1.5		1.5	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL	2	10.5	2	13.5	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PAL+PLA	3	13	3	16	ns
t_{CF}	Clock to internal feedback node delay time		6		7.5	ns
t_{INIT}	Delay from valid V_{CC} to valid reset		50		50	µs
t_{ER}	Input to output disable [3]		13		15.5	ns
t_{EA}	Input to output valid		13		15.5	ns
t_{RP}	Input to register preset		15		17	ns
t_{RR}	Input to register reset		15		17	ns

Notes:

1. Specifications measured with one output switching. See Figure 6 and Table 8 for derating.
2. This parameter guaranteed by design and characterization, not by test.
3. Output C_L = 5 pF.

Switching Characteristics

The test load circuit and load values for the AC Electrical Characteristics are illustrated below.



COMPONENT	VALUES
R1	390Ω
R2	390Ω
C1	35 pF

MEASUREMENT	S1	S2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Closed
t_P	Closed	Closed

Note: For t_{PHZ} and t_{PLZ} C = 5 pF, and 3-state levels are measured 0.5V from steady-state active level.

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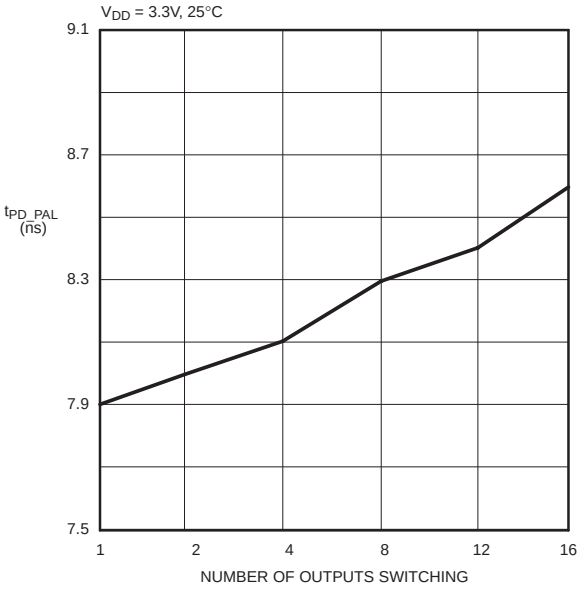

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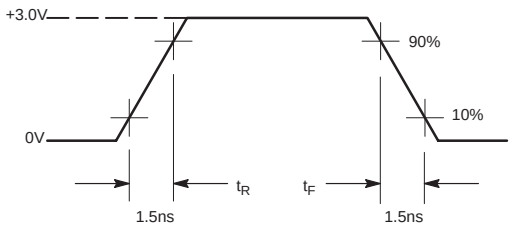
Figure 6: t_{PD_PAL} vs. Output Switching



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MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Figure 7: Voltage Waveform

Table 6: t_{PD_PAL} vs. Number of Outputs Switching
(V_{CC} = 3.3 V, T = 25°C)

Number Of Outputs	1	2	4	8	12	16
Typical (ns)	7.9	8	8.1	8.3	8.4	8.6

Pin Function And Layout

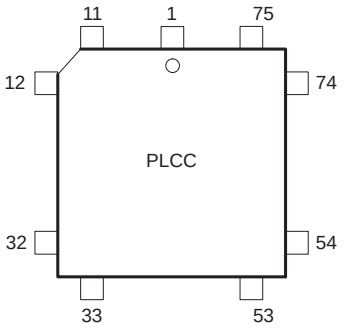
XCR3128: 100-pin and 160-pin PQFP Pin Function Table

Pin #	Function PQFP		Pin #	Function PQFP		Pin #	Function PQFP		Pin #	Function PQFP	
	100-pin	160-pin		100-pin	160-pin		100-pin	160-pin		100-pin	160-pin
1	I/O-A5	NC	41	V_{CC}	I/O-C0	81	I/O-H7	NC	121	-	I/O-H0
2	I/O-A4	NC	42	I/O-E0/CLK1	GND	82	I/O-H8	NC	122	-	I/O-H2
3	I/O-A2	NC	43	I/O-E2	I/O-D15	83	I/O-H10	NC	123	-	I/O-H3
4	I/O-A0	NC	44	I/O-E4	NC	84	V_{CC}	NC	124	-	NC
5	V_{CC}	NC	45	GND	NC	85	I/O-H12	NC	125	-	NC
6	I/O-B15 (TDI)	NC	46	I/O-E5	NC	86	I/O-H13	NC	126	-	NC
7	I/O-B13	NC	47	I/O-E7	NC	87	I/O-H15	NC	127	-	NC
8	I/O-B12	V_{CC}	48	I/O-E8	I/O-D13	88	GND	I/O-F2	128	-	I/O-H4
9	I/O-B10	I/O-B15 (TDI)	49	I/O-E10	I/O-D12	89	IN0/CK0	I/O-F3	129	-	I/O-H5
10	I/O-B8	I/O-B13	50	I/O-E12	I/O-D11	90	IN2/gtsn	I/O-F4	130	-	I/O-H7
11	I/O-B7	I/O-B12	51	I/O-E13	I/O-D10	91	IN1	I/O-F5	131	-	I/O-H8
12	I/O-B5	I/O-B11	52	I/O-E15	I/O-D8	92	IN3	I/O-F7	132	-	I/O-H10
13	GND	I/O-B10	53	V_{CC}	I/O-D7	93	V_{CC}	I/O-F8	133	-	V_{CC}
14	I/O-B4	I/O-B8	54	I/O-F0	I/O-D5	94	I/O-A15/CK3	I/O-F10	134	-	I/O-H11
15	I/O-B2	I/O-B7	55	I/O-F2	V_{CC}	95	I/O-A13	GND	135	-	I/O-H12
16	I/O-B0	I/O-B5	56	I/O-F4	I/O-D4	96	I/O-A12	I/O-F11	136	-	I/O-H13
17	I/O-C15 (TMS)	GND	57	I/O-F5	I/O-D3	97	GND	I/O-F12	137	-	I/O-H15
18	I/O-C13	I/O-B4	58	I/O-F7	I/O-D2	98	I/O-A10	I/O-F13	138	-	GND
19	I/O-C12	I/O-B3	59	I/O-F8	I/0-D0/CLK2	99	I/O-A8	I/O-F15 (TCK)	139	-	IN0/CK0
20	V_{CC}	I/O-B2	60	I/O-F10	GND	100	I/O-A7	I/O-G0	140	-	IN2/gtsn
21	I/O-C10	I/O-B0	61	GND	V_{CC}	101	-	I/O-G2	141	-	IN1
22	I/O-C8	I/O-C15 (TMS)	62	I/O-F12	I/0-E0/CLK1	102	-	I/O-G3	142	-	IN3
23	I/O-C7	I/O-C13	63	I/O-F13	I/O-E2	103	-	I/O-G4	143	-	V_{CC}
24	I/O-C5	I/O-C12	64	I/O-F15 (TCK)	I/O-E3	104	-	V_{CC}	144	-	I/O-A0/CK3
25	I/O-C4	I/O-C11	65	I/O-G0	I/O-E4	105	-	I/O-G5	145	-	I/O-A13
26	I/O-C2	V_{CC}	66	I/O-G2	GND	106	-	I/O-G7	146	-	I/O-A12
27	I/O-C0	I/O-C10	67	I/O-G4	I/0-E5	107	-	I/O-G8	147	-	I/O-A11
28	GND	I/O-C8	68	V_{CC}	I/0-E7	108	-	I/O-G10	148	-	GND
29	I/O-D15	I/O-C7	69	I/O-G5	I/0-E8	109	-	I/O-G11	149	-	I/O-A10
30	I/O-D13	I/O-C5	70	I/O-G7	I/0-E10	110	-	I/O-G12	150	-	I/O-A8
31	I/O-D12	I/O-C4	71	I/O-G8	I/O-E11	111	-	I/O-G13	151	-	I/O-A7
32	I/O-D10	I/O-C3	72	I/O-G10	I/0-E12	112	-	I/O-G15 (TDO)	152	-	I/O-A5
33	I/O-D8	I/O-C2	73	I/O-G12	I/0-E13	113	-	GND	153	-	I/O-A4
34	I/O-D7	NC	74	I/O-G13	NC	114	-	NC	154	-	NC
35	I/O-D5	NC	75	I/O-G15 (TDO)	NC	115	-	NC	155	-	NC
36	V_{CC}	NC	76	GND	NC	116	-	NC	156	-	NC
37	I/O-D4	NC	77	I/O-H0	NC	117	-	NC	157	-	NC
38	I/O-D2	NC	78	I/O-H2	I/O-E15	118	-	NC	158	-	I/O-A3
39	I/O-D0/CK2	NC	79	I/O-H4	V_{CC}	119	-	NC	159	-	I/O-A2
40	GND	NC	80	I/O-H5	I/O-F0	120	-	NC	160	-	I/O-A0

XCR3128: 84-pin PLCC, 100-Pin VQFP, and 128-pin TQFP Pin Function Table

Pin #	Function			Pin #	Function			Pin #	Function			Pin #	Function		
	PLCC	VQFP	TQFP		PLCC	VQFP	TQFP		PLCC	VQFP	TQFP		PLCC	VQFP	TQFP
1	IN1	I/O-A2	I/O-A3	33	I/O-D15	I/O-D5	NC	65	I/O-G4	I/O-G4	I/O-E15	97	-	I/O-A8	NC
2	IN3	I/O-A0	I/O-A2	34	I/O-D12	V_{CC}	NC	66	V_{CC}	V_{CC}	V_{CC}	98	-	I/O-A7	NC
3	V_{CC}	V_{CC}	I/O-A0	35	I/O-D10	I/O-D4	NC	67	I/O-G7	I/O-G5	I/O-F0	99	-	I/O-A5	NC
4	I/O-A15/ CLK3	I/O-B15 (TDI)	NC	36	I/O-D8	I/O-D2	I/O-C0	68	I/O-G8	I/O-G7	NC	100	-	I/O-A4	I/O-H0
5	I/O-A13	I/O-B13	NC	37	I/O-D7	I/O-D0/ CLK2	GND	69	I/O-G10	I/O-G8	NC	101	-	-	I/O-H2
6	I/O-A12	I/O-B12	NC	38	V_{CC}	GND	I/O-D15	70	I/O-G12	I/O-G10	NC	102	-	-	I/O-H3
7	GND	I/O-B10	V_{CC}	39	I/O-D4	V_{CC}	I/O-D13	71	I/O-G15 (TDO)	I/O-G12	I/O-F2	103	-	-	I/O-H4
8	I/O-A10	I/O-B8	I/O-B15 (TDI)	40	I/O-D2	I/O-E0/ CLK1	I/O-D12	72	GND	I/O-G13	I/O-F3	104	-	-	I/O-H5
9	I/O-A7	I/O-B7	I/O-B13	41	I/O-D0/C LK2	I/O-E2	I/O-D11	73	I/O-H2	I/O-G15 (TDO)	I/O-F4	105	-	-	I/O-H7
10	I/O-A5	I/O-B5	I/O-B12	42	GND	I/O-E4	I/O-D10	74	I/O-H4	GND	I/O-F5	106	-	-	I/O-H8
11	I/O-A4	GND	I/O-B11	43	V_{CC}	GND	I/O-D8	75	I/O-H5	I/O-H0	I/O-F7	107	-	-	I/O-H10
12	I/O-A2	I/O-B4	I/O-B10	44	I/O-E0/C LK1	I/O-E5	I/O-D7	76	I/O-H7	I/O-H2	I/O-F8	108	-	-	V_{CC}
13	V_{CC}	I/O-B2	I/O-B8	45	I/O-E2	I/O-E7	I/O-D5	77	I/O-H10	I/O-H4	I/O-F10	109	-	-	I/O-H11
14	I/O-B15 (TDI)	I/O-B0	I/O-B7	46	I/O-E4	I/O-E8	V_{CC}	78	V_{CC}	I/O-H5	GND	110	-	-	I/O-H12
15	I/O-B12	I/O-C15 (TMS)	I/O-B5	47	GND	I/O-E10	I/O-D4	79	I/O-H12	I/O-H7	I/O-F11	111	-	-	I/O-H13
16	I/O-B10	I/O-C13	GND	48	I/O-E7	I/O-E12	I/O-D3	80	I/O-H13	I/O-H8	I/O-F12	112	-	-	I/O-H15
17	I/O-B8	I/O-C12	I/O-B4	49	I/O-E8	I/O-E13	I/O-D2	81	I/O-H15	I/O-H10	I/O-F13	113	-	-	GND
18	I/O-B7	V_{CC}	I/O-B3	50	I/O-E10	I/O-E15	I/O-D0/C LK2	82	GND	V_{CC}	I/O-F15 (TCK)	114	-	-	IN0/CLK0
19	GND	I/O-C10	I/O-B2	51	I/O-E12	V_{CC}	GND	83	IN0/ CLK0	I/O-H12	I/O-G0	115	-	-	IN2/gtsn
20	I/O-B4	I/O-C8	I/O-B0	52	I/O-E15	I/O-F0	V_{CC}	84	IN2/gtsn	I/O-H13	I/O-G2	116	-	-	IN1
21	I/O-B2	I/O-C7	I/O-C15 (TMS)	53	V_{CC}	I/O-F2	I/O-E0/ CLK1	85	-	I/O-H15	I/O-G3	117	-	-	IN3
22	I/O-B0	I/O-C5	I/O-C13	54	I/O-F2	I/O-F4	I/O-E2	86	-	GND	I/O-G4	118	-	-	V_{CC}
23	I/O-C15 (TMS)	I/O-C4	I/O-C12	55	I/O-F4	I/O-F5	I/O-E3	87	-	IN0/CLK0	V_{CC}	119	-	-	I/O-A15/ CLK3
24	I/O-C13	I/O-C2	I/O-C11	56	I/O-F5	I/O-F7	I/O-E4	88	-	IN2/gtsn	I/O-G5	120	-	-	I/O-A13
25	I/O-C12	I/O-C0	V_{CC}	57	I/O-F7	I/O-F8	GND	89	-	IN1	I/O-G7	121	-	-	I/O-A12
26	V_{CC}	GND	I/O-C10	58	I/O-F10	I/O-F10	I/O-E5	90	-	IN3	I/O-G8	122	-	-	I/O-A11
27	I/O-C10	I/O-D15	I/O-C8	59	GND	GND	I/O-E7	91	-	V_{CC}	I/O-G10	123	-	-	GND
28	I/O-C7	I/O-D13	I/O-C7	60	I/O-F12	I/O-F12	I/O-E8	92	-	I/O-A15/C LK3	I/O-G11	124	-	-	I/O-A10
29	I/O-C5	I/O-D12	I/O-C5	61	I/O-F13	I/O-F13	I/O-E10	93	-	I/O-A13	I/O-G12	125	-	-	I/O-A8
30	I/O-C4	I/O-D10	I/O-C4	62	I/O-F15 (TCK)	I/O-F15 (TCK)	I/O-E11	94	-	I/O-A12	I/O-G13	126	-	-	I/O-A7
31	I/O-C2	I/O-D8	I/O-C3	63	I/O-G0	I/O-G0	I/O-E12	95	-	GND	I/O-G15 (TDO)	127	-	-	I/O-A5
32	GND	I/O-D7	I/O-C2	64	I/O-G2	I/O-G2	I/O-E13	96	-	I/O-A10	GND	128	-	-	I/O-A4

84-pin PLCC



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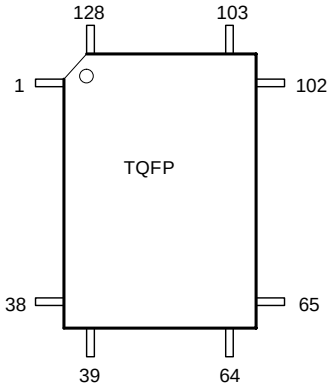
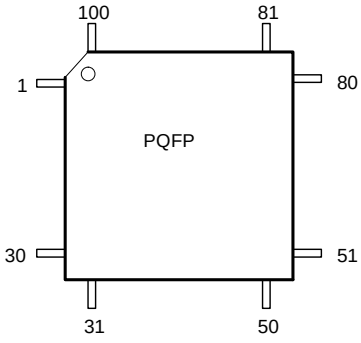
128-pin TQFP



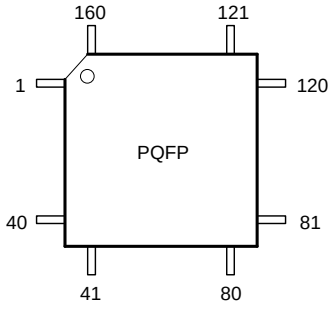
SP00469B

100-pin PQFP



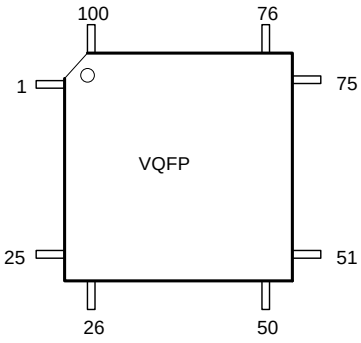
SP00468A

160-pin PQFP



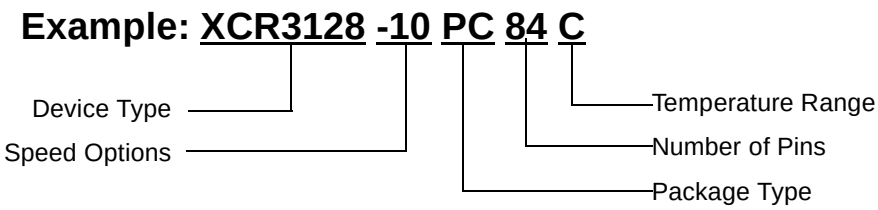
SP00470B

100-pin VQFP



SP00485A

Ordering Information



Speed Options
-15: 15 ns pin-to-pin delay
-12: 12 ns pin-to-pin delay
-10: 10 ns pin-to-pin delay

Temperature Range
C = Commercial, T_A = 0°C to +70°C
I = Industrial, T_A = –40°C to +85°C

Packaging Options
PC84: 84-pin PLCC
PQ100: 100-pin PQFP
VQ100: 100-pin VQFP
TQ128: 128-pin TQFP
PQ160: 160-pin PQFP

Component Availability

Pins		84	100		128	160
Type		Plastic PLCC	Plastic PQFP	Plastic VQFP	Plastic TQFP	Plastic PQFP
Code		PC84	PQ100	VQ100	TQ128	PQ160
XCR3128	-15	C, I	C, I	C, I	C, I	C, I
	-12	C, I	C, I	C, I	C, I	C, I
	-10	C	C	C	C	C

Revision Table

Date	Version #	Revision
8/4/99	1.0	Initial Xilinx release
2/10/00	1.1	Converted to Xilinx format and updated.
8/10/00	1.2	Updated pinout tables.