CATALYST SEMICONDUCTOR, INC.

CAT25640

64-Kb SPI Serial CMOS EEPROM

FEATURES

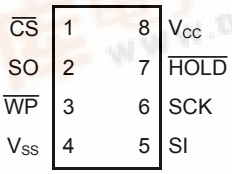
- 10 MHz SPI compatible
- 1.8V to 5.5V supply voltage range
- SPI modes (0,0) & (1,1)
- 64-byte page write buffer
- Self-timed write cycle
- Hardware and software protection
- Block write protection
  - Protect 1/4, 1/2 or entire EEPROM array
- Low power CMOS technology
- 1,000,000 program/erase cycles
- 100 year data retention
- Industrial temperature range
- RoHS-compliant 8 lead PDIP, SOIC, TSSOP and 8-pad TDFN packages

DESCRIPTION

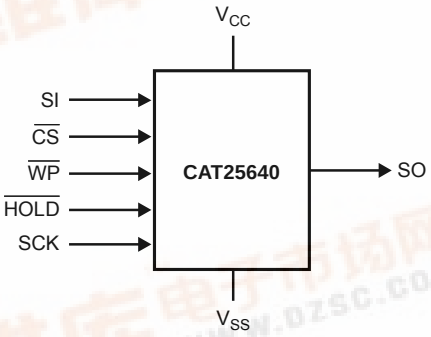
The CAT25640 is a 64-Kb Serial CMOS EEPROM device internally organized as 8Kx8 bits. This features a 64-byte page write buffer and supports the Serial Peripheral Interface (SPI) protocol. The device is enabled through a Chip Select ($\overline{CS}$) input. In addition, the required bus signals are clock input (SCK), data input (SI) and data output (SO) lines. The $\overline{HOLD}$ input may be used to pause any serial communication with the CAT25640 device. The device features software and hardware write protection, including partial as well as full array protection.

PIN CONFIGURATION

PDIP (L)
SOIC (V)
TSSOP (Y)
TDFN (VP2)



FUNCTIONAL SYMBOL



PIN FUNCTION

Pin Name	Function
$\overline{CS}$	Chip Select
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock
$\overline{HOLD}$	Hold Transmission Input
V_{CC}	Power Supply

For Ordering Information details, see page 15.

ABSOLUTE MAXIMUM RATINGS[1]

Parameters	Ratings	Units
Storage Temperature	–65 to +150	ºC
Voltage on any Pin with Respect to Ground[2]	–0.5 to + 6.5	V

RELIABILITY CHARACTERISTICS[3]

Symbol	Parameter	Min	Units
N_{END}[4]	Endurance	1,000,000	Program/ Erase Cycles
T_{DR}	Data Retention	100	Years

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +5.5V, T_A=-40°C to +85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CCR}	Supply Current (Read Mode)	Read, V_{CC} = 5.5V, f_{SCK} = 10MHz, SO open		2	mA
I_{CCW}	Supply Current (Write Mode)	Write, V_{CC} = 5.5V, f_{SCK} = 10MHz, SO open		3	mA
I_{SB1}	Standby Current	V_{IN} = GND or V_{CC} , $\overline{CS}$ = V_{CC} , $\overline{WP}$ = V_{CC}, V_{CC} = 5.5V		1	µA
I_{SB2}	Standby Current	V_{IN} = GND or V_{CC} , $\overline{CS}$ = V_{CC} , $\overline{WP}$ = GND, V_{CC} = 5.5V		3	µA
I_L	Input Leakage Current	V_{IN} = GND or V_{CC}	-2	2	µA
I_{LO}	Output Leakage Current	$\overline{CS}$ = V_{CC} , V_{OUT} = GND or V_{CC}	-1	1	µA
V_{IL}	Input Low Voltage		-0.5	$0.3V_{CC}$	V
V_{IH}	Input High Voltage		$0.7V_{CC}$	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	$V_{CC} \geq$ 2.5V, I_{OL} = 3.0mA		0.4	V
V_{OH1}	Output High Voltage	$V_{CC} \geq$ 2.5V, I_{OH} = -1.6mA	V_{CC} - 0.8V		V
V_{OL2}	Output Low Voltage	V_{CC} < 2.5V, I_{OL} = 150µA		0.2	V
V_{OH2}	Output High Voltage	V_{CC} < 2.5V, I_{OH} = -100µA	V_{CC} - 0.2V		V

PIN CAPACITANCE[3]

T_A = 25˚C, f = 1.0MHz, V_{CC} = +5.0V

Symbol	Test	Conditions	Min	Typ	Max	Units
C_{OUT}	Output Capacitance (SO)	V_{OUT} = 0V			8	pF
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	V_{IN} = 0V			8	pF

Notes:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) The DC input voltage on any pin should not be lower than -0.5V or higher than V_{CC} + 0.5V. During transitions, the voltage on any pin may undershoot to no less than -1.5V or overshoot to no more than V_{CC} + 1.5V, for periods of less than 20ns.

(3) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

(4) Page Mode, V_{CC} = 5V, 25°C

A.C. CHARACTERISTICS

T_A = -40°C to +85°C, unless otherwise specified.(1)

Symbol	Parameter	V_{CC} = 1.8V-5.5V		V_{CC} = 2.5V-5.5V		Units
		Min.	Max.	Min.	Max.	
f_{SCK}	Clock Frequency	DC	5	DC	10	MHz
t_{SU}	Data Setup Time	40		20		ns
t_H	Data Hold Time	40		20		ns
t_{WH}	SCK High Time	80		40		ns
t_{WL}	SCK Low Time	80		40		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z		50		25	ns
t_{RI}(2)	Input Rise Time		2		2	µs
t_{FI}(2)	Input Fall Time		2		2	µs
t_{HD}	$\overline{HOLD}$ Setup Time	0		0		ns
t_{CD}	$\overline{HOLD}$ Hold Time	10		10		ns
t_V	Output Valid from Clock Low		75		40	ns
t_{HO}	Output Hold Time	0		0		ns
t_{DIS}	Output Disable Time		50		20	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z		100		25	ns
t_{CS}	$\overline{CS}$ High Time	50		15		ns
t_{CSS}	$\overline{CS}$ Setup Time	50		15		ns
t_{CSH}	$\overline{CS}$ Hold Time	50		15		ns
t_{WPS}	$\overline{WP}$ Setup Time	10		10		ns
t_{WPH}	$\overline{WP}$ Hold Time	10		10		ns
t_{WC}(4)	Write Cycle Time		5		5	ms

Power-Up Timing(2)(3)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Notes:

(1) AC Test Conditions:
Input Pulse Voltages: 0.3V_{CC} to 0.7V_{CC}
Input rise and fall times: ≤ 10ns
Input and output reference voltages: 0.5V_{CC}
Output load: current source $I_{OL\ max}$/$I_{OH\ max}$; C_L = 50pF

(2) This parameter is tested initially and after a design or process change that affects the parameter.

(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence to the end of the internal write cycle.

PIN DESCRIPTION

SI: The serial data input pin accepts op-codes, addresses and data. In SPI modes (0,0) and (1,1) input data is latched on the rising edge of the SCK clock input.

SO: The serial data output pin is used to transfer data out of the device. In SPI modes (0,0) and (1,1) data is shifted out on the falling edge of the SCK clock.

SCK: The serial clock input pin accepts the clock provided by the host and used for synchronizing communication between host and CAT25640.

$\overline{CS}$: The chip select input pin is used to enable/disable the CAT25640. When $\overline{CS}$ is high, the SO output is tri-stated (high impedance) and the device is in Standby Mode (unless an internal write operation is in progress). *Every communication session between host and CAT25640 must be preceded by a high to low transition and concluded with a low to high transition of the $\overline{CS}$ input.*

$\overline{WP}$: The write protect input pin will allow all write operations to the device when held high. When $\overline{WP}$ pin is tied low and the WPEN bit in the Status Register (refer to Status Register description, later in this Data Sheet) is set to "1", writing to the Status Register is disabled.

$\overline{HOLD}$: The $\overline{HOLD}$ input pin is used to pause trans–mission between host and CAT25640, without having to retransmit the entire sequence at a later time. To pause, $\overline{HOLD}$ must be taken low and to resume it must be taken back high, with the SCK input low during both transitions. When not used for pausing, the $\overline{HOLD}$ input should be tied to V_{CC}, either directly or through a resistor.

FUNCTIONAL DESCRIPTION

The CAT25640 device supports the Serial Peripheral Interface (SPI) bus protocol, modes (0,0) and (1,1). The device contains an 8-bit instruction register. The instruction set and associated op-codes are listed in Table 1.

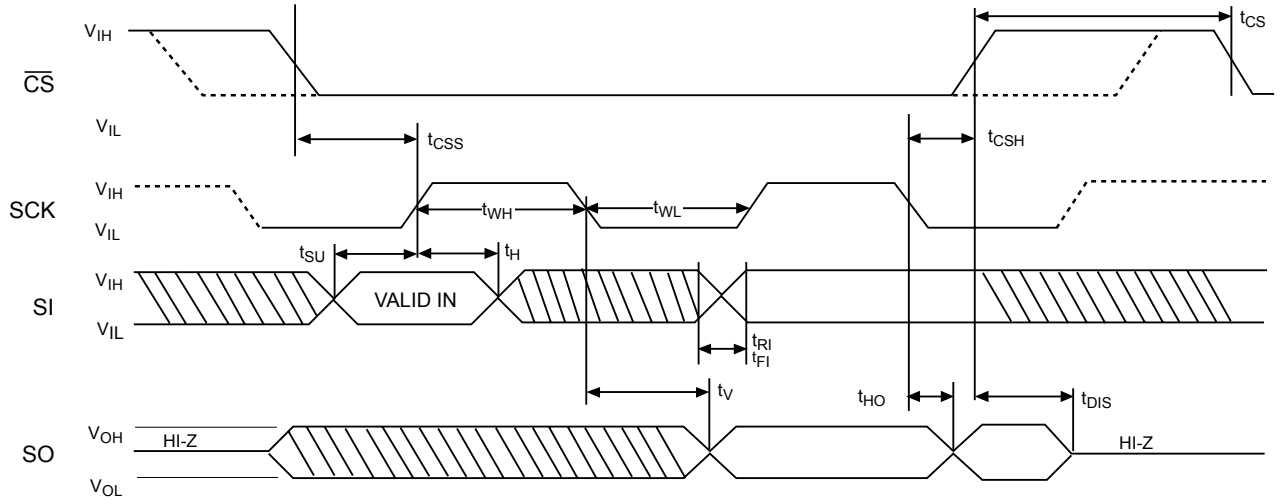
Reading data stored in the CAT25640 is accomplished by simply providing the READ command and an address. Writing to the CAT25640, in addition to a WRITE command, address and data, also requires enabling the device for writing by first setting certain bits in a Status Register, as will be explained later.

After a high to low transition on the $\overline{CS}$ input pin, the CAT25640 will accept any one of the six instruction op-codes listed in Table 1 and will ignore all other possible 8-bit combinations. The communication protocol follows the timing from Figure 1.

Table 1: Instruction Set

Instruction	Opcode	Operation
WREN	0000 0110	Enable Write Operations
WRDI	0000 0100	Disable Write Operations
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory
WRITE	0000 0010	Write Data to Memory

Figure 1. Synchronous Data Timing



Note: Dashed Line = mode (1, 1) - - - - - -

STATUS REGISTER

The Status Register, as shown in Table 2, contains a number of status and control bits.

The $\overline{RDY}$ (Ready) bit indicates whether the device is busy with a write operation. This bit is automatically set to 1 during an internal write cycle, and reset to 0 when the device is ready to accept commands. For the host, this bit is read only.

The WEL (Write Enable Latch) bit is set/reset by the WREN/WRDI commands. When set to 1, the device is in a Write Enable state and when set to 0, the device is in a Write Disable state.

The BP0 and BP1 (Block Protect) bits determine which blocks are currently write protected. They are set by the user with the WRSR command and are non-volatile. The user is allowed to protect a quarter, one half or the entire memory, by setting these bits according to Table 3. The protected blocks then become read-only.

The WPEN (Write Protect Enable) bit acts as an enable for the $\overline{WP}$ pin. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is 1. This condition prevents writing to the status register and to the block protected sections of memory. While hardware write protection is active, only the non-block protected memory can be written. Hardware write protection is disabled when the $\overline{WP}$ pin is high or the WPEN bit is 0. The WPEN bit, $\overline{WP}$ pin and WEL bit combine to either permit or inhibit Write operations, as detailed in Table 4.

Table 2. Status Register

7	6	5	4	3	2	1	0
WPEN	0	0	0	BP1	BP0	WEL	$\overline{RDY}$

Table 3. Block Protection Bits

Status Register Bits		Array Address Protected	Protection
BP1	BP0		
0	0	None	No Protection
0	1	1800-1FFF	Quarter Array Protection
1	0	1000-1FFF	Half Array Protection
1	1	0000-1FFF	Full Array Protection

Table 4. Write Protect Conditions

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

WRITE OPERATIONS

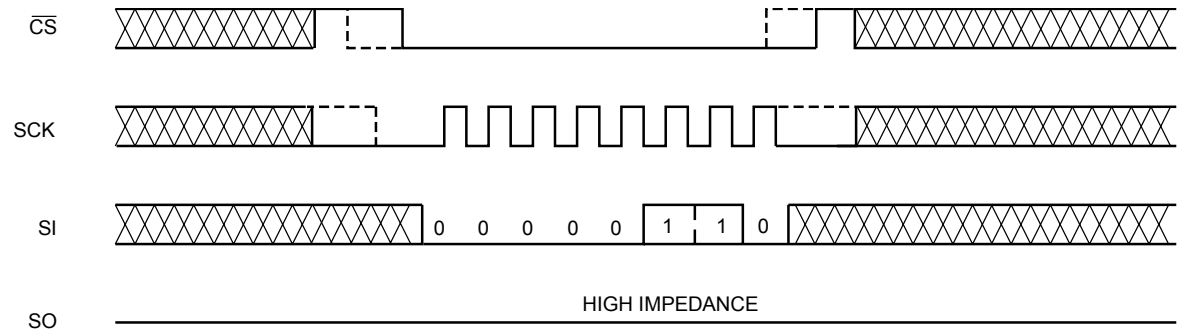
The CAT25640 device powers up into a write disable state. The device contains a Write Enable Latch (WEL) which must be set before attempting to write to the memory array or to the status register. In addition, the address of the memory location(s) to be written must be outside the protected area, as defined by BP0 and BP1 bits from the status register.

Write Enable and Write Disable

The internal Write Enable Latch and the correspon–ding Status Register WEL bit are set by sending the WREN instruction to the CAT25640. Care must be taken to take the $\overline{CS}$ input high after the WREN instruction, as otherwise the Write Enable Latch will not be properly set. WREN timing is illustrated in Figure 2. The WREN instruction must be sent prior any WRITE or WRSR instruction.

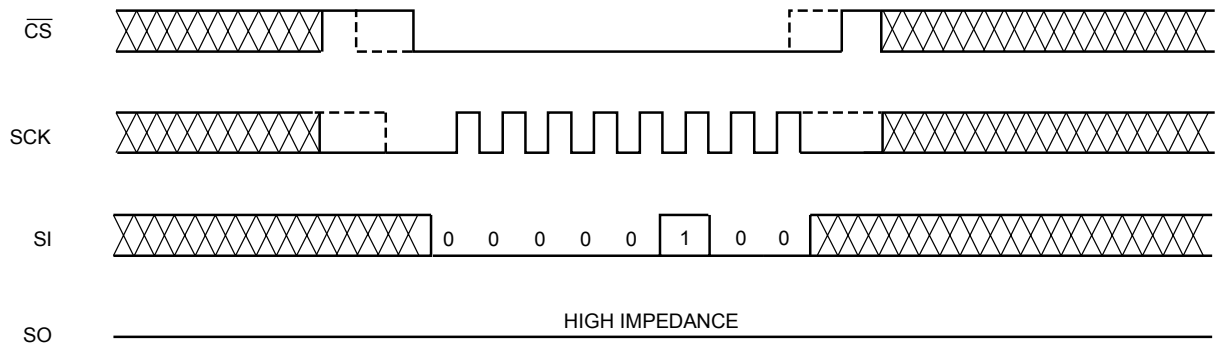
The internal write enable latch is reset by sending the WRDI instruction as shown in Figure 3. Disabling write operations by resetting the WEL bit, will protect the device against inadvertent writes.

Figure 2. WREN Timing



Note: Dashed Line = mode (1, 1) - - - - - -

Figure 3. WRDI Timing



Note: Dashed Line = mode (1, 1) - - - - - -

Byte Write

Once the WEL bit is set, the user may execute a write sequence, by sending a WRITE instruction, a 16-bit address and data as shown in Figure 4. Only 13 significant address bits are used by the CAT25640. The rest are don't care bits, as shown in Table 5. Internal programming will start after the low to high $\overline{CS}$ transition. During an internal write cycle, all commands, except for RDSR (Read Status Register) will be ignored. The $\overline{RDY}$ bit will indicate if the internal write cycle is in progress ($\overline{RDY}$ high), or the the device is ready to accept commands ($\overline{RDY}$ low).

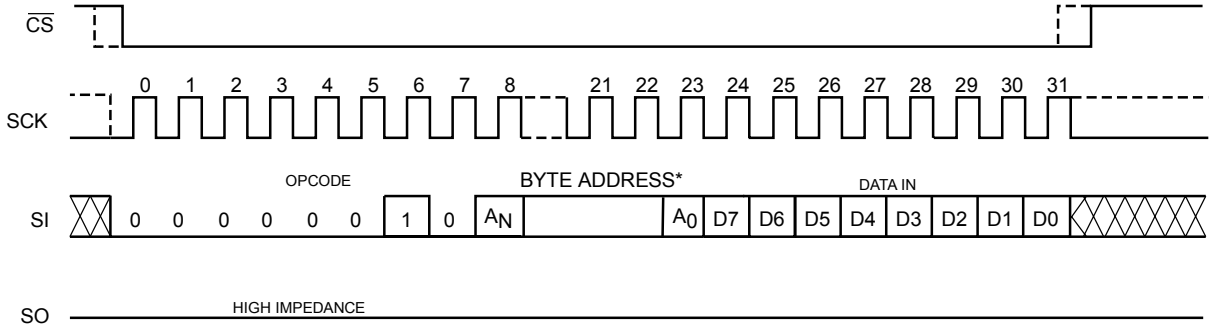
Page Write

After sending the first data byte to the CAT25640, the host may continue sending data, up to a total of 64 bytes, according to timing shown in Figure 5. After each data byte, the lower order address bits are automatically incremented, while the higher order address bits (page address) remain unchanged. If during this process the end of page is exceeded, then loading will "roll over" to the first byte in the page, thus possibly overwriting previouly loaded data. Following completion of the write cycle, the CAT25640 is automatically returned to the write disable state.

Table 5. Byte Address

Device	Address Significant Bits	Address Don't Care Bits	# Address Clock Pulses
CAT25640	A12 - A0	A15 - A13	16

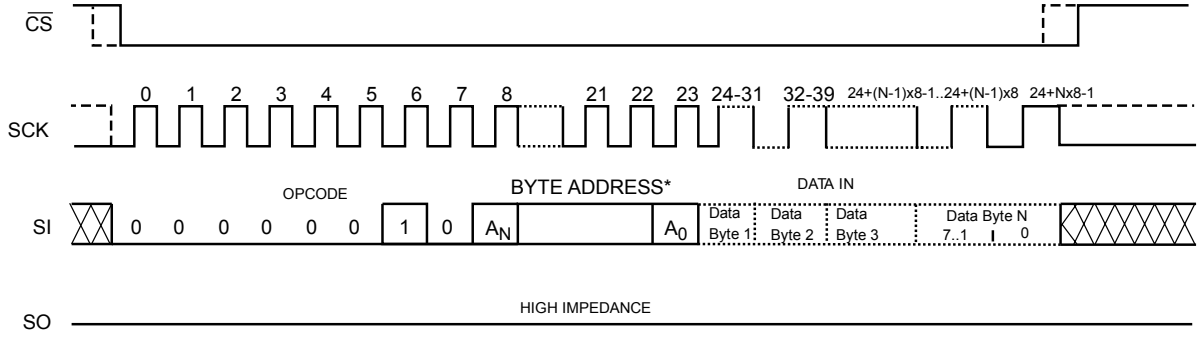
Figure 4. Byte WRITE Timing



* Please check the Byte Address Table (Table 5)

Note: Dashed Line = mode (1, 1) - - - - - -

Figure 5. Page WRITE Timing



*Please check the Byte Address Table. (Table 5)

Note: Dashed Line = mode (1, 1) - - - - - -

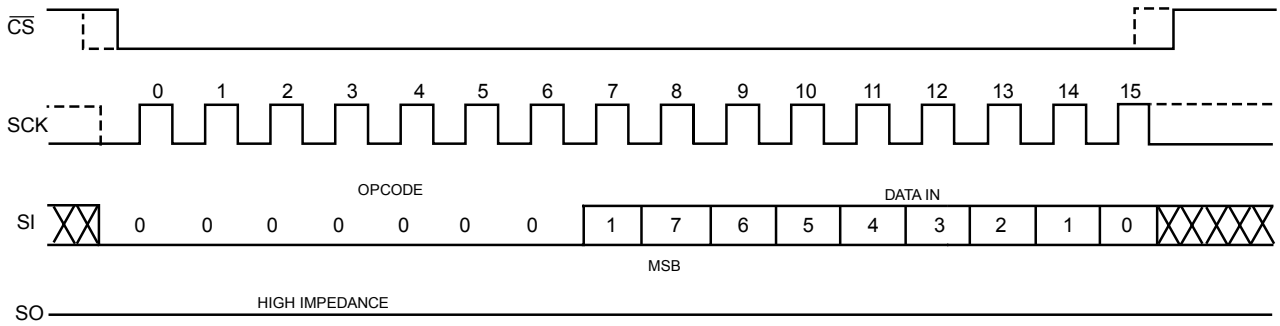
Write Status Register

The Status Register is written by sending a WRSR instruction according to timing shown in Figure 6. Only bits 2, 3 and 7 can be written using the WRSR command.

Write Protection

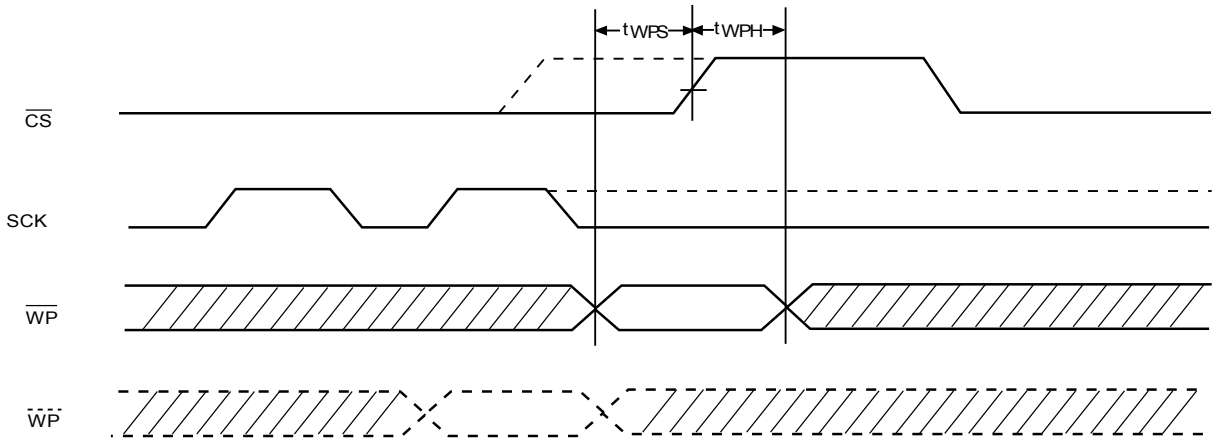
The Write Protect ($\overline{WP}$) pin can be used to protect the Block Protect bits BP0 and BP1 against being inadvertently altered. When $\overline{WP}$ is low and the WPEN bit is set to "1", write operations to the Status Register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the Status Register. The $\overline{WP}$ pin function is blocked when the WPEN bit is set to "0". The $\overline{WP}$ input timing is shown in Figure 7.

Figure 6. WRSR Timing



Note: Dashed Line = mode (1, 1) - - - - - -

Figure 7. $\overline{WP}$ Timing



Note: Dashed Line = mode (1, 1) - - - - - -

READ OPERATIONS

Read from Memory Array

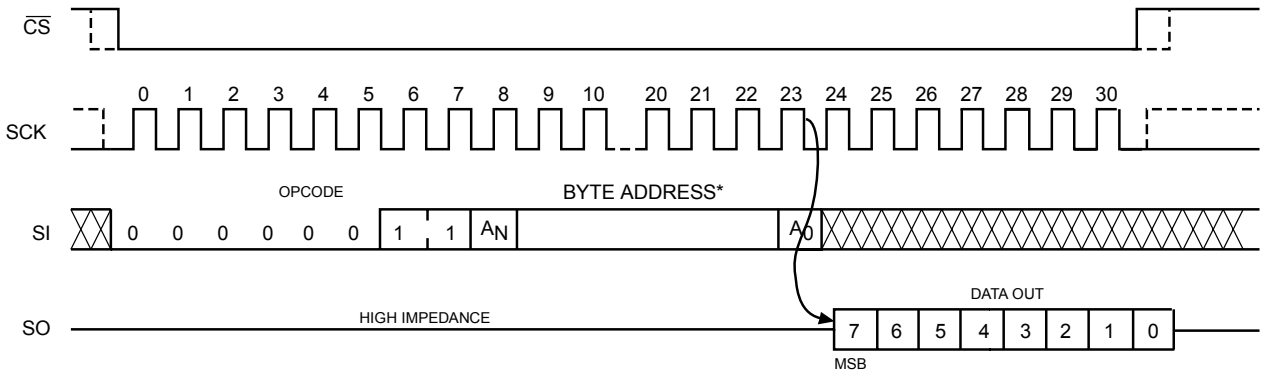
To read from memory, the host sends a READ instruction followed by a 16-bit address (see Table 5 for the number of significant address bits).

After receiving the last address bit, the CAT25640 will respond by shifting out data on the SO pin (as shown in Figure 8). Sequentially stored data can be read out by simply continuing to run the clock. The internal address pointer is automatically incremented to the next higher address as data is shifted out. After reaching the highest memory address, the address counter "rolls over" to the lowest memory address, and the read cycle can be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high.

Read Status Register

To read the status register, the host simply sends a RDSR command. After receiving the last bit of the command, the CAT25640 will shift out the contents of the status register on the SO pin (Figure 9). The status register may be read at any time, including during an internal write cycle.

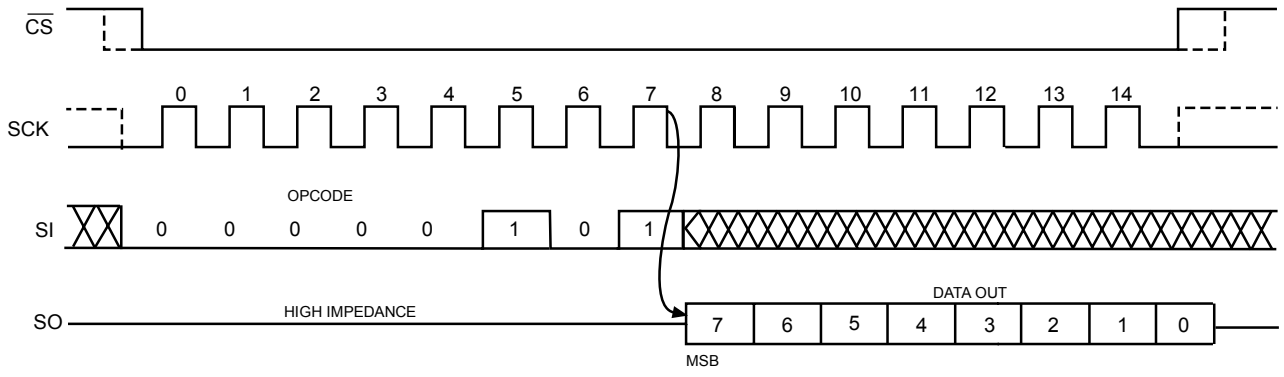
Figure 8. READ Timing



* Please check the Byte Address Table (Table 5).

Note: Dashed Line = mode (1, 1) - - - - - -

Figure 9. RDSR Timing



Note: Dashed Line = mode (1, 1) - - - - - -

Hold Operation

The $\overline{HOLD}$ input can be used to pause communication between host and CAT25640. To pause, $\overline{HOLD}$ must be taken low while SCK is low (Figure 10). During the hold condition the device must remain selected ($\overline{CS}$ low). During the pause, the data output pin (SO) is tri-stated (high impedance) and SI transitions are ignored. To resume communication, $\overline{HOLD}$ must be taken high while SCK is low.

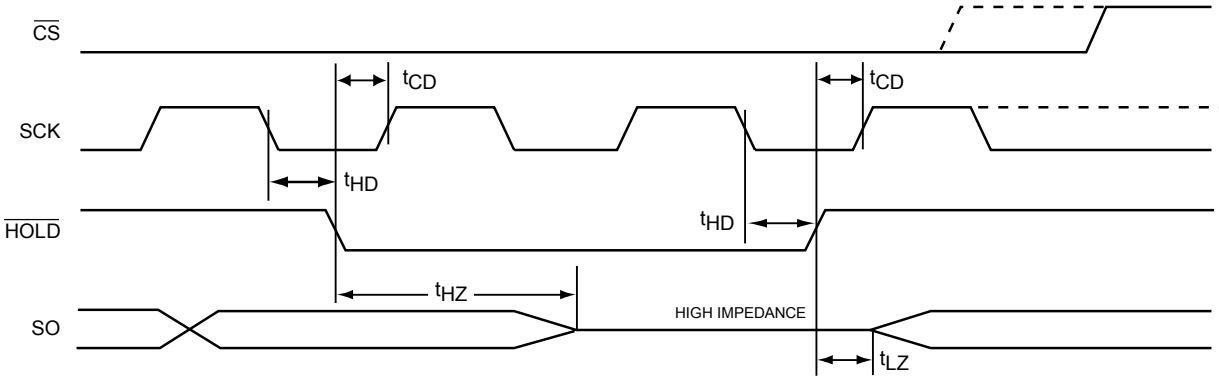
DESIGN CONSIDERATIONS

The CAT25640 device incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi-directional POR behavior protects the device against 'brown-out' failure following a temporary loss of power.

The CAT25640 device powers up in a write disable state and in a low power standby mode. A WREN instruction must be issued prior any writes to the device.

After power up, the $\overline{CS}$ pin must be brought low to enter a ready state and receive an instruction. After a successful byte/page write or status register write, the device goes into a write disable mode. The $\overline{CS}$ input must be set high after the proper number of clock cycles to start the internal write cycle. Access to the memory array during an internal write cycle is ignored and programming is continued. Any invalid op-code will be ignored and the serial output pin (SO) will remain in the high impedance state.

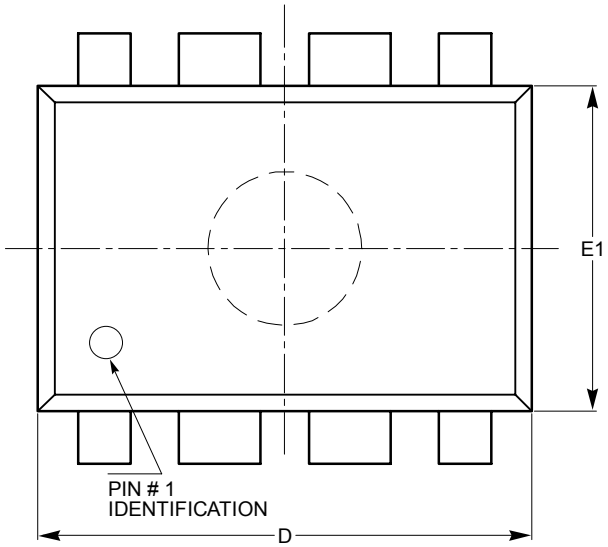
Figure 10. $\overline{HOLD}$ Timing



Note: Dashed Line = mode (1, 1) - - - - - -

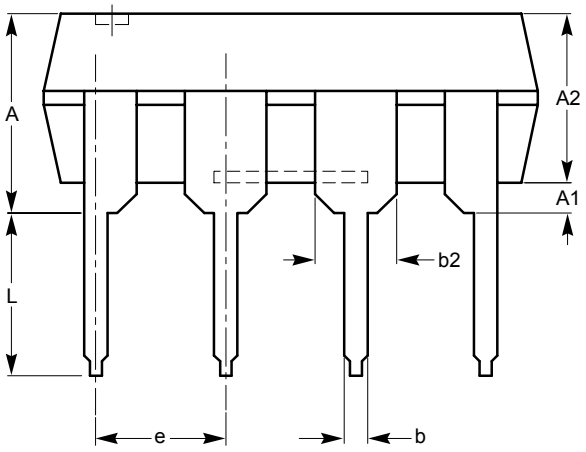
PACKAGE OUTLINES

PDIP 8-Lead 300mils (L)

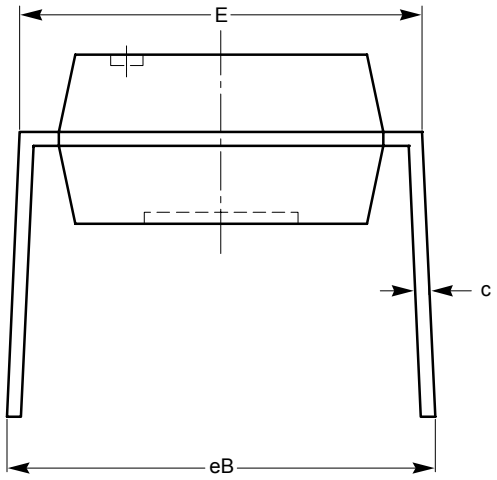


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
e		2.54 BSC	
E1	6.10	6.35	7.11
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

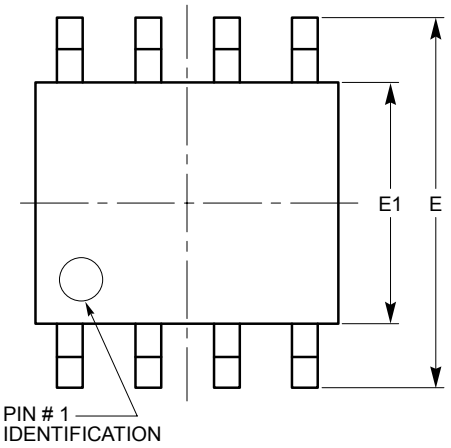


END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

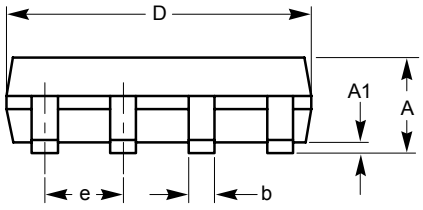
Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

SOIC 8-Lead 150mils (V)

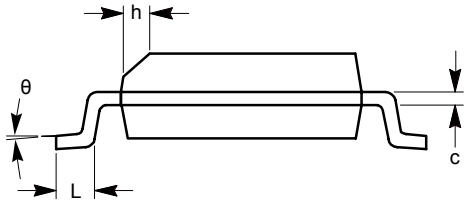


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

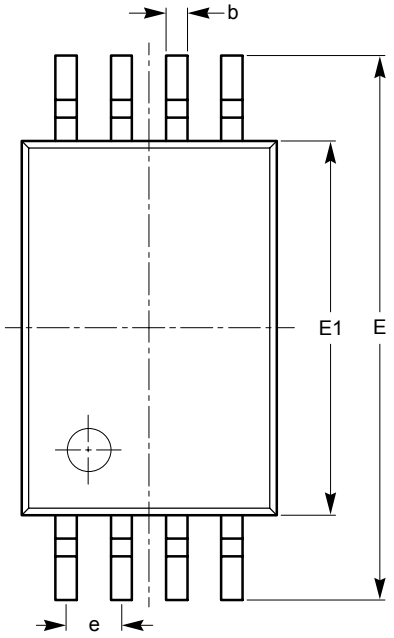
For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:

(1) All dimensions are in millimeters.

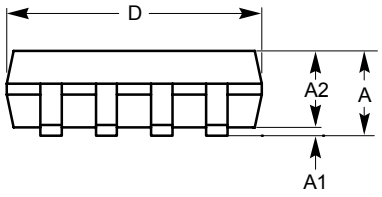
(2) Complies with JEDEC specification MS-012.

TSSOP 8-Lead 4.4mm (Y)

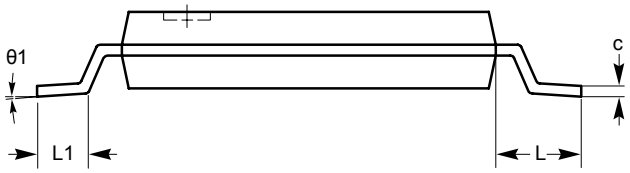


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L		1.00 REF	
L1	0.50	0.60	0.75
θ1	0°		8°



SIDE VIEW

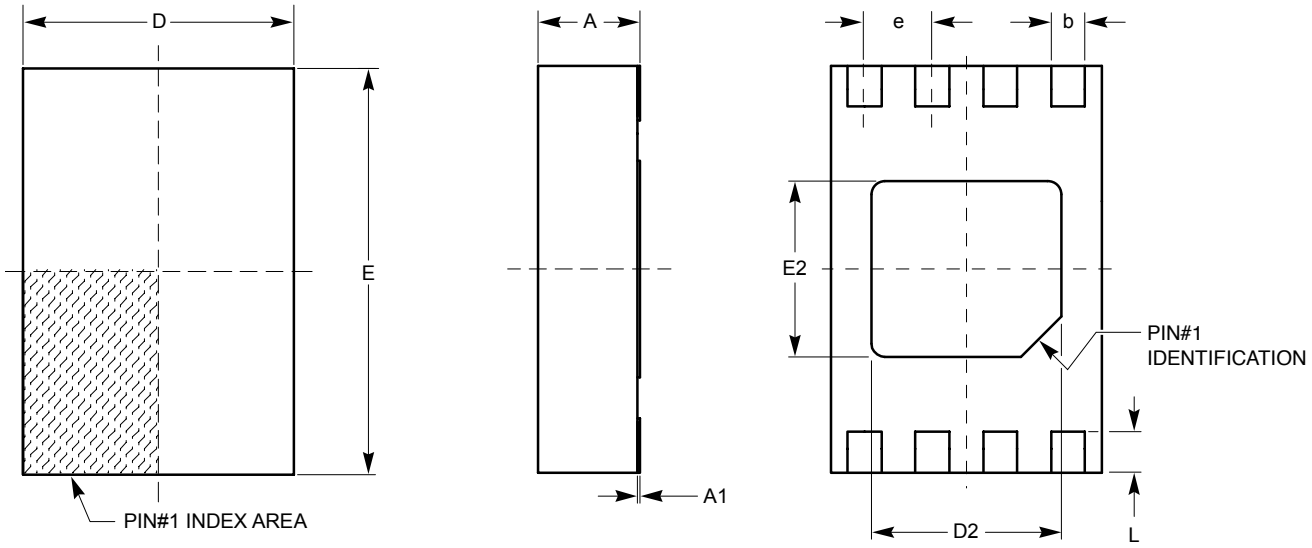


END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

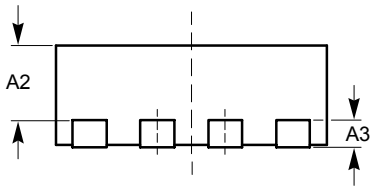
Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC Standard MO-153

TDFN 8-Pad 2 x 3mm (VP2)



TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3		0.20 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
e		050 TYP	
L	0.20	0.30	0.40



FRONT VIEW

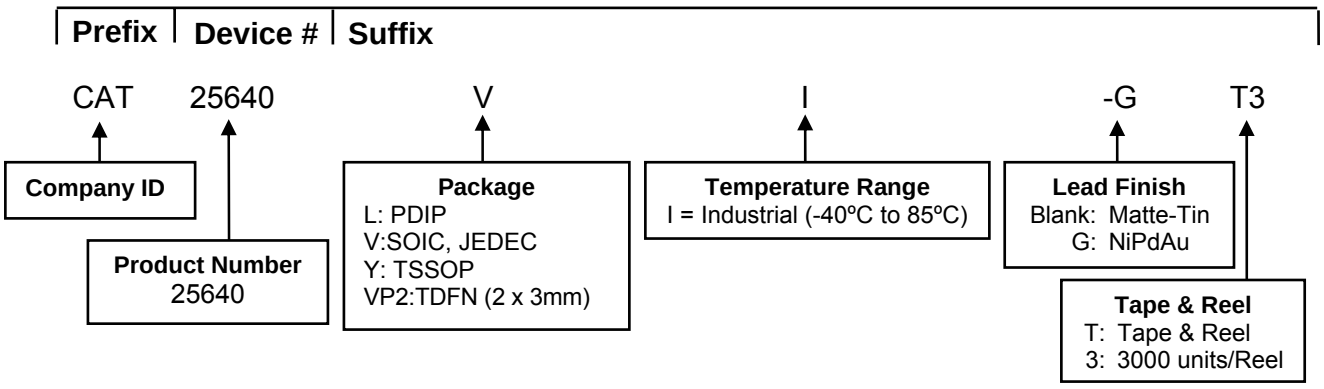
For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:

(1) All dimensions are in millimeters.

(2) Complies with JEDEC Standard MO-229.

EXAMPLE OF ORDERING INFORMATION



Notes:

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).

(2) The standard lead finish is NiPdAu.

(3) The device used in the above example is a CAT25640VI-GT3 (SOIC, Industrial Temperature, NiPdAu, Tape & Reel).

(4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

REVISION HISTORY

Date	Rev.	Comments
5/18/07	A	Initial Issue
10/01/07	B	Update Absolute Maximum Ratings table Update all Package Outline Drawings

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