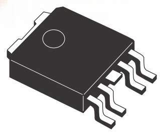
LD49300

3A Very low drop for low output voltage regulator

Feature summary

- Input voltage range:
  V_I = 1.4V to 5.5V
  V_{BIAS} = 3V to 6V
- Stable with ceramic capacitor
- ±1.5% initial tolerance
- Maximum dropout voltage (V_I - V_O) of 400mV over temperature
- Adjustable output voltage down to 0.8V
- Ultra fast transient response (up to 10MHz bandwidth)
- Excellent line and load regulation specifications
- Logic controlled shutdown option
- Thermal shutdown and current limit protection
- Junction temperature range: –25°C to 125°C



PPAK

Description

The LD49300 is a high-bandwidth, low-dropout, 3.0A voltage regulator, ideal for powering core voltages of low-power microprocessors. The LD49300 implements a dual supply configuration allowing for very low output impedance and very fast transient response. The LD49300 requires a bias input supply and a main input supply, allowing for ultra-low input voltages on the main supply rail. The input supply operates from 1.4V to 5.5V and the bias supply requires between 3V and 6V for proper operation. The LD49300 offers fixed output voltages from 0.8V to 1.8V and adjustable output voltages down to 0.8V.

The LD49300 requires a minimum output capacitance for stability, and work optimally with small ceramic capacitors.

Applications

- Graphics processors
- PC Add-In Cards
- Microprocessor core voltage supply
- Low voltage digital ICs
- High Efficiency Linear power supplies
- SMPS post regulators

Order code

Part number	Package	Packaging
LD49300PT08R (1)	PPAK (Tape&Reel)	2500 parts per reel
LD49300PT10R	PPAK (Tape&Reel)	2500 parts per reel
LD49300PT12R	PPAK (Tape&Reel)	2500 parts per reel

1. Adjustable Version.

Contents

1 Typical application circuits

Figure 1. Adjustable version

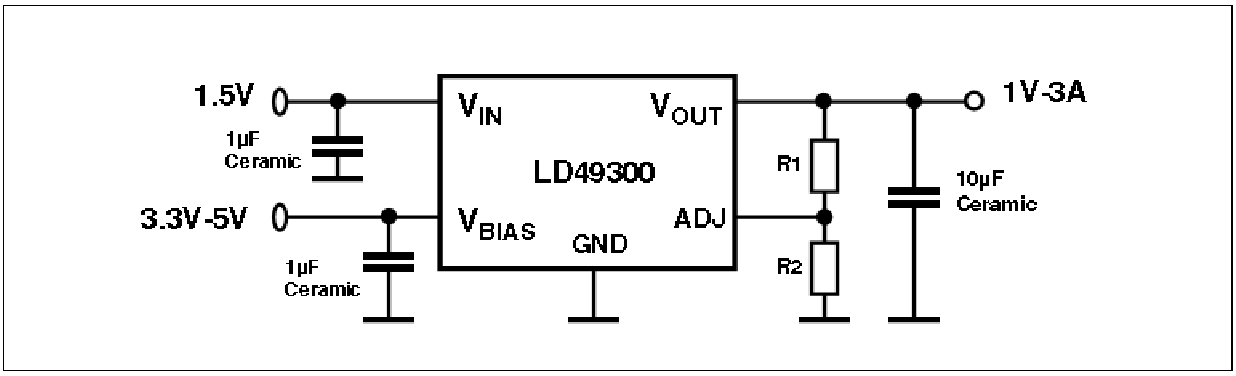
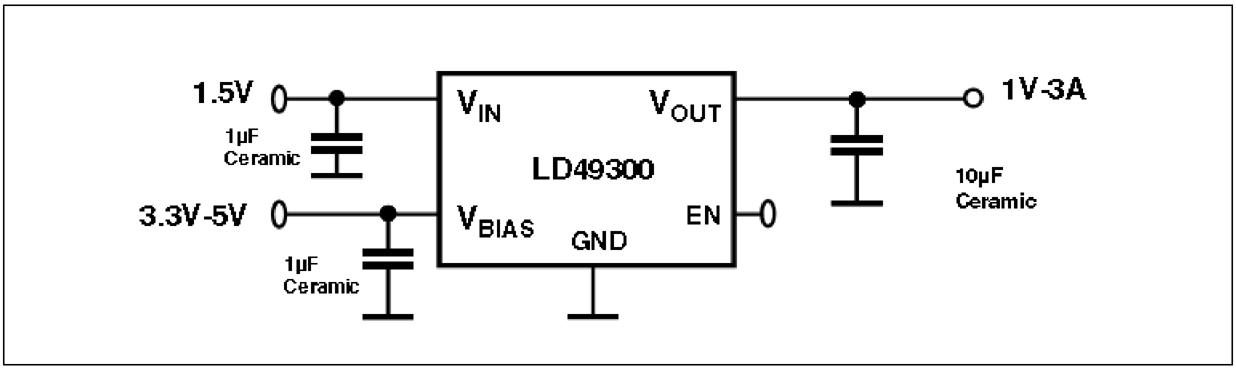


Figure 2. Fixed version with Enable



2 Alternative application circuits

Figure 3. Single supply voltage solution

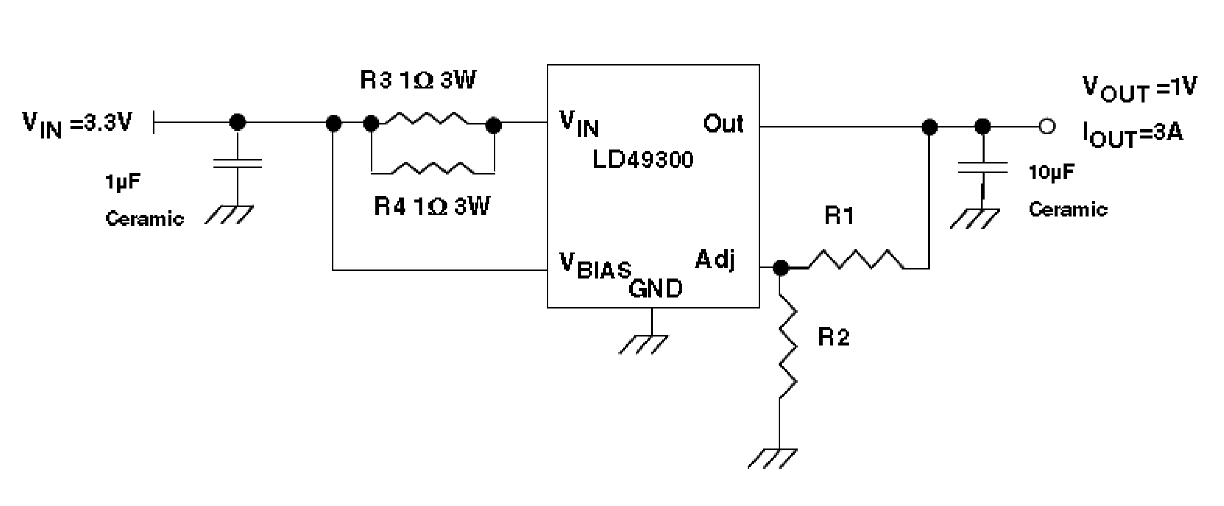
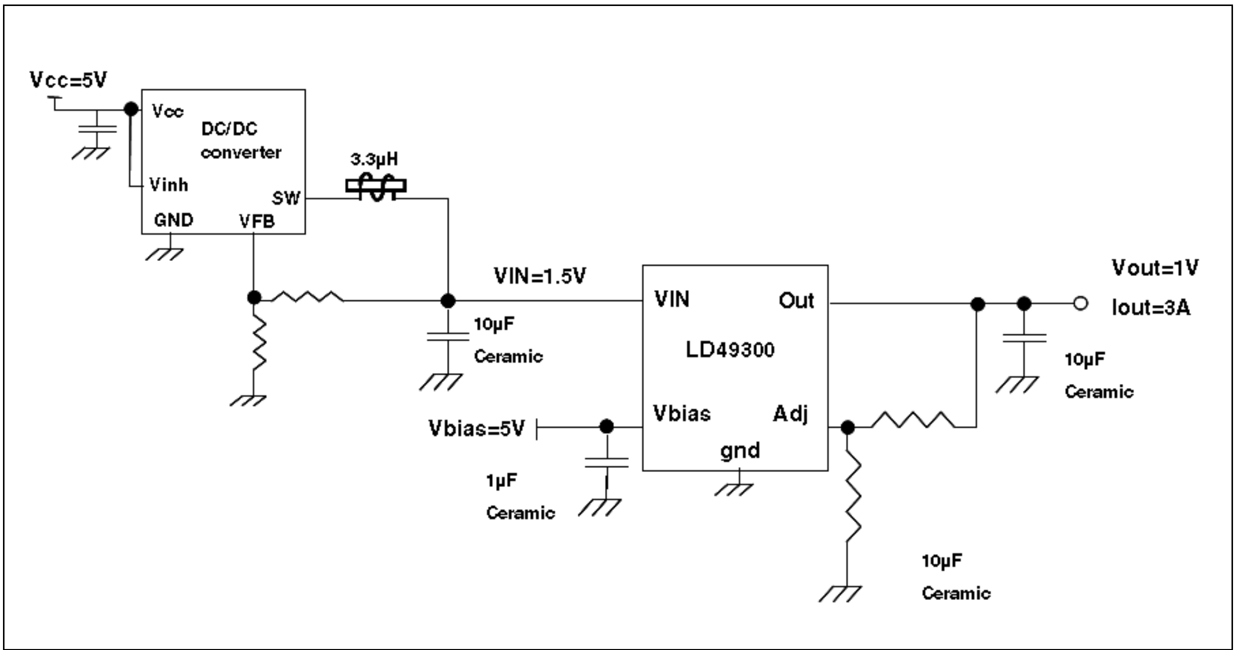


Figure 4. LD49300 plus DC/DC pre-regulator to reduce power dissipation



3 Pin configuration

Figure 5. Pin connections (top view)

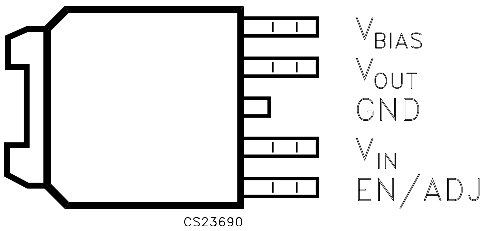
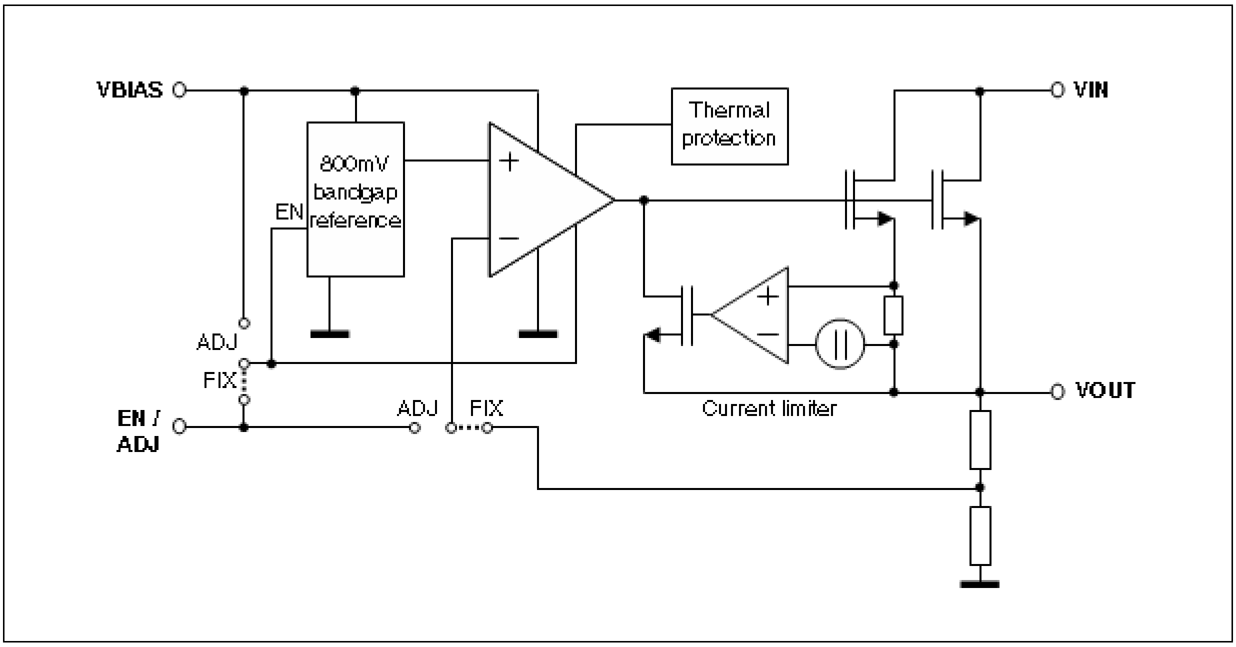


Table 1. Pin description

PIn n°	Symbol	Note
1	EN	Enable (Input): Logic High = Enable, Logic Low = Shutdown.
	ADJ	Adjustable regulator feedback input. Connect to resistor voltage divider.
2	V_{IN}	Input voltage which supplies current to the output power device.
3	GND	Ground (TAB is connected to ground).
4	V_{OUT}	Regulator output.
5	V_{BIAS}	Input bias voltage for powering all circuitry on the regulator with the exception of the output power device.

4 Diagram

Figure 6. Block diagram



5 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Supply voltage	-0.3 to 7	V
V_{OUT}	Output voltage	-0.3 to V_{IN} + 0.3 -0.3 to V_{BIAS} + 0.3	V
V_{BIAS}	BIAS Supply voltage	-0.3 to 7	V
V_{EN}	Enable input voltage	-0.3 to 7	V
P_D	Power dissipation	Internally Limited	
T_{STG}	Storage temperature range	-50 to 150	°C

Note: 1 Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional Operation under these conditions is not implied.

2 All the values are referred to ground.

Table 3. Operating ratings

Symbol	Parameter	Value	Unit
V_{IN}	Supply voltage	1.4 to 5.5	V
V_{OUT}	Output voltage	0.8 to 4.5	V
V_{BIAS}	BIAS Supply voltage	3 to 6	V
V_{EN}	Enable input voltage	0 to V_{BIAS}	V
T_J	Junction temperature range	-25 to 125	°C

6 Electrical characteristics

Table 4. Electrical characteristics

(T_J = -25°C to 125 °C, $V_{BIAS} = V_O$+2.1V [1]; $V_I = V_O$+1V; $V_{EN} = V_{BIAS}$ [2], I_O = 10mA; C_I = 1µF; C_O = 10µF; C_{BIAS} = 1µF; unless otherwise specified. Typical values are referred to T_J = 25°C).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage accuracy	T_J = 25°C, fixed voltage options	-1.5		1.5	%
		Over temperature range	-3		3	
V_{LINE}	Line regulation	$V_I = V_O$+1V to 5.5V	-0.1		0.1	%/V
V_{LOAD}	Load regulation	I_L = 0mA to 3A, $V_{BIAS} \geq 3V$			1	%
V_{DROP}	Dropout voltage (V_I - V_O)	I_L = 1.5A			200	mV
		I_L = 3A			400	
V_{DROP}	Dropout voltage (V_{BIAS}- V_O)	I_L = 3A [1]		1.5	2.1	V
I_{GND}	Ground pin current	I_L = 0mA		4	6	mA
		I_L = 3A		4	6	
I_{GND_SHD}	Ground pin current in shutdown	$V_{EN} \leq 0.4V$ [2]			5	µA
I_{VBIAS}	Current through V_{BIAS}	I_L = 0mA		3	5	mA
		I_L = 3A		3	5	
I_L	Current limit	V_O = 0V	4.5			A
Enable Input [2]						
V_{EN}	Enable input threshold (fixed voltage only)	Regulator Enable	1.4			V
		Regulator Shutdown			0.4	
I_{EN}	Enable pin input current			0.1	1	µA
Reference						
V_{REF}	Reference voltage	T_J = 25°C	0.788	0.8	0.812	V
		Over temperature range	0.776	0.8	0.824	
SVR	Supply voltage rejection	V_I = 2.5V±0.5V, V_O = 1V, F = 120Hz, V_{BIAS} = 3.3V		68		dB

1. For $V_O \leq 1V$, V_{BIAS} dropout specification does not apply due to a minimum 3V V_{BIAS} input.
2. Fixed output voltage version only.

7 Typical characteristics

Figure 7. Reference voltage vs temperature

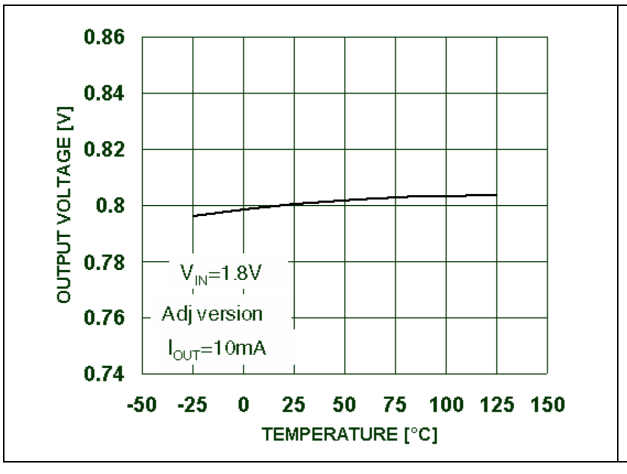


Figure 8. Output voltage vs temperature

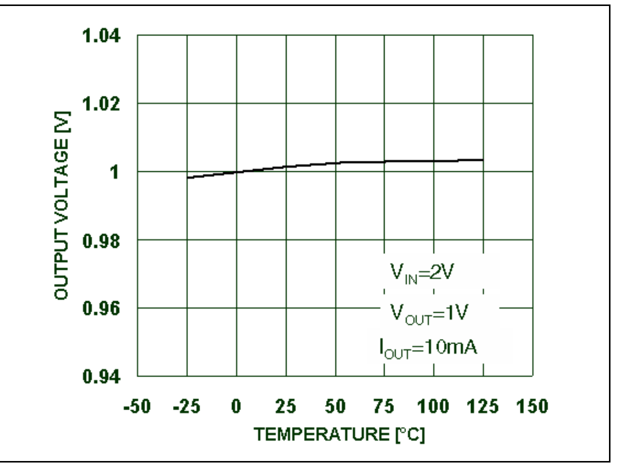


Figure 9. Load regulation vs temperature

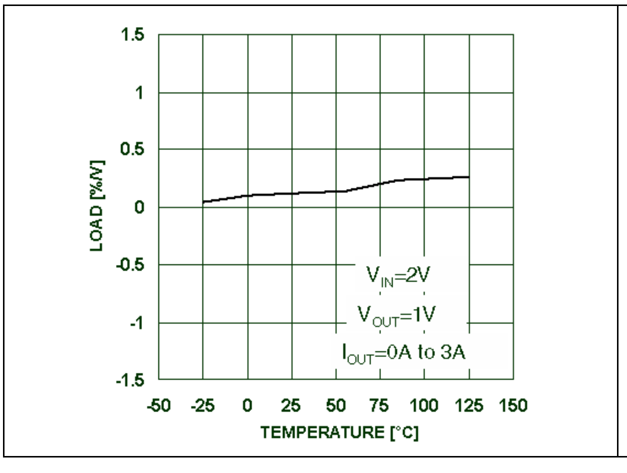


Figure 10. Line regulation vs temperature

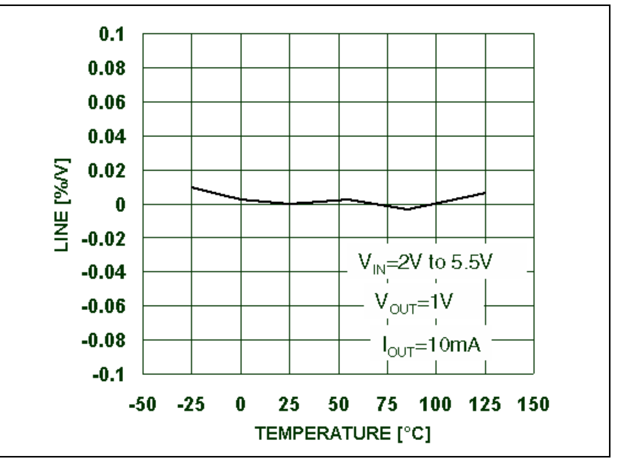


Figure 11. Output voltage vs input voltage

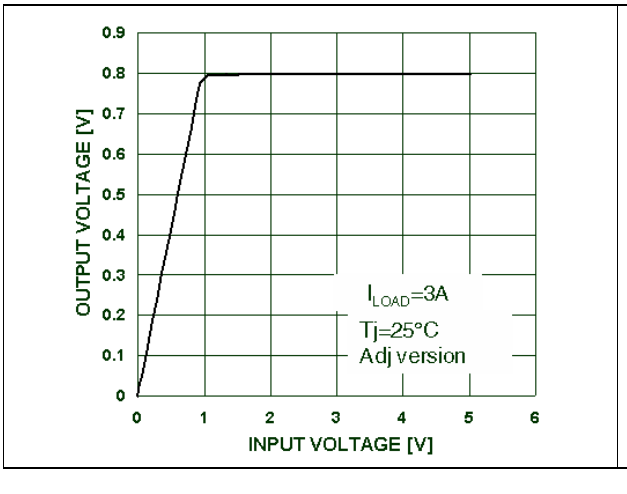


Figure 12. Dropout voltage (V_{IN}-V_{OUT}) vs temperature

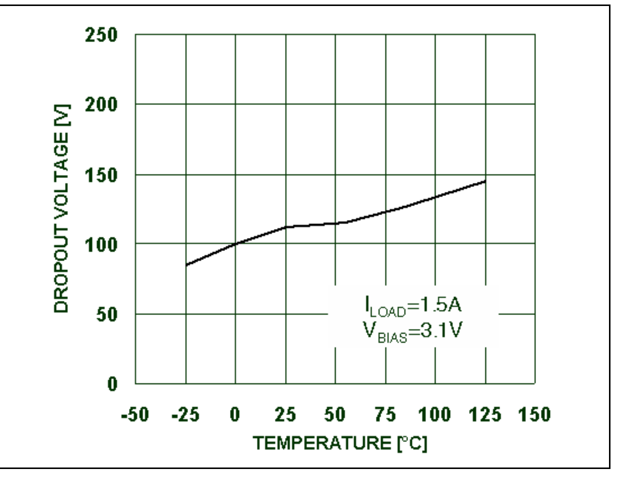


Figure 13. Dropout voltage (V_{IN}-V_{OUT}) vs temperature

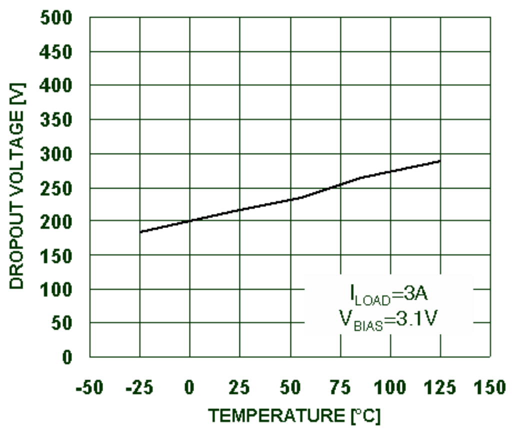


Figure 14. V_{BIAS} pin current vs temperature

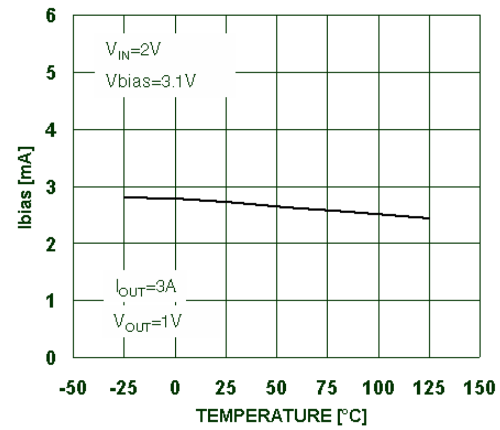


Figure 15. Noise vs frequency

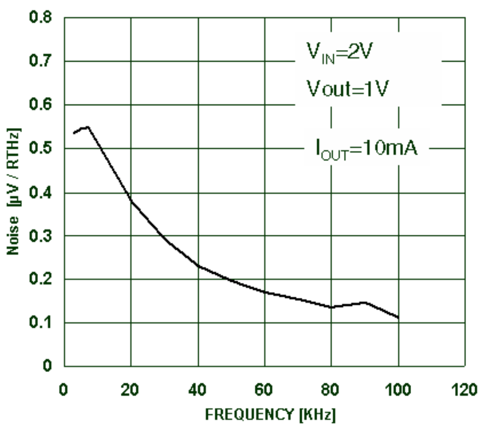


Figure 16. Quiescent current vs temperature

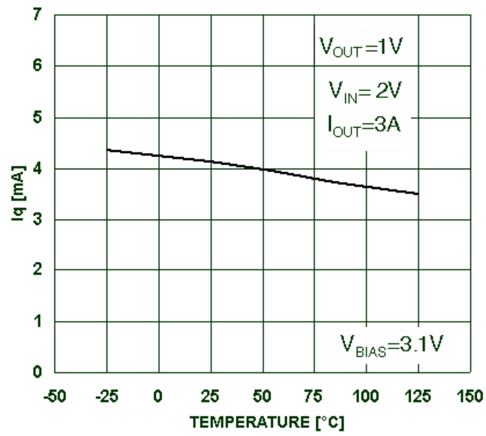


Figure 17. Supply voltage rejection vs output current

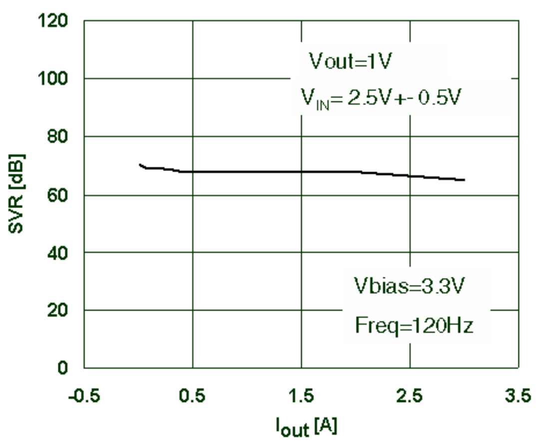


Figure 18. Stability region vs C_{OUT} & High ESR

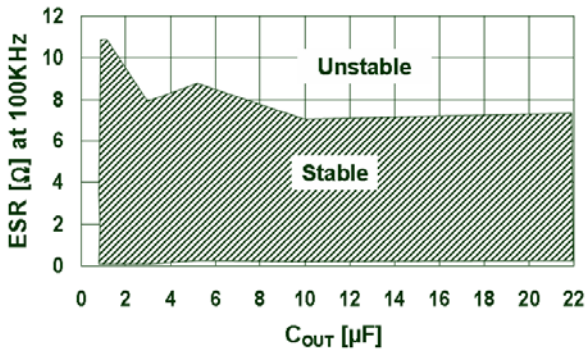


Figure 19. Stability region vs C_{OUT} & Low ESR

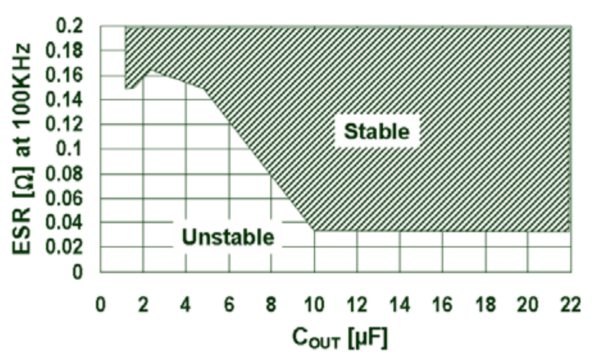
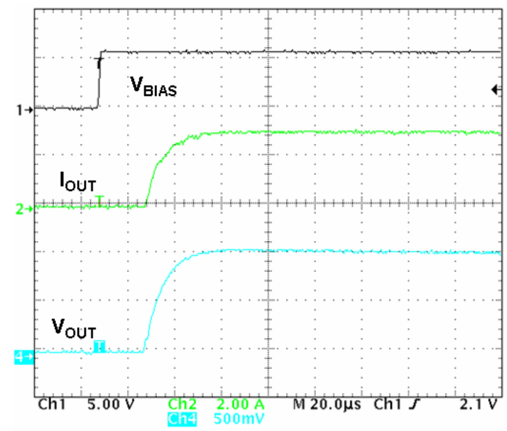
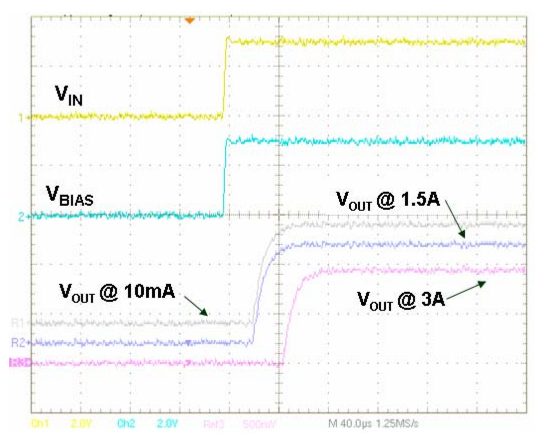


Figure 20. V_{BIAS} Start Up transient (V_{IN} Start Up before V_{BIAS})



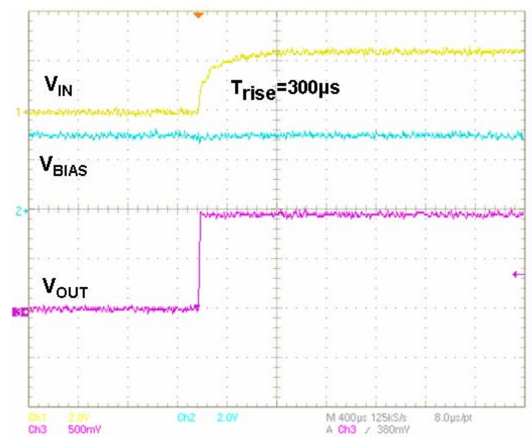
V_{IN}=2V, V_{INH}=V_{BIAS}, I_{OUT}=3A, V_{OUT}=1V, C_{IN}=C_{OUT}=1µF

Figure 21. V_{BIAS} & V_{IN} Start Up transient response (V_{IN} and V_{BIAS} Start Up at the same time)



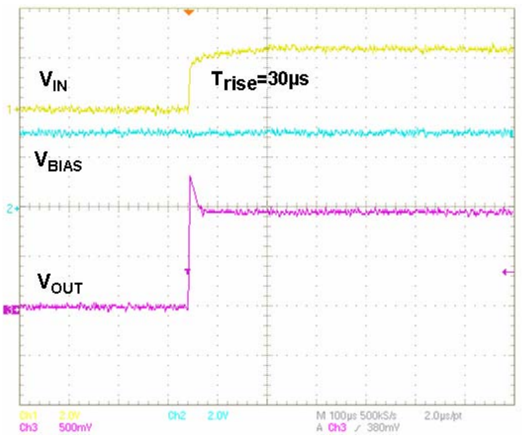
V_{IN}=V_{BIAS}=V_{INH}=3.1V, V_{OUT}=1V, C_{OUT}=1µF

Figure 22. V_{IN} Start Up transient response (V_{BIAS} Start Up before V_{IN})



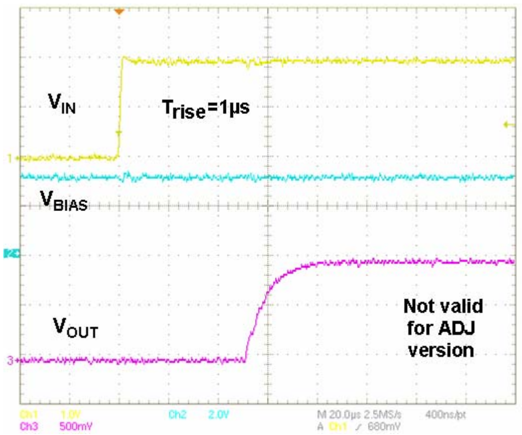
V_{IN}=2.5V, V_{BIAS}=V_{INH}=3.1V, V_{OUT}=1V, C_{OUT}=1µF

Figure 23. V_{IN} Start Up transient response (V_{BIAS} Start Up before V_{IN})



V_{IN}=2.5V, V_{BIAS}=V_{INH}=3.1V, V_{OUT}=1V, C_{OUT}=1µF

Figure 24. V_{IN} Start Up transient response (V_{BIAS} Start Up before V_{IN} and V_{INH}=V_{IN})



V_{IN}=V_{INH}=2.5V, V_{BIAS}=3.1V, V_{OUT}=1V, C_{OUT}=1µF

Figure 25. Load transient response

V_{IN}=2.5V, V_{BIAS}=5V, V_{OUT}=1.8V, I_{OUT}=10mA to 3A, C_{OUT}=10µF

8 Application hints

The LD49300 is an ultra-high performance, low dropout linear regulator, designed for high current application that requires fast transient response. The LD49300 operates from two input voltages, to reduce dropout voltage. The LD49300 is designed so that a minimum of external component are necessary.

8.1 Input supply voltage (V_{IN})

V_{IN} provides the power input current to the LD49300. The minimum input voltage can be as low as 1.4V, allowing conversion from very low voltage supplies to achieve low output voltage levels with very low power dissipation.

8.2 Bias supply voltage (V_{BIAS})

The LD49300 control circuitry is supplied the V_{BIAS} pin which requires a very low bias current (3mA typ.) even at the maximum output current level (3A). A bypass capacitor on the bias pin is recommended to improve the performance of the LD49300 during line and load transient. The small ceramic capacitor from V_{BIAS} to ground reduces high frequency noise that could be injected into the control circuitry from the bias rail. In typical applications a 1µF ceramic chip capacitor may be used. The V_{BIAS} input voltage must be 2.1V above the output voltage, with a minimum V_{BIAS} input voltage of 3V.

8.3 External capacitors

To assure regulator stability, input and output capacitors are required as shown in the typical application circuit.

8.4 Output capacitor

The LD49300 requires a minimum output capacitance to maintain stability. A ceramic chip capacitor of at least 1µF is required. However, specific capacitor selection could be needed to ensure the transient response. A 1µF ceramic chip capacitor satisfies most applications but 10µF is recommended to ensure better transient performances. In applications where the V_{IN} level is close to the maximum operating voltage (V_{IN}>4V), it is strongly recommended to use an output capacitors of, at least, 10µF in order to avoid over-voltage stress on the Input/output power pins during short circuit conditions due to parasitic inductive effect. The output capacitor must be located as close as possible to the output pin of the LD49300. The ESR (equivalent series resistance) of the output capacitor must be within the "STABLE" region as shown in the typical characteristics figures. Both ceramic and tantalum capacitors are suitable.

8.5 Minimum load current

The LD49300 does not require a minimum load to maintain output voltage regulation.

8.6 V_{IN} and V_{BIAS} power sequencing

In common applications where the power on transient of V_{IN} and V_{BIAS} voltages are not particularly fast (T_r>100µs), no power sequencing is required. Where voltage transient input (T_r<100µs) is very fast, it is recommended to have the V_{IN} voltage present before or, at least, at the same time as the V_{BIAS} voltage in order to avoid overvoltage spikes during the power on transient (refer to the figures in the typical characteristics). Where V_{IN} transient input (T_r<<100µs) is very fast for the fixed V_{OUT} versions, it is possible to avoid start-up overvoltage spikes by pulling the V_{INH} pin up to V_{IN} voltage (refer to relative typical characteristics figures at pages 11 and 12).

8.7 Power dissipation/heatsinking

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$P_D = V_{IN} \times I_{IN} + V_{BIAS} \times I_{BIAS} - V_{OUT} \times I_{OUT}$

Where:

- V_{IN}, Input supply voltage
- V_{BIAS}, Bias supply voltage
- V_{OUT}, Output voltage
- I_{OUT}, Load current

From this data, we can calculate the thermal resistance (θ_{SA}) required for the heat sink using the following formula:

$\theta_{SA} = (T_J - T_A/P_D) - (\theta_{JC} + \theta_{CS})$

The maximum allowed temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

$T_{Rmax} = T_{Jmax} - T_{Amax}$

The maximum allowable value for junction to ambient thermal resistance, θ_{JA}, can be calculated using the formula:

$\theta_{JAmax} = T_{Rmax} / P_D$

This part is available for the PPAK package.

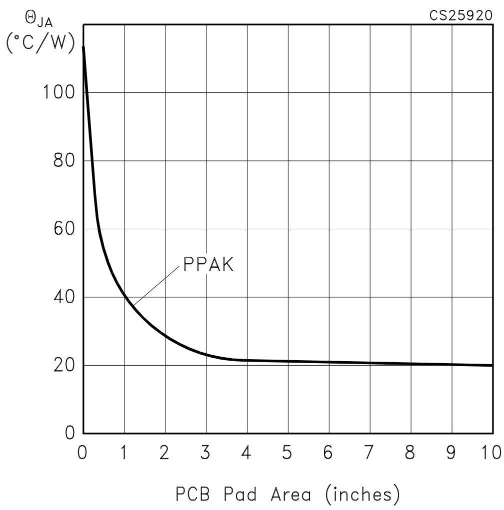
The thermal resistance depends on the amount of copper area or heat sink, and on air flow. If the maximum allowable value of θ_{JA} calculated above is ≥100 °C/W for the PPAK package, no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable θ_{JA} falls below these limits, a heat sink is required as described below.

8.8 Heatsinking PPAK package

The PPAK package uses the copper plane on the PCB as a heatsink. The tab of these packages is soldered to the copper plane for heat sinking. It is also possible to use the PCB ground plane a heatsink. This area can be the inner GND layer of a multi-layer PCB, or, in a dual layer PCB, it can be an unbroken GND area on the opposite side where the IC is situated with a dissipating area thermally connected through vias holes, filled by solder.

Figure 26 shows a curve for θ_{JA} of the PPAK package for different copper area sizes, using a typical PCB with 1/16 in thick G10/FR4.

Figure 26. θ_{JA} vs Copper Area for PPAK package



8.9 Adjustable regulator design

The LD49300 adjustable version allows fixing output voltage anywhere between 0.8V and 4.5V using two resistors as shown in the typical application circuit. For example, to fix the R1 resistor value between V_{OUT} and the ADJ pin, the resistor value between ADJ and GND (R2) is calculated by:

$R2 = R1\ [0.8/(V_{OUT} - 0.8)]$

Where V_{OUT} is the desired output voltage.

It is suggested to use R1 values lower than 10KΩ to obtain better load transient performances. Even, higher values up to 100KΩ are suitable.

8.10 Enable

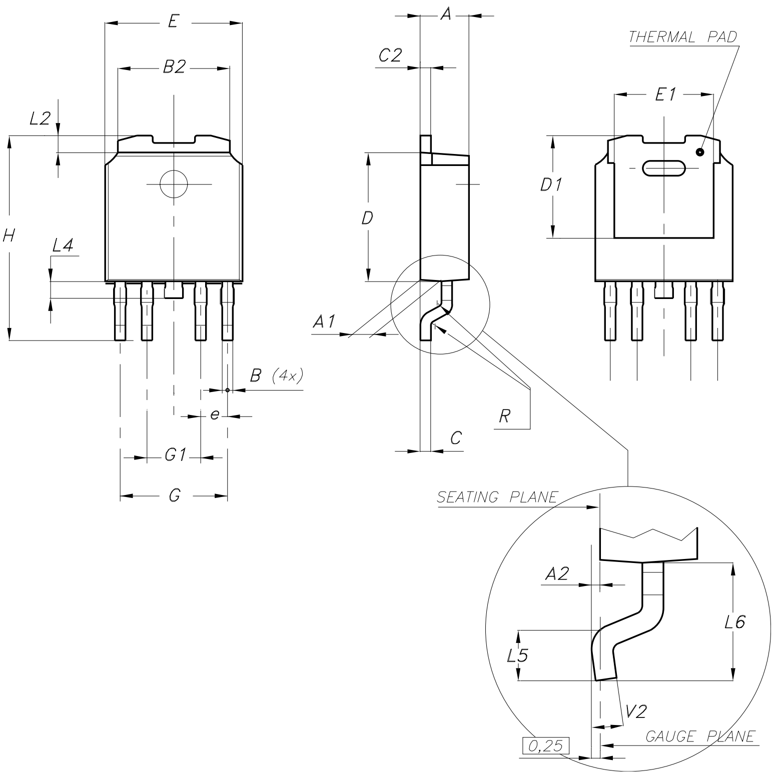
The fixed output voltage versions of LD49300 feature an active high Enable input (EN) that allows on-off control of the regulator. The EN input threshold is guaranteed between 0.4V and 1.4V, for simple logic interfacing. The regulator is set in shut down mode when V_{EN}<0.4V and it is in operating mode (V_{OUT} activated) when V_{EN}>1.4V. If not in use, the EN pin must be tied directly to the V_{IN} to keep the regulator continuously activated. The En pin must not be left at high impedance.

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

PPAK MECHANICAL DATA

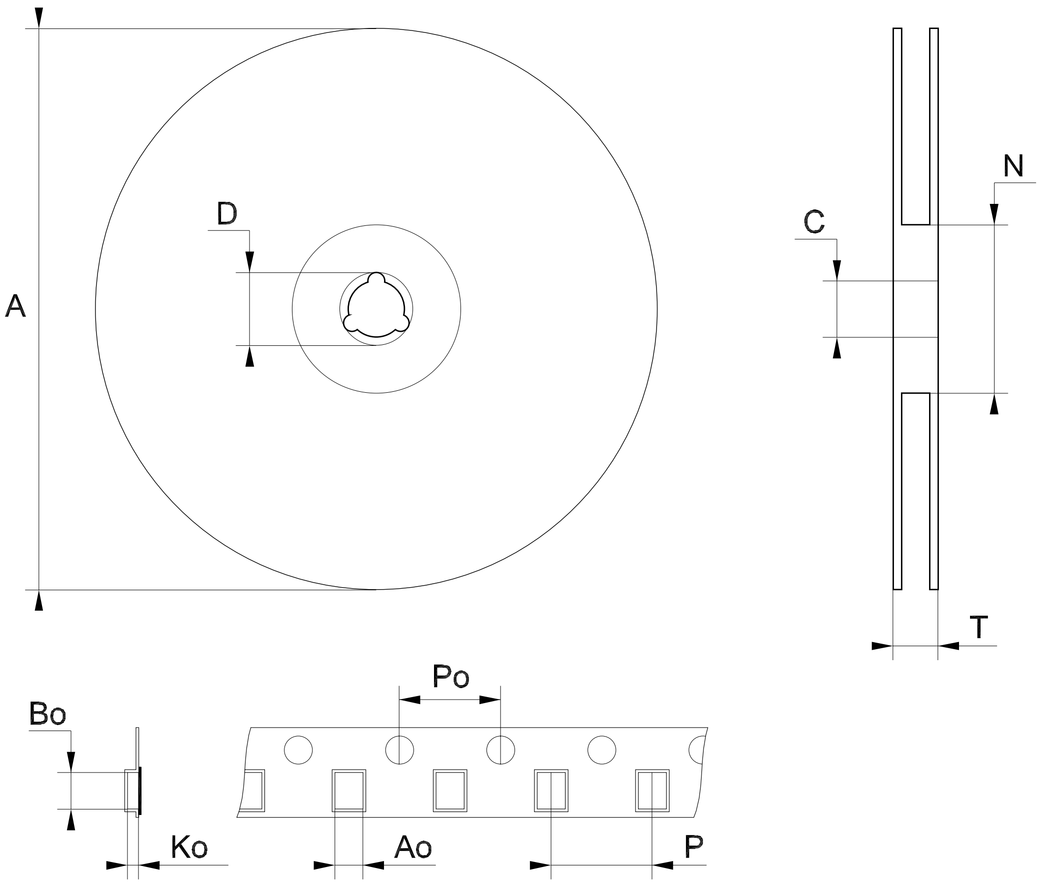
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.4		0.6	0.015		0.023
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.201	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		1.27			0.050	
G	4.9		5.25	0.193		0.206
G1	2.38		2.7	0.093		0.106
H	9.35		10.1	0.368		0.397
L2		0.8	1		0.031	0.039
L4	0.6		1	0.023		0.039
L5	1			0.039		
L6		2.8			0.110	



0078180-E

Tape & Reel DPAK-PPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.80	6.90	7.00	0.268	0.272	0.2.76
Bo	10.40	10.50	10.60	0.409	0.413	0.417
Ko	2.55	2.65	2.75	0.100	0.104	0.105
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	7.9	8.0	8.1	0.311	0.315	0.319



Note: Drawing not in scale

10 Revision history

Table 5. Revision history

Date	Revision	Changes
20-Nov-2006	1	Initial release.
01-Dec-2006	2	Add note in cover page : *Order code*.

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