

# International IR Rectifier

PD-95592

## IRL520NSPbF IRL520NLPbF

HEXFET® Power MOSFET

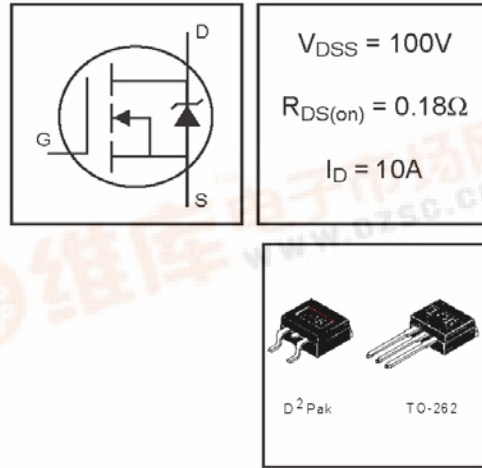
- Logic-Level Gate Drive
- Advanced Process Technology
- Surface Mount (IRL520NS)
- Low-profile through-hole (IRL520NL)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

### Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRL520NL) is available for low-profile applications.



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}^{\text{⑤}}$	10	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}^{\text{⑤}}$	7.1	
$I_{DM}$	Pulsed Drain Current ①⑤	35	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation	3.8	W
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	48	W
	Linear Derating Factor	0.32	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 16$	V
$E_{AS}$	Single Pulse Avalanche Energy②⑤	85	mJ
$I_{AR}$	Avalanche Current①	6.0	A
$E_{AR}$	Repetitive Avalanche Energy①	4.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
$T_J$	Operating Junction and	-55 to +175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

### Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	3.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	---	40	



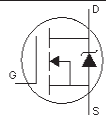
# IR520NS/LPbF

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## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	---	---	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	---	0.11	---	$V/^\circ C$	Reference to $25^\circ C, I_D = 1mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	---	---	0.18	$\Omega$	$V_{GS} = 10V, I_D = 6.0A$ ④
		---	---	0.22		$V_{GS} = 5.0V, I_D = 6.0A$ ④
		---	---	0.26		$V_{GS} = 4.0V, I_D = 5.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	---	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	3.1	---	---	S	$V_{DS} = 25V, I_D = 6.0A$ ⑤
$I_{DSS}$	Drain-to-Source Leakage Current	---	---	25	A	$V_{DS} = 100V, V_{GS} = 0V$
		---	---	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 150^\circ C$
$I_{GSS}$	Gate-to-Source Forward Leakage	---	---	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	---	---	-100		$V_{GS} = -16V$
$Q_g$	Total Gate Charge	---	---	20	nC	$I_D = 6.0A$
$Q_{gs}$	Gate-to-Source Charge	---	---	4.6		$V_{DS} = 80V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	---	---	10		$V_{GS} = 5.0V, \text{See Fig. 6 and 13}$ ④⑤
$t_{d(on)}$	Turn-On Delay Time	---	4.0	---		ns
$t_r$	Rise Time	---	35	---	$I_D = 6.0A$	
$t_{d(off)}$	Turn-Off Delay Time	---	23	---	$R_G = 11\Omega, V_{GS} = 5.0V$	
$t_f$	Fall Time	---	22	---	$R_D = 8.2\Omega, \text{See Fig. 10}$ ④⑤	
$L_S$	Internal Source Inductance	---	7.5	---	nH	Between lead, and center of die contact
$C_{iss}$	Input Capacitance	---	440	---	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	---	97	---		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	---	50	---		$f = 1.0MHz, \text{See Fig. 5}$ ⑤

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	---	---	10	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	---	---	35		
$V_{SD}$	Diode Forward Voltage	---	---	1.3	V	$T_J = 25^\circ C, I_S = 6.0A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	---	110	160	ns	$T_J = 25^\circ C, I_F = 6.0A$
$Q_{rr}$	Reverse Recovery Charge	---	410	620	nC	$di/dt = 100A/\mu s$ ④⑤
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

### Notes:

① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )

②  $V_{DD} = 25V$ , starting  $T_J = 25^\circ C$ ,  $L = 4.7mH$   
 $R_G = 25\Omega, I_{AS} = 6.0A$ . (See Figure 12)

③  $I_{SD} \leq 6.0A, di/dt \leq 340A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ C$

④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .

⑤ Uses IRL520N data and test conditions

\*\* When mounted on 1" square PCB ( FR-4 or G-10 Material ).

For recommended footprint and soldering techniques refer to application note #AN-994.

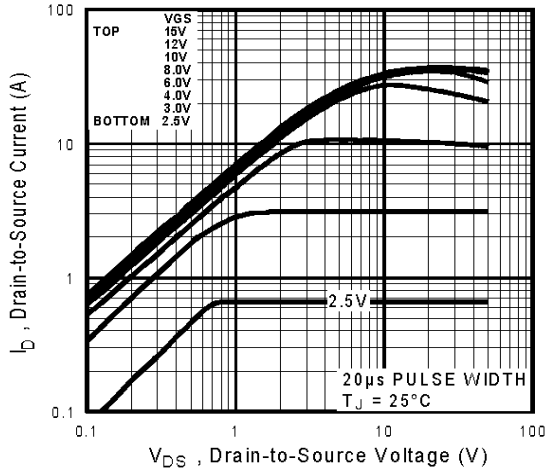


Fig 1. Typical Output Characteristics

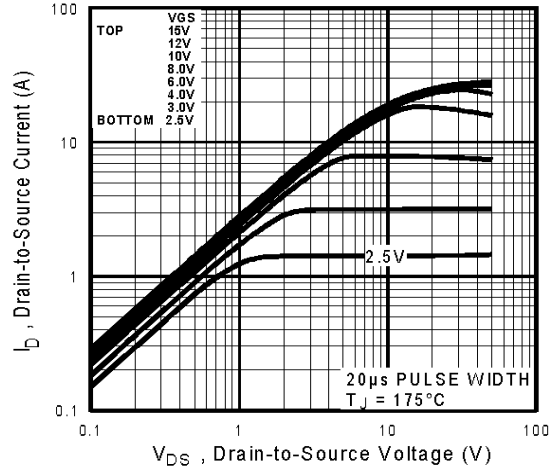


Fig 2. Typical Output Characteristics

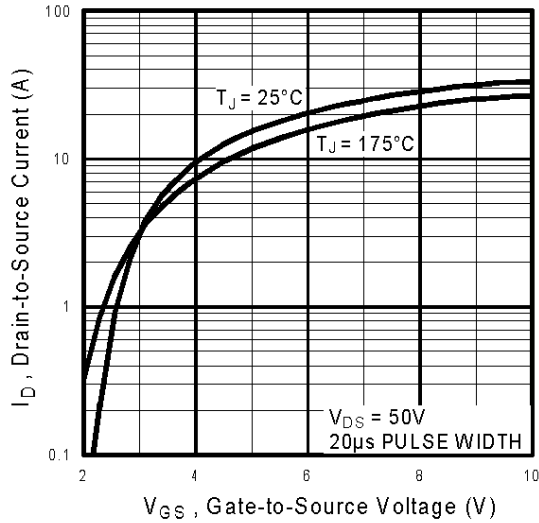


Fig 3. Typical Transfer Characteristics

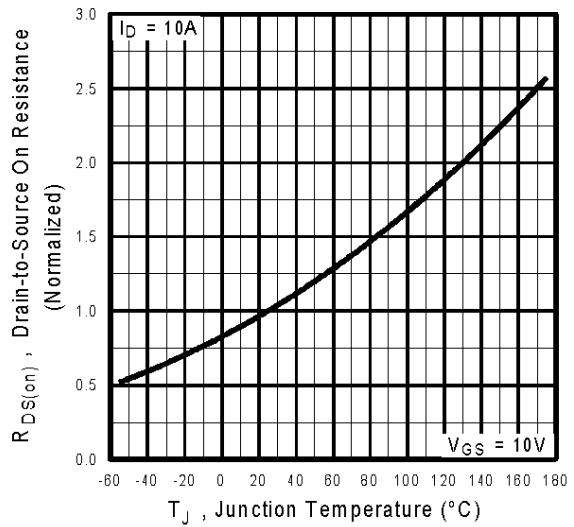
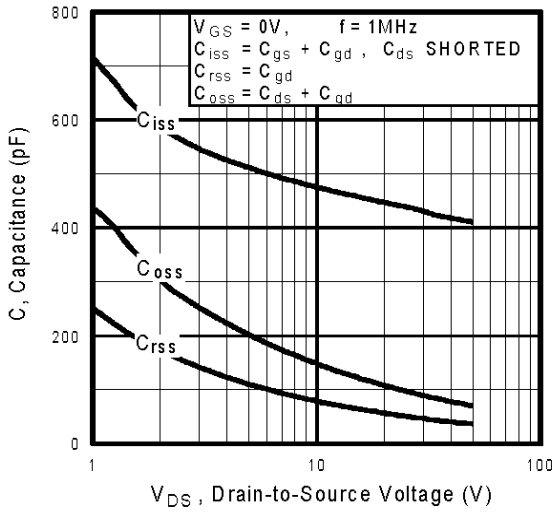


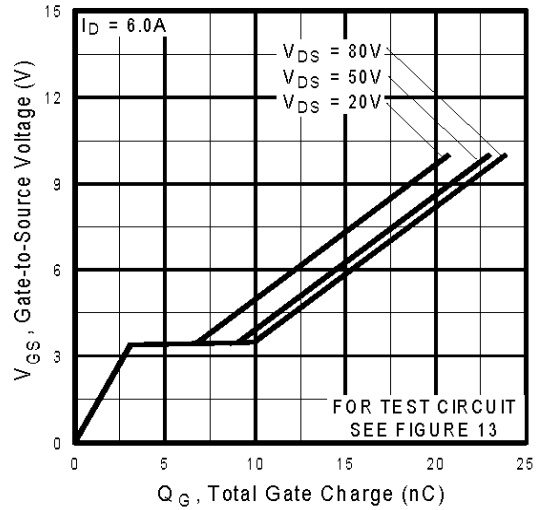
Fig 4. Normalized On-Resistance Vs. Temperature

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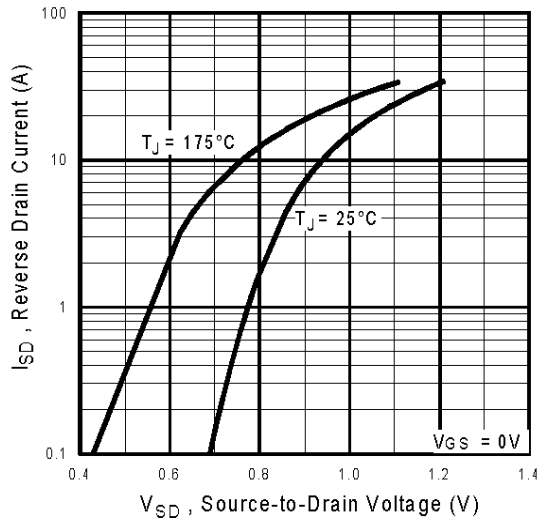
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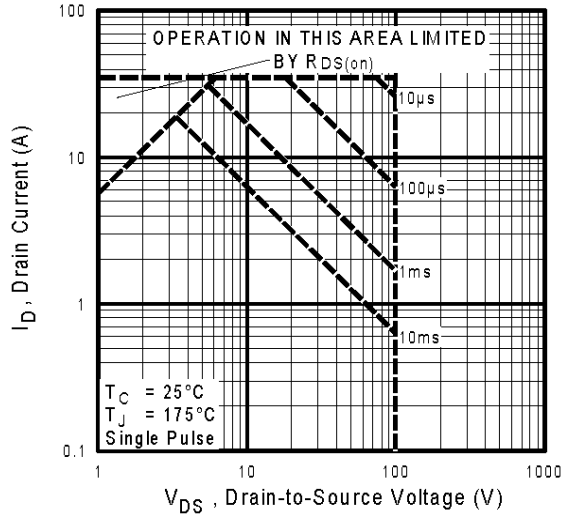
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



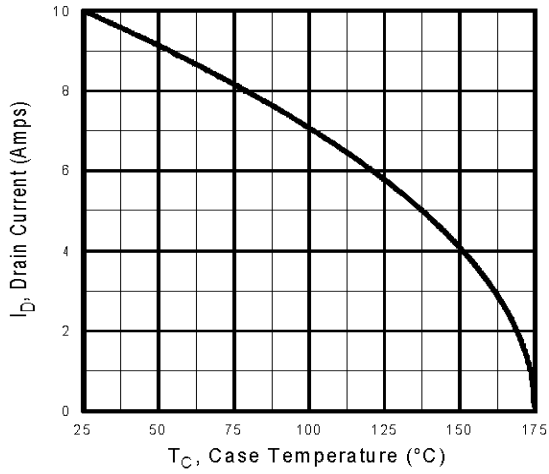
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



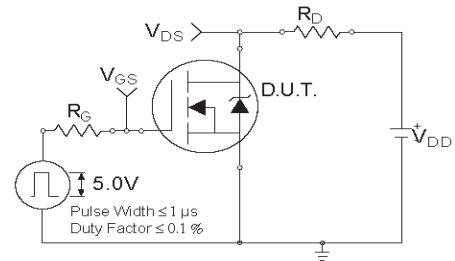
**Fig 7.** Typical Source-Drain Diode Forward Voltage



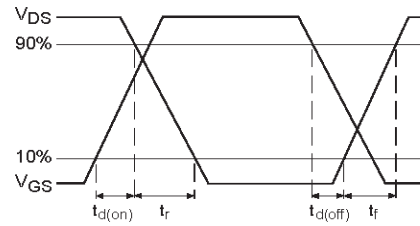
**Fig 8.** Maximum Safe Operating Area



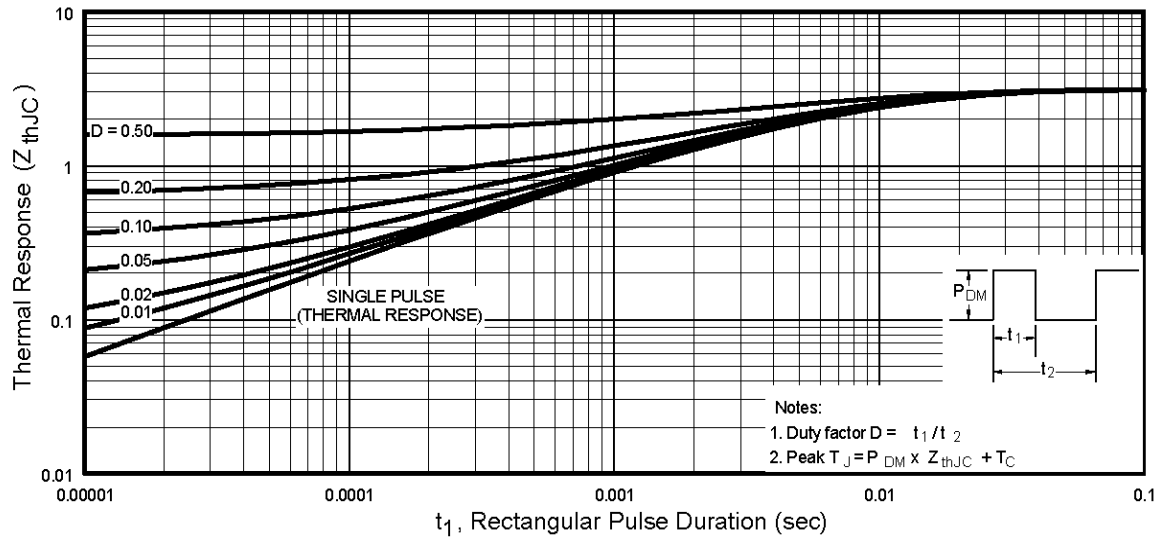
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



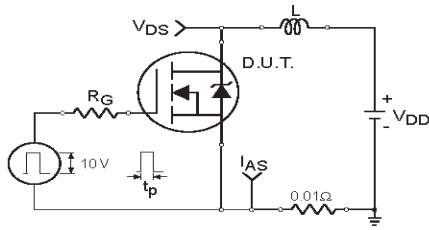
**Fig 10b.** Switching Time Waveforms



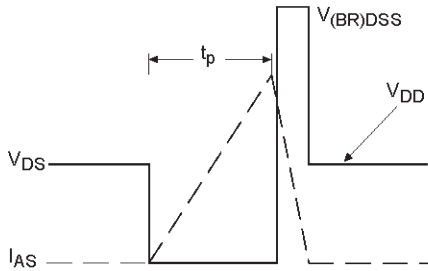
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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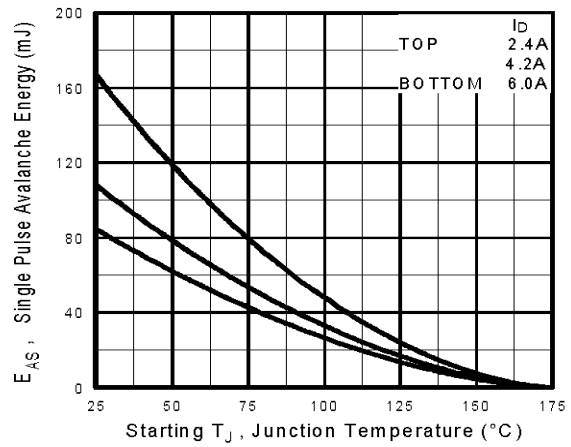
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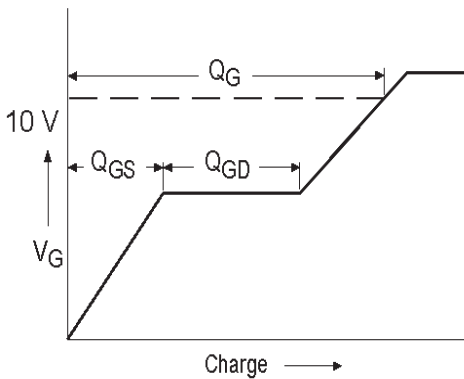
**Fig 12a.** Unclamped Inductive Test Circuit



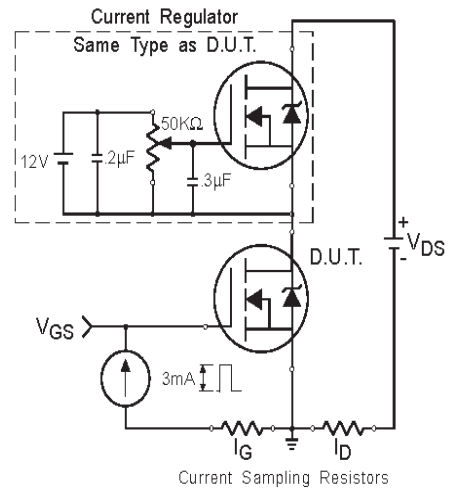
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

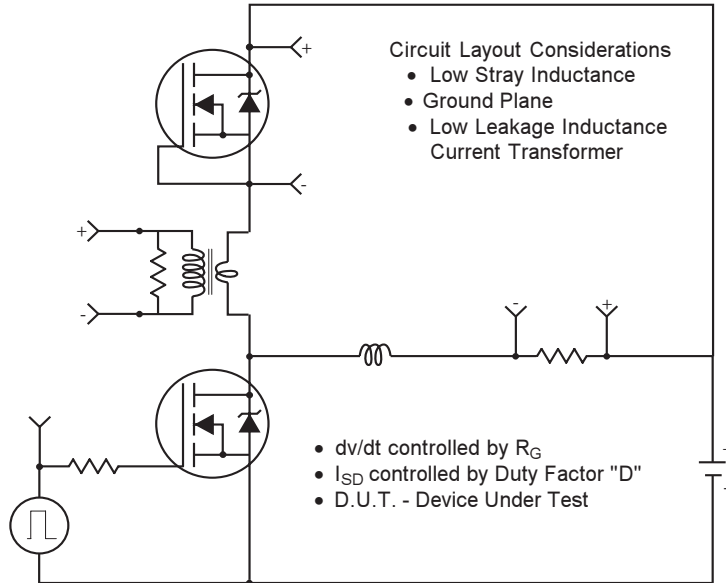


**Fig 13a.** Basic Gate Charge Waveform

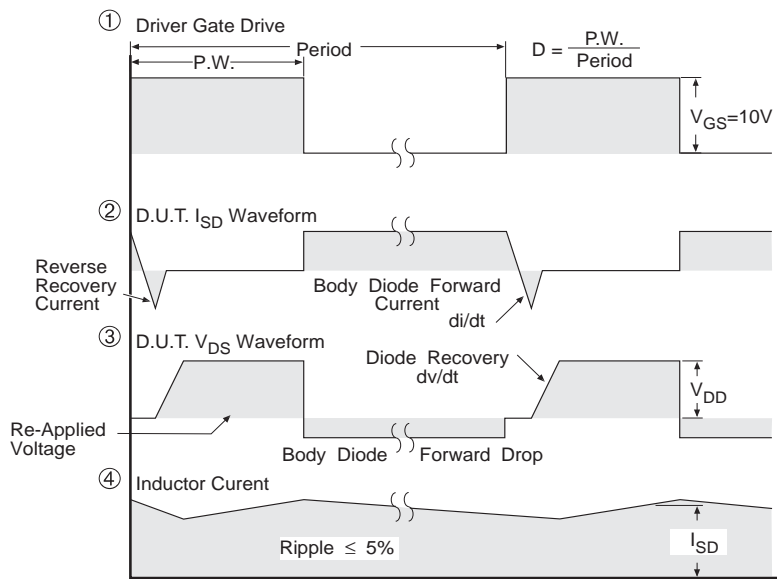


**Fig 13b.** Gate Charge Test Circuit

**Peak Diode Recovery dv/dt Test Circuit**



\* Reverse Polarity for P-Channel  
\*\* Use P-Channel Driver for P-Channel Measurements



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

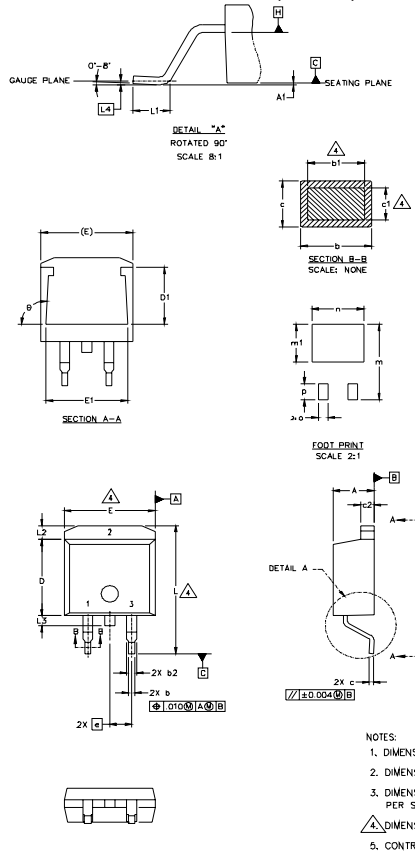
**Fig 14 For N Channel HEXFETS**

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## D<sup>2</sup>Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	4
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

### LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

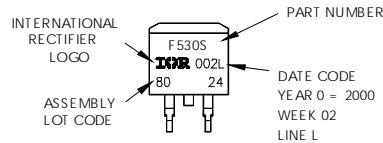
\* PART DEPENDENT.

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  5. CONTROLLING DIMENSION: INCH.

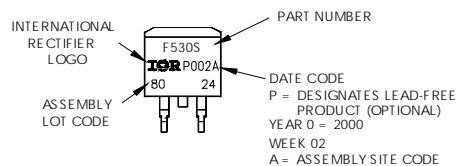
## D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line  
position indicates "Lead-Free"



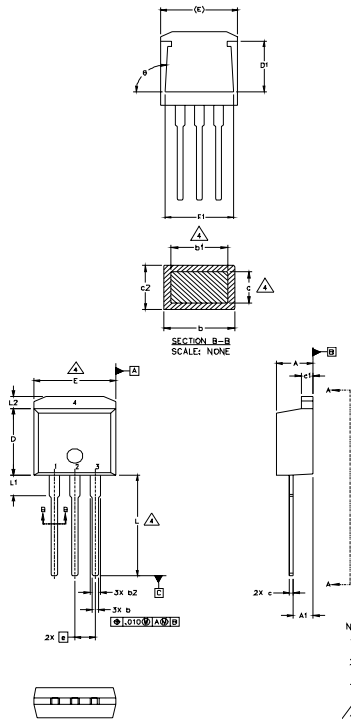
**OR**





## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	3
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	
D1	5.33		.210		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

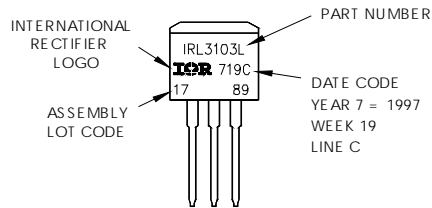
### LEAD ASSIGNMENTS

HEXFET	IGBT
1. - GATE	1 - GATE
2. - DRAIN	2 - COLLECTOR
3. - SOURCE	3 - EMITTER
4. - DRAIN	

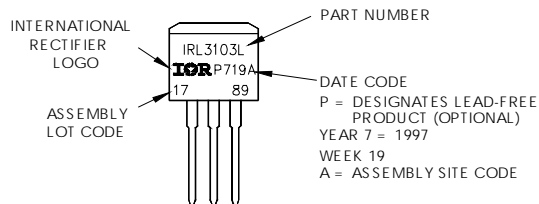
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  5. CONTROLLING DIMENSION: INCH.

## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"  
  
Note: "P" in assembly line  
position indicates "Lead-Free"



OR

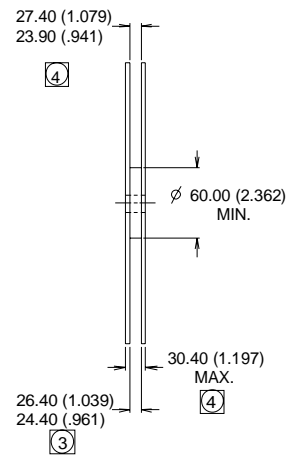
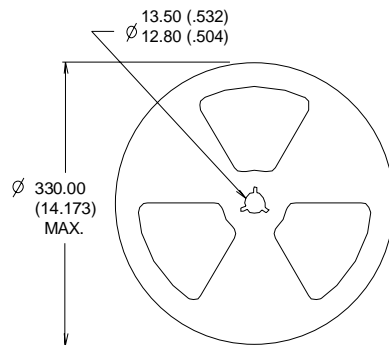
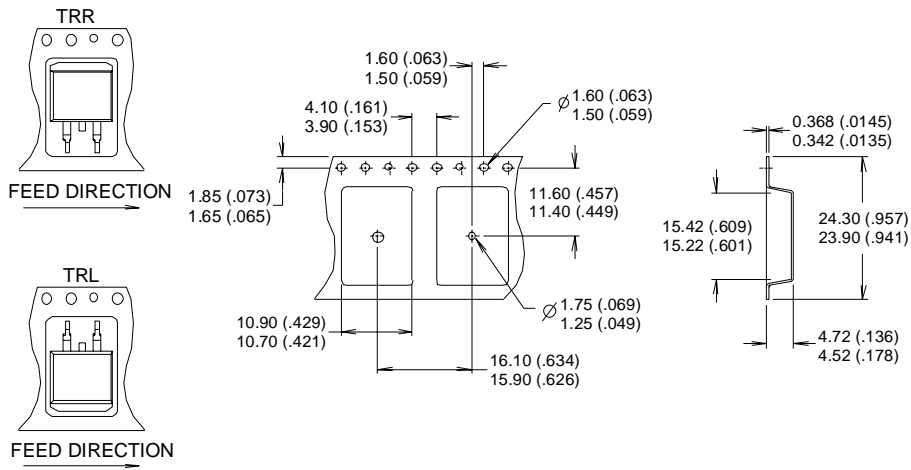


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## D<sup>2</sup>Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  - ③ DIMENSION MEASURED @ HUB.
  - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.

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