



# STD70NH02L STD70NH02L-1

N-channel 24V - 0.0062Ω - 60A - DPAK/IPAK  
STripFET™ II Power MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD70NH02L-1	24V	<0.008Ω	60A <sup>(1)</sup>
STD70NH02L	24V	<0.008Ω	60A <sup>(1)</sup>

1. Value limited by wire bonding

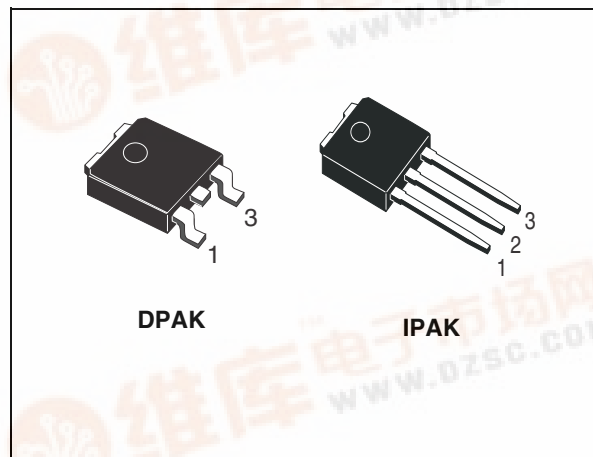
- R<sub>DS(ON)</sub> \* Q<sub>g</sub> industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device

## Description

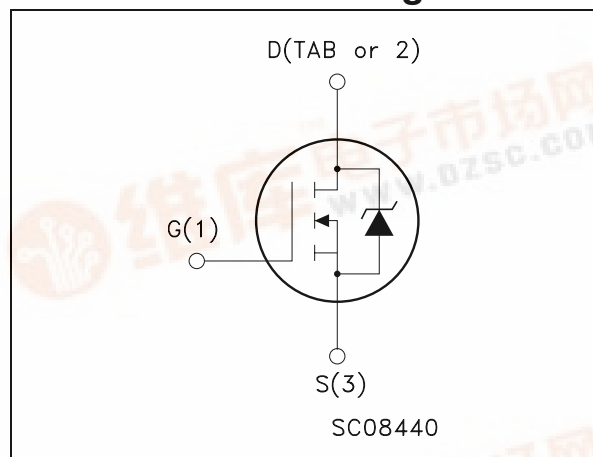
The device utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

## Applications

- Switching application



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STD70NH02LT4	D70NH02L	DPAK	Tape & reel
STD70NH02L-1	D70NH02L	IPAK	Tube



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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{\text{spike}}^{(1)}$	Drain-source voltage rating	30	V
$V_{\text{DS}}$	Drain-source voltage ( $V_{\text{GS}} = 0$ )	24	V
$V_{\text{DGR}}$	Drain-gate voltage ( $R_{\text{GS}} = 20\text{k}\Omega$ )	24	V
$V_{\text{GS}}$	Gate-source voltage	$\pm 20$	V
$I_{\text{D}}^{(2)}$	Drain current (continuous) at $T_{\text{C}} = 25^{\circ}\text{C}$	60	A
$I_{\text{D}}$	Drain current (continuous) at $T_{\text{C}} = 100^{\circ}\text{C}$	50	A
$I_{\text{DM}}^{(3)}$	Drain current (pulsed)	240	A
$P_{\text{TOT}}$	Total dissipation at $T_{\text{C}} = 25^{\circ}\text{C}$	70	W
	Derating factor	0.47	W/ $^{\circ}\text{C}$
$E_{\text{AS}}^{(4)}$	Single pulse avalanche energy	360	mJ
$T_{\text{j}}$ $T_{\text{stg}}$	Operating junction temperature Storage temperature	-55 to 175	$^{\circ}\text{C}$

1. Guaranteed when external  $R_{\text{g}} = 4.7\Omega$  and  $T_{\text{f}} < T_{\text{fmax}}$
2. Value limited by wire bonding
3. Pulse width limited by safe operating area
4. Starting  $T_{\text{j}} = 25^{\circ}\text{C}$ ,  $I_{\text{d}} = 30\text{A}$ ,  $V_{\text{dd}} = 15\text{V}$

**Table 2. Thermal data**

$R_{\text{thj-case}}$	Thermal resistance junction-case max	2.14	$^{\circ}\text{C}/\text{W}$
$R_{\text{thj-amb}}$	Thermal resistance junction-to ambient max	100	$^{\circ}\text{C}/\text{W}$
$T_{\text{J}}$	Maximum lead temperature for soldering purpose	275	$^{\circ}\text{C}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 25mA, V_{GS} = 0$	24			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 20V$ $V_{DS} = 20V, T_C = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.8		V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 30A$ $V_{GS} = 5V, I_D = 15A$		0.0062 0.008	0.008 0.014	$\Omega$ $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10V, I_D = 18A$		27		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1MHz,$ $V_{GS} = 0$		2050 545 70		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 10V, I_D = 40A$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ (see <a href="#">Figure 13</a> )		12 200 18 25		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 5V, I_D = 60A,$ $V_{GS} = 10V, R_G = 4.7\Omega$ (see <a href="#">Figure 14</a> )		17 7.7 3.5	22	nC nC nC
$Q_{oss}^{(2)}$	Output charge	$V_{DS} = 10V, V_{GS} = 0V$		14		nC
$R_G$	Gate input resistance	f=1MHz Gate DC Bias =0 Test Signal Level =20mV Open Drain		1		$\Omega$

1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

2.  $Q_{oss} = C_{oss} * \Delta V_{in}$ ,  $C_{oss} = C_{gd} + C_{gd}$ . See [Chapter 4: Appendix A](#)

**Table 5. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				60	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				240	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 30A, V_{GS} = 0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 60A, di/dt = 100A/\mu s,$		36		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 15V, T_j = 150^\circ C$		35		$\mu C$
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 15</a> )		3.6		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

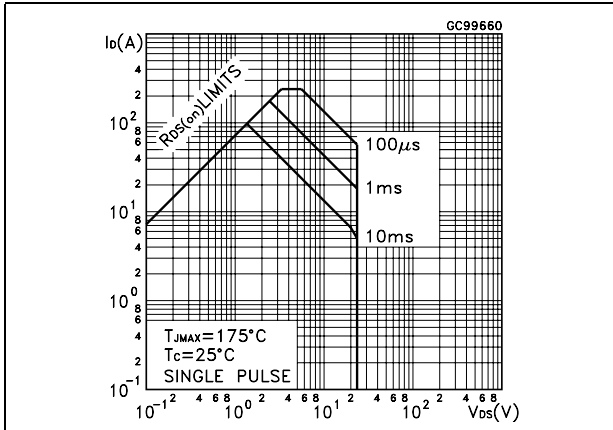


Figure 2. Thermal impedance

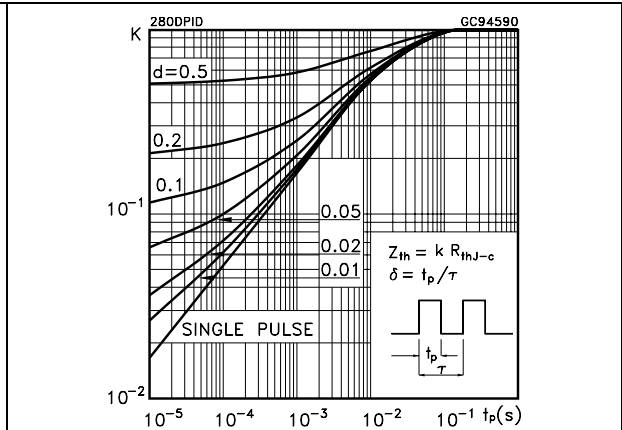


Figure 3. Output characteristics

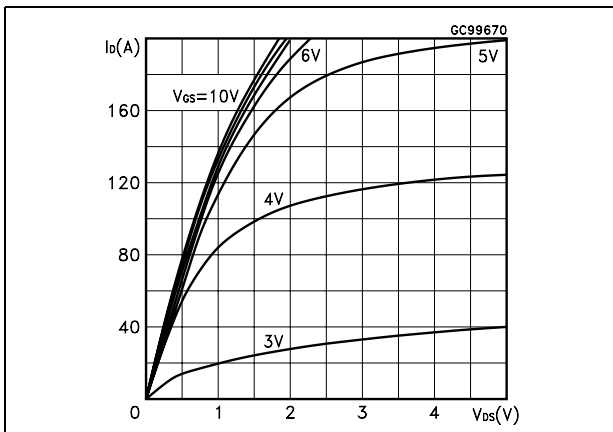


Figure 4. Transfer characteristics

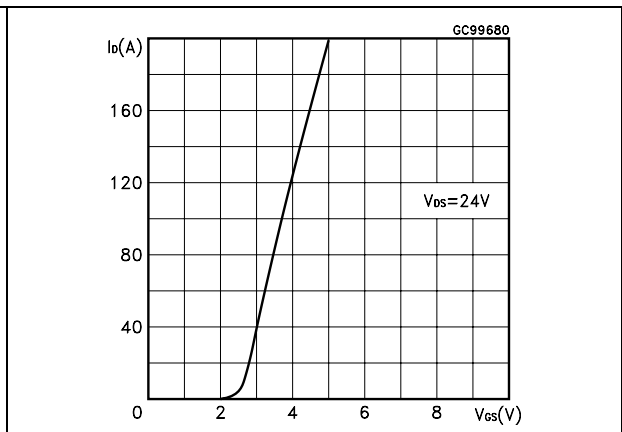


Figure 5. Transconductance

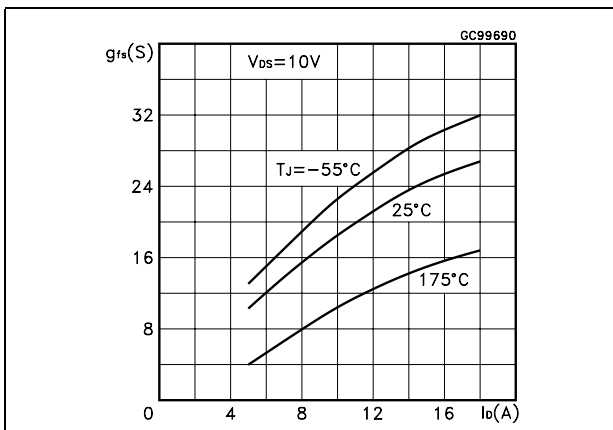


Figure 6. Static drain-source on resistance

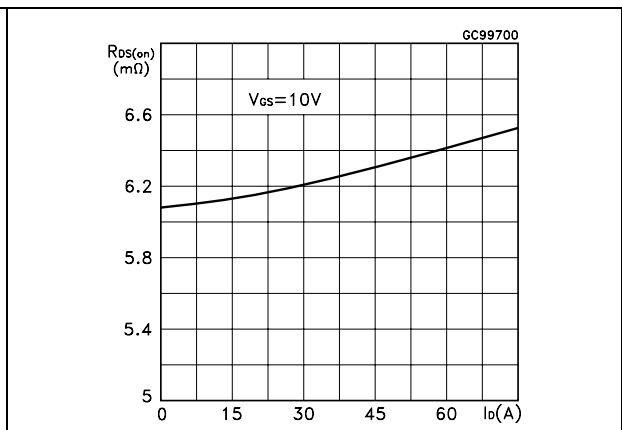


Figure 7. Gate charge vs gate-source voltage    Figure 8. Capacitance variations

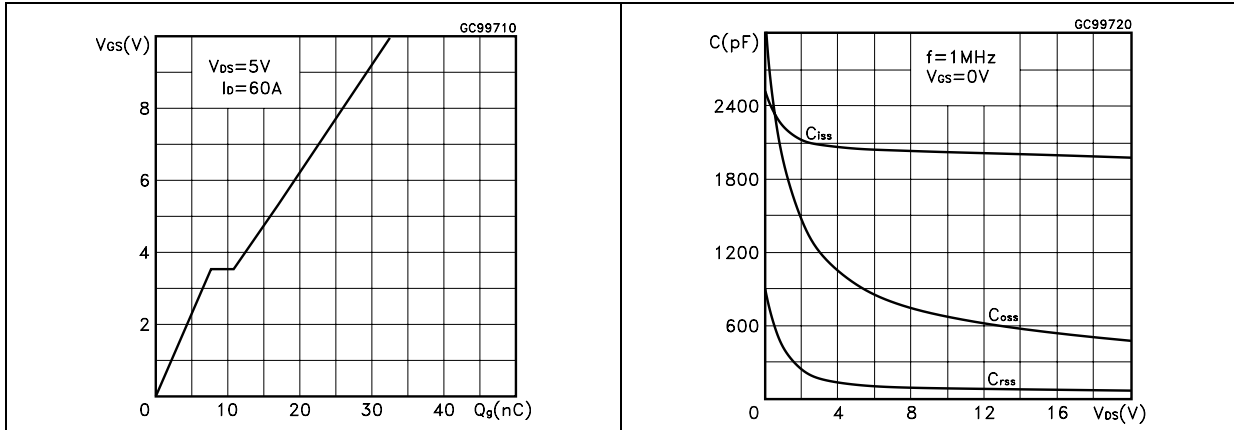


Figure 9. Normalized gate threshold voltage vs temperature    Figure 10. Normalized on resistance vs temperature

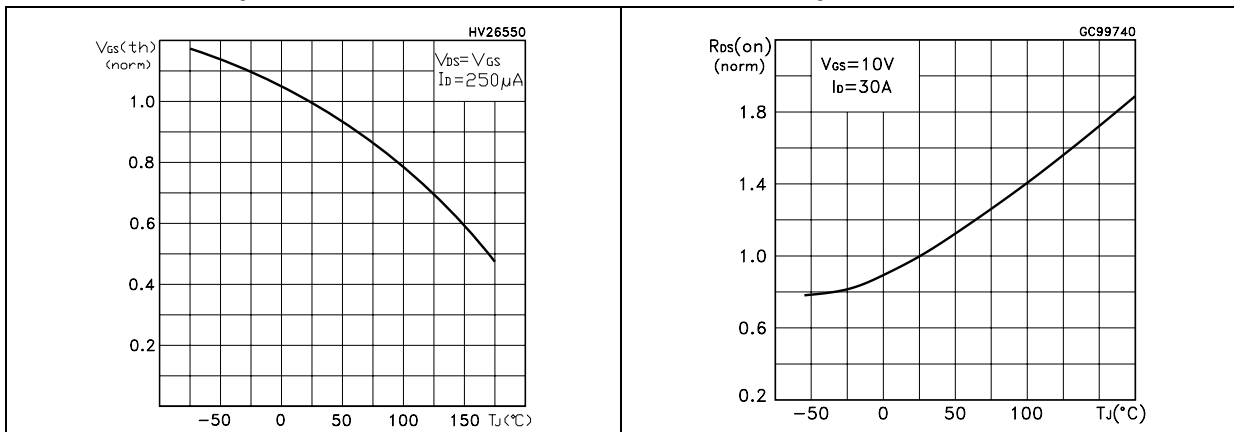
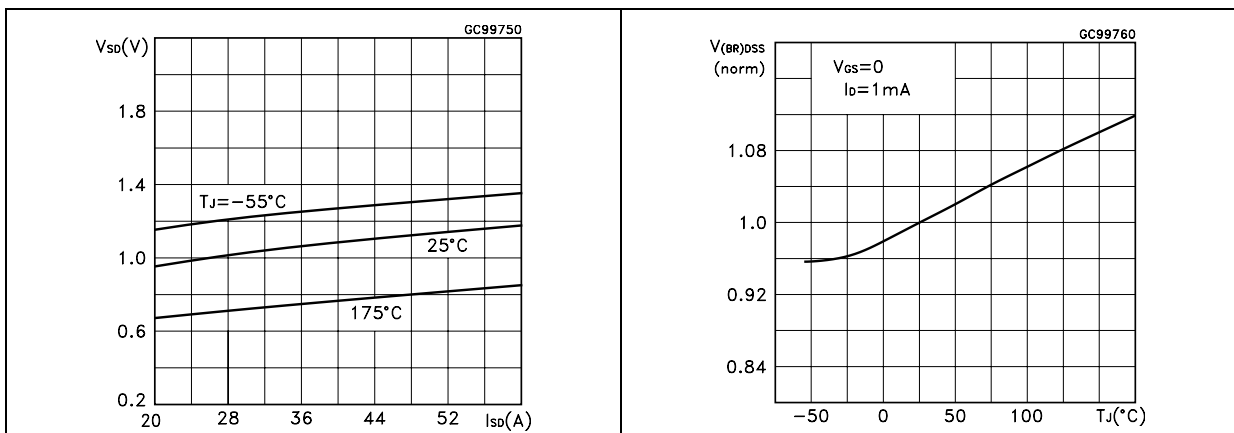


Figure 11. Source-drain diode forward characteristics    Figure 12. Normalized  $BV_{DSS}$  vs temperature



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

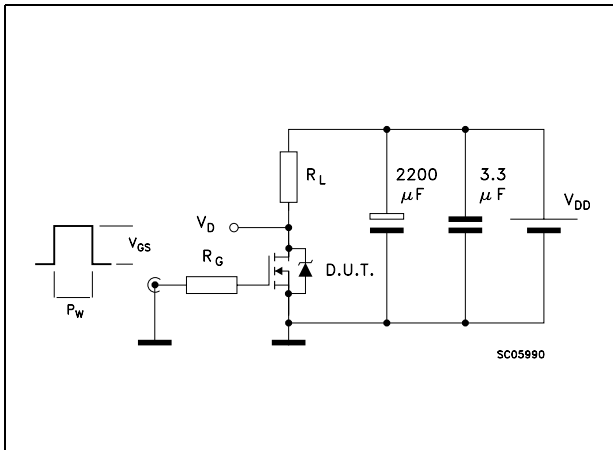


Figure 14. Gate charge test circuit

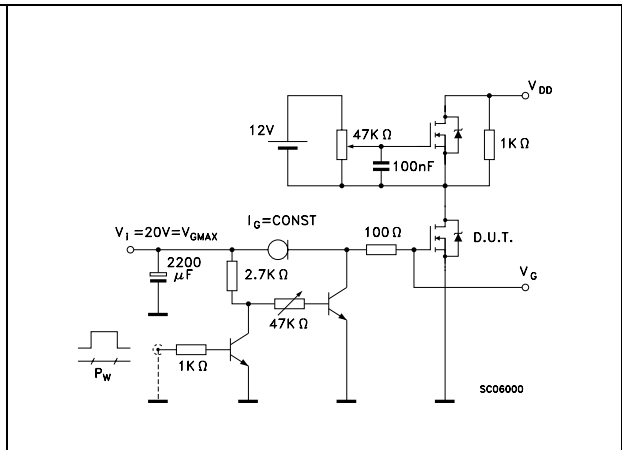


Figure 15. Test circuit for inductive load switching and diode recovery times

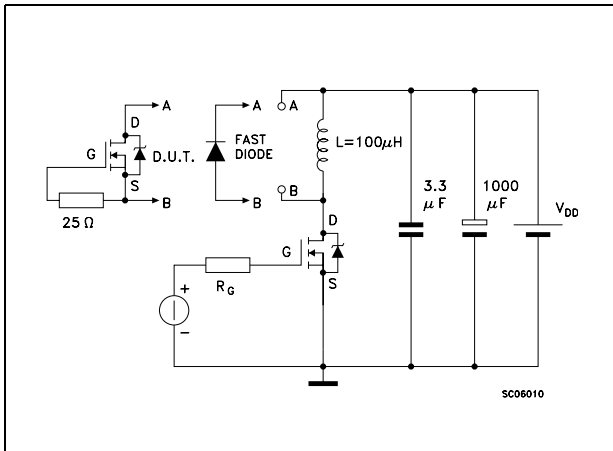


Figure 16. Unclamped Inductive load test circuit

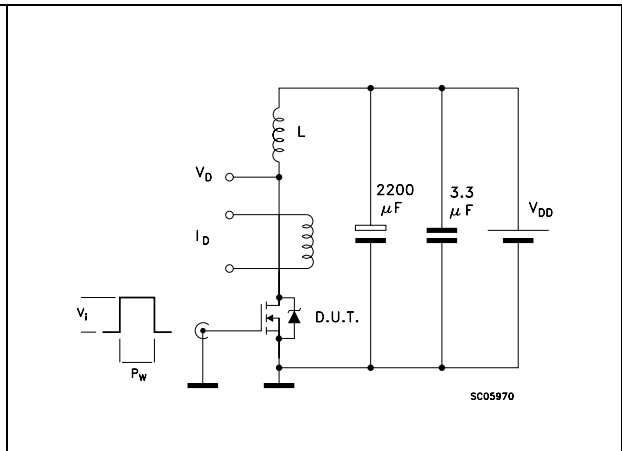


Figure 17. Unclamped inductive waveform

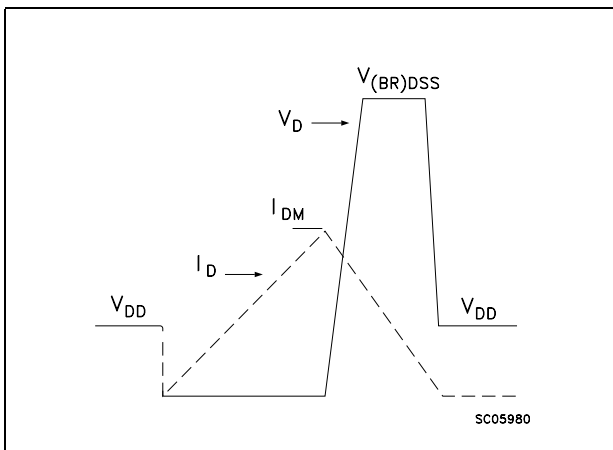
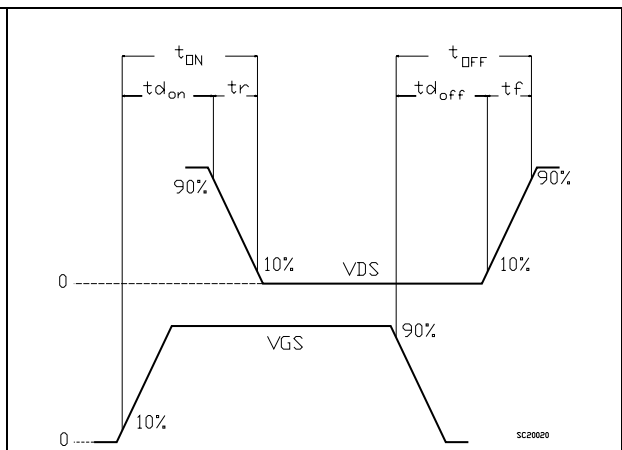


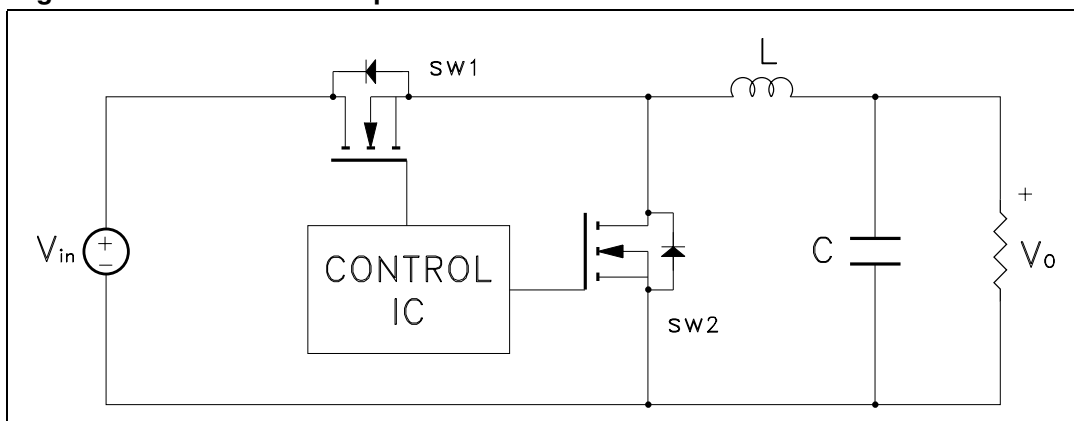
Figure 18. Switching time waveform





## 4 Appendix A

Figure 19. Buck converter: power losses estimation



The power losses associated with the FETs in a synchronous buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

- The low side (SW2) device requires:
- Very low  $R_{DS(on)}$  to reduce conduction losses
- Small  $Q_{gls}$  to reduce the gate charge losses
- Small  $C_{oss}$  to reduce losses due to output capacitance
- Small  $Q_{rr}$  to reduce losses on SW1 during its turn-on
- The  $C_{gd}/C_{gs}$  ratio lower than  $V_{th}/V_{gg}$  ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;
- The high side (SW1) device requires:
- Small  $R_g$  and  $L_s$  to allow higher gate current peak and to limit the voltage feedback on the gate
- Small  $Q_g$  to have a faster commutation and to reduce gate charge losses
- Low  $R_{DS(on)}$  to reduce the conduction losses.

Table 6. Power losses calculation

	High side switching (SW1)	Low side switch (SW2)
Pconduction	$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1 - \delta)$
Pswitching	$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching

**Table 6. Power losses calculation**

		High side switching (SW1)	Low side switch (SW2)
P <sub>diode</sub>	Recovery <sup>(1)</sup>	Not applicable	$V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
P <sub>gate(Q<sub>G</sub>)</sub>		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P <sub>Qoss</sub>		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

1. Dissipated by SW1 during turn-on

**Table 7. Parameters meaning**

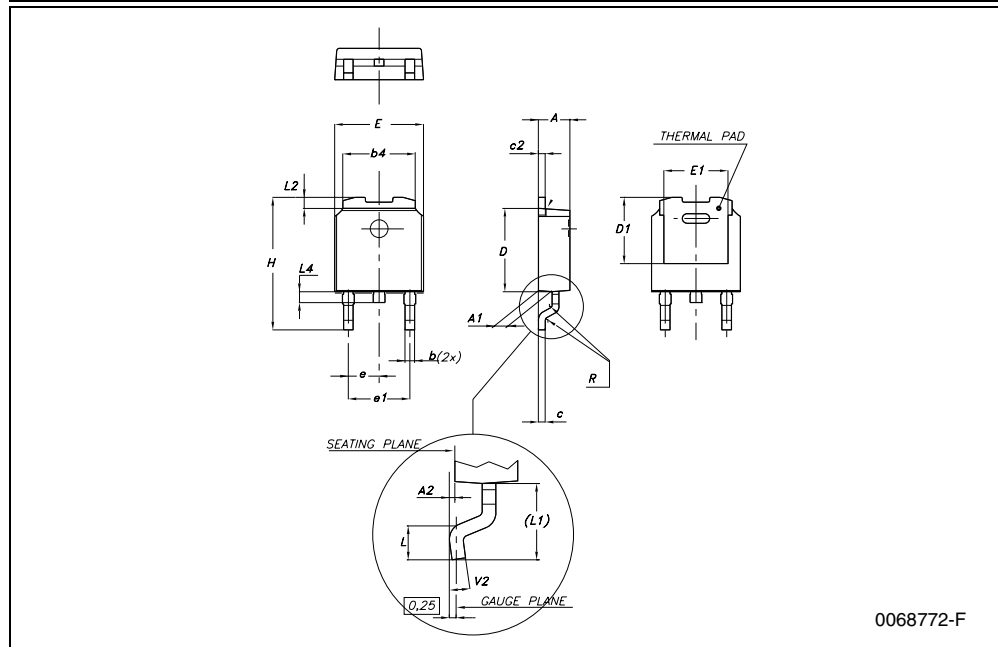
Parameter	Meaning
d	Duty-cycle
Q <sub>gsth</sub>	Post threshold gate charge
Q <sub>gls</sub>	Third quadrant gate charge
P <sub>conduction</sub>	On state losses
P <sub>switching</sub>	On-off transition losses
P <sub>diode</sub>	Conduction and reverse recovery diode losses
P <sub>gate</sub>	Gate drive losses
P <sub>Qoss</sub>	Output capacitance losses

## 5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**DPAK MECHANICAL DATA**

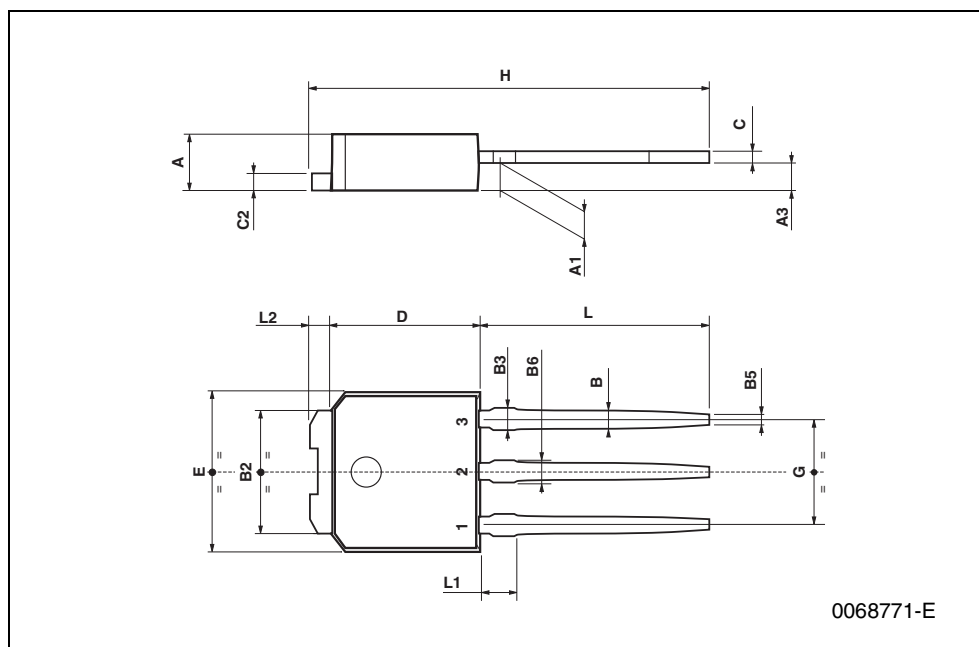
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



0068772-F

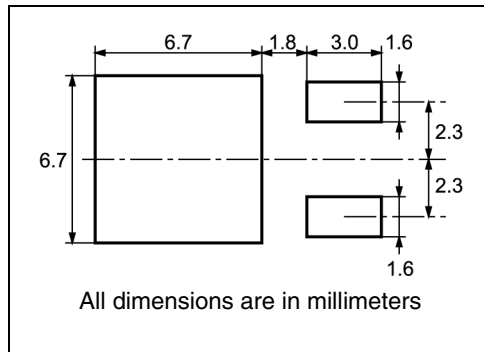
**TO-251 (IPAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



## 6 Packing mechanical data

### DPAK FOOTPRINT



### TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

#### REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

#### TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

For machine ref. only including draft and radii concentric around B0

10 pitches cumulative tolerance on tape  $\pm 0.2$  mm

Center line of cavity

Bending radius R min.

## 7 Revision history

**Table 8. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
09-Sep-2004	2	Preliminary version
10-Feb-2005	3	Complete version with curves
04-Feb-2006	4	Inserted new package: IPAK
19-Jul-2006	5	New template, no content change

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