National Semiconductor

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# LM3880
# Power Sequencer

## General Description

The LM3880 Power Sequencer offers the easiest method to control power up and power down of multiple power supplies (switchers or linear regulators). By staggering the startup sequence, it is possible to avoid latch conditions or large in-rush currents that can affect the reliability of the system.

Available in a SOT23-6 package, the Power Sequencer contains a precision enable pin and three open drain output flags. Upon enabling the LM3880 the three output flags will sequentially release, after individual time delays, permitting the connected power supplies to startup. The output flags will follow a reverse sequence during power down to avoid latch conditions.

Standard timing option of 30ms is available.

EPROM capability allows every delay and sequence to be fully adjustable. Contact National Semiconductor if a non-standard configuration is required.

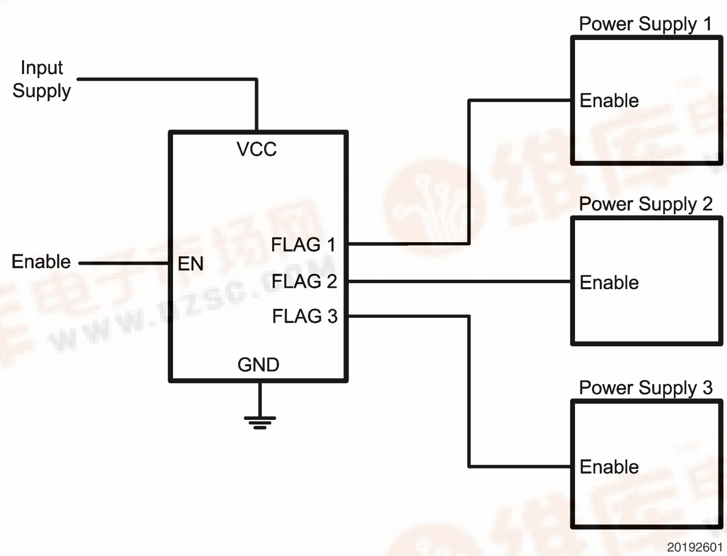
## Features

- Easiest method to sequence rails
- Power up and power down control
- Input voltage range of 2.7V to 5.5V
- Small footprint SOT23-6
- Low quiescent current of 20 µA
- Standard timing options available
- Customization of timing and sequence available through factory programmability

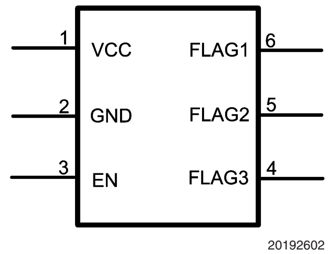
## Applications

- Multiple supply sequencing
- Microprocessor / Microcontroller sequencing
- FPGA sequencing

## Typical Application Circuit



## Connection Diagram

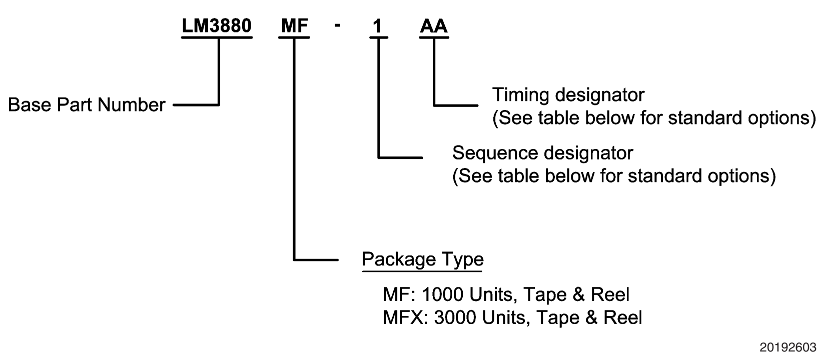



**Top View**
**SOT23–6 Package**

## Pin Descriptions

| Pin # | Name | Function |
|---|---|---|
| 1 | VCC | Input supply |
| 2 | GND | Ground |
| 3 | EN | Precision enable pin |
| 4 | FLAG3 | Open drain output #3 |
| 5 | FLAG2 | Open drain output #2 |
| 6 | FLAG1 | Open drain output #1 |

## Ordering Information




**Sequence Designator Table**

| Sequence Number | Flag Order | |
|---|---|---|
| | Power Up | Power Down |
| 1 | 1 - 2 - 3 | 3 - 2 - 1 |
| 2 | 1 - 2 - 3 | 3 - 1 - 2 |
| 3 | 1 - 2 - 3 | 2 - 3 - 1 |
| 4 | 1 - 2 - 3 | 2 - 1 - 3 |
| 5 | 1 - 2 - 3 | 1 - 3 - 2 |
| 6 | 1 - 2 - 3 | 1 - 2 - 3 |

See timing diagrams for more information

## Ordering Information (Continued)

**Timing Designator Table**

| Timing Designator | $t_{d1}$ | $t_{d2}$ | $t_{d3}$ | $t_{d4}$ | $t_{d5}$ | $t_{d6}$ |
|---|---|---|---|---|---|---|
| AA | 10ms | 10ms | 10ms | 10ms | 10ms | 10ms |
| AB | 30ms | 30ms | 30ms | 30ms | 30ms | 30ms |
| AC | 60ms | 60ms | 60ms | 60ms | 60ms | 60ms |
| AD | 120ms | 120ms | 120ms | 120ms | 120ms | 120ms |

See timing diagrams for more information

**LM3880 Ordering Information**

| Order Number | Timer settings | | | | | | Sequence Order | Supplied As | Package Type | NSC Package Drawing | Package Marking |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $t_{d1}$ | $t_{d2}$ | $t_{d3}$ | $t_{d4}$ | $t_{d5}$ | $t_{d6}$ | | | | | |
| LM3880MF-1AB | 30ms | 30ms | 30ms | 30ms | 30ms | 30ms | 1 | 1k units T&R | SOT23-6 | MF06A | F21A |
| LM3880MFX-1AB | 30ms | 30ms | 30ms | 30ms | 30ms | 30ms | 1 | 3k units T&R | SOT23-6 | MF06A | F21A |

Non-standard parts are available upon request. Please contact National Semiconductor for more information.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| VCC | –0.3V to +6.0V |
| EN, FLAG1, FLAG2, FLAG3 | –0.3V to +6.0V |
| Storage Temperature Range | –65˚C to +150˚C |
| Junction Temperature | 150˚C |
| Lead Temperature (Soldering, 5 sec.) | 260˚C |
| Minimum ESD Rating | ±2 kV |

## Operating Ratings (Note 1)

| | |
|---|---|
| VCC to GND | 2.7V to 5.5V |
| Junction Temperature | –40˚C to +125˚C |

## Electrical Characteristics

Specifications with standard typeface are for $T_J$ = 25˚C, and those in bold face type apply over the full Operating Temperature Range ($T_J$ = -40˚C to +125˚C). Minimum and Maximum limits are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25˚C and are provided for reference purposes only. Unless otherwise specified VCC = 3.3V.

| Symbol | Parameter | Conditions | Min (Note 3) | Typ (Note 4) | Max (Note 3) | Unit |
|---|---|---|---|---|---|---|
| $I_Q$ | Operating Quiescent current | | | 20 | **80** | µA |
| **Open Drain Flags** | | | | | | |
| $I_{FLAG}$ | FLAGx Leakage Current | $V_{FLAGx}$ = 3.3V | | 1 | **20** | nA |
| $V_{OL}$ | FLAGx Output Voltage Low | $I_{FLAGx}$ = 1.2mA | | | **0.4** | V |
| **Power Up Sequence** | | | | | | |
| $t_{d1}$ | Timer delay 1 accuracy | | **-15** | | **15** | % |
| $t_{d2}$ | Timer delay 2 accuracy | | **-15** | | **15** | % |
| $t_{d3}$ | Timer delay 3 accuracy | | **-15** | | **15** | % |
| **Power Down Sequence** | | | | | | |
| $t_{d4}$ | Timer delay 4 accuracy | | **-15** | _ | **15** | % |
| $t_{d5}$ | Timer delay 5 accuracy | | **-15** | | **15** | % |
| $t_{d6}$ | Timer delay 6 accuracy | | **-15** | | **15** | % |
| **Timing Delay Error** | | | | | | |
| ($t_{d(x)}$ – 400 us) / $t_{d(x+1)}$ | Ratio of timing delays | For x = 1 or 4 | **95** | | **105** | % |
| $t_{d(x)}$ / $t_{d(x+1)}$ | Ratio of timing delays | For x = 2 or 5 | **95** | | **105** | % |
| **ENABLE Pin** | | | | | | |
| $V_{EN}$ | EN pin threshold | | **0.9** | | **1.4** | V |
| $I_{EN}$ | EN pin pull-up current | $V_{EN}$ = 0V | | 16 | | µA |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and conditions, see the Electrical Characteristics.

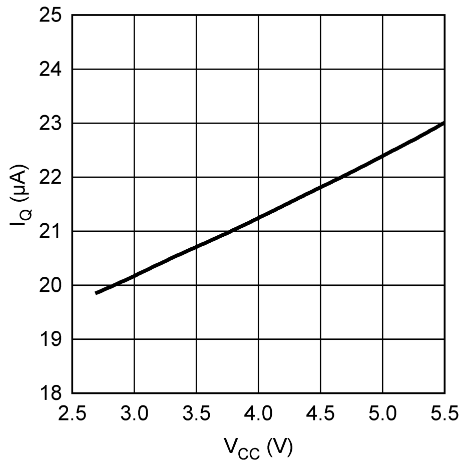
**Note 2:** The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

**Note 3:** Limits are 100% production tested at 25˚. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).

**Note 4:** Typical numbers are at 25˚C and represent the most likely parametric norm.

# Typical Performance Characteristics

**Quiescent Current vs VCC**

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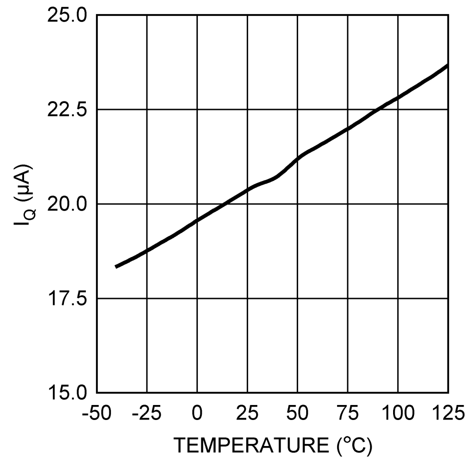
**Quiescent Current vs Temperature (VCC = 3.3V)**

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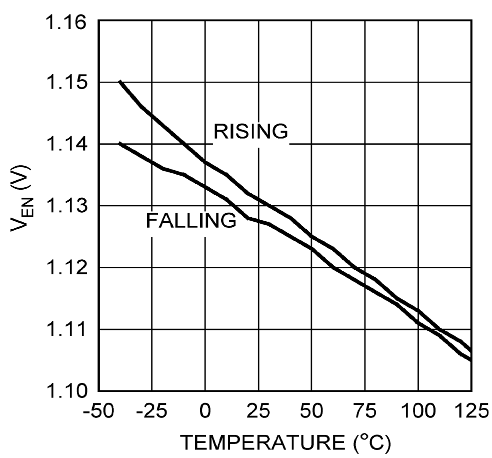
**Enable Threshold vs Temperature**

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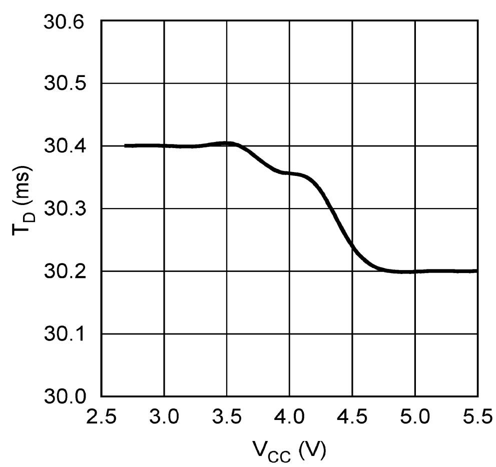
**Time Delay (30ms) vs VCC**

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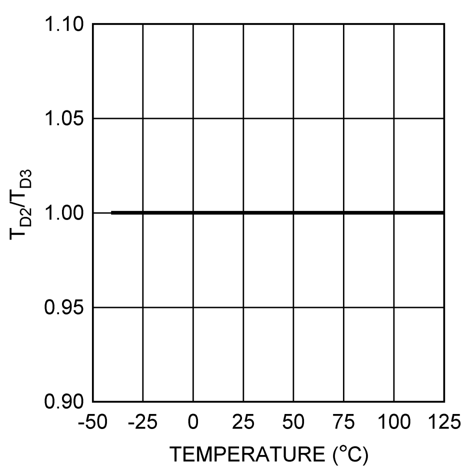
**Time Delay Ratio vs Temperature**

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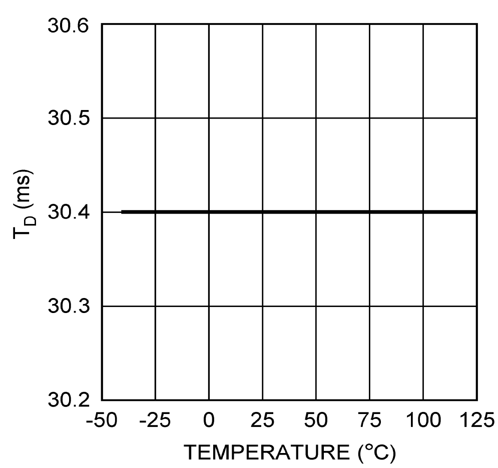
**Time Delay (30ms) vs Temperature**

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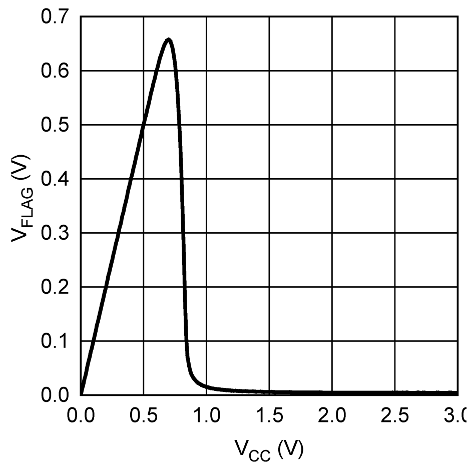
## Typical Performance Characteristics (Continued)

**FLAG $V_{OL}$ vs VCC ($R_{FLAG}$ = 100 kΩ)**

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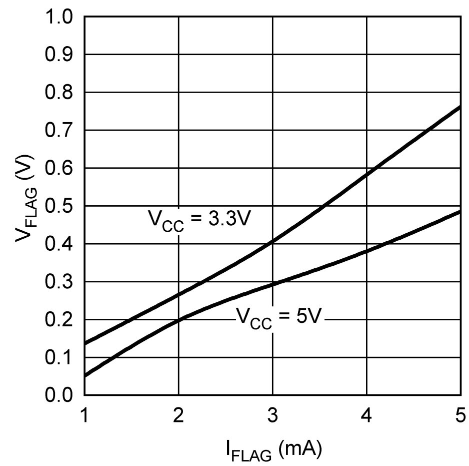
**FLAG Voltage vs Current**

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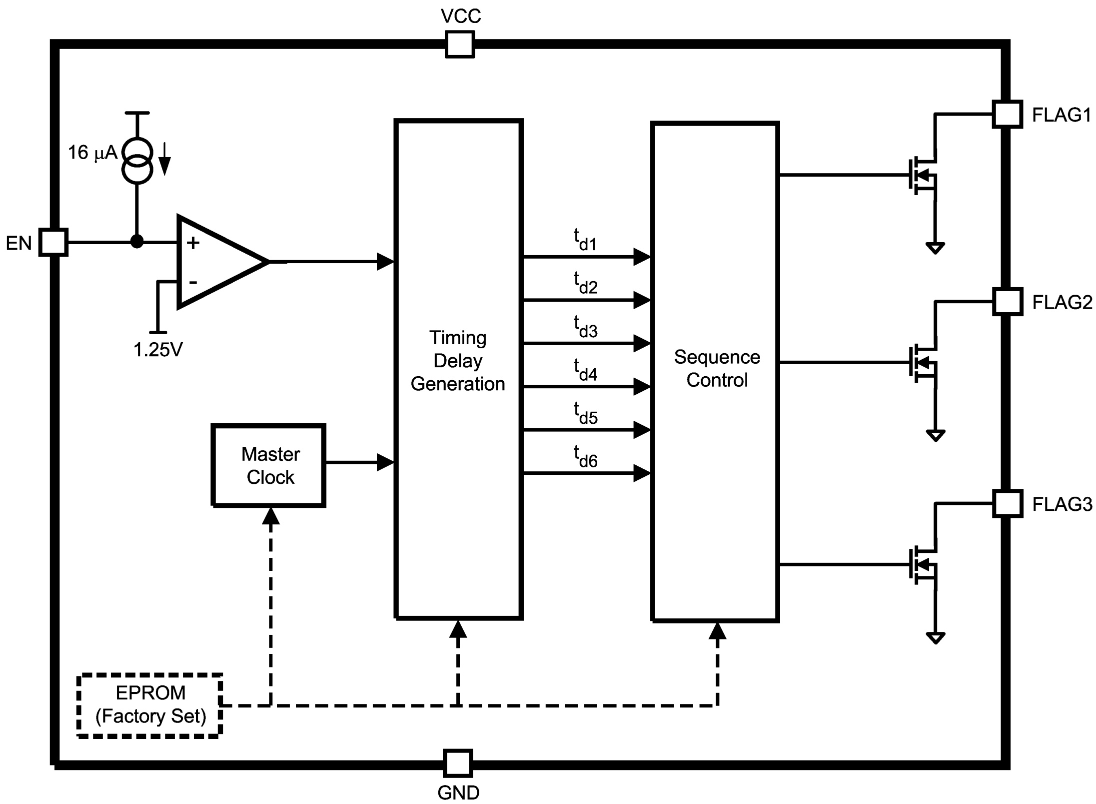
## Block Diagram

**Block Diagram**

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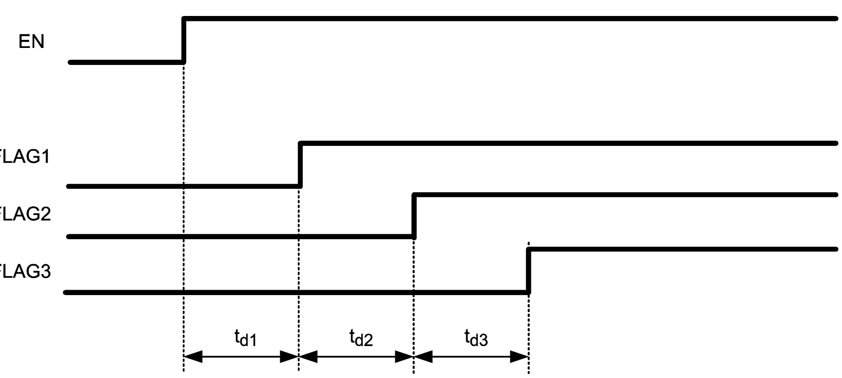
## Timing Diagrams (Sequence 1)

All standard options use this sequence for output flags rise and fall order.

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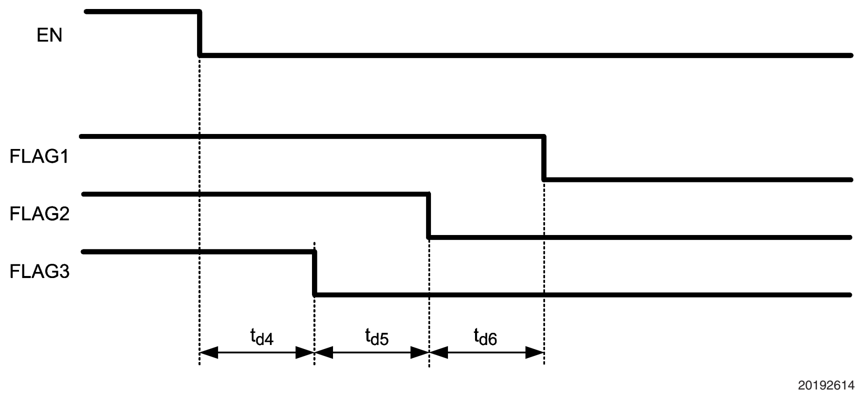
**Power Up Sequence**

## Timing Diagrams (Sequence 1) (Continued)




**Power Down Sequence**

# Application Information

### OVERVIEW

The LM3880 Power Sequencer provides an easy solution for sequencing multiple rails in a controlled manner. Six independent timers are integrated to control the timing sequence (power up and power down) of three open drain output flags. These flags permit connection to either a shutdown / enable pin of linear regulators and switchers to control the power supplies' operation. This allows a complete power system to be designed without worrying about large in-rush currents or latch-up conditions that can occur.

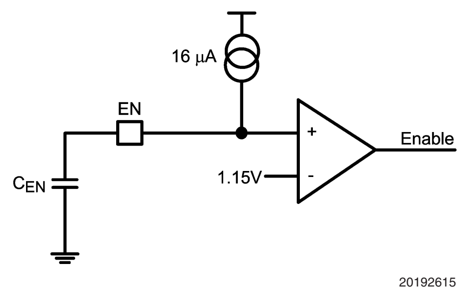
The timing sequence of the LM3880 is controlled entirely by the enable (EN) pin. Upon power up, all the flags are held low until this precision enable is pulled high. After the EN pin is asserted, the power up sequence will commence. An internal counter will delay the first flag (FLAG1) from rising until a fixed time period has expired. Upon the release of the first flag another timer will begin to delay the release of the second flag (FLAG2). This process repeats until all three flags have sequentially been released. The three timers that control the delays are all independent of each other and can be individually programmed if needed. (See custom sequencer section).

The power down sequence is the same as power-up, but in reverse. When EN pin is de-asserted a timer will begin that delays the third flag (FLAG3) from pulling low. The second and first flag will then follow in a sequential manner after their appropriate delays. The three timers that are used to control the power down scheme can also be individually programmed and are completely independent of the power up timers.

Additional sequence patterns are also available in addition to customizable timers. For more information see the custom sequencer section.

### PART OPERATION

The timing sequence of the LM3880 is controlled by the assertion of the enable signal. The enable pin is designed with an internal comparator, referenced to a bandgap voltage (1.15V), to provide a precision threshold. This allows a delayed timing to be externally set using a capacitor or to start the sequencing based on a certain event, such as a line voltage reaching 90% of nominal. For an additional delayed sequence from the rail powering VCC, simply attach a capacitor to the EN pin as shown below.




**Cap Timing**

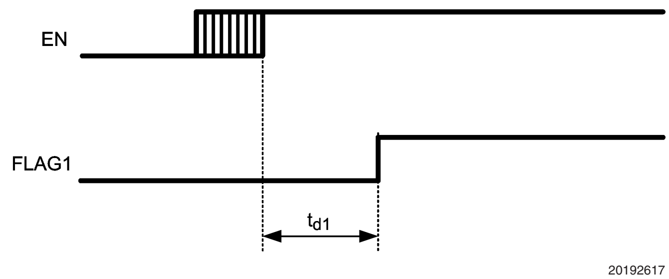
Using the internal pull-up current source to charge the external capacitor ($C_{EN}$) the enable pin delay can be calculated by the equation below:

$$t_{enable\_delay} = \frac{1.15V \times C_{EN}}{16\ \mu A}$$

A resistor divider can also be used to enable the LM3880 based on a certain voltage threshold. Care needs to be taken when sizing the resistor divider to include the effects of the internal current source.

One of the features of the enable pin is that it provides glitch free operation. The first timer will start counting at a rising threshold, but will always reset if the enable pin is de-asserted before the first output flag is released. This can be shown in the timing diagram below:

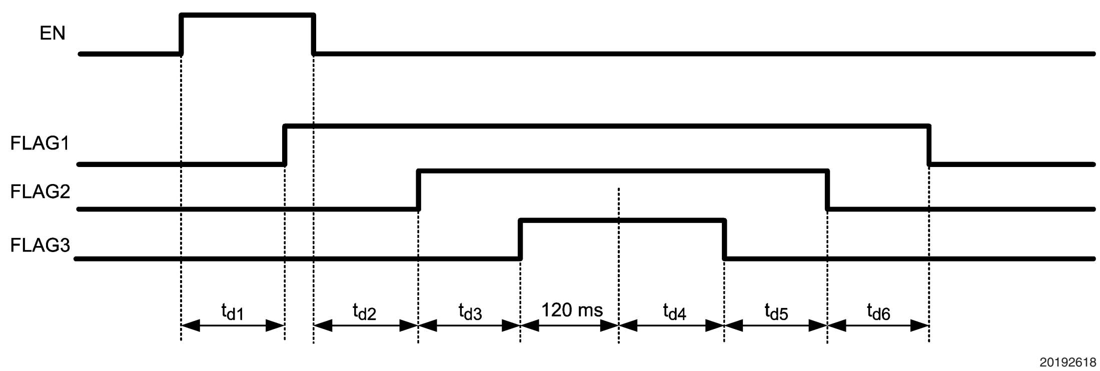
## Application Information (Continued)




**EN Glitch**

If the enable signal remains high for the entire power-up sequence, then the part will operate as shown in the standard timing diagrams. However, if the enable signal is de-asserted before the power-up sequence is completed the part will enter a controlled shutdown. This allows the system to walk through a controlled power cycling, preventing any latch conditions from occuring. This state only occurs if the enable pin is de-asserted after the completion of timer 1, but before the entire power-up sequence is completed.

When this event occurs, the falling edge of enable pin resets the current timer and will allow the remaining power-up cycle to complete before beginning the power down sequence. The power down sequence starts approximately 120ms after the final power-up flag. This allows output voltages in the system to stabilize before everything is shutdown. An example of this operation can be seen below:




**Incomplete Sequence**

All the internal timers are generated by a master clock that has an extremely low tempco. This allows for tight accuracy across temperature and a consistent ratio between the individual timers. There is a slight additional delay of approximately 400us to timers 1 and 4 which is a result of the EPROM refresh. This refresh time is in addition to the programmed delay time and will be almost insignificant to all but the shortest of timer delays.

### CUSTOM SEQUENCER

The LM3880 Power Sequencer is based on a CMOS process utilizing an EPROM that has the capability to be custom programmed at the factory. Approximately 500,000,000 different options are available allowing even the most complex system to be simply sequenced. Because of the vast options that are possible, customization is limited to orders of a certain quantity. Please contact National Semiconductor for more information.

The variables that can be programmed include the six delay timers and the reverse sequence order. For the timers, each can be individually selected from one of the timer selector columns in the table shown below. However, all six time delays must be from the same column.

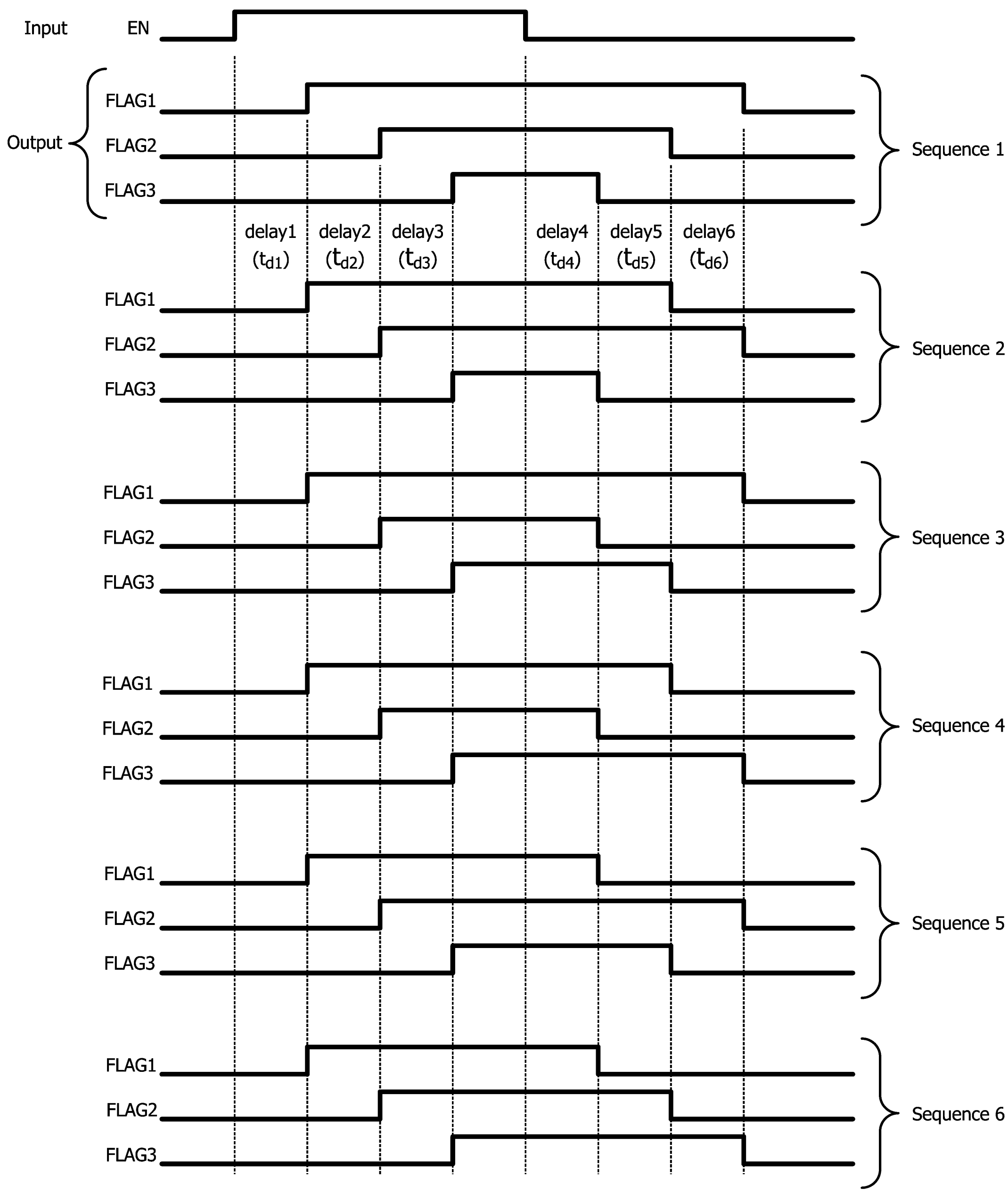
## Application Information (Continued)

| Timer Options 1 | Timer Options 2 | Timer Options 3 | Timer Options 4 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 2 | 4 | 6 | 8 |
| 4 | 8 | 12 | 16 |
| 6 | 12 | 18 | 24 |
| 8 | 16 | 24 | 32 |
| 10 | 20 | 30 | 40 |
| 12 | 24 | 36 | 48 |
| 14 | 28 | 42 | 56 |
| 16 | 32 | 48 | 64 |
| 18 | 36 | 54 | 72 |
| 20 | 40 | 60 | 80 |
| 22 | 44 | 66 | 88 |
| 24 | 48 | 72 | 96 |
| 26 | 52 | 78 | 104 |
| 28 | 56 | 84 | 112 |
| 30 | 60 | 90 | 120 |

All times listed are in milliseconds

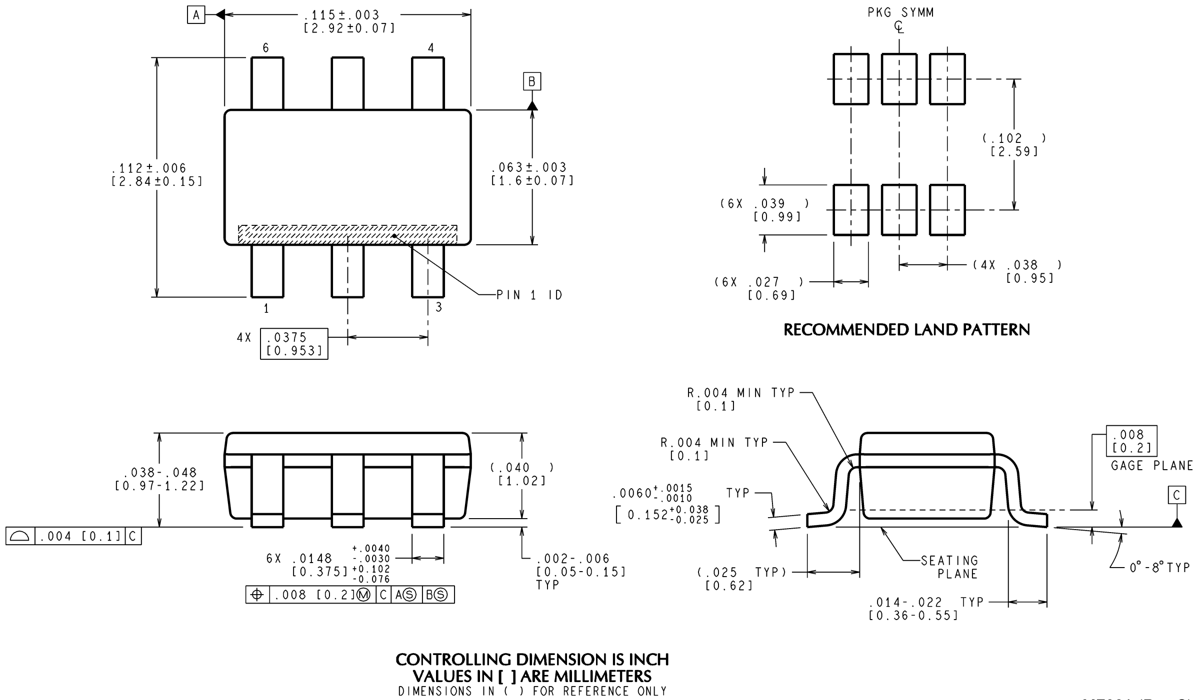
The sequencing order for power up is always controlled by layout. The flag number translates directly into the sequence order during power up (ie FLAG1 will always be first). However, for some systems a different power down order could be required. To allow flexibility for this aspect in a design, the Power Sequencer incorporates six different options for controlling the power down sequence. These options can be seen in the timing diagrams on the next page. This ability can be programmed in addition to the custom timers.

## Application Information (Continued)




**Power Down Sequence Options**

## Physical Dimensions inches (millimeters) unless otherwise noted




MF06A (Rev C)

**SOT23-6 Package**
**NS Package Number MF06A**



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