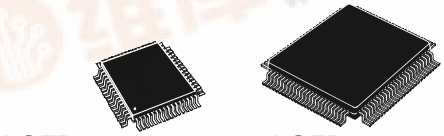
STR750F

ARM7TDMI-S™ 32-bit MCU with Flash, SMI, 3 std 16-bit timers, PWM timer, fast 10-bit ADC, I2C, UART, SSP, USB and CAN

- Core
  - ARM7TDMI-S 32-bit RISC CPU
  - 54 DMIPS @ 60 MHz
- Memories
  - Up to 256 KB Flash program memory (10k erase/write cycles, retention 20 yrs at 85°C)
  - 16KB Read-While-Write Flash for data (100k erase/write cycles, retention 20 yrs@ 85°C)
  - Flash Data Readout and Write Protection
  - 16KBytes embedded high speed SRAM
  - Memory mapped interface (SMI) to ext. Serial Flash (64 MB) w. boot capability
- Clock, Reset and Supply Management
  - Single supply 3.3V ±10% or 5V ±10%
  - Embedded 1.8V Voltage Regulators with Low Power features
  - Smart Clock Controller with flexible clock generation capability:
  - Internal RC for fast start-up and backup clock mechanism
  - Up to 60 MHz operation using internal PLL with 4 or 8 MHz crystal/ceramic osc.
  - Smart Low Power Modes: SLOW, WFI, STOP and STANDBY with backup registers
  - Real Time Clock, driven by low power internal RC or 32.768 kHz dedicated osc, for clock-calendar and Auto Wake-up
- Nested interrupt controller
  - Fast interrupt handling with 32 vectors
  - 16 IRQ priorities, 2 maskable FIQ sources
  - 16 external interrupt / wake-up Lines
- DMA
  - 4-channel DMA controller
  - Circular buffer management
  - Support for UART, SSP, Timers, ADC
- 6 Timers
  - 16-bit watchdog timer (WDG)



LQFP64 10x10 mm LQFP100 14 x 14 mm

LFBGA64 8 x 8 x 1.7 mm LFBGA100 10 x 10 x 1.7 mm

  - 16-bit timer for system timebase functions
  - 3 synchronizable timers each with up to 2 input captures and 2 output compare/PWMs.
  - 16-bit 6-channel synchronizable PWM timer
  - Dead time generation, edge/center-aligned waveforms and emergency stop
  - Ideal for induction/brushless DC motors
- 8 Communications Interfaces
  - 1 I^2C interface
  - 3 HiSpeed UARTs w. Modem/LIN capability
  - 2 SSP interfaces (SPI or SSI) up to 16 Mb/s
  - 1 CAN interface (2.0B Active)
  - 1 USB full-speed 12 Mb/s interface with 8 configurable endpoint sizes
- 10-bit A/D Converter
  - 16/11 chan. with prog. Scan Mode & FIFO
  - Programmable Analog Watchdog feature
  - Conversion: min. 3.75 µs, range: 0 to V_{DD_IO}
  - Start conversion can be triggered by timers
- Up to 72/38 I/O ports
  - 72/38 GPIO lines with High Sink capabilities
  - Atomic bit SET and RES operations

Contents

1 Introduction

This Datasheet contains the description of the STR750 family features, pinout, Electrical Characteristics, Mechanical Data and Ordering information.

For complete information on the Microcontroller memory, registers and peripherals. Please refer to the STR750 Reference Manual.

For information on the ARM7TDMI-S core please refer to the ARM7TDMI-S Technical Reference Manual available from Arm Ltd.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash Programming Reference Manual

For information on third-party development tools, please refer to the http://www.st.com/mcu website.

Table 1. Device summary

Features	STR755FRx	STR751FRx	STR752FRx	STR755FVx	STR750FVx
Flash - Bank 0 (bytes)	64K/128K/256K				
Flash - Bank 1 (bytes)	16K RWW				
RAM (bytes)	16K				
Operating Temp.	-40 to +85°C / -40 to +105°C (see *Table 44*)				
Common Peripherals	3 UARTs, 2 SSPs, 1 I2C, 3 timers 1 PWM timer, 38 I/Os 13 Wake-up lines, 11 A/D Channels			3 UARTs, 2 SSPs, 1 I^2C, 3 timers 1 PWM timer, 72 I/Os 15 Wake-up lines, 16 A/D Channels	
USB/CAN peripherals	None	USB	CAN	None	USB+CAN
Operating Voltage	3.3V or 5V	3.3V	3.3V or 5V		
Packages (**x**)	**T**=LQFP64 10x10, **H**=LFBGA64			**T**=LQFP100 14x14, **H**=LFBGA100	

1.1 Overview

The STR750 family includes devices in 2 package sizes: 64-pin and 100-pin. Both types have the following common features:

ARM7TDMI-S™ core with embedded Flash & RAM

STR750 family has an embedded ARM core and is therefore compatible with all ARM tools and software. It combines the high performance ARM7TDMI-S™ CPU with an extensive range of peripheral functions and enhanced I/O capabilities. All devices have on-chip high-speed single voltage FLASH memory and high-speed RAM.

Figure 1 shows the general block diagram of the device family.

Embedded Flash Memory

Up to 256 KBytes of embedded Flash is available in Bank 0 for storing programs and data. An additional Bank 1 provides 16 Kbytes of RWW (Read While Write) memory allowing it to be erased/programmed on-the-fly. This partitioning feature is ideal for storing application parameters.

- When configured in burst mode, access to Flash memory is performed at CPU clock speed with 0 wait states for sequential accesses and 1 wait state for random access (maximum 60 MHz).
- When not configured in burst mode, access to Flash memory is performed at CPU clock speed with 0 wait states (maximum 32 MHz)

Embedded SRAM

16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

Enhanced Interrupt Controller (EIC)

In addition to the standard ARM interrupt controller, the STR750F embeds a nested interrupt controller able to handle up to 32 vectors and 16 priority levels. This additional hardware block provides flexible interrupt management features with minimal interrupt latency.

Serial Memory Interface (SMI)

The Serial Memory interface is directly able to access up to 4 serial FLASH devices. It communicates at a speed of up to 48 MHz. It can be used to access data, execute code directly or boot the application from external memory. The memory is addressed as 4 banks of up to 16 Mbytes each.

Clocks and start-up

After RESET or when exiting from Low Power Mode, the CPU is clocked immediately by an internal RC oscillator (FREEOSC) at a frequency centered around 5 MHz, so the application code can start executing without delay. In parallel, the 4/8 MHz Oscillator is enabled and its stabilization time is monitored using a dedicated counter.

An oscillator failure detection is implemented: when the clock disappears on the XT1 pin, the circuit automatically switches to the FREEOSC oscillator and an interrupt is generated.

In Run mode, the AHB and APB clock speeds can be set at a large number of different frequencies thanks to the PLL and various prescalers: up to 60 MHz for AHB and up to 32 MHz for APB when fetching from Flash (64 MHz and 32 MHz when fetching from SRAM).

In SLOW mode, the AHB clock can be significantly decreased to reduce power consumption.

The built-in Clock Controller also provides the 48 MHz USB clock directly without any extra oscillators or PLL. For instance, starting from the 4 MHz crystal source, it is possible to obtain in parallel 60 MHz for the AHB clock, 48 MHz for the USB clock and 30 MHz for the APB peripherals.

Boot modes

At start-up, boot pins are used to select one of five boot options:

- Boot from internal flash
- Boot from external serial Flash memory
- Boot from internal boot loader
- Boot from internal SRAM

Booting from SMI memory allows booting from a serial flash. This way, a specific boot monitor can be implemented. Alternatively, the STR750F can boot from the internal boot loader that implements a boot from UART.

Power Supply Schemes

You can connect the device in any of the following ways depending on your application.

- **Power Scheme 1: Single external 3.3V power source**. In this configuration the V_{CORE} supply required for the internal logic is generated internally by the main voltage regulator and the V_{BACKUP} supply is generated internally by the low power voltage regulator. This scheme has the advantage of requiring only one 3.3V power source.
- **Power Scheme 2: Dual external 3.3V and 1.8V power sources.** In this configuration, the internal voltage regulators are switched off by forcing the VREG_DIS pin to high level. V_{CORE} is provided externally through the V_{18} and V_{18REG} power pins and V_{BACKUP} through the V_{18_BKP} pin. This scheme is intended to save power consumption for applications which already provide an 1.8V power supply.
- **Power Scheme 3: Single external 5.0V power source.** In this configuration the V_{CORE} supply required for the internal logic is generated internally by the main voltage regulator and the V_{BACKUP} supply is generated internally by the low power voltage regulator. This scheme has the advantage of requiring only one 5.0V power source.
- **Power Scheme 4: Dual external 5.0V and 1.8V power sources.** In this configuration, the internal voltage regulators are switched off, by forcing the VREG_DIS pin to high level. V_{CORE} is provided externally through the V_{18} and V_{18REG} power pins and V_{BACKUP} through the V_{18_BKP} pin. This scheme is intended to provide 5V I/O capability.

Caution: When powered by 5.0V, the USB peripheral cannot operate.

Low Power modes

The STR750F supports 5 low power modes, SLOW, PCG, WFI, STOP and STANDBY.

- SLOW MODE: the system clock speed is reduced. Alternatively, the PLL and the main oscillator can be stopped and the device is driven by a low power clock (f_{RTC}). The clock is either an external 32.768 kHz oscillator or the internal low power RC oscillator.
- PCG MODE (Peripheral Clock Gating MODE): When the peripherals are not used, their APB clocks are gated to optimize the power consumption.
- WFI MODE (Wait For Interrupts): only the CPU clock is stopped, all peripherals continue to work and can wake-up the CPU when IRQs occur.
- STOP MODE: all clocks/peripherals are disabled. It is also possible to disable the oscillators and the Main Voltage Regulator (In this case the V_{CORE} is entirely powered by V_{18_BKP}). This mode is intended to achieve the lowest power consumption with SRAM and registers contents retained. The system can be woken up by any of the external interrupts / wake-up lines or by the RTC timer which can optionally be kept running. The RTC can be clocked either by the 32.768 kHz Crystal or the Low Power RC Oscillator.
  Alternatively, STOP mode gives flexibility to keep the either main oscillator, or the Flash or the Main Voltage Regulator enabled when a fast start after wake-up is preferred (at the cost of some extra power consumption).
- STANDBY MODE: This mode (only available in single supply power schemes) is intended to achieve the lowest power consumption even when the temperature is increasing. The digital power supply (V_{CORE}) is completely removed (no leakage even at high ambient temperature). SRAM and all register contents are lost. Only the RTC remains powered by V_{18_BKP}. The STR750F can be switched back from STANDBY to RUN mode by a trigger event on the WKP_STDBY pin or an alarm timeout on the RTC counter.

Caution: It is important to bear in mind that it is forbidden to remove power from the V_{DD_IO} power supply in any of the Low Power Modes (even in STANDBY MODE).

DMA

The flexible 4-channel general-purpose DMA is able to manage memory to memory, peripheral to memory and memory to peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

The DMA can be used with the main peripherals: UART0, SSP0, Motor control PWM timer (PWM), standard timer TIM0 and ADC.

RTC (Real Time Clock)

The real time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by an external 32.768 kHz oscillator or the internal low power RC oscillator. The RC has a typical frequency of 300 kHz and can be calibrated.

WDG (Watchdog Timer)

The watchdog timer is based on a 16-bit downcounter and 8-bit prescaler. It can be used as watchdog to reset the device when a problem occurs, or as free running timer for application time out management.

Timebase Timer (TB)

The timebase timer is based on a 16-bit auto-reload counter and not connected to the I/O pins. It can be used for software triggering, or to implement the scheduler of a real time operating system.

Synchronizable Standard Timers (TIM2:0)

The three standard timers are based on a 16-bit auto-reload counter and feature up to 2 input captures and 2 output compares (for external triggering or time base / time out management). They can work together with the PWM timer via the Timer Link feature for synchronization or event chaining. In reset state, timer Alternate Function I/Os are connected to the same
I/O ports in both 64-pin and 100-pin devices. To optimize timer functions in 64-pin devices, timer Alternate Function I/Os can be connected, or “remapped”, to other I/O ports as summarized in *Table 2* and detailed in *Table 5*. This remapping is done by the application via a control register.

Table 2. Standard timer alternate function I/Os

Standard Timer Functions		Number of Alternate Function I/Os		
		100-pin package	64-pin package	
			Default mapping	Remapped
TIM 0	Input Capture	2	1	2
	Output Compare/PWM	2	1	2
TIM 1	Input Capture	2	1	1
	Output Compare/PWM	2	1	1
TIM 2	Input Capture	2	2	2
	Output Compare/PWM	2	1	2

Any of the standard timers can be used to generate PWM outputs. One timer (TIM0) is mapped to a DMA channel.

Motor Control PWM timer (PWM)

The Motor Control PWM Timer (PWM) can be seen as a three-phase PWM multiplexed on 6 channels. The 16-bit PWM generator has full modulation capability (0...100%), edge or centre-aligned patterns and supports dead-time insertion. It has many features in common with the standard TIM timers which has the same architecture and it can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.The PWM timer is mapped to a DMA channel.

I²C bus

The I²C bus interface can operate in multi-master and slave mode. It can support standard and fast modes (up to 400KHz).

High Speed Universal Asynch. Receiver Transmitter (UART)

The three UART interfaces are able to communicate at speeds of up to 2 Mbit/s. They provide hardware management of the CTS and RTS signals and have LIN Master capability.

To optimize the data transfer between the processor and the peripheral, two FIFOs (receive/transmit) of 16 bytes each have been implemented.

One UART can be served by the DMA controller (UART0).

Synchronous Serial Peripheral (SSP)

The two SSPs are able to communicate up to 8 Mbit/s (SSP1) or up to 16 Mbit/s (SSP0) in standard full duplex 4-pin interface mode as a master device or up to 2.66 Mbit/s as a slave device. To optimize the data transfer between the processor and the peripheral, two FIFOs (receive/transmit) of 8 x 16 bit words have been implemented. The SSPs support the Motorola SPI or TI SSI protocols.

One SSP can be served by the DMA controller (SSP0).

Controller Area Network (CAN)

The CAN is compliant with the specification 2.0 part B (active) with a bit rate up to 1Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Up to 32 message objects are handled through an internal RAM buffer. In LQFP64 devices, CAN and USB cannot be connected simultaneously.

Universal Serial Bus (USB)

The STR750F embeds a USB device peripheral compatible with the USB Full speed 12Mbs. The USB interface implements a full speed (12 Mbit/s) function interface. It has software configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock source is generated from the internal main PLL. V_{DD} must be in the range 3.3V±10% for USB operation.

ADC (Analog to Digital Converter)

The 10-bit Analog to Digital Converter, converts up to 16 external channels (11 channels in 64-pin devices) in single-shot or scan modes. In scan mode, continuous conversion is performed on a selected group of analog inputs. The minimum conversion time is 3.75 µs (including the sampling time).
The ADC can be served by the DMA controller.

An analog watchdog feature allows you to very precisely monitor the converted voltage of up to four channels. An IRQ is generated when the converted voltage is outside the programmed thresholds.

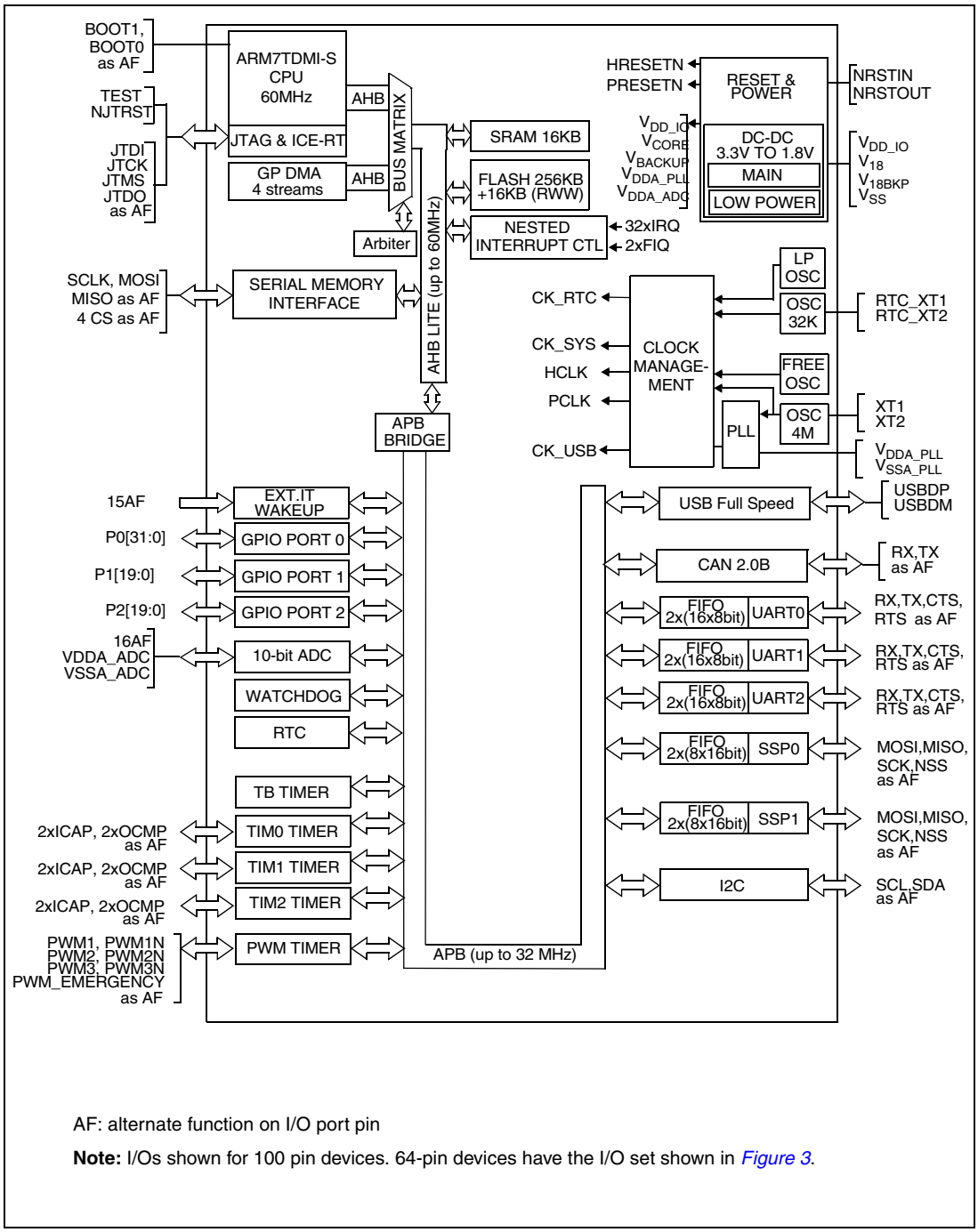
The events generated by TIM0, TIM2 and PWM timers can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

GPIOs (General Purpose Input/Output)

Each of the 72 GPIO pins (38 GPIOs in 64-pin devices) can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as Peripheral Alternate Function. Port 1.15 is an exception, it can be used as general-purpose input only or wake-up from STANDBY mode (WKP_STDBY). Most of the GPIO pins are shared with digital or analog alternate functions.

1.2 Block Diagram

Figure 1. STR750 block diagram



AF: alternate function on I/O port pin

Note: I/Os shown for 100 pin devices. 64-pin devices have the I/O set shown in *Figure 3*.

2 Pin Description

Figure 2. LQFP100 Pinout

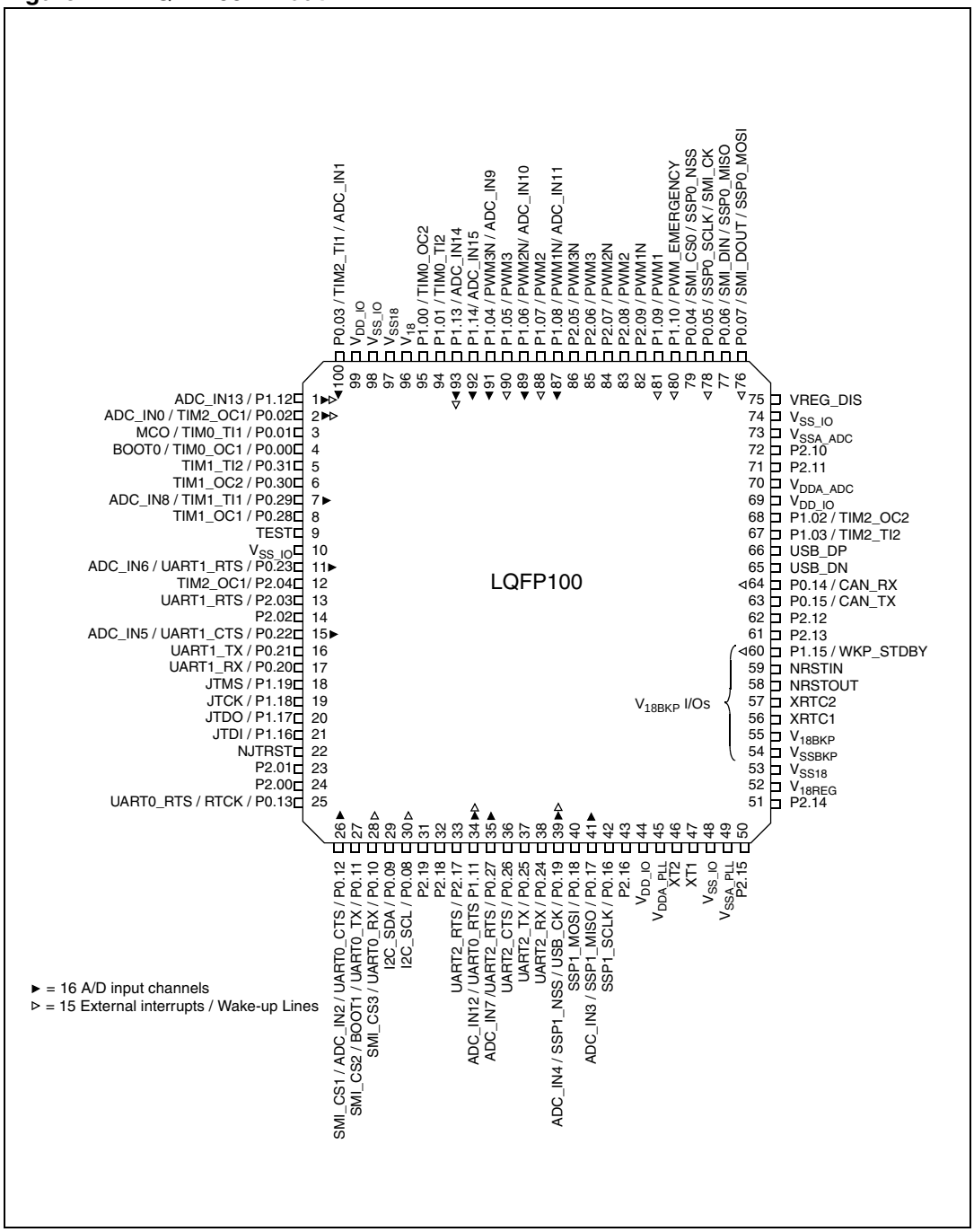


Figure 3. LQFP64 Pinout

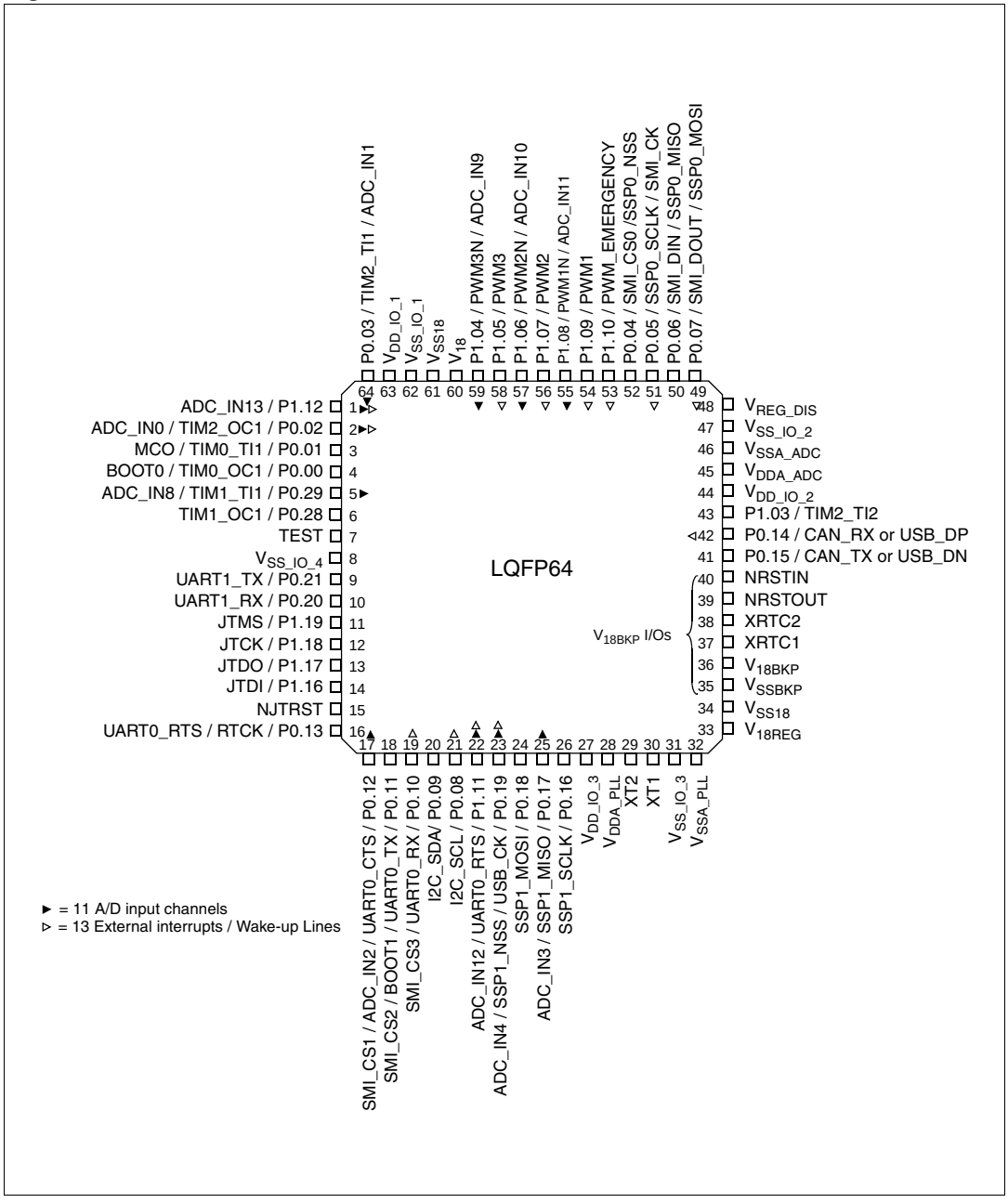


Table 3. LFBGA100 ball connections

	1	2	3	4	5	6	7	8	9	10
A	P0.03	P1.13	P1.14	P1.04	P1.06	P1.08	P0.05	P0.06	P0.07	P1.02
B	P1.12	P0.02	P0.01	P1.05	P1.07	P1.09	P0.04	P2.13	P1.03	P2.10
C	P0.31	P0.00	V_{DD_IO}	V_{18}	P1.10	P2.09	V_{SS_IO}	V_{SSA_ADC}	P2.11	USB_DP
D	P0.29	P0.30	V_{SS_IO}	V_{SS18}	P1.01	P1.15	V_{DD_IO}	V_{DDA_ADC}	P2.12	USB_DN
E	P0.28	P0.23	P0.22	V_{SS_IO}	TEST	P1.00	NRSTOUT	VREG_DIS	NRSTIN	P0.14
F	P2.03	P0.21	P0.20	P2.02	P2.04	P2.05	P2.06	V_{SS18}	V_{SSBKP}	P0.15
G	NJTRST	P1.18	P1.19	P2.01	P2.00	P2.07	2.08	V_{18REG}	V_{18BKP}	XRTC2
H	P0.13	P1.16	P1.17	P2.19	P2.18	P2.17	P0.24	P2.14	P2.16	XRTC1
J	P0.11	P0.12	P1.11	P0.27	P0.19	P0.26	P0.25	P2.15	V_{DD_IO}	V_{SS_IO}
K	P0.10	P0.09	P0.08	P0.18	P0.17	P0.16	XT1	XT2	V_{DDA_PLL}	V_{SSA_PLL}

Table 4. LFBGA64 ball connections

	1	2	3	4	5	6	7	8
A	P0.03	V_{SS_IO}	P1.04	P1.06	P1.08	P0.05	P0.06	P0.07
B	P1.12	V_{DD_IO}	P1.05	P1.07	P1.09	P0.04	P1.10	P1.03
C	P0.01	P0.02	P0.00	V_{18}	V_{SS18}	V_{DD_IO}	V_{SS_IO}	P0.14
D	P0.29	P0.28	TEST	V_{SS_IO}	VREG_DIS	V_{DDA_ADC}	V_{SSA_ADC}	P0.15
E	P1.18	P1.19	P0.20	P0.21	NRSTOUT	NRSTIN	V_{18BKP}	XRTC2
F	P0.13	NJTRST	P1.16	P1.17	V_{18REG}	V_{SS18}	V_{SSBKP}	XRTC1
G	P0.11	P0.12	P1.11	P0.19	V_{DD_IO}	V_{SS_IO}	V_{DDA_PLL}	V_{SSA_PLL}
H	P0.10	P0.09	P0.08	P0.17	P0.18	P0.16	XT2	XT1

2.0.1 Pin Description Table

Legend / Abbreviations for *Table 5*:

Type: I = input, O = output, S = supply,

Input Levels: All Inputs are LVTTL at V_{DD_IO} = 3.3V+/-0.3V or TTL at V_{DD_IO} = 5V± 0.5V. In both cases, T_T means V_{ILmax} =0.8V V_{IHmin}=2.0V

Inputs: All inputs can be configured as floating or with internal weak pull-up or pull down (pu/pd)

Outputs: All Outputs can be configured as Open Drain (OD) or Push-Pull (PP) (see also note 6 below *Table 5*). There are 3 different types of Output with different drives and speed characteristics:

– O8: f_{max} = 40 MHz on C_L=50pF and 8 mA static drive capability for V_{OL}=0.4V and up to 20 mA for V_{OL}=1.3V (see*Output driving current on page 54*)

– O4: f_{max} = 20 MHz on C_L=50pF and 4 mA static drive capability for V_{OL}=0.4V (see*Output driving current on page 54*)

– O2: f_{max} = 10 MHz on C_L=50pF and 2 mA static drive capability of for V_{OL}=0.4V (see*Output driving current on page 54*)

External Interrupts/wake-up lines: EITx

Port Reset State

The reset state of the I/O ports is GPIO input floating. Exceptions are P1[19:16] and P0.13 which are configured as JTAG alternate functions:

- The JTAG inputs (JTDI, JTMS and JTDI) are configured as input floating and are ready to accept JTAG sequences.
- The JTAG output JTDO is configured as floating when idle (no JTAG operation) and is configured in output push-pull only when serial JTAG data must be output.
- The JTAG output RTCK is always configured as output push-pull. It outputs '0' level during the reset phase and then outputs the JTCK input signal resynchronized 3 times by the internal AHB clock.
- The GPIO_PCx registers do not control JTAG AF selection, so the reset values of GPIO_PCx for P1[19:16] and P0. 13 are the same as other ports. Refer to the GPIO section of the STR750 Reference Manual for the register description and reset values.
- P0.11 and P0.00 are sampled by the boot logic after reset, prior to fetching the first word of user code at address 0000 0000h.
- When booting from SMI (and only in this case), the reset state of the following GPIOs is "SMI alternate function output enabled":
  - P0.07 (SMI_DOUT)
  - P0.05 (SMI_CLK)
  - P0.04 (SMI_CS0)
  - P0.06 (SMI_DIN)

  Note that the other SMI pins: SMI_CS1,2,3 (P0.12, P0.11, P0.10) are not affected.

To avoid excess power consumption, unused I/O ports must be tied to ground.

Table 5. STR750F pin description

Pin n°				Pin Name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100	LFBGA100	LQFP64	LFBGA64			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (1)	PP				
1	B1	1	B1	P1.12 / ADC_IN13	I/O	T_T	**X**	X	EIT12	O8	X	X		**Port 1.12**	ADC: Analog input 13	
2	B2	2	C2	P0.02 / TIM2_OC1 / ADC_IN0	I/O	T_T	**X**	X	EIT0	O8	X	X		**Port 0.02**	TIM2: Output Compare 1(2)	ADC: Analog input 0
3	B3	3	C1	P0.01 / TIM0_TI1 / MCO	I/O	T_T	**X**	X		O8	X	X		**Port 0.01**	TIM0: Input Capture / trigger / external clock 1	Main Clock Output
4	C2	4	C3	P0.00 / TIM0_OC1 / BOOT0	I/O	T_T	**X**	X		O8	X	X		**Port 0.00 / Boot mode selection input 0**	TIM0: Output Compare 1	
5	C1			P0.31 / TIM1_TI2	I/O	T_T	**X**	X		O2	X	X		**Port 0.31**	TIM1: Input Capture / trigger / external clock 2	
6	D2			P0.30 / TIM1_OC2	I/O	T_T	**X**	X		O2	X	X		**Port 0.30**	TIM1: Output Compare 2	

Table 5. STR750F pin description (continued)

Pin n°				Pin Name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100	LFBGA100	LQPFP64	LFBGA64			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (1)	PP				
7	D1	5	D1	P0.29 / TIM1_TI1 / ADC_IN8	I/O	T_T	**X**	X		O2	X	X		**Port 0.29**	TIM1: Input Capture 1	ADC: Analog input 8
8	E1	6	D2	P0.28 / TIM1_OC1	I/O	T_T	**X**	X		O2	X	X		**Port 0.28**	TIM1: Output Compare 1	
9	E5	7	D3	TEST	I									Reserved, must be tied to ground		
10	E4	8	D4	VSS_IO	S									Ground Voltage for digital I/Os		
11	E2			P0.23 / UART1_RTS / ADC_IN6	I/O	T_T	**X**	X		O2	X	X		**Port 0.23**	UART1: Ready To Send output(2)	ADC analog input 6
12	F5			P2.04 / TIM2_OC1	I/O	T_T	**X**	X		O2	X	X		**Port 2.04**	TIM2: Output Compare 1(2)	
13	F1			P2.03 / UART1_RTS	I/O	T_T	**X**	X		O2	X	X		**Port 2.03**	UART1: Ready To Send output(2)	
14	F4			P2.02	I/O	T_T	**X**	X		O2	X	X		**Port 2.02**		
15	E3			P0.22 / UART1_CTS / ADC_IN5	I/O	T_T	**X**	X		O2	X	X		**Port 0.22**	UART1: Clear To Send input	ADC: Analog input 5
16	F2	9	E4	P0.21 / UART1_TX	I/O	T_T	**X**	X		O2	X	X		**Port 0.21**	UART1: Transmit data output (remappable to P0.15)(2)	
17	F3	10	E3	P0.20 / UART1_RX	I/O	T_T	**X**	X		O2	X	X		**Port 0.20**	UART1: Receive data input (remappable to P0.14)(2)	
18	G3	11	E2	P1.19 / JTMS	I/O	T_T	X	X		O2	X	X		**JTAG mode selection input(4)**	Port 1.19	
19	G2	12	E1	P1.18 / JTCK	I/O	T_T	X	X		O2	X	X		**JTAG clock input(4)**	Port 1.18	
20	H3	13	F4	P1.17 / JTDO	I/O	T_T	X	X		O8	X	X		**JTAG data output(4)**	Port 1.17	
21	H2	14	F3	P1.16 / JTDI	I/O	T_T	X	X		O2	X	X		**JTAG data input(4)**	Port 1.16	
22	G1	15	F2	NJTRST	I	T_T								JTAG reset input(3)		
23	G4			P2.01	I/O	T_T	**X**	X		O2	X	X		**Port 2.01**		
24	G5			P2.00	I/O	T_T	**X**	X		O2	X	X		**Port 2.00**		
25	H1	16	F1	P0.13 / RTCK / UART0_RTS	I/O	T_T	X	X		O8	X	X		**JTAG return clock output(4)**	Port 0.13	
															UART0: Ready To Send output(2)	
26	J2	17	G2	P0.12 / UART0_CTS / ADC_IN2 / SMI_CS1	I/O	T_T	**X**	X		O4	X	X		**Port 0.12**	UART0: Clear To Send input	ADC: Analog input 2
															Serial Memory Interface: chip select output 1	

Table 5. STR750F pin description (continued)

Pin n°				Pin Name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100	LFBGA100	LQFP64	LFBGA64			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (1)	PP				
27	J1	18	G1	P0.11 / UART0_TX / BOOT1 / SMI_CS2	I/O	T_T	**X**	X		O4	X	X		**Port 0.11/Boot mode selection input 1**	UART0: Transmit data output	Serial Memory Interface: chip select output 2
28	K1	19	H1	P0.10 / UART0_RX / SMI_CS3	I/O	T_T	**X**	X	EIT4	O2	X	X		**Port 0.10**	UART0: Receive Data input	Serial Memory Interface: chip select output 3
29	K2	20	H2	P0.09 / I2C_SDA	I/O	T_T	**X**	X		O4	X	X		**Port 0.09**	I2C: Serial Data	
30	K3	21	H3	P0.08 / I2C_SCL	I/O	T_T	**X**	X	EIT3	O4	X	X		**Port 0.08**	I2C: Serial clock	
31	H4			P2.19	I/O	T_T	**X**	X		O2	X	X		**Port 2.19**		
32	H5			P2.18	I/O	T_T	**X**	X		O2	X	X		**Port 2.18**		
33	H6			P2.17 / UART2_RTS	I/O	T_T	**X**	X		O2	X	X		**Port 2.17**	UART2: Ready To Send output(2)	
34	J3	22	G3	P1.11 /UART0_RTS ADC_IN12	I/O	T_T	**X**	X	EIT11	O8	X	X		**Port 1.11**	UART0: Ready To Send output(2)	ADC: Analog input 12
35	J4			P0.27 / UART2_RTS / ADC_IN7	I/O	T_T	**X**	X		O2	X	X		**Port 0.27**	UART2: Ready To Send output(6)	ADC: Analog input 7
36	J6			P0.26 / UART2_CTS	I/O	T_T	**X**	X		O2	X	X		**Port 0.26**	UART2: Clear To Send input	
37	J7			P0.25 / UART2_TX	I/O	T_T	**X**	X		O2	X	X		**Port 0.25**	UART2: Transmit data output (remappable to P0.13)(6)	
38	H7			P0.24 / UART2_RX	I/O	T_T	**X**	X		O2	X	X		**Port 0.24**	UART2: Receive data input (remappable to P0.12)(6)	
39	J5	23	G4	P0.19 / USB_CK / SSP1_NSS / ADC_IN4	I/O	T_T	**X**	X	EIT6	O2	X	X		**Port 0.19**	SSP1: Slave select input (remappable to P0.11)(6)	ADC: Analog input 4
															USB: 48 MHz Clock input	
40	K4	24	H5	P0.18 / SSP1_MOSI	I/O	T_T	**X**	X		O2	X	X		**Port 0.18**	SSP1: Master out/slave in data (remappable to P0.10)(6)	
41	K5	25	H4	P0.17 / SSP1_MISO / ADC_IN3	I/O	T_T	**X**	X		O2	X	X		**Port 0.17**	SSP1: Master in/slave out data (remappable to P0.09)(6)	ADC: Analog input 3
42	K6	26	H6	P0.16 / SSP1_SCLK	I/O	T_T	**X**	X		O2	X	X		**Port 0.16**	SSP1: serial clock (remappable to P0.08)(6)	
43	H9			P2.16	I/O	T_T	**X**	X		O2	X	X		**Port 2.16**		
44	J9	27	G5	VDD_IO	S									Supply voltage for digital I/Os		
45	K9	28	G7	VDDA_PLL	S									Supply voltage for PLL		

Table 5. STR750F pin description (continued)

Pin n°				Pin Name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function
LQFP100	LFBGA100	LQFP64	LFBGA64			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (1)	PP			
46	K8	29	H7	XT2										4 MHz main oscillator	
47	K7	30	H8	XT1											
48	J10	31	G6	VSS_IO	S									Ground voltage for digital I/Os	
49	K10	32	G8	VSSA_PLL	S									Ground voltage for PLL	
50	J8			P2.15	I/O	T_T	**X**	X		O2	X	X		**Port 2.15**	
51	H8			P2.14	I/O	T_T	**X**	X		O2	X	X		**Port 2.14**	
52	G8	33	F5	V18REG	S									Stabilization for main voltage regulator. Requires external capacitors of at least 10µF between V18REG and VSS18. See *Figure 4*. To be connected to the 1.8V external power supply when embedded regulators are not used,	
53	F8	34	F6	VSS18	S									Ground Voltage for the main voltage regulator	
54	F9	35	F7	VSSBKP	S									Stabilization for low power voltage regulator.	
55	G9	36	E7	V18BKP	S									Ground Voltage for the low power voltage regulator. Requires external capacitors of at least 1µF between V18BKP and VSSBKP. See *Figure 4*. To be connected to the 1.8V external power supply when embedded regulators are not used,	
56	H10	37	F8	XRTC1									X	32 kHz oscillator for Realtime Clock	
57	G10	38	E8	XRTC2									X		
58	E7	39	E5	NRSTOUT	O								X	Reset output	
59	E9	40	E6	NRSTIN	I	T_T							X	Reset input	
60	D6			P1.15 / WKP_STDBY	I	T_T	**X**		EIT15				X	**Port 1.15**	Wake-up from STANDBY input pin
61	B8			P2.13	I/O	T_T	**X**	X		O2	X	X		**Port 2.13**	
62	D9			P2.12	I/O	T_T	**X**	X		O2	X	X		**Port 2.12**	
63	F10	41 (5)	D8 (5)	P0.15 / CAN_TX	I/O	T_T	**X**	X		O2	X	X		**Port 0.15**	CAN: Transmit data output
64	E10	42 (5)	C8 (5)	P0.14 / CAN_RX	I/O	T_T	**X**	X	EIT5	O2	X	X		**Port 0.14**	CAN: Receive data input
65	D10	41 (5)	D8 (5)	USB_DN	I/O									USB: bidirectional data (data -)	
66	C10	42 (5)	C8 (5)	USB_DP	I/O									USB: bidirectional data (data +)	
67	B9	43	B8	P1.03 / TIM2_TI2	I/O	T_T	**X**	X		O2	X	X		**Port 1.03**	TIM2: Input Capture / trigger / external clock 2 (remappable to P0.07)(6)
68	A10			P1.02 / TIM2_OC2	I/O	T_T	**X**	X		O2	X	X		**Port 1.02**	TIM2: Output compare 2 (remappable to P0.06)(6)
69	D7	44	C6	VDD_IO	S									Supply Voltage for digital I/Os	
70	D8	45	D6	VDDA_ADC	S									Supply Voltage for A/D converter	

Table 5. STR750F pin description (continued)

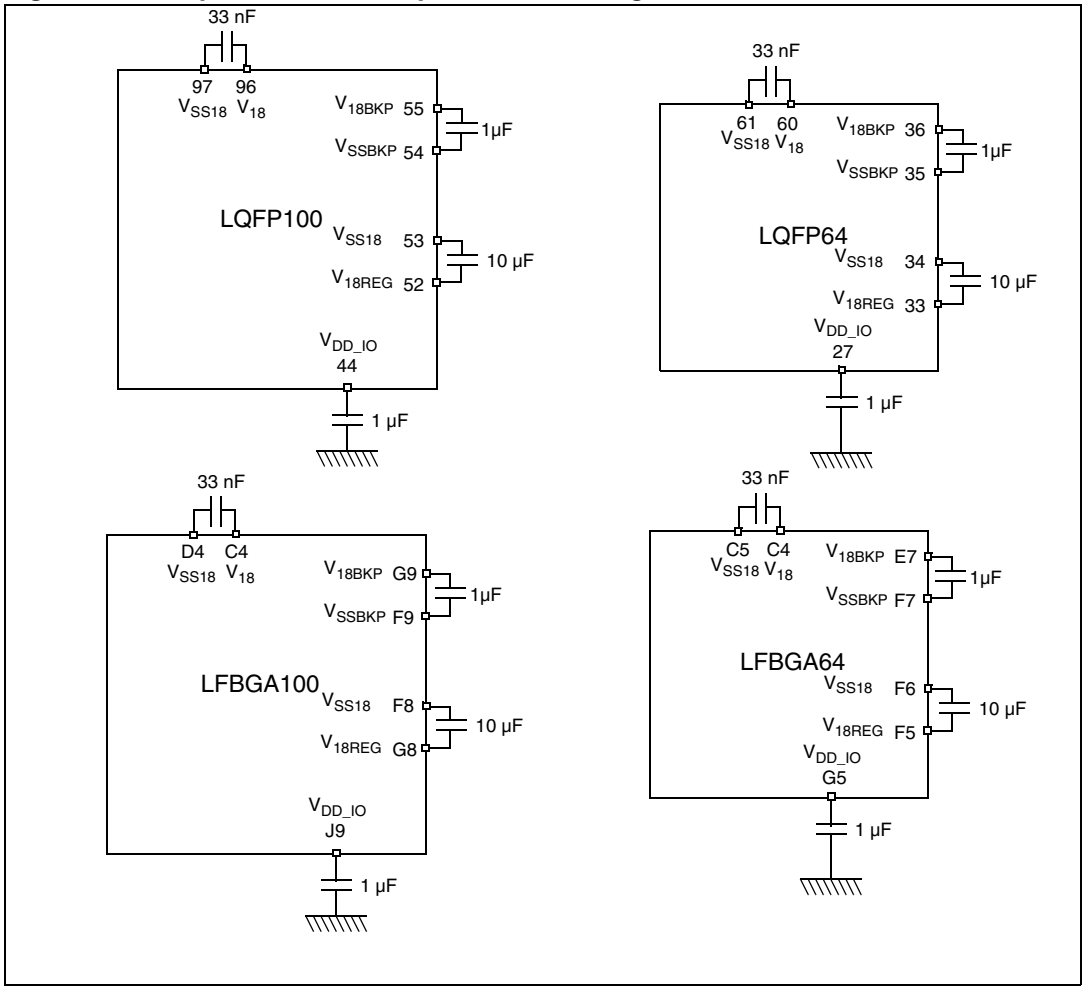
Pin n°				Pin Name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100	LFBGA100	LQPFP64	LFBGA64			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (1)	PP				
71	C9			P2.11	I/O	T_T	**X**	X		O2	X	X		**Port 2.11**		
72	B10			P2.10	I/O	T_T	**X**	X		O2	X	X		**Port 2.10**		
73	C8	46	D7	VSSA_ADC	S									Ground Voltage for A/D converter		
74	C7	47	C7	VSS_IO	S									Ground Voltage for digital I/Os		
75	E8	48	D5	VREG_DIS	I	T_T								Voltage Regulator Disable input		
76	A9	49	A8	P0.07 / SMI_DOUT / SSP0_MOSI	I/O	T_T	**X**	X	EIT2	O4	X	X		**Port 0.07**	Serial Memory Interface: data output	SSP0: Master out Slave in data
77	A8	50	A7	P0.06 / SMI_DIN / SSP0_MISO	I/O	T_T	**X**	X		O4	X	X		**Port 0.06**	Serial Memory Interface: data input	SSP0: Master in Slave out data
78	A7	51	A6	P0.05 / SSP0_SCLK / SMI_CK	I/O	T_T	**X**	X	EIT1	O4	X	X		**Port 0.05**	SSP0: Serial clock	Serial Memory Interface: Serial clock output
79	B7	52	B6	P0.04 / SMI_CS0 / SSP0_NSS	I/O	T_T	**X**	X		O4	X	X		**Port 0.04**	Serial Memory Interface: chip select output 0	SSP0: Slave select input
80	C5	53	B7	P1.10 PWM_EMERGENCY	I/O	T_T	**X**	X	EIT10	O2	X	X		**Port 1.10**	PWM: Emergency input	
81	B6	54	B5	P1.09 / PWM1	I/O	T_T	**X**	X	EIT9	O4	X	X		**Port 1.09**	PWM: PWM1 output	
82	C6			P2.09 / PWM1N	I/O	T_T	**X**	X		O2	X	X		**Port 2.09**	PWM: PWM1 complementary output(2)	
83	G7			P2.08 / PWM2	I/O	T_T	**X**	X		O2	X	X		**Port 2.08**	PWM: PWM2 output(2)	
84	G6			P2.07 / PWM2N	I/O	T_T	**X**	X		O2	X	X		**Port 2.07**	PWM: PWM2 complementary output(2)	
85	F7			P2.06 / PWM3	I/O	T_T	**X**	X		O2	X	X		**Port 2.06**	PWM: PWM3 output(2)	
86	F6			P2.05 / PWM3N	I/O	T_T	**X**	X		O2	X	X		**Port 2.05**	PWM: PWM3 complementary output(2)	
87	A6	55	A5	P1.08 / PWM1N / ADC_IN11	I/O	T_T	**X**	X		O4	X	X		**Port 1.08**	PWM: PWM1 complementary output(6)	ADC: analog input 11
88	B5	56	B4	P1.07 / PWM2	I/O	T_T	**X**	X	EIT8	O4	X	X		**Port 1.07**	PWM: PWM2 output(2)	
89	A5	57	A4	P1.06 / PWM2N / ADC_IN10	I/O	T_T	**X**	X		O4	X	X		**Port 1.06**	PWM: PWM2 complementary output(2)	ADC: analog input 10
90	B4	58	B3	P1.05 / PWM3	I/O	T_T	**X**	X	EIT7	O4	X	X		**Port 1.05**	PWM: PWM3 output(2)	
91	A4	59	A3	P1.04 / PWM3N / ADC_IN9	I/O	T_T	**X**	X		O4	X	X		**Port 1.04**	PWM: PWM3 complementary output(2)	ADC: analog input 9
92	A3			P1.14 / ADC_IN15	I/O	T_T	**X**	X		O8	X	X		**Port 1.14**	ADC: analog input 15	
93	A2			P1.13 / ADC_IN14	I/O	T_T	**X**	X	EIT13	O8	X	X		**Port 1.13**	ADC: analog input 14	

Table 5. STR750F pin description (continued)

Pin n°				Pin Name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100	LFBGA100	LQPFP64	LFBGA64			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (1)	PP				
94	D5			P1.01 / TIM0_TI2	I/O	T_T	**X**	X		O2	X	X		**Port 1.01**	TIM0: Input Capture / trigger / external clock 2 (remappable to P0.05)(6)	
95	E6			P1.00 / TIM0_OC2	I/O	T_T	**X**	X		O2	X	X		**Port 1.00**	TIM0: Output compare 2 (remappable to P0.04)(6)	
96	C4	60	C4	V18	S									Stabilization for main voltage regulator. Requires external capacitors 33nF between V18 and VSS18. See *Figure 4*. To be connected to the 1.8V external power supply when embedded regulators are not used.		
97	D4	61	C5	VSS18	S									Ground Voltage for the main voltage regulator.		
98	D3	62	A2	VSS_IO	S									Ground Voltage for digital I/Os		
99	C3	63	B2	VDD_IO	S									Supply Voltage for digital I/Os		
100	A1	64	A1	P0.03 / TIM2_TI1 / ADC_IN1	I/O	T_T	**X**	X		O2	X	X		**Port 0.03**	TIM2: Input Capture / trigger / external clock 1	ADC: analog input 1

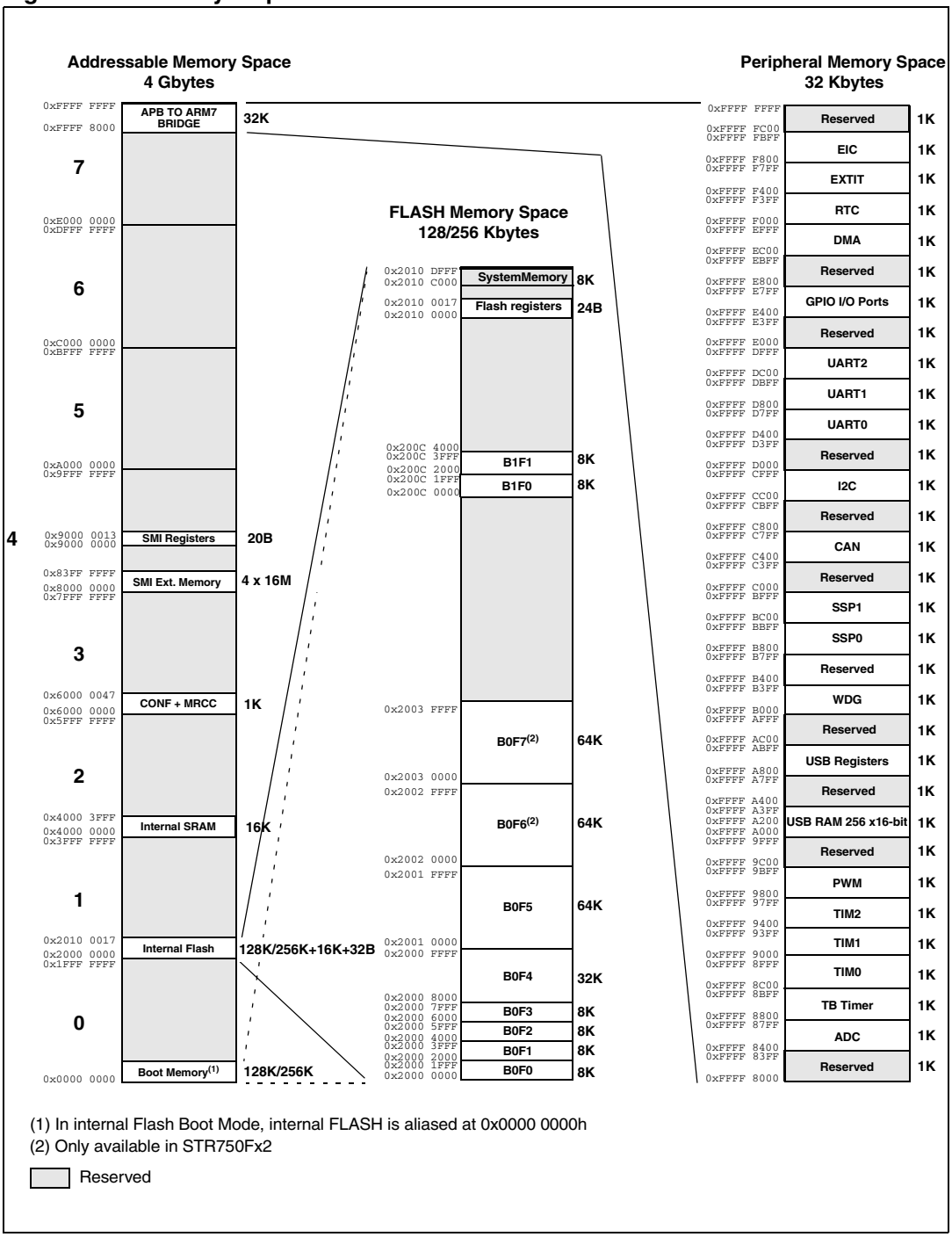
1. None of the I/Os are True Open Drain: when configured as Open Drain, there is always a protection diode between the I/O pin and VDD_IO.
2. In the 100-pin package, this Alternate Function is duplicated on two ports. You can configure one port to use this AF, the other port is then free for general purpose I/O (GPIO), external interrupt/wake-up lines, or analog input (ADC_IN) where these functions are listed in the table.
3. It is mandatory that the NJTRST pin is reset to ground during the power-up phase. It is recommended to connect this pin to NRSTOUT pin (if available) or NRSTIN.
4. After reset, these pins are enabled as JTAG alternate function see (*Port Reset State on page 15*). To use these ports as general purpose I/O (GPIO), the DBGOFF control bit in the GPIO_REMAP0R register must be set by software (in this case, debugging these I/Os via JTAG is not possible).
5. There are two different TQFP and BGA 64-pin packages: in the first one, pins 41 and 42 are mapped to USB DN/DP while for the second one, they are mapped to P0.15/CAN_TX and P0.14/RX.
6. For details on remapping these alternate functions, refer to the GPIO_REMAP0R register description.

Figure 4. Required external capacitors when regulators are used



2.1 Memory map

Figure 5. Memory map



(1) In internal Flash Boot Mode, internal FLASH is aliased at 0x0000 0000h
(2) Only available in STR750Fx2

Reserved

3 Electrical parameters

3.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

3.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25° C and T_A=$T_A$max (given by the selected temperature range).

Data based on product characterisation, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

3.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25° C, V_{DD_IO}=3.3 V (for the 3.0 V≤V_{DD_IO}≤3.6 V voltage range) and V_{18}=1.8 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

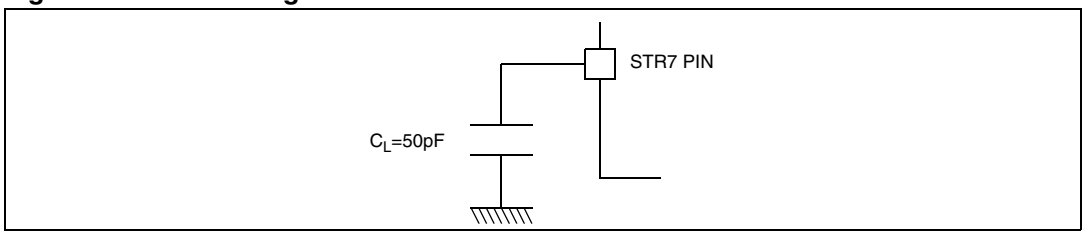
3.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

3.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

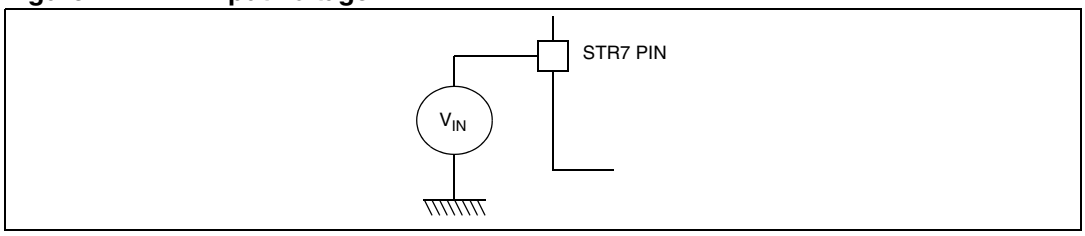
Figure 6. Pin loading conditions



3.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 7. Pin input voltage

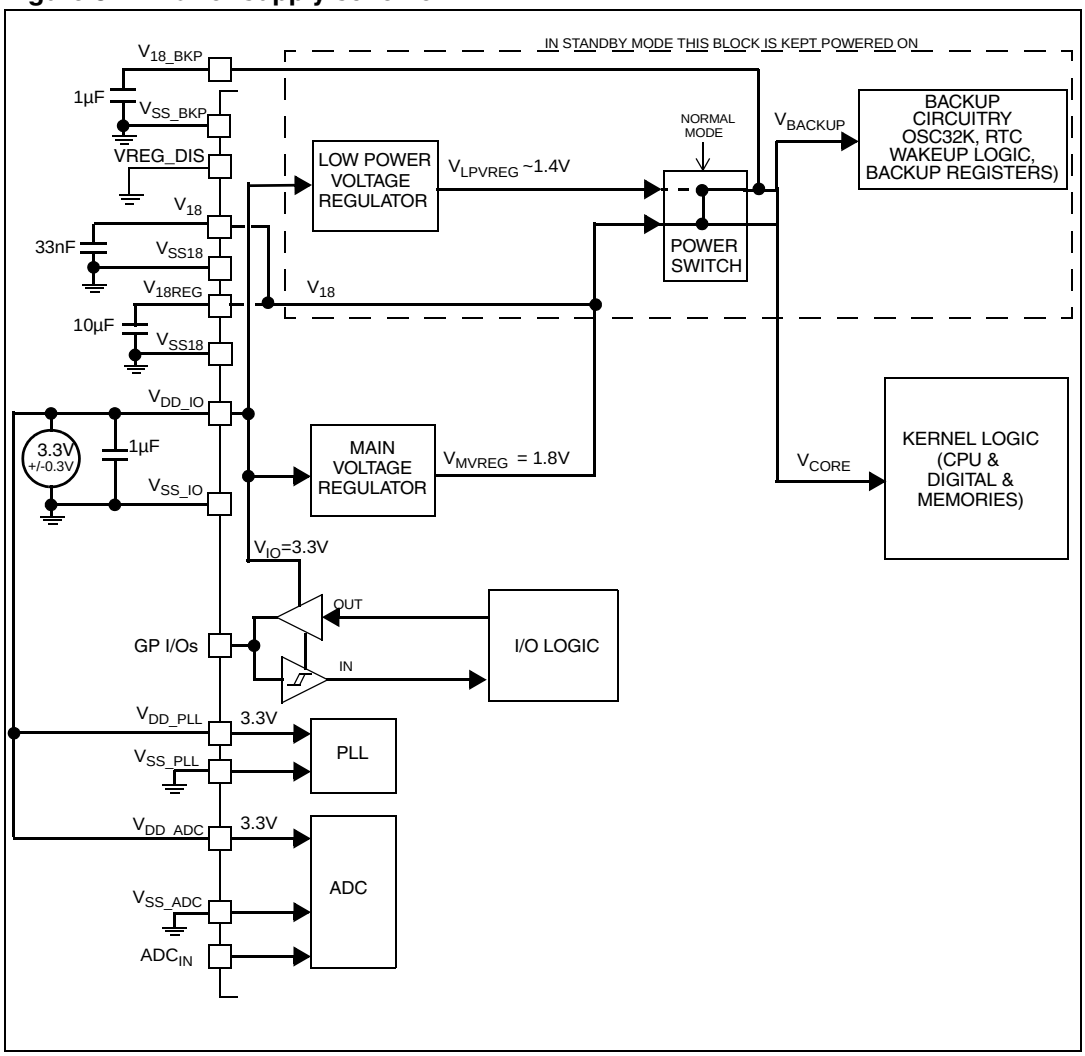


3.1.6 Power Supply Schemes

When mentioned, some electrical parameters can refer to a dedicated power scheme among the four possibilities. The four different power schemes are described below.

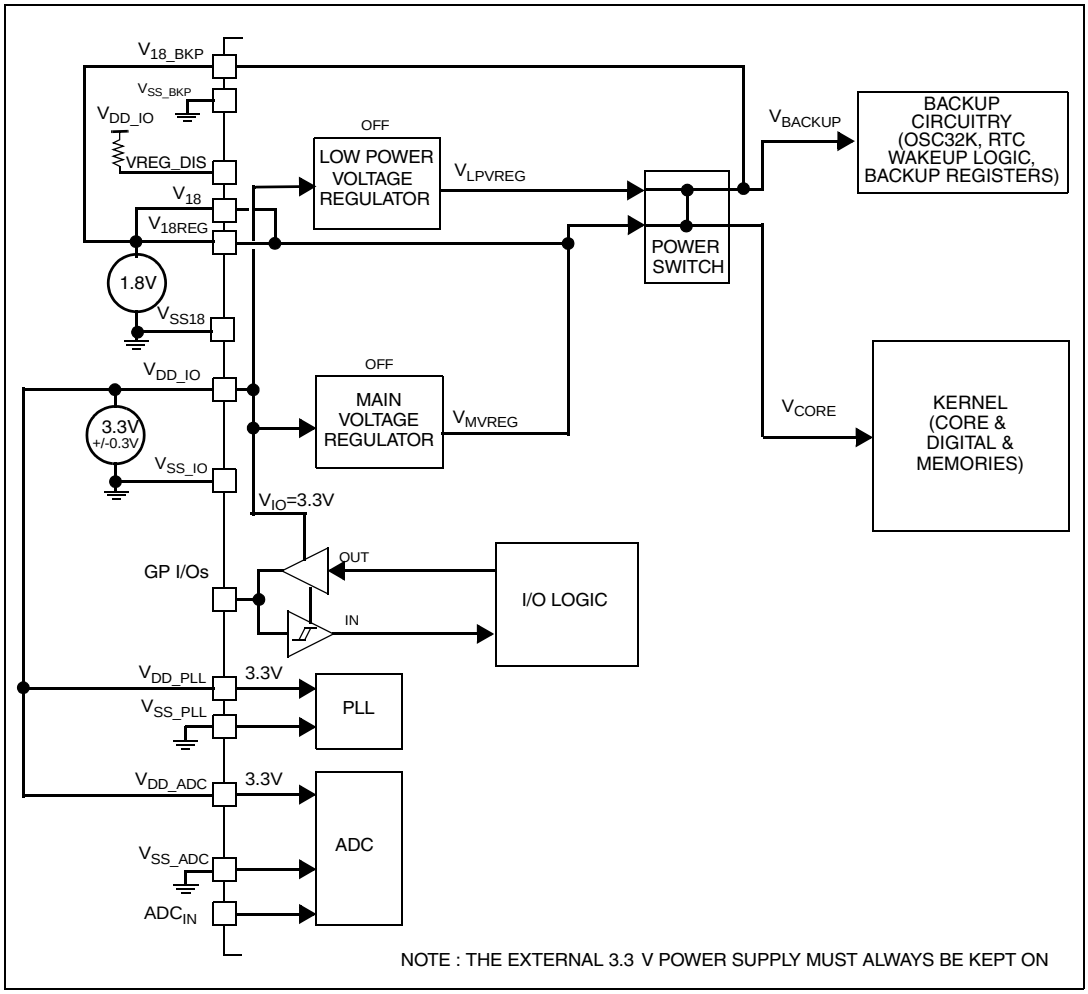
Power supply scheme 1: Single external 3.3 V power source

Figure 8. Power supply scheme 1



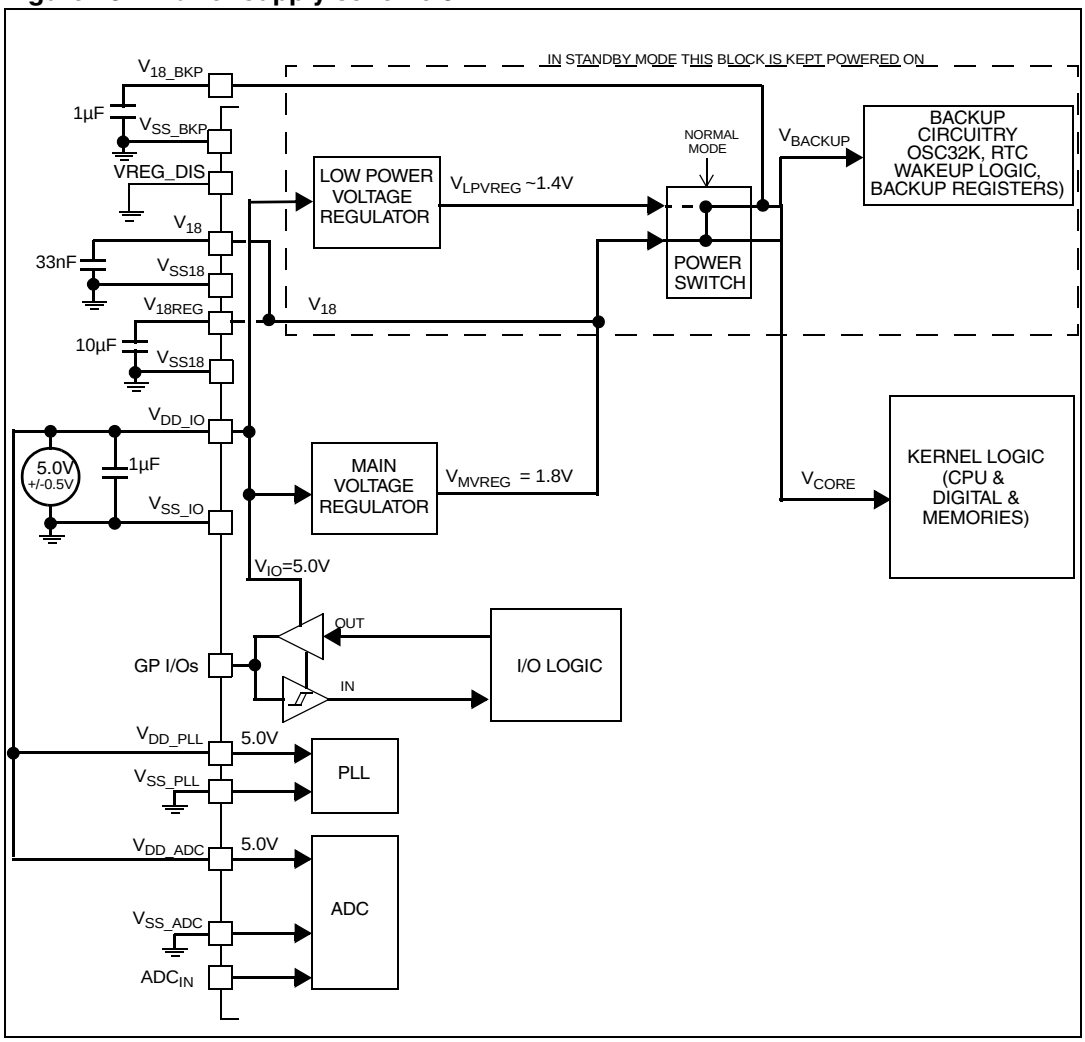
Power supply scheme 2: Dual external 1.8V and 3.3V supply

Figure 9. Power supply scheme 2



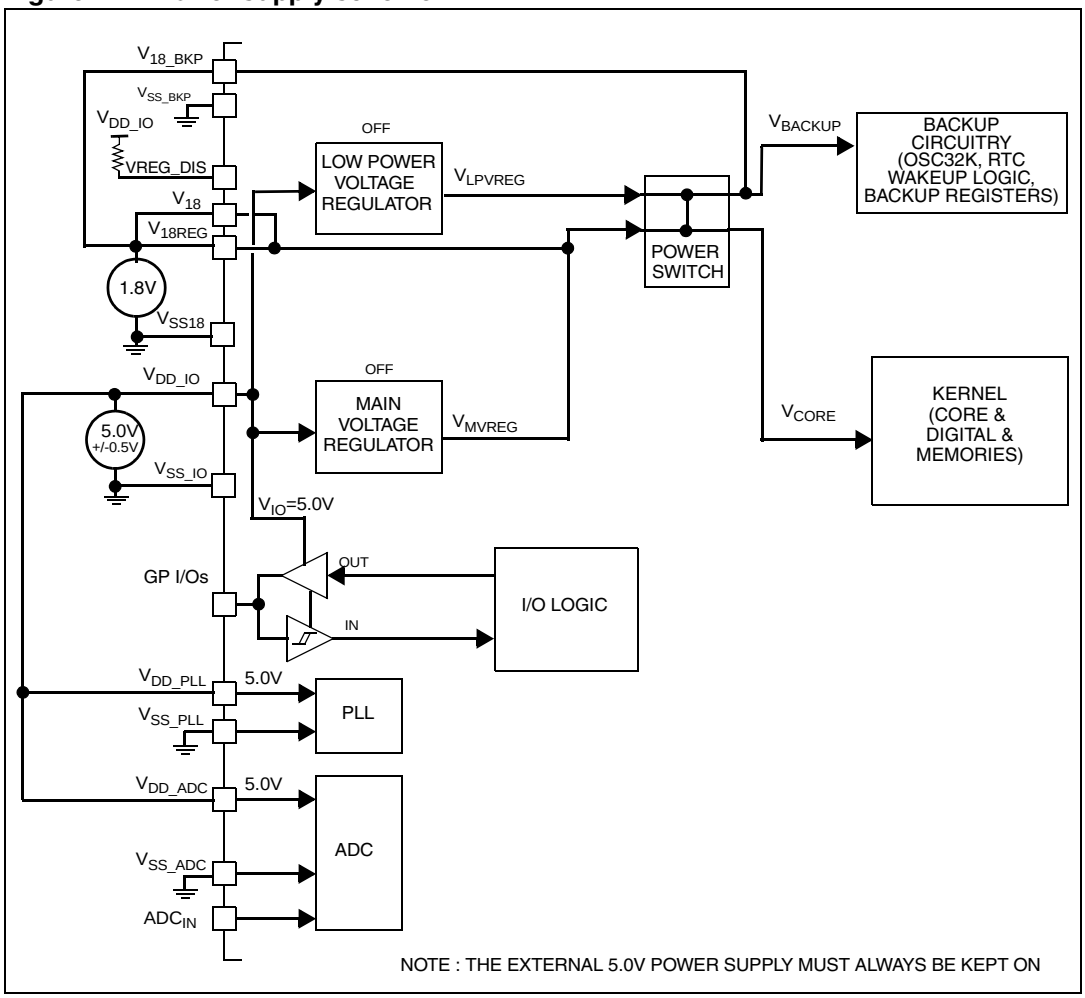
Power supply scheme 3: Single external 5 V power source

Figure 10. Power supply scheme 3



Power supply scheme 4: Dual external 1.8 V and 5.0 V supply

Figure 11. Power supply scheme 4



3.1.7 I/O characteristics versus the various power schemes (3.3V or 5.0V)

Unless otherwise mentioned, all the I/O characteristics are valid for both

- V_{DD_IO}=3.0 V to 3.6 V with bit EN33=1
- V_{DD_IO}=4.5 V to 5.5 V with bit EN33=0

When V_{DD_IO}=3.0 V to 3.6 V, I/Os are not 5V tolerant.

3.1.8 Current Consumption Measurements

All the current consumption measurements mentioned below refer to Power scheme 1 and 2 as described in *Figure 12* and *Figure 13*

Figure 12. Power consumption measurements in power scheme 1 (regulators enabled)

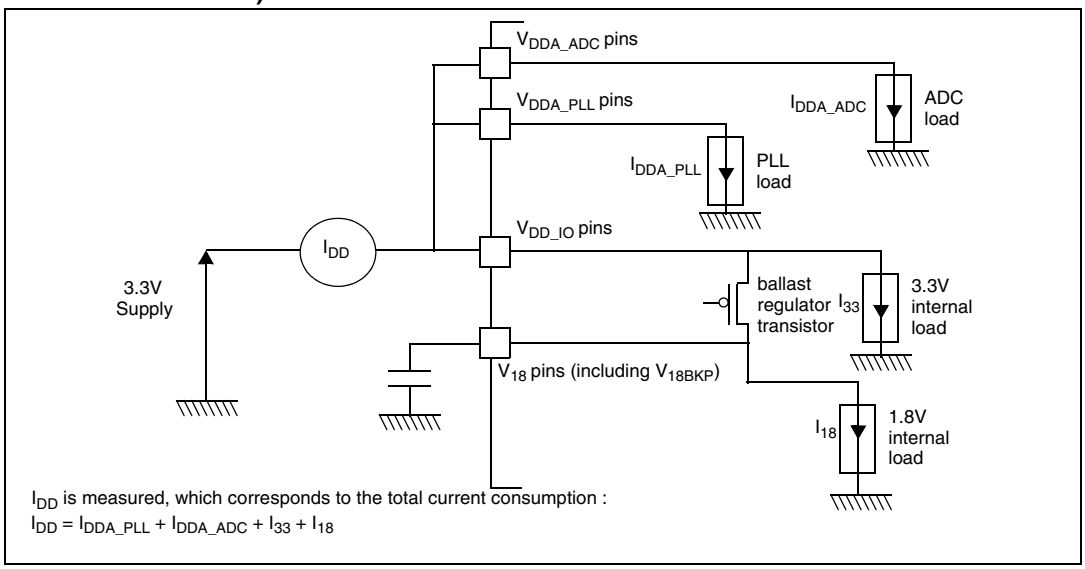


Figure 13. Power consumption measurements in power scheme 2 (regulators disabled)

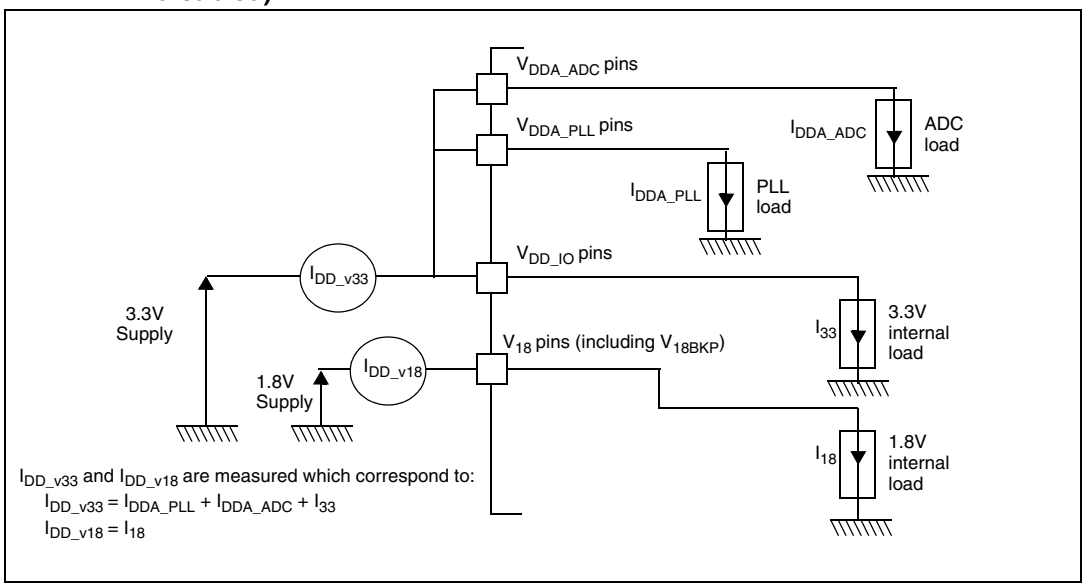


Figure 14. Power consumption measurements in power scheme 3 (regulators enabled)

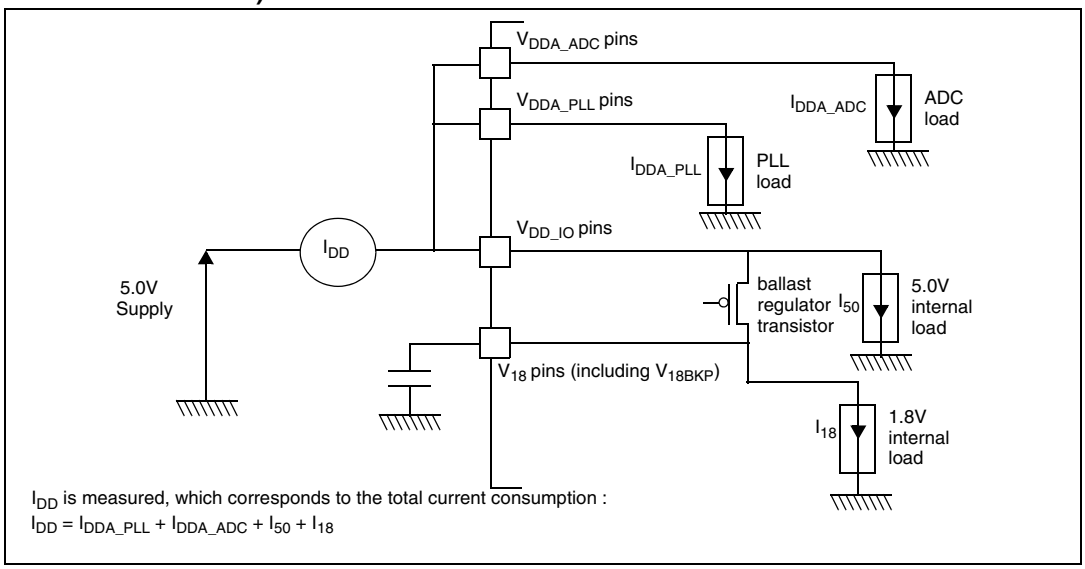
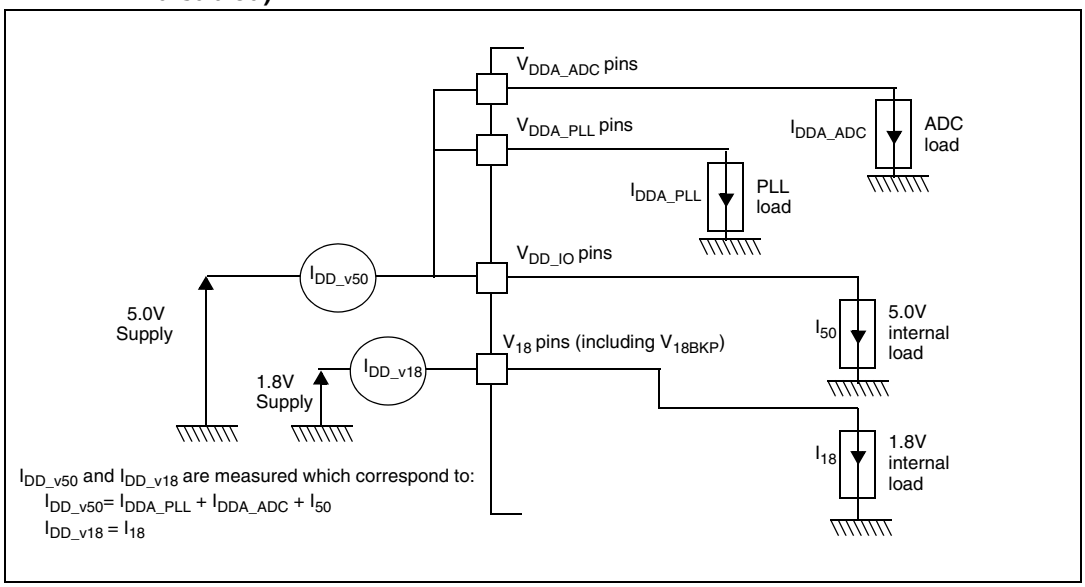


Figure 15. Power consumption measurements in power scheme 4 (regulators disabled)



3.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3.2.1 Voltage characteristics

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD_x} - V_{SS_X} (1)	Including V_{DDA_ADC} and V_{DDA_PLL}	-0.3	6.5	V
V_{18} - V_{SS18}	Digital 1.8 V Supply voltage on all V_{18} power pins (when 1.8 V is provided externally)	-0.3	2.0	
V_{IN}	Input voltage on any pin (2)	V_{SS}-0.3 to V_{DD_IO}+0.3	V_{SS}-0.3 to V_{DD_IO}+0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different 3.3 V or 5.0 V power pins		50	mV
$\lvert\Delta V_{18x}\rvert$	Variations between different 1.8 V power pins(3)		25	
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins		50	
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	see *: Absolute Maximum Ratings (Electrical Sensitivity) on page 51*	see *: Absolute Maximum Ratings (Electrical Sensitivity) on page 51*	
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)			

1. All 3.3 V or 5.0 V power (V_{DD_IO}, V_{DDA_ADC}, V_{DDA_PLL}) and ground (V_{SS_IO}, V_{SSA_ADC}, V_{DDA_ADC}) pins must always be connected to the external 3.3V or 5.0V supply. When powered by 3.3V, I/Os are not 5V tolerant.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
3. Only when using external 1.8 V power supply. All the power (V_{18}, V_{18REG}, V_{18BKP}) and ground (V_{SS18}, V_{SSBKP}) pins must always be connected to the external 1.8 V supply.

3.2.2 Current characteristics

Table 7. Current characteristics

Symbol	Ratings	Maximum value	Unit
I_{VDD_IO} (1)	Total current into V_{DD_IO} power lines (source) (2)	150	mA
I_{VSS_IO} (1)	Total current out of V_{SS} ground lines (sink) (2)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}$ (3) & (4)	Injected current on NRSTIN pin	± 5	
	Injected current on XT1 and XT2 pins	± 5	
	Injected current on any other pin (5)	± 5	
$\Sigma I_{INJ(PIN)}$ (3)	Total injected current (sum of all I/O and control pins) (5)	± 25	

1. The user can use GPIOs to source or sink high current (up to 20 mA for O8 type High Sink I/Os). In this case, the user must ensure that these absolute max. values are not exceeded (taking into account the RUN power consumption) and must follow the rules described in *Section 3.3.8: I/O port pin characteristics on page 53*.
2. All 3.3 V or 5.0 V power (V_{DD_IO}, V_{DDA_ADC}, V_{DDA_PLL}) and ground (V_{SS_IO}, V_{SSA_ADC}, V_{DDA_ADC}) pins must always be connected to the external 3.3V or 5.0V supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
4. Negative injection disturbs the analog performance of the device. See note in *Section 3.3.12: 10-bit ADC characteristics on page 64*.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

3.2.3 Thermal characteristics

Table 8. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (see Section 4.2: *Thermal characteristics on page 70*)		

3.3 Operating conditions

3.3.1 General operating conditions

Subject to general operating conditions for V_{DD_IO}, and T_A unless otherwise specified.

Table 9. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB Clock frequency	Accessing SRAM with 0 wait states	0	64	MHz
		Accessing Flash in burst mode, $T_A \leq 85°$ C	0	60	
		Accessing Flash in burst mode $T_A > 85°$ C		56	
		Accessing Flash with 0 wait states	0	32	
		Accessing Flash in RWW mode	0	16	
f_{PCLK}	Internal APB Clock frequency		0	32	MHz
V_{DD_IO}	Standard Operating Voltage Power Scheme 1 & 2		3.0	3.6	V
	Standard Operating Voltage Power Scheme 3 & 4		4.5	5.5	
V_{18}	Standard Operating Voltage Power Scheme 2 & 4		1.65	1.95	
T_A	Ambient temperature range	6 Suffix Version	-40	85	°C
		7 Suffix Version	-40	105	°C

3.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 10. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{VDD_IO}	V_{DD_IO} rise time rate		20			µs/V
					20	ms/V
t_{V18}	V_{18} rise time rate (1)	When 1.8 V power is supplied externally	20			µs/V
					20	ms/V

1. Data guaranteed by characterization, not tested in production.

3.3.3 Embedded voltage regulators

Subject to general operating conditions for V_{DD_IO}, and T_A

Table 11. Embedded voltage regulators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{MVREG}	MVREG power supply(1)	load <150 mA	1.65	1.80	1.95	V
V_{LPVREG}	LPVREG power supply(2)	load <10 mA	1.30	1.40	1.50	V
t_{VREG_PWRUP}(1)	Voltage Regulators start-up time (to reach 90% of final V_{18} value) at V_{DD_IO} power-up(3)	V_{DD_IO} rise slope = 20 µs/V		80		µs
		V_{DD_IO} rise slope = 20 ms/V		35		ms

1. V_{MVREG} is observed on the V_{18}, V_{18REG} and V_{18BKP} pins except in the following case:
   - In STOP mode with MVREG OFF (LP_PARAM13 bit). See note 2.
   - In STANDBY mo*de. See note 2.*
2. In STANDBY mode, V_{LPVREG} is observed on the V_{18BKP} pin
   In STOP mode, V_{LPVREG} is observed on the V_{18}, V_{18REG} and V_{18BKP} pins.
3. Once V_{DD_IO} has reached 3.0 V, the RSM (Regulator Startup Monitor) generates an internal RESET during this start-up time.

3.3.4 Supply current characteristics

The current consumption is measured as described in *Figure 12 on page 29* and *Figure 13 on page 29*.

Subject to general operating conditions for V_{DD_IO}, and T_A

Maximum power consumption

For the measurements in *Table 12* and *Table 13*, the MCU is placed under the following conditions:

- All I/O pins are configured in output push-pull 0
- All peripherals are disabled except if explicitly mentioned.
- Embedded Regulators are used to provide 1.8 V (except if explicitly mentioned).

Table 12. Maximum power consumption in RUN and WFI modes

Symbol	Parameter	Conditions (1)		Typ(2)	Max (3)	Unit
I_{DD}	Supply current in RUN mode	External Clock with PLL multiplication, code running from RAM, all peripherals enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz Single supply scheme see *Figure 12* / *Figure 14*	3.3V and 5V range	80	90	mA
	Supply current in WFI mode	External Clock, code running from RAM: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz Single supply scheme see *Figure 12*./ *Figure 14* Parameter setting BURST=1, WFI_FLASHEN=1	3.3V and 5V range	62	67	mA

1. The conditions for these consumption measurements are described at the beginning of *Section 3.3.4*.
2. Typical data are based on T_A=25°C, V_{DD_IO}=3.3V or 5.0V and V_{18}=1.8V unless otherwise specified.
3. Data based on product characterisation, tested in production at V_{DD_IO} max and V_{18} max (1.95V in dual supply mode or regulator output value in single supply mode) and T_A max.

Table 13. Maximum power consumption in STOP and STANDBY modes

Symbol	Parameter	Conditions[1]		Typ[2]	Max[3]			Unit
					T_A 25°C	T_A 85°C	T_A 105°C	
I_{DD}	Supply current in STOP mode	LP_PARAM bits: ALL OFF[4] Single supply scheme see *Figure 12*.	3.3V range	12	16	117	250	µA
		LP_PARAM bits: ALL OFF Dual supply scheme see *Figure 13*.	I_{DD_V18} I_{DD_V33}	5 <1	8 3	60 TBD	110 TBD	µA
		LP_PARAM bits: ALL OFF[4] Single supply scheme see *Figure 10*	5V range	15	22	160	310	µA
		LP_PARAM bits: ALL OFF Dual supply scheme see *Figure 11*	I_{DD_V18} I_{DD_V50}	5 3	8 5	60 TBD	110 TBD	µA
	Supply current in STANDBY mode	RTC OFF	3.3 V range	10	20	25	28	
			5V range	15	25	30	33	

1. The conditions for these consumption measurements are described at the beginning of *Section 3.3.4*.
2. Typical data are based on T_A=25°C, V_{DD_IO}=3.3V or 5.0V and V_{18}=1.8V unless otherwise specified.
3. Data based on product characterisation, tested in production at V_{DD_IO} max and V_{18} max (1.95V in dual supply mode or regulator output value in single supply mode).
4. In this mode, the whole digital circuitry is powered internally by the LPVREG at approximately 1.4V, which significantly reduces the leakage currents.

Figure 16. Power consumption in STOP mode in Single supply scheme (3.3 V range)

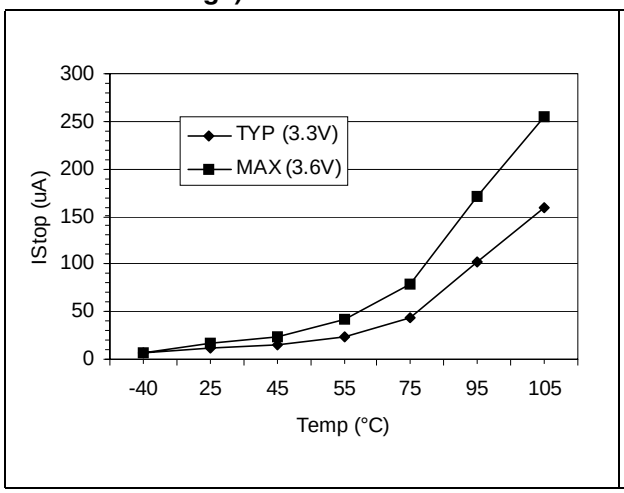


Figure 17. Power consumption in STOP mode Single supply scheme (5 V range)

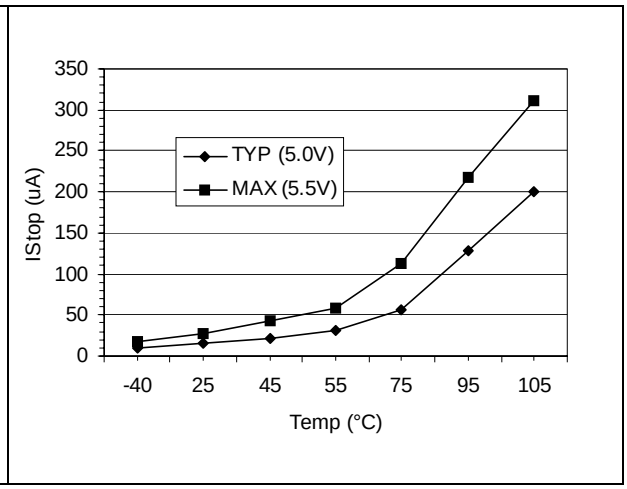


Figure 18. Power consumption in STANDBY mode (3.3 V range)

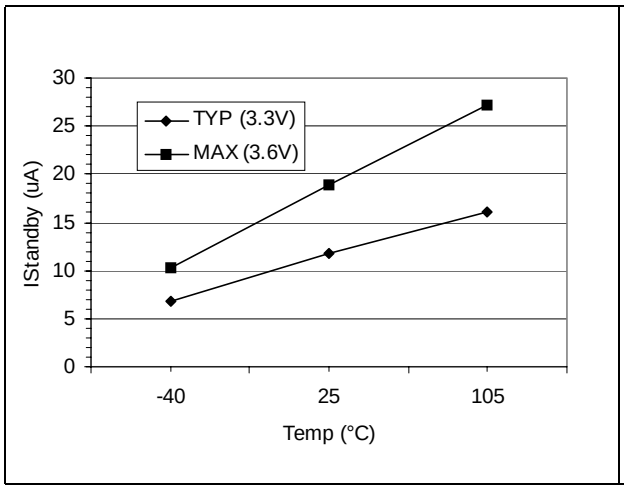
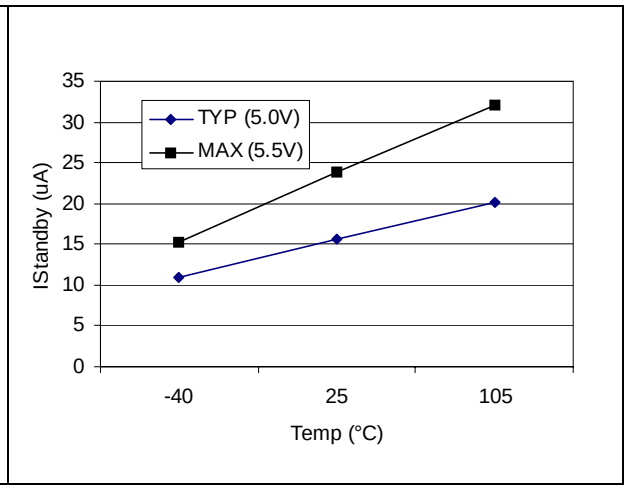


Figure 19. Power consumption in STANDBY mode (5 V range)



Typical power consumption

The following measurement conditions apply to *Table 14*, *Table 15* and *Table 16*.

In RUN mode:

- Program is executed from Flash (except if especially mentioned). The program consists of an infinite loop. When $f_{HCLK} > 32$ MHz, burst mode is activated.
- A standard 4 MHz crystal source is used.
- In all cases the PLL is used to multiply the frequency.
- All measurements are done in the single supply scheme with internal regulators used (see *Figure 12*)

In WFI Mode:

- In WFI Mode the measurement conditions are similar to RUN mode (OSC4M and PLL enabled). In addition, the Flash can be disabled depending on burst mode activation:
  - For AHB frequencies greater than 32 MHz, burst mode is activated and the Flash is kept enabled by setting the WFI_FLASH_EN bit (this bit cannot be reset when burst mode is activated).
  - For AHB frequencies less than or equal to 32 MHz, burst mode is deactivated, WFI_FLASH_EN is reset and the LP_PARAM14 bit is set (Flash is disabled in WFI mode).

In SLOW mode:

- The same program as in RUN mode is executed from Flash. The CPU is clocked by the FREEOSC, OSC4M, LPOSC or OSC32K. Only EXTIT peripheral is enabled in the MRCC_PCLKEN register.

In SLOW-WFI mode:

- In SLOW-WFI, the measurement conditions are similar to SLOW mode (CPU clocked by a low frequency clock). In addition, the LP_PARAM14 bit is set (FLASH is OFF). The WFI routine itself is executed from SRAM (it is not allowed to execute a WFI from the internal FLASH)

In STOP mode:

- Several measurements are given: in the single supply scheme with internal regulators used (see *Figure 12*): and in the dual supply scheme (see *Figure 13*).

In STANDBY mode:

- Three measurements are given:
  - The RTC is disabled, only the consumption of the LPVREG and RSM remain (almost no leakage currents)
  - The RTC is running, clocked by a standard 32.768 kHz crystal.
  - The RTC is running, clocked by the internal Low Power RC oscillator (LPOSC)
- STANDBY mode is only supported in the single supply scheme (see *Figure 12*)

Subject to general operating conditions for V_{DD_IO}, and T_A

Table 14. Single supply typical power consumption in Run, WFI, Slow and Slow-WFI modes

Symbol	Para meter	Conditions	3.3V typ(1)	5V typ(2)	Unit
I_{DD} (3)	Supply current in RUN mode(4)	Clocked by OSC4M with PLL multiplication, all peripherals enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz f_{HCLK}=56 MHz, f_{PCLK}=28 MHz f_{HCLK}=48 MHz, f_{PCLK}=24 MHz f_{HCLK}=32 MHz, f_{PCLK}=32 MHz f_{HCLK}=16 MHz, f_{PCLK}=16 MHz f_{HCLK}=8 MHz, f_{PCLK}=8 MHz	 80 75 65 59 34 20	 82 77 67 61 37 22	mA
		Clocked by OSC4M with PLL multiplication, only EXTIT peripheral enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz f_{HCLK}=56 MHz, f_{PCLK}=28 MHz f_{HCLK}=48 MHz, f_{PCLK}=24 MHz f_{HCLK}=32 MHz, f_{PCLK}=32 MHz f_{HCLK}=16 MHz, f_{PCLK}=16 MHz f_{HCLK}=8 MHz, f_{PCLK}=8 MHz	 65 60 54 42 22 16	 67 62 55 44 24 18	mA
	Supply current in WFI mode(4)	Clocked by OSC4M with PLL multiplication, only EXTIT peripheral enabled in the MRCC_PLCKEN register: f_{HCLK}=60 MHz, f_{PCLK}=30 MHz(5) f_{HCLK}=56 MHz, f_{PCLK}=28 MHz(5) f_{HCLK}=48 MHz, f_{PCLK}=24 MHz(5) f_{HCLK}=32 MHz, f_{PCLK}=32 MHz(6) f_{HCLK}=16 MHz, f_{PCLK}= 16 MHz (6) f_{HCLK}= 8 MHz, f_{PCLK}= 8 MHz(6)	 62 59 53 22 13 10	 63 60 54 23 15 11	mA
	Supply current in SLOW mode(4) (7)	Clocked by FREEOSC: f_{HCLK}=f_{PCLK}=~5 MHz, Clocked by OSC4M: f_{HCLK}=f_{PCLK}=4 MHz Clocked by LPOSC: f_{HCLK}=f_{PCLK}=~300 kHz Clocked by OSC32K: f_{HCLK}=f_{PCLK}=32.768 kHz	9 8 3.65 3.5	10 9 3.9 4.2	mA
	Supply current in SLOW-WFI mode(4) (7)	Clocked by FREEOSC: f_{HCLK}=f_{PCLK}=~5 MHz Clocked by OSC4M: f_{HCLK}=f_{PCLK}=4 MHz Clocked by LPOSC: f_{HCLK}=f_{PCLK}=~300 kHz Clocked by OSC32K: f_{HCLK}=f_{PCLK}=32.768 kHz	3.5 3.1 1.15 0.98	4.0 3.75 1.65 1.5	mA

1. Typical data based on T_A=25° C and V_{DD_IO}=3.3V.
2. Typical data based on T_A=25° C and V_{DD_IO}=5.0V.
3. The conditions for these consumption measurements are described at the beginning of *Section 3.3.4 on page 35*.
4. Single supply scheme see *Figure 14*.
5. Parameter setting BURST=1, WFI_FLASHEN=1
6. Parameter setting BURST=0, WFI_FLASHEN=0
7. Parameter setting WFI_FLASHEN=0, OSC4MOFF=1

Table 15. Dual supply supply typical power consumption in Run, WFI, Slow and Slow-WFI modes

To calculate the power consumption in Dual supply mode, refer to the values given in *Table 14*. and consider that this consumption is split as follows:

$I_{DD(single\ supply)} \sim I_{DD(dual\ supply)} = I_{DD\_V18} + I_{DD(VDD\_IO)}$

For 3.3V range: $I_{DD(VDD\_IO)}$ ~ 1 to 2 mA
For 5V range: $I_{DD(VDD\_IO)}$ ~ 2 to 3 mA
Therefore most of the consumption is sunk on the V_{18} power supply
This formula does not apply in STOP and STANDBY modes, refer to *Table 16*.

Subject to general operating conditions for V_{DD_IO}, and T_A

Table 16. Typical power consumption in STOP and STANDBY modes

Symbol	Parameter	Conditions		3.3V Typ(1)	5V Typ(2)	Unit
I_{DD}(3)	Supply current in STOP mode(4)	LP_PARAM bits: ALL OFF(5)		12	15	µA
		LP_PARAM bits : MVREG ON, OSC4M OFF, FLASH OFF(6)		130	135	
		LP_PARAM bits: MVREG ON, OSC4M ON , FLASH OFF(6)		1950	1930	
		LP_PARAM bits: MVREG ON, OSC4M OFF, FLASH ON (6)		630	635	
		LP_PARAM bits: MVREG ON, OSC4M ON, FLASH ON (6)		2435	2425	
	Supply current in STOP mode(7)	LPPARAM bits: ALL OFF, with V_{18}=1.8 V	I_{DD_V18} I_{DD_V33}	5 <1	5 <1	µA
		LP_PARAM bits: OSC4M ON, FLASH OFF	I_{DD_V18} I_{DD_V33}	410 1475	410 1435	
		LP_PARAM bits: OSC4M OFF, FLASH ON	I_{DD_V18} I_{DD_V33}	550 <1	550 1	
		LP_PARAM bits: OSC4M ON, FLASH ON	I_{DD_V18} I_{DD_V33}	910 1475	910 1445	
	Supply current in STANDBY mode(4)	RTC OFF		11	14	µA
		RTC ON clocked by OSC32K		14	18	

1. Typical data are based on T_A=25°C, V_{DD_IO}=3.3 V and V_{18}=1.8 V unless otherwise indicated in the table.
2. Typical data are based on T_A=25°C, V_{DD_IO}=5.0 V and V_{18}=1.8 V unless otherwise indicated in the table.
3. The conditions for these consumption measurements are described at the beginning of *Section 3.3.4 on page 35*.
4. Single supply scheme see *Figure 12*.
5. In this mode, the whole digital circuitry is powered internally by the LPVREG at approximately 1.4 V, which significantly reduces the leakage currents.
6. In this mode, the whole digital circuitry is powered internally by the MVREG at 1.8 V.
7. Dual supply scheme see *Figure 13*.

Supply and Clock manager power consumption

Table 17. Supply and Clock manager power consumption

Symbol	Parameter	Conditions[1]	3.3V Typ	5V Typ	Unit
$I_{DD(OSC4M)}$	Supply current of resonator oscillator in STOP or WFI mode (LP_PARAM bit: OSC4M ON)	External components specified in*: 4/8 MHz Crystal / Ceramic Resonator Oscillator (XT1/XT2) on page 45*	1815	1795	µA
$I_{DD(FLASH)}$	FLASH static current consumption in STOP or WFI mode (LP_PARAM bit FLASH ON)		515	515	
$I_{DD(MVREG)}$	Main Voltage Regulator static current consumption in STOP mode (LP_PARAM bit: MVREG ON)		130	135	
$I_{DD(LPVREG)}$	Low Power Voltage Regulator + RSM current static current consumption	STOP mode includes leakage where V_{18} is internally set to 1.4 V	12	15	
		STANDBY mode where V_{18BKP} and V_{18} are internally set to 1.4 V and 0 V respectively	11	14	

1. Measurements performed in 3.3V single supply mode see *Figure 12*

On-Chip peripheral power consumption

Conditions:

- V_{DD_IO}=V_{DDA_ADC}=V_{DDA_PLL}=3.3 V or 5 V ±10% unless otherwise specified.
- T_A= 25° C
- Clocked by OSC4M with PLL multiplication, f_{CK_SYS}=64 MHz, f_{HCLK}=32 MHz, f_{PCLK}=32 MHz

Table 18. On-Chip peripherals

Symbol	Parameter	Typ (3.3V and 5.0V)	Unit
$I_{DD(TIM)}$	TIM Timer supply current (1)	0.7	mA
$I_{DD(PWM)}$	PWM Timer supply current(2)	1	
$I_{DD(SSP)}$	SSP supply current (3)	1.3	
$I_{DD(UART)}$	UART supply current (4)	1.6	
$I_{DD(I2C)}$	I2C supply current (5)	0.3	
$I_{DD(ADC)}$	ADC supply current when converting (6)	1.2	
$I_{DD(USB)}$	USB supply current (7) **Note:** V_{DD_IO} must be 3.3 V ±10%	0.90	
$I_{DD(CAN)}$	CAN supply current (8)	2.8	

1. Data based on a differential I_{DD} measurement between reset configuration and timer counter running at 32 MHz. No IC/OC programmed (no I/O pads toggling)
2. Data based on a differential I_{DD} measurement between reset configuration and PWM running at 32 MHz. This measurement does not include PWM pads toggling consumption.
3. Data based on a differential I_{DD} measurement between reset configuration and permanent SPI master communication at maximum speed 16 MHz. The data sent is 55h. This measurement does not include the pad toggling consumption.
4. Data based on a differential I_{DD} measurement between reset configuration and a permanent UART data transmit sequence at 1Mbauds. This measurement does not include the pad toggling consumption.
5. Data based on a differential I_{DD} measurement between reset configuration (I2C disabled) and a permanent I2C master communication at 100kHz (data sent equal to 55h). This measurement includes the pad toggling consumption but not the external 10kOhm external pull-up on clock and data lines.
6. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions at 8 MHz in scan mode on 16 inputs configured as AIN.
7. Data based on a differential I_{DD} measurement between reset configuration and a running generic HID application.
8. Data based on a differential IDD measurement between reset configuration (CAN disabled) and a permanent CAN data transmit sequence in loopback mode at 1MHz. This measurement does not include the pad toggling consumption.

3.3.5 Clock and timing characteristics

XT1 external Clock source

Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 19. XT1 external Clock source

Symbol	Parameter	Conditions(1) (2)	Min	Typ	Max	Unit
f_{XT1}	External clock source frequency	see *Figure 20*		4	60	MHz
V_{XT1H}	XT1 input pin high level voltage		$0.7xV_{DD\_IO}$		V_{DD_IO}	V
V_{XT1L}	XT1 input pin low level voltage		V_{SS}		$0.3xV_{DD\_IO}$	
$t_{w(XT1H)}$ $t_{w(XT1L)}$	XT1 high or low time (3)		6			ns
$t_{r(XT1)}$ $t_{f(XT1)}$	XT1 rise or fall time (3)				5	
I_L	XTx Input leakage current	$V_{SS} \le V_{IN} \le V_{DD\_IO}$			±1	µA

1. Data based on typical application software.
2. Time measured between interrupt event and interrupt vector fetch. $\Delta t_{c(INST)}$ is the number of t_{CPU} cycles needed to finish the current instruction execution.
3. Data based on design simulation and/or technology characteristics, not tested in production.

XRTC1 external Clock source

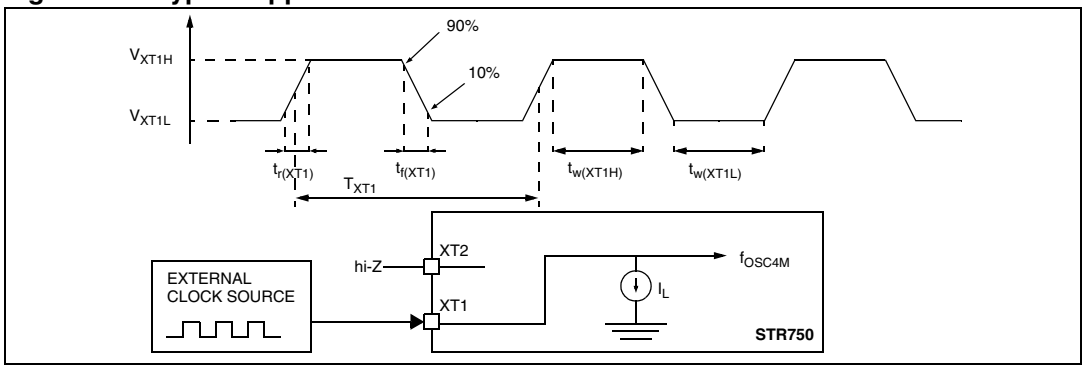
Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 20. XRTC1 external Clock source

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
f_{XRTC1}	External clock source frequency	see *Figure 20*		32.768	500	kHz
V_{XRTC1H}	XRTC1 input pin high level voltage		$0.7xV_{DD\_IO}$		V_{DD_IO}	V
V_{XRTC1L}	XRTC1 input pin low level voltage		V_{SS}		$0.3xV_{DD\_IO}$	
$t_{w(XRTC1H)}$ $t_{w(XRTC1L)}$	XRTC1 high or low time(2)		990			ns
$t_{r(XRTC1)}$ $t_{f(XRTC1)}$	XRTC1 rise or fall time(2)				5	
I_L	XRTCx Input leakage current	$V_{SS} \le V_{IN} \le V_{DD\_IO}$			±1	µA

1. Data based on typical application software.
2. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 20. Typical application with an external Clock source



4/8 MHz Crystal / Ceramic Resonator Oscillator (XT1/XT2)

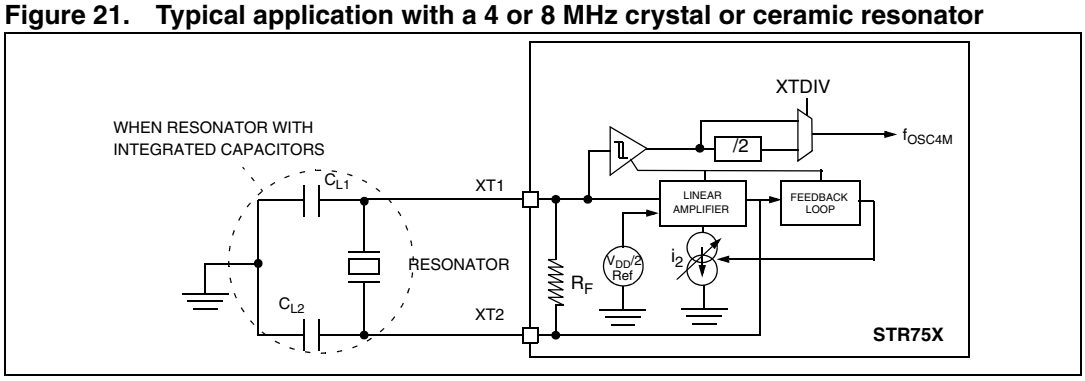
The STR750 system clock or the input of the PLL can be supplied by a OSC4M which is a 4 MHz clock generated from a 4 MHz or 8 MHz crystal or ceramic resonator. If using an 8 MHz oscillator, software set the XTDIV bit to enable a divider by 2 and generate a 4 MHz OSC4M clock. All the information given in this paragraph are based on product characterisation with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal/ceramic resonator manufacturer for more details (frequency, package, accuracy...).

Table 21. 4/8 MHz crystal / ceramic resonator oscillator (XT1/XT2)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC4M}	Oscillator frequency	4 MHz Crystal/Resonator Oscillator connected on XT1/XT2 XTDIV=0 or 8 MHz Crystal/Resonator Oscillator connected on XT1/XT2 XTDIV=1		4		MHz
R_F	Feedback resistor		200	240	270	kΩ
C_{L1}(2) C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal or ceramic resonator (R_S)(3)	R_S=200Ω			60	pF
i_2	XT2 driving current	V_{DD_IO}=3.3 V or 5.0 V		425		µA
$t_{SU(OSC4M)}$(4)	Startup time at V_{DD_IO} power-up			1		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5-pF to 25-pF range (typ.) designed for high-frequency applications and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included when sizing C_{L1} and C_{L2} (10 pF can be used as a rough estimate of the combined pin and board capacitance).
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(OSC4M)}$ is the typical start-up time measured from the moment V_{DD_IO} is powered (with a quick V_{DD_IO} ramp-up from 0 to 3.3V (<50µs) to a stabilized 4MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal/ceramic resonator manufacturer.

Figure 21. Typical application with a 4 or 8 MHz crystal or ceramic resonator



OSC32K crystal / ceramic resonator oscillator

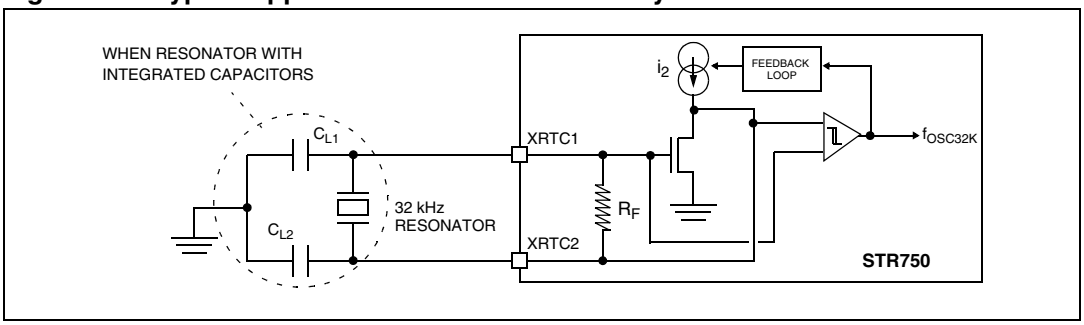
The STR7 RTC clock can be supplied with a 32.768 kHz Crystal/Ceramic resonator oscillator. All the information given in this paragraph are based on product characterisation with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal/ceramic resonator manufacturer for more details (frequency, package, accuracy...).

Table 22. OSC32K crystal / ceramic resonator oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC32K}	Oscillator Frequency			32.768		kHz
R_F	Feedback resistor	V_{DD_IO}=3.3 V	270	310	370	kΩ
		V_{DD_IO}=5.0 V	TBD	TBD	TBD	
C_{L1} C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal or ceramic resonator (R_S)(1)	R_S=TBD	TBD		TBD	pF
i_2	XT2 driving current	V_{DD_IO}=3.3 V or 5.0 V V_{IN}=V_{SS}	160		250	µA
$t_{SU(OSC32K)}$(2)	startup time	V_{DD_IO} is stabilized		2.5		s

1. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value. Refer to crystal/ceramic resonator manufacturer for more details
2. $t_{SU(OSC32K)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 32 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal/ceramic resonator manufacturer

Figure 22. Typical application with a 32.768 kHz crystal or ceramic resonator



PLL Characteristics

PLL Jitter Terminology

- Self-referred single period jitter (period jitter)

  Period Jitter is defined as the difference of the maximum period (T_{max}) and minimum period (T_{min}) at the output of the PLL where T_{max} is the maximum time difference between 2 consecutive clock rising edges and T_{min} is the minimum time difference between 2 consecutive clock rising edges.

  See *Figure 23*

- Self-referred long term jitter (N period jitter)

  Self-referred long term Jitter is defined as the difference of the maximum period (T_{max}) and minimum period (T_{min}) at the output of the PLL where T_{max} is the maximum time

difference between N+1 consecutive clock rising edges and T_{min} is the minimum time difference between N+1 consecutive clock rising edges.

N should be kept sufficiently large to have a long term jitter (ex: thousands).

For N=1, this becomes the single period jitter.

See *Figure 23*

- Cycle-to-cycle jitter (N period jitter)

  This corresponds to the time variation between adjacent cycles over a random sample of adjacent clock cycles pairs. Jitter(cycle-to-cycle) = Max(Tcycle n- Tcycle n-1) for n=1 to N.

  See *Figure 24*

Figure 23. Self-referred jitter (single and long term)

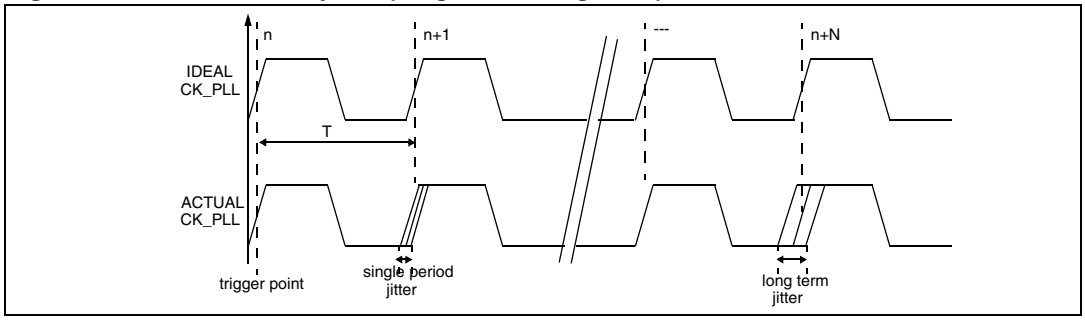
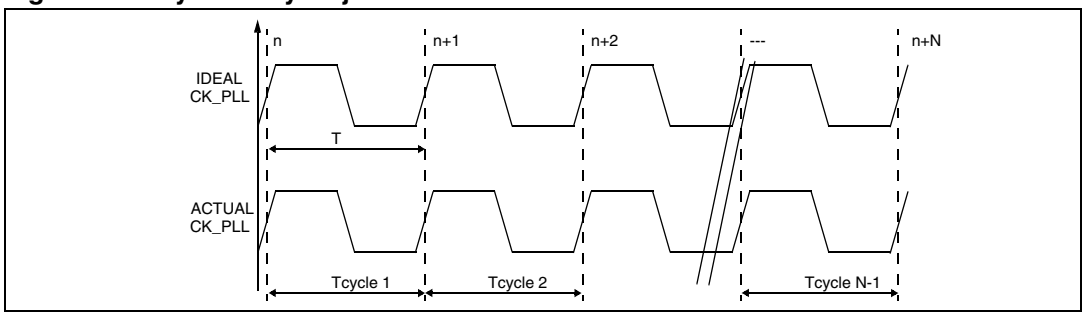


Figure 24. Cycle-to-cycle jitter



PLL characteristics

Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 23. PLL characteristics

Symbol	Parameter	Test Conditions	Value			Unit
			Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock			4.0		MHz
	PLL input clock duty cycle		40		60	%
f_{PLL_OUT}	PLL multiplier output clock	f_{PLL_IN}x 24			165	MHz
f_{VCO}	VCO frequency range	When PLL operates (locked)	336		960	MHz
t_{LOCK}	PLL lock time				300	µs
$\Delta t_{JITTER1}$(2)(3)	Single period jitter (+/-3Σ peak to peak)	f_{PLL_IN} = 4 MHz(4) V_{DD_IO} is stable			+/-250	ps
$\Delta t_{JITTER2}$(2)(3)	Long term jitter (+/-3Σ peak to peak)	f_{PLL_IN} = 4 MHz(4) V_{DD_IO} is stable			+/-2.5	ns
$\Delta t_{JITTER3}$(2)(3)	Cycle to cycle jitter (+/-3Σ peak to peak)	f_{PLL_IN} = 4 MHz(4) V_{DD_IO} is stable			+/-500	ps

1. Data based on product characterisation, not tested in production.
2. Refer to jitter terminology in *: PLL Characteristics on page 46* for details on how jitter is specified.
3. The jitter specification holds true only up to 50mV (peak-to-peak) noise on V_{DDA_PLL} and V_{18} supplies. Jitter will increase if the noise is more than 50mV. In addition, it assumes that the input clock has no jitter.
4. The PLL parameters (MX1, MX0, PRESC1, PRESC2) must respect the constraints described in*: PLL Characteristics on page 46*.

Internal RC Oscillators (FREEOSC & LPOSC)

Subject to general operating conditions for V_{DD_IO}, and T_A.

Table 24. Internal RC Oscillators (FREEOSC & LPOSC)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{CK\_FREEOSC}$	FREEOSC Oscillator Frequency		3	5	8	MHz
f_{CK_LPOSC}	LPOSC Oscillator Frequency		150	300	500	kHz

3.3.6 Memory characteristics

Flash memory

Subject to general operating conditions for V_{DD_IO} and V_{18}, T_A = -40 to 105 °C unless otherwise specified.

Table 25. Flash memory characteristics

Symbol	Parameter	Test Conditions	Value		Unit
			Typ	Max(1)	
t_{PW}	Word Program		35		µs
t_{PDW}	Double Word Program		60		µs
t_{PB0}	Bank 0 Program (256K)	Single Word programming of a checker-board pattern	2	4.9(2)	s
t_{PB1}	Bank 1 Program (16K)	Single Word programming of a checker-board pattern	125	224(2)	ms
t_{ES}	Sector Erase (64K)	Not preprogrammed (all 1) Preprogrammed (all 0)	1.54 1.176	2.94(2) 2.38(2)	s
t_{ES}	Sector Erase (8K)	Not preprogrammed (all 1) Preprogrammed (all 0)	392 343	560(2) 532(2)	ms
t_{ES}	Bank 0 Erase (256K)	Not preprogrammed (all 1) Preprogrammed (all 0)	8.0 6.6	13.7 11.2	s
t_{ES}	Bank 1 Erase (16K)	Not preprogrammed (all 1) Preprogrammed (all 0)	0.9 0.8	1.5 1.3	s
t_{RPD}	Recovery when disabled			20	µs
t_{PSL}	Program Suspend Latency			10	µs
t_{ESL}	Erase Suspend Latency			300	µs

1. Data based on characterisation not tested in production
2. 10K program/erase cycles.

Table 26. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END_B0}	Endurance (Bank 0 sectors)		10			kcycles
N_{END_B1}	Endurance (Bank 1 sectors)		100			kcycles
Y_{RET}	Data Retention	T_A=85° C	20			Years
t_{ESR}	Erase Suspend Rate	Min time from Erase Resume to next Erase Suspend	20			ms

1. Data based on characterisation not tested in production.

3.3.7 EMC characteristics

Susceptibilitytests are performed on a sample basis during product characterization.

Functional EMS (Electro Magnetic Susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behaviour is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 27. EMC characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, f_{CK_SYS}=32 MHz conforms to IEC 1000-4-2	Class A
V_{EFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, f_{CK_SYS}=32 MHz conforms to IEC 1000-4-4	Class A

Electro Magnetic Interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 28. EMI characteristics

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f_{OSC4M}/f_{HCLK}]		Unit
				4/32MHz	4/60MHz	
S_{EMI}	Peak level	Flash devices: V_{DD_IO}=3.3 V or 5 V, T_A=+25° C, LQFP64 package conforming to SAE J 1752/3	0.1 MHz to 30 MHz	22	26	dBµV
			30 MHz to 130 MHz	31	26	
			130 MHz to 1 GHz	19	23	
			SAE EMI Level	>4	>4	-

Absolute Maximum Ratings (Electrical Sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electro-Static Discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard.

Table 29. Absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25° C	2000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)		200	
$V_{ESD(CDM)}$	Electro-static discharge voltage (Charge Device Model)		750	

1. Data based on product characterisation, not tested in production.

Static and dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Table 30. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A=+25° C T_A=+85° C T_A=+105° C	Class A
DLU	Dynamic latch-up class	V_{DD}= 5.5 V, f_{OSC4M}=4 MHz, f_{CK_SYS}=32 MHz, T_A=+25° C	Class A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

3.3.8 I/O port pin characteristics

General characteristics

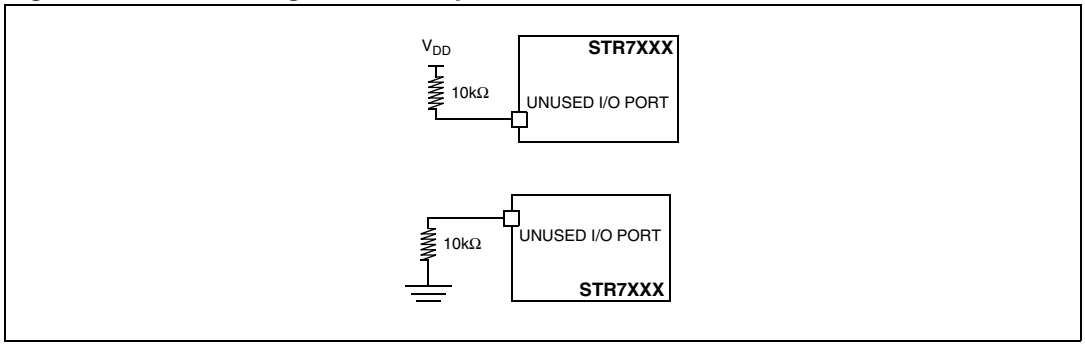
Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

Table 31. General characteristics

I/O static characteristics							
Symbol	**Parameter**	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
V_{IL}	Input low level voltage	TTL ports				0.8	V
V_{IH}	Input high level voltage			2			
V_{hys}	Schmitt trigger voltage hysteresis(1)				400		mV
$I_{INJ(PIN)}$	Injected Current on any I/O pin					± 4	mA
$\Sigma I_{INJ(PIN}$ (2)	Total injected current (sum of all I/O and control pins)					± 25	
I_{lkg}	Input leakage current on robust pins	See *Section 3.3.12 on page 64*					
	Input leakage current(3)	$V_{SS} \le V_{IN} \le V_{DD\_IO}$				±1	µA
I_S	Static current consumption(4)	Floating input mode			200		
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN}=V_{SS}$	V_{DD_IO}=3.3 V	50	95	200	kΩ
			V_{DD_IO}=5 V	20	58	150	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN}=V_{DD\_IO}$	V_{DD_IO}=3.3 V	30	80	180	kΩ
			V_{DD_IO}=5 V	20	50	120	kΩ
C_{IO}	I/O pin capacitance				5		pF
$t_{w(IT)in}$	External interrupt/wake-up lines pulse time(6)			2			T_{APB}

1. Hysteresis voltage between Schmitt trigger switching levels.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{DD\_IO}$ while a negative injection is induced by $V_{IN}<V_{SS}$. Refer to *Section 3.2 on page 31* for more details.
3. Leakage could be higher than max. if negative current is injected on adjacent pins.
4. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor (see *Figure 25*). Data based on design simulation and/or technology characteristics, not tested in production.
5. The R_{PU} pull-up and R_{PD} pull-down equivalent resistor are based on a resistive transistor.
6. To generate an external interrupt, a minimum pulse width has to be applied on an I/O port pin configured as an external interrupt source.

Figure 25. Connecting unused I/O pins



Output driving current

The GP I/Os have different drive capabilities:

- O2 outputs can sink or source up to +/-2 mA.
- O4 outputs can sink or source up to +/-4 mA.
- outputs can sink or source up to +/-8 mA or can sink +20 mA (with a relaxed V_{OL}).

In the application, the user must limit the number of I/O pins which can drive current to respect the absolute maximum rating specified in *Section 3.2.2* :

- The sum of the current sourced by all the I/Os on $V_{DD\_IO,}$ plus the maximum RUN consumption of the MCU sourced on $V_{DD\_IO,}$ can not exceed the absolute maximum rating IV_{DD_IO}.
- The sum of the current sunk by all the I/Os on V_{SS_IO} plus the maximum RUN consumption of the MCU sunk on V_{SS_IO} can not exceed the absolute maximum rating IV_{SS_IO}.

Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

Table 32. Output driving current

I/O Output Drive characteristics for V_{DD_IO} = 3.0 to 3.6 V and EN33 bit =1 or V_{DD_IO} = 4.5 to 5.5 V and EN33 bit =0						
I/O Type	**Symbol**	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
O2	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+2 mA		0.4	V
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-2 mA	V_{DD_IO}-0.8		
O4	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+4 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-4 mA	V_{DD_IO}-0.8		
O8	V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time	I_{IO}=+8 mA		0.4	
		Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time	I_{IO}=+20 mA, T_A≤85°C T_A≥85°C		1.3 1.5	
			I_{IO}=+8 mA		0.4	
	V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time	I_{IO}=-8 mA	V_{DD_IO}-0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 3.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS_IO}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Section 3.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD_IO}.

Output speed

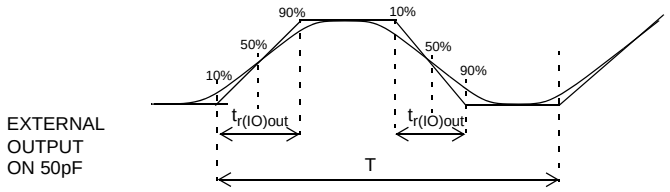
Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

Table 33. Output speed

I/O dynamic characteristics for V_{DD_IO} = 3.0 to 3.6V and EN33 bit =1 or V_{DD_IO} = 4.5 to 5.5V and EN33 bit =0							
I/O Type	**Symbol**	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
O2	$F_{max(IO)out}$	Maximum Frequency(1)	C_L=50 pF			10	MHz
	$t_{f(IO)out}$	Output high to low level fall time(2)	C_L=50 pF Between 10% and 90%			30	ns
	$t_{r(IO)out}$	Output low to high level rise time(2)				30	
O4	$F_{max(IO)out}$	Maximum Frequency(1)	C_L=50 pF			25	MHz
	$t_{f(IO)out}$	Output high to low level fall time(2)	C_L=50 pF Between 10% and 90%			12	ns
	$t_{r(IO)out}$	Output low to high level rise time(2)				12	
O8	$F_{max(IO)out}$	Maximum Frequency(1)	C_L=50pF			40	MHz
	$t_{f(IO)out}$	Output high to low level fall time(2)	C_L=50 pF Between 10% and 90%			6	ns
	$t_{r(IO)out}$	Output low to high level rise time(2)				6	

1. The maximum frequency is defined as described in *Figure 26*.
2. Data based on product characterisation, not tested in production.

Figure 26. I/O output speed definition



Maximum frequency is achieved if $(t_r + t_f) \leq (2/3)T$ and if the duty cycle is (45-55%) when loaded by 50pF

NRSTIN and NRSTOUT pins

NRSTIN Pin Input Driver is TTL/LVTTL as for all GP I/Os. A permanent pull-up is present which is the same as R_{PU} (see : General characteristics on page 53)

NRSTOUT Pin Output Driver is equivalent to the O2 type driver except that it works only as an open-drain (the P-MOS is de-activated). A permanent pull-up is present which is the same as R_{PU} (see : General characteristics on page 53)

Subject to general operating conditions for V_{DD_IO} and T_A unless otherwise specified.

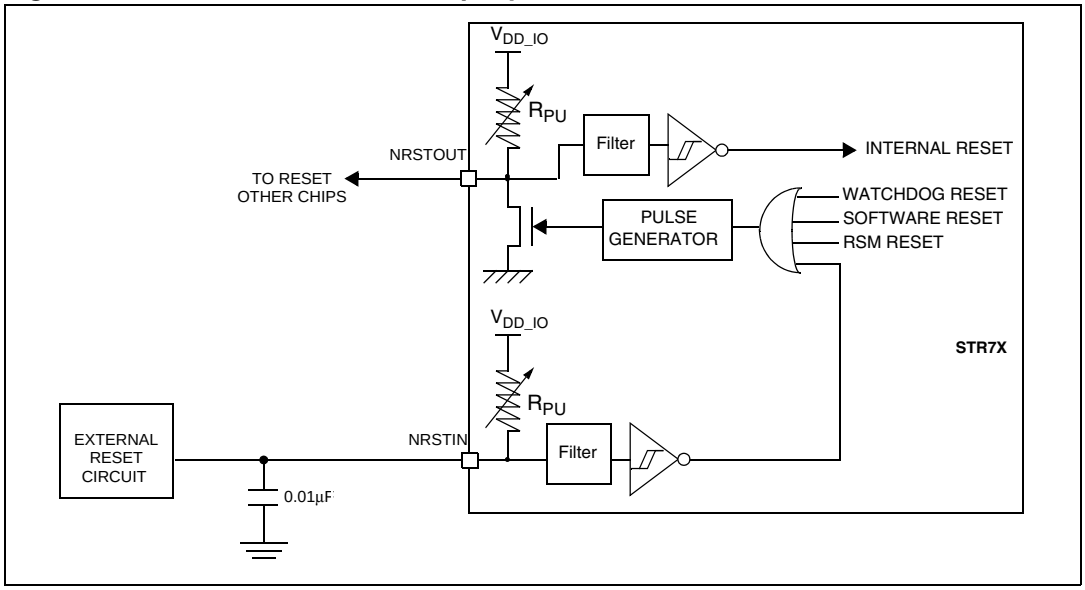
Table 34. NRSTIN and NRSTOUT pins

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
$V_{IL(NRSTIN)}$	NRSTIN Input low level voltage(1)					0.8	V
$V_{IH(NRSTIN)}$	NRSTIN Input high level voltage(1)			2			
$V_{hys(NRSTIN)}$	NRSTIN Schmitt trigger voltage hysteresis(2)				400		mV
$V_{OL(NRSTIN)}$	NRSTOUT Output low level voltage(3)	I_{IO}=+2 mA				0.4	V
$R_{PU(NRSTIN)}$	NRSTIN Weak pull-up equivalent resistor(4)	V_{IN}=V_{SS}	V_{DD_IO}=3.3 V	25	50	100	kΩ
			V_{DD_IO}=5 V	20	31	100	kΩ
$t_{w(RSTL)out}$	Generated reset pulse duration (visible at NRSTOUT pin)(5)	Internal reset source		15	20		µs
$t_{h(RSTL)in}$	External reset pulse hold time at NRSTIN pin(6)	At V_{DD_IO} power-up(5)		20			µs
		When V_{DD_IO} is established(5)		1			µs
$t_{g(RSTL)in}$	maximum negative spike duration filtered at NRSTIN pin(7)	The time between two spikes must be higher than 1/2 of the spike duration.			150		ns

1. Data based on product characterisation, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels.
3. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 3.2.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
4. The R_{PU} pull-up equivalent resistor are based on a resistive transistor
5. To guarantee the reset of the device, a minimum pulse of 15 µs has to be applied to the internal reset. At V_{DD_IO} power-up, the built-in reset stretcher may not generate the 15 µs pulse duration while once V_{DD_IO} is established, an external reset pulse will be internally stretched up to 15 µs thanks to the reset pulse stretcher.
6. The reset network (the resistor and two capacitors) protects the device against parasitic resets, especially in noisy environments.
7. In fact the filter is made to ignore all incoming pulses with short duration:
   - all negative spikes with a duration less than 150 ns are filtered
   - all trains of negative spikes with a ratio of 1/2 are filtered. This means that all spikes with a maximum duration of 150 ns with minimum interval between spikes of 75 ns are filtered.

   Data guaranteed by design, not tested in production.

Figure 27. Recommended NRSTIN pin protection



1. The user must ensure that the level on the NRSTIN pin can go below the $V_{IL(NRSTIN)}$ max. level specified in *NRSTIN and NRSTOUT pins on page 57*. Otherwise the reset will not be taken into account internally.

3.3.9 TB and TIM timer characteristics

Subject to general operating conditions for V_{DD_IO}, f_{CK_SYS}, and T_A unless otherwise specified.

Refer to *Section 3.3.8: I/O port pin characteristics on page 53* for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

Table 35. TB and TIM timers

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time	TIM0,1,2		2			t_{CK_TIM}
$t_{res(TIM)}$	Timer resolution time(1)	TB	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	1			t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	16.6(1)			ns
		TIM0,1,2	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	1			t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60MHz	16.6(1)			ns
f_{EXT}	Timer external clock frequency on TI1 or TI2	TIM0,1,2	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	0		$f_{CK\_TIM}/4$	MHz
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0		15	MHz
Res_{TIM}	Timer resolution					16	bit
$t_{COUNTER}$	16-bit Counter clock period when internal clock is selected (16-bit Prescaler)	TB		1		65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0.0166		1092	µs
		TIM0,1,2		1		65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	0.0166		1092	µs
t_{MAX_COUNT}	Maximum Possible Count	TB				65536x65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz			71.58	s
		TIM0,1,2				65536x65536	t_{CK_TIM}
			$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz			71.58	s

1. Take into account the frequency limitation due to the I/O speed capability when outputting the PWM to I/O pin, described in *: Output speed on page 56*.

Table 36. PWM Timer (PWM)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(PWM)}$	PWM resolution time	$f_{CK\_TIM(MAX)} = f_{CK\_SYS}$	1			t_{CK_TIM}
		$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz	16.6(1)			ns
Res_{PWM}	PWM resolution				16	bit
V_{OS}(1)	PWM/DAC output step voltage	V_{DD_IO}=3.3 V, Res=16-bits		50(1)		µV
		V_{DD_IO}=5.0 V, Res=16-bits		76(1)		µV
$t_{COUNTER}$	Timer clock period when internal clock is selected		1		65536	t_{CK_TIM}
		f_{CK_TIM}=60 MHz	0.0166		1087	µs
t_{MAX_COUNT}	Maximum Possible Count				65536x 65536	t_{CK_TIM}
		$f_{CK\_TIM} = f_{CK\_SYS}$ = 60 MHz			71.58	s

1. Take into account the frequency limitation due to the I/O speed capability when outputting the PWM to an I/O pin, as described in *: Output speed on page 56*.

3.3.10 Communication interface characteristics

I²C - Inter IC control interface

Subject to general operating conditions for V_{DD_IO}, f_{PCLK}, and T_A unless otherwise specified.

The ST7 I²C interface meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Restriction: The I/O pins which SDA and SCL are mapped to are not “True” Open-Drain: when configured as open-drain, the PMOS connected between the I/O pin and V_{DD_IO} is disabled, but it is still present. Also, there is a protection diode between the I/O pin and V_{DD_IO}. Consequently, when using this I²C in a multi-master network, it is not possible to power off the STR7x while some another I²C master node remains powered on: otherwise, the STR7x will be powered by the protection diode.

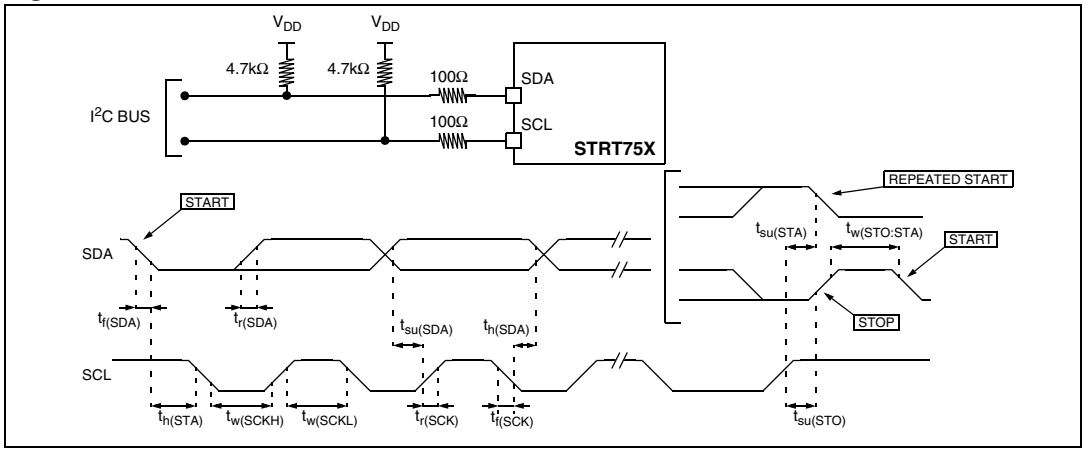
Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 37. SDA and SCL characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20+0.1C_b	300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. f_{PCLK}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz).
2. Data based on standard I²C protocol requirement, not tested in production.
3. The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 28. Typical application with I²C bus and timing diagram



1. Measurement points are done at CMOS levels: $0.3xV_{DD}$ and $0.7xV_{DD}$.

3.3.11 USB characteristics

The USB interface is USB-IF certified (Low Speed and High Speed).

Table 38. USB characteristics

USB DC Electrical Characteristics					
Symbol	**Parameter**	**Conditions**	**Min.(1)(2)**	**Max.(1)(2)**	**Unit**
Input Levels					
V_{DI}	Differential Input Sensitivity	I(DP, DM)	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	
V_{SE}	Single Ended Receiver Threshold		1.3	2.0	
Output Levels					
V_{OL}	Static Output Level Low	R_L of 1.5 kΩ to 3.6V(3)		0.3	V
V_{OH}	Static Output Level High	R_L of 15 kΩ to V_{SS}(3)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. It is important to be aware that the DP/DM pins are not 5 V tolerant. As a consequence, in case of a a shortcut with Vbus (typ: 5.0V), the protection diodes of the DP/DM pins will be direct biased . This will not damage the device if not more than 50 mA is sunk for longer than 24 hours but the reliability may be affected.
3. R_L is the load connected on the USB drivers

Figure 29. USB: data signal rise and fall time

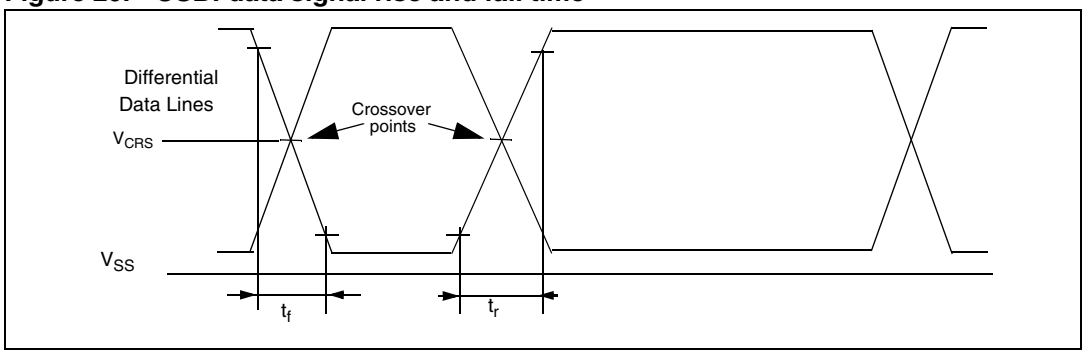


Table 39. USB: Full speed electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
Driver characteristics:					
t_r	Rise time(1)	C_L=50 pF	4	20	ns
t_f	Fall Time1)	C_L=50 pF	4	20	ns
t_{rfm}	Rise/ Fall Time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal Crossover Voltage		1.3	2.0	V

1. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

3.3.12 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA_ADC}, f_{PCLK}, and T_A unless otherwise specified.

Table 40. 10-bit ADC characteristics

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
f_{ADC}	ADC clock frequency		0.4		8	MHz
V_{AIN}	Conversion voltage range		V_{SSA_ADC}		V_{DDA_ADC}	V
R_{AIN}	External input impedance		TBD(2)(3)(4)			kΩ
C_{AIN}	External capacitor on analog input					pF
I_{lkg}	Induced input leakage current	+400 µA injected on any pin			1	µA
		-400 µA injected on any pin except specific adjacent pins in *Table 41*			1	µA
		-400µA injected on specific adjacent pins in *Table 41*		40		µA
C_{ADC}	Internal sample and hold capacitor			3.5		pF
t_{CAL}	Calibration Time	f_{CK_ADC}=8 MHz	725.25			µs
			5802			$1/f_{ADC}$
t_{CONV}	Total Conversion time (including sampling time)	f_{CK_ADC}=8 MHz	3.75			µs
			30 (11 for sampling + 19 for Successive Approximation)			$1/f_{ADC}$
I_{ADC}		Sunk on V_{DDA_ADC}		3.7		mA

1. Unless otherwise specified, typical data are based on T_A=25°C. They are given only as design guidelines and are not tested.
2. $C_{PARASITIC}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3 pF). A high $C_{PARASITIC}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Depending on the input signal variation (f_{AIN}), C_{AIN} can be increased for stabilization time and reduced to allow the use of a larger serial resistor (R_{AIN}). It is valid for all f_{ADC} frequencies ≤ 8 MHz.
4. Calibration is needed once after each power-up.

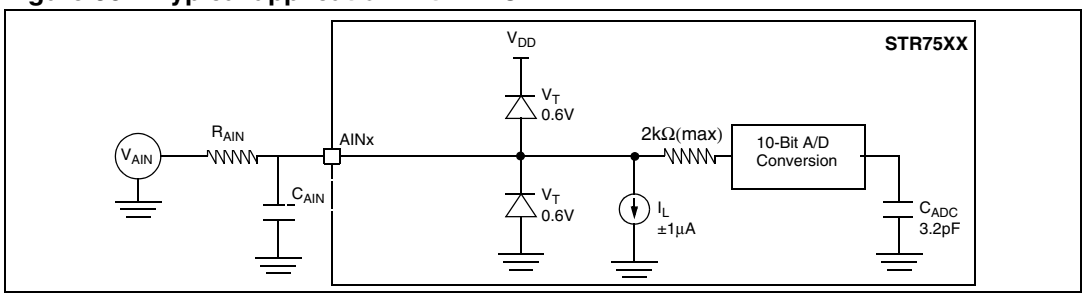
ADC Accuracy vs. Negative Injection Current

Injecting negative current on specific pins listed in *Table 41* (generally adjacent to the analog input pin being converted) should be avoided as this significantly reduces the accuracy of the conversion being performed. It is recommended to add a Schottky diode (pin to ground) to pins which may potentially inject negative current.

Table 41. List of adjacent pins

Analog input	Related adjacent pins
a	None
AIN1/P0.03	None
AIN2/P0.12	P0.11
AIN3/P0.17	P0.18 and P0.16
AIN4/P0.19	P0.24
AIN5/P0.22	None
AIN6/P0.23	P2.04
AIN7/P0.27	P1.11 and P0.26
AIN8/P0.29	P0.30 and P0.28
AIN9/P1.04	None
AIN10/P1.06	P1.05
AIN11/P1.08	P1.04 and P1.13
AIN12/P1.11	P2.17 and P0.27
AIN13/P1.12	None
AIN14/P1.13	P1.14 and P1.01
AIN15/P1.14	None

Figure 30. Typical application with ADC



Analog Power Supply and Reference Pins

The V_{DDA_ADC} and V_{SSA_ADC} pins are the analog power supply of the A/D converter cell.

Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see *: General PCB Design Guidelines on page 66*).

General PCB Design Guidelines

To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1 µF and optionally, if needed 10 pF capacitors as close as possible to the STR7 power supply pins and a 1 to 10 µF capacitor close to the power source (see *Figure 31*).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{DDA_ADC} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs near the A/D input being converted.

Software Filtering of Spurious Conversion Results

For EMC performance reasons, it is recommended to filter A/D conversion outliers using software filtering techniques.

Figure 31. Power supply filtering

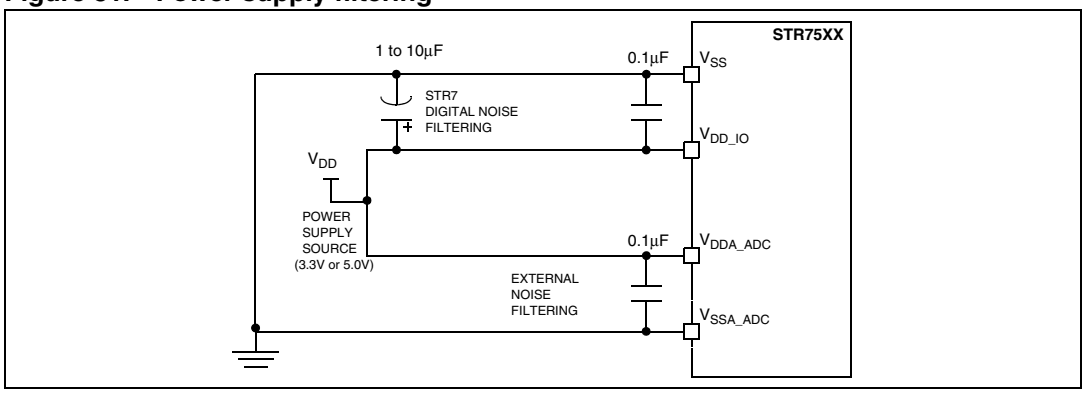
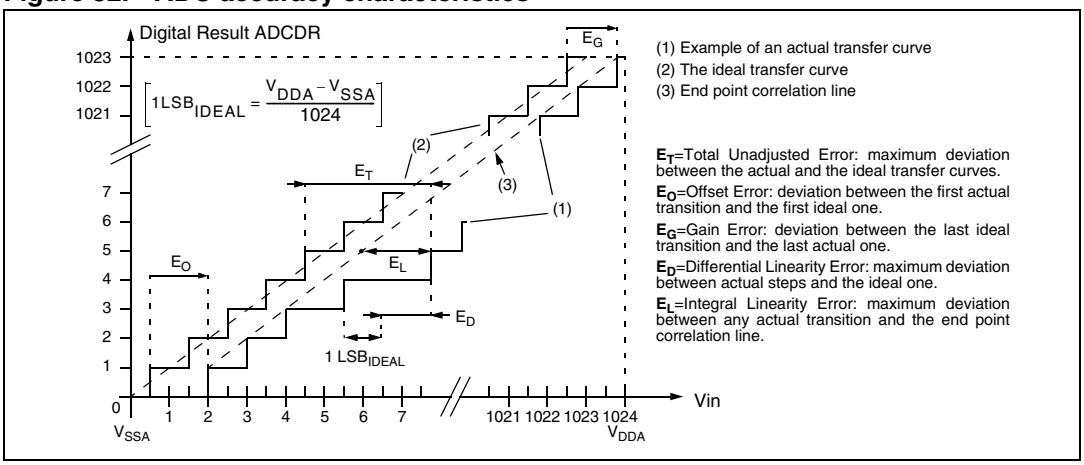


Table 42. ADC accuracy

ADC Accuracy with f_{CK_SYS} = 20 MHz, f_{ADC}=8 MHz, R_{AIN} < 10 kΩ This assumes that the ADC is calibrated(1)					
Symbol	**Parameter**	**Conditions**	**Typ**	**Max**	**Unit**
$\|E_T\|$	Total unadjusted error (2) (3)	V_{DDA_ADC}=3.3 V	1	1.2	LSB
		V_{DDA_ADC}=5.0 V	1	1.2	
$\|E_O\|$	Offset error(2) (3)	V_{DDA_ADC}=3.3 V	0.15	0.5	
		V_{DDA_ADC}=5.0 V	0.15	0.5	
E_G	Gain Error (2) (3)	V_{DDA_ADC}=3.3 V	-0.8	-0.2	
		V_{DDA_ADC}=5.0 V	-0.8	-0.2	
$\|E_D\|$	Differential linearity error(2) (3)	V_{DDA_ADC}=3.3 V	0.7	0.9	
		V_{DDA_ADC}=5.0 V	0.7	0.9	
$\|E_L\|$	Integral linearity error (2) (3)	V_{DDA_ADC}=3.3 V	0.6	0.8	
		V_{DDA_ADC}=5.0 V	0.6	0.8	

1. Calibration is needed once after each power-up.
2. Refer to *ADC Accuracy vs. Negative Injection Current on page 65*
3. ADC Accuracy vs. MCO (Main Clock Output): the ADC accuracy can be significantly degraded when activating the MCO on pin P0.01 while converting an analog channel (especially those which are close to the MCO pin). To avoid this, when an ADC conversion is launched, it is strongly recommended to disable the MCO.

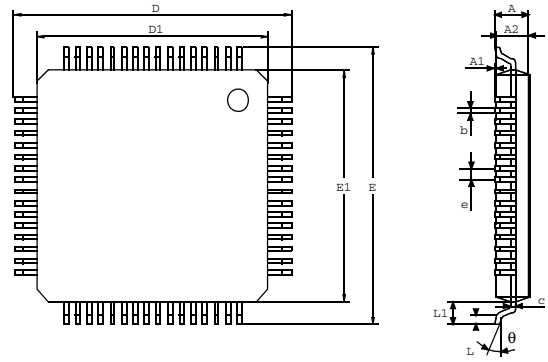
Figure 32. ADC accuracy characteristics



4 Package characteristics

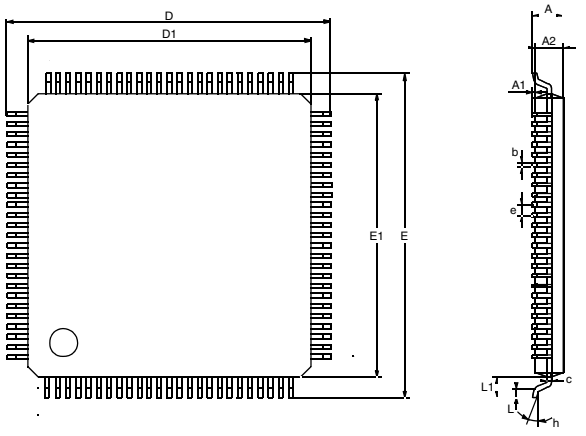
4.1 Package mechanical data

Figure 33. 64-Pin Low Profile Quad Flat Package (10x10)



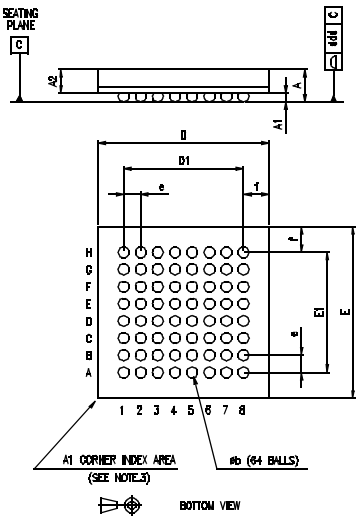
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
E		12.00			0.472	
E1		10.00			0.394	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	64					

Figure 34. 100-Pin Low Profile Flat Package (14x14)



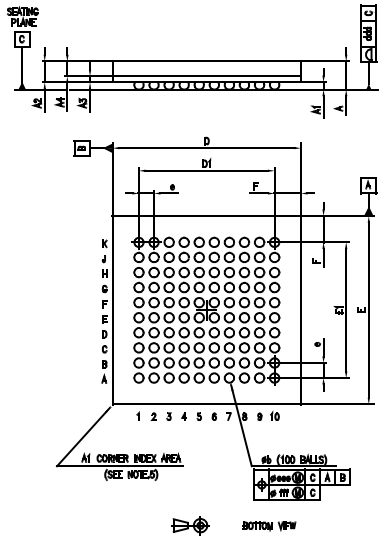
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
E		16.00			0.630	
E1		14.00			0.551	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	100					

Figure 35. 64-Low Profile Fine Pitch Ball Grid Array Package



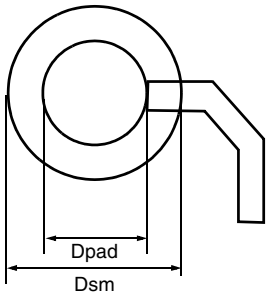
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	1.210		1.700	0.048		0.067
A1	0.270			0.011		
A2		1.120			0.044	
b	0.450	0.500	0.550	0.018	0.020	0.022
D	7.750	8.000	8.150	0.305	0.315	0.321
D1		5.600			0.220	
E	7.750	8.000	8.150	0.305	0.315	0.321
E1		5.600			0.220	
e	0.720	0.800	0.880	0.028	0.031	0.035
f	1.050	1.200	1.350	0.041	0.047	0.053
ddd			0.120			0.005
	Number of Pins					
N	64					

Figure 36. 100-Low Profile Fine Pitch Ball Grid Array Package



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.700			0.067
A1	0.270			0.011		
A2		1.085			0.043	
A3		0.30			0.012	
A4			0.80			0.031
b	0.45	0.50	0.55	0.018	0.020	0.022
D	9.85	10.00	10.15	0.388	0.394	0.40
D1		7.20			0.283	
E	9.85	10.00	10.15	0.388	0.394	0.40
E1		7.20			0.283	
e		0.80			0.031	
F		1.40			0.055	
ddd			0.12			0.005
eee			0.15			0.006
fff			0.08			0.003
	Number of Balls					
N	100					

Figure 37. Recommended PCB design rules (0.80/0.75mm pitch BGA)



Dpad	0.37 mm
Dsm	0.52 mm typ. (depends on solder mask registration tolerance
Solder paste	0.37 mm aperture diameter
– Non solder mask defined pads are recommended – 4 to 6 mils screen print	

4.2 Thermal characteristics

The average chip-junction temperature, T_J must never exceed 125° C.

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$T_J = T_A + (P_D \times \Theta_{JA})$(1)

Where:

- T_A is the Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in ° C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the Chip Internal Power.
- $P_{I/O}$ represents the Power Dissipation on Input and Output Pins;

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$P_D = K / (T_J + 273°C)$ (2)

Therefore (solving equations 1 and 2):

$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2$(3)

where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Table 43. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 100 - 14 x 14 mm / 0.5 mm pitch	46	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LQFP 64 - 10 x 10 mm / 0.5 mm pitch	45	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 64 - 8 x 8 x 1.7mm	58	°C/W
Θ_{JA}	**Thermal Resistance Junction-Ambient** LFBGA 100 - 10 x 10 x 1.7mm	41	°C/W

5 Order codes

Table 44. Order codes

Partnumber	Flash Prog. Memory (Bank 0) Kbytes	Package	CAN Periph	USB Periph	Temp. Range
STR750FV0T6	64	LQFP100 14x14	Yes	Yes	-40 to +85°C
STR750FV1T6	128				
STR750FV2T6	256				
STR750FV2H6(1)	256	LFBGA100 10x10			
STR751FR0T6	64	LQFP64 10x10	-	Yes	-40 to +85°C
STR751FR1T6	128				
STR751FR2T6	256				
STR751FR2H6(1)	256	LFBGA64 8x8			
STR752FR0T6	64	LQFP64 10x10	Yes	-	-40 to +85°C
STR752FR1T6	128				
STR752FR2T6	256				
STR752FR2H6(1)	256	LFBGA64 8x8			
STR752FR0T7	64	LQFP64 10x10	Yes	-	-40 to +105°C
STR752FR1T7	128				
STR752FR2T7	256				
STR752FR2H7(1)	256	LFBGA64 8x8			
STR755FR0T6	64	LQFP64 10x10	-	-	-40 to +85°C
STR755FR1T6	128				
STR755FR2T6	256				
STR755FR2H6(1)	256	LFBGA64 8x8			
STR755FV0T6	64	LQFP100 14x14			
STR755FV1T6	128				
STR755FV2T6	256				
STR755FV2H6(1)	256	LFBGA100 10x10			

1. For other memory sizes, contact sales office.

6 Revision history

Table 45. Revision history

Date	Revision	Description of Changes
25-Sep-2006	1	Initial release
30-Oct-2006	2	Added power consumption data for 5V operation in *Section 3*

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