

KM681000E Family

CMOS SRAM

Document Title

128Kx8 bit Low Power CMOS Static RAM

Revision History

| <u>Revision No.</u> | <u>History</u> | <u>Draft Data</u> | <u>Remark</u> |
|---------------------|--|-------------------|---------------|
| 0.0 | Design target | October 12, 1998 | Preliminary |
| 1.0 | Finalize - Improve twp form 55ns to 50ns for 70ns product. - Remove 55ns speed bin for industrial product. | August 30, 1999 | Final |
| 1.01 | Errata correction | December 1, 1999 | |



128Kx8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 128Kx8
- Power Supply Voltage: 4.5-5.5V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-DIP-600, 32-SOP-525, 32-TSOP1-0820F

GENERAL DESCRIPTION

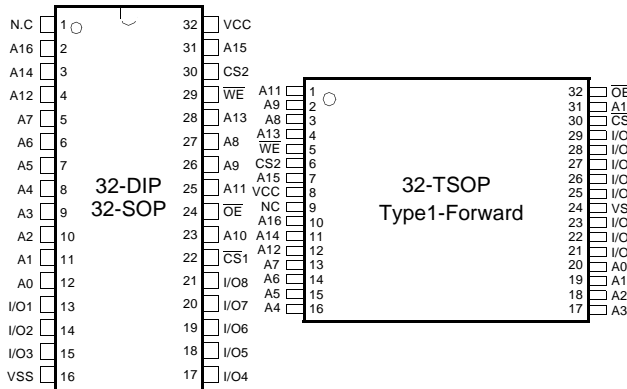
The KM681000E families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed | Power Dissipation | | PKG Type |
|----------------|-----------------------|-----------|-----------------------|----------------------------------|------------------------------------|----------------------------------|
| | | | | Standby (I _{SB1} , Max) | Operating (I _{CC2} , Max) | |
| KM681000EL | Commercial(0~70°C) | 4.5~5.5V | 55 ¹ /70ns | 50µA | 50mA | 32-DIP, 32-SOP 32-TSOP1-0820F |
| KM681000EL-L | | | | 10µA | | |
| KM681000ELI | Industrial(-40~85°C) | | 70ns | 50µA | | 32-SOP -525 32-TSOP1-0820F |
| KM681000ELI-L | | | 15µA | | | |

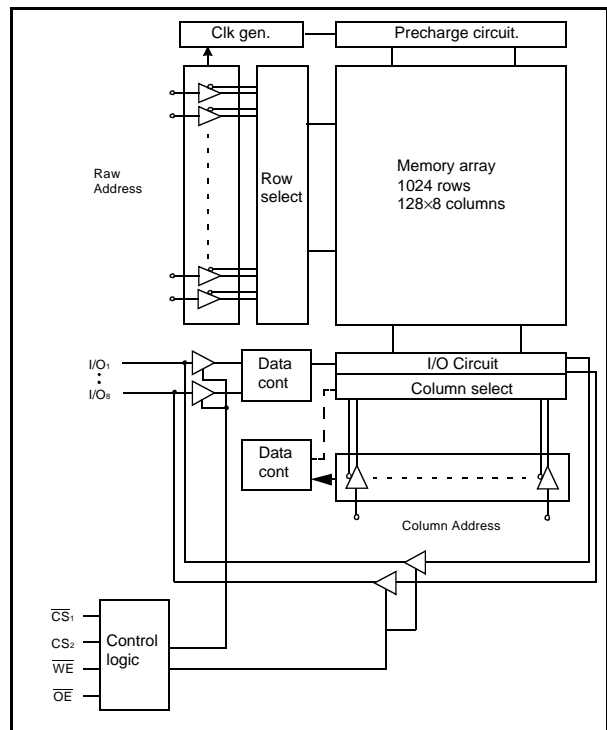
1. The parameters are tested with 50pF test load

PIN DESCRIPTION



| Name | Function |
|------------------------------------|---------------------|
| \overline{CS}_1, CS_2 | Chip Select Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| I/O ₁ -I/O ₈ | Data Inputs/Outputs |
| A ₀ -A ₁₆ | Address Inputs |
| Vcc | Power |
| Vss | Ground |
| N.C. | No Connection |

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

| Commercial Temperature Products(0~70°C) | | Industrial Temperature Products(-40~85°C) | |
|---|--------------------------------|---|--------------------------------|
| Part Name | Function | Part Name | Function |
| KM681000ELP-5 | 32-DIP, 55ns, Low Power | KM681000ELGI-7 | 32-SOP, 70ns, Low Power |
| KM681000ELP-7 | 32-DIP, 70ns, Low Power | KM681000ELGI-7L | 32-SOP, 70ns, Low Low Power |
| KM681000ELP-5L | 32-DIP, 55ns, Low Low Power | KM681000ELTI-7L | 32-TSOP F, 70ns, Low Low Power |
| KM681000ELP-7L | 32-DIP, 70ns, Low Low Power | | |
| KM681000ELG-5 | 32-SOP, 55ns, Low Power | | |
| KM681000ELG-7 | 32-SOP, 70ns, Low Power | | |
| KM681000ELG-5L | 32-SOP, 55ns, Low Low Power | | |
| KM681000ELG-7L | 32-SOP, 70ns, Low Low Power | | |
| KM681000ELT-5L | 32-TSOP F, 55ns, Low Low Power | | |
| KM681000ELT-7L | 32-TSOP F, 70ns, Low Low Power | | |

FUNCTIONAL DESCRIPTION

| \overline{CS}_1 | CS_2 | \overline{OE} | \overline{WE} | I/O | Mode | Power |
|-------------------|-----------------|-----------------|-----------------|--------|-----------------|---------|
| H | X ¹⁾ | X ¹⁾ | X ¹⁾ | High-Z | Deselected | Standby |
| X ¹⁾ | L | X ¹⁾ | X ¹⁾ | High-Z | Deselected | Standby |
| L | H | H | H | High-Z | Output Disabled | Active |
| L | H | L | H | Dout | Read | Active |
| L | H | X ¹⁾ | L | Din | Write | Active |

1. X means don't care (Must be in high or low states)

ABSOLUTE MAXIMUM RATINGS¹⁾

| Item | Symbol | Ratings | Unit | Remark |
|---|------------------------------------|-------------|------|-------------|
| Voltage on any pin relative to V _{SS} | V _{IN} , V _{OUT} | -0.5 to 7.0 | V | - |
| Voltage on V _{CC} supply relative to V _{SS} | V _{CC} | -0.5 to 7.0 | V | - |
| Power Dissipation | P _D | 1.0 | W | - |
| Storage temperature | T _{STG} | -65 to 150 | °C | - |
| Operating Temperature | T _A | 0 to 70 | °C | KM681000EL |
| | | -40 to 85 | °C | KM681000ELI |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

| Item | Symbol | Product | Min | Typ | Max | Unit |
|--------------------|-----------------|------------------|--------------------|-----|------------------------------------|------|
| Supply voltage | V _{CC} | KM681000E Family | 4.5 | 5.0 | 5.5 | V |
| Ground | V _{SS} | All Family | 0 | 0 | 0 | V |
| Input high voltage | V _{IH} | KM681000E Family | 2.2 | - | V _{CC} +0.5 ²⁾ | V |
| Input low voltage | V _{IL} | KM681000E Family | -0.5 ³⁾ | - | 0.8 | V |

Note:

1. Commercial Product: T_A=0 to 70°C, and Industrial Product: T_A=-40 to 85°C, otherwise specified
2. Overshoot : V_{CC}+3.0V in case of pulse width≤30ns
3. Undershoot : -3.0V in case of pulse width≤30ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

| Item | Symbol | Test Condition | Min | Max | Unit |
|--------------------------|-----------------|---------------------|-----|-----|------|
| Input capacitance | C _{IN} | V _{IN} =0V | - | 6 | pF |
| Input/Output capacitance | C _{IO} | V _{IO} =0V | - | 8 | pF |

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

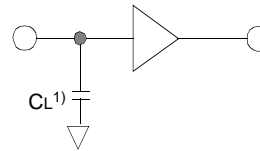
| Item | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--------------------------------|------------------|--|-----|-----|------------------|------|
| Input leakage current | I _{LI} | V _{IN} =V _{SS} to V _{CC} | -1 | - | 1 | μA |
| Output leakage current | I _{LO} | $\overline{CS}_1=V_{IH}$ or CS ₂ =V _{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC} | -1 | - | 1 | μA |
| Operating power supply current | I _{CC} | I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL} , Read | - | - | 10 | mA |
| Average operating current | I _{CC1} | Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS}_1\leq 0.2V$, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V | - | - | 7 | mA |
| | I _{CC2} | Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL} | - | - | 50 | mA |
| Output low voltage | V _{OL} | I _{OL} =2.1mA | - | - | 0.4 | V |
| Output high voltage | V _{OH} | I _{OH} =-1.0mA | 2.4 | - | - | V |
| Standby Current(TTL) | I _{SB} | $\overline{CS}_1=V_{IH}$, CS ₂ =V _{IL} , Other inputs=V _{IH} or V _{IL} | - | - | 3 | mA |
| Standby Current(CMOS) | I _{SB1} | $\overline{CS}_1\geq V_{CC}-0.2V$, CS ₂ ≥V _{CC} -0.2V or CS ₂ ≤0.2V, Other inputs=0~V _{CC} | - | - | 50 ¹⁾ | μA |

1. 50μA for Low power product, in case of Low Low power products are commercial=10μA, industrial=15μA.

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.8 to 2.4V
 Input rising and falling time : 5ns
 Input and output reference voltage : 1.5V
 Output load(see right) : $C_L=100\text{pF}+1\text{TTL}$
 $C_L=50\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

AC CHARACTERISTICS (V_{CC}=4.5~5.5V, Commercial Product : T_A=0 to 70°C, Industrial Product : T_A=-40 to 85°C)

| Parameter List | | Symbol | Speed Bins | | | | Units |
|----------------|---------------------------------|-------------------------------------|------------|-----|------|-----|-------|
| | | | 55ns | | 70ns | | |
| | | | Min | Max | Min | Max | |
| Read | Read cycle time | t _{RC} | 55 | - | 70 | - | ns |
| | Address access time | t _{AA} | - | 55 | - | 70 | ns |
| | Chip select to output | t _{CO1} , t _{CO2} | - | 55 | - | 70 | ns |
| | Output enable to valid output | t _{OE} | - | 25 | - | 35 | ns |
| | Chip select to low-Z output | t _{LZ} | 10 | - | 10 | - | ns |
| | Output enable to low-Z output | t _{OLZ} | 5 | - | 5 | - | ns |
| | Chip disable to high-Z output | t _{HZ} | 0 | 20 | 0 | 25 | ns |
| | Output disable to high-Z output | t _{OHZ} | 0 | 20 | 0 | 25 | ns |
| | Output hold from address change | t _{OH} | 10 | - | 10 | - | ns |
| Write | Write cycle time | t _{WC} | 55 | - | 70 | - | ns |
| | Chip select to end of write | t _{CW} | 45 | - | 60 | - | ns |
| | Address set-up time | t _{AS} | 0 | - | 0 | - | ns |
| | Address valid to end of write | t _{AW} | 45 | - | 60 | - | ns |
| | Write pulse width | t _{WP} | 40 | - | 50 | - | ns |
| | Write recovery time | t _{WR} | 0 | - | 0 | - | ns |
| | Write to output high-Z | t _{WHZ} | 0 | 20 | 0 | 25 | ns |
| | Data to write time overlap | t _{DW} | 20 | - | 25 | - | ns |
| | Data hold from write time | t _{DH} | 0 | - | 0 | - | ns |
| | End write to output low-Z | t _{OW} | 5 | - | 5 | - | ns |

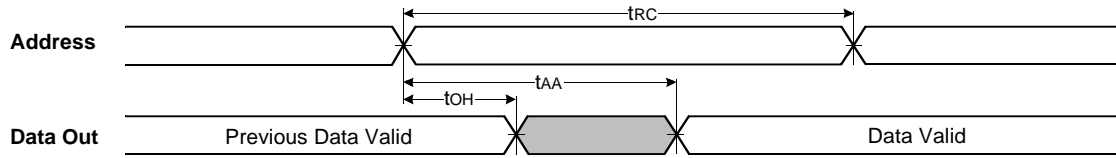
DATA RETENTION CHARACTERISTICS

| Item | Symbol | Test Condition | Min | Typ | Max | Unit | |
|------------------------------------|------------------|---|---------------|-----|-----|------|----|
| V _{CC} for data retention | V _{DR} | $\overline{CS}_1 \geq V_{CC}-0.2V^1$ | 2.0 | - | 5.5 | V | |
| Data retention current | I _{DR} | $V_{CC}=3.0V, \overline{CS}_1 \geq V_{CC}-0.2V^1$ | KM681000EL | - | - | 20 | μA |
| | | | KM681000EL-L | - | - | 10 | |
| | | | KM681000ELI | - | - | 25 | |
| | | | KM681000ELI-L | - | - | 10 | |
| Data retention set-up time | t _{SDR} | See data retention waveform | 0 | - | - | ms | |
| Recovery time | t _{RDR} | | 5 | - | - | | |

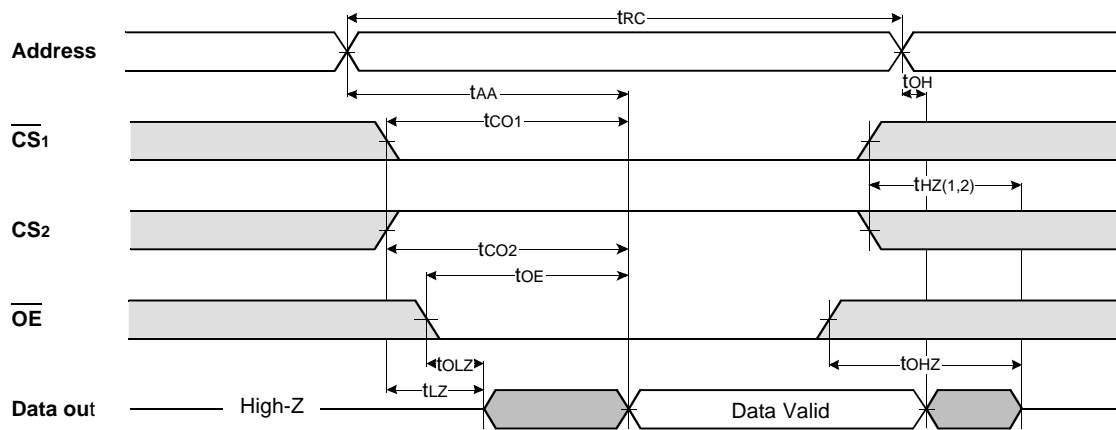
1. $\overline{CS}_1 \geq V_{CC}-0.2V, CS_2 \geq V_{CC}-0.2V$ (\overline{CS}_1 controlled) or $CS_2 \leq 0.2V$ (CS_2 controlled)

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$)



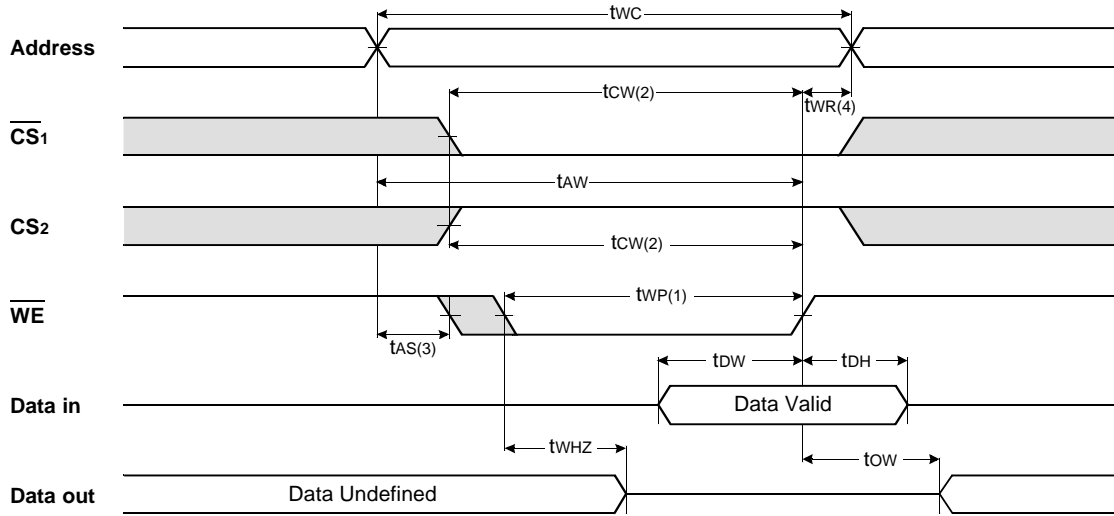
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



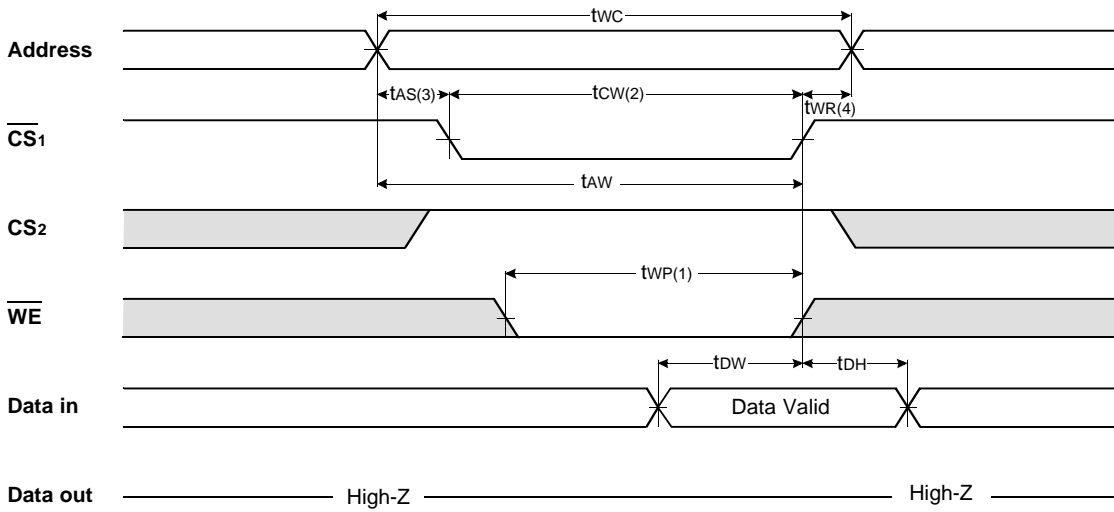
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

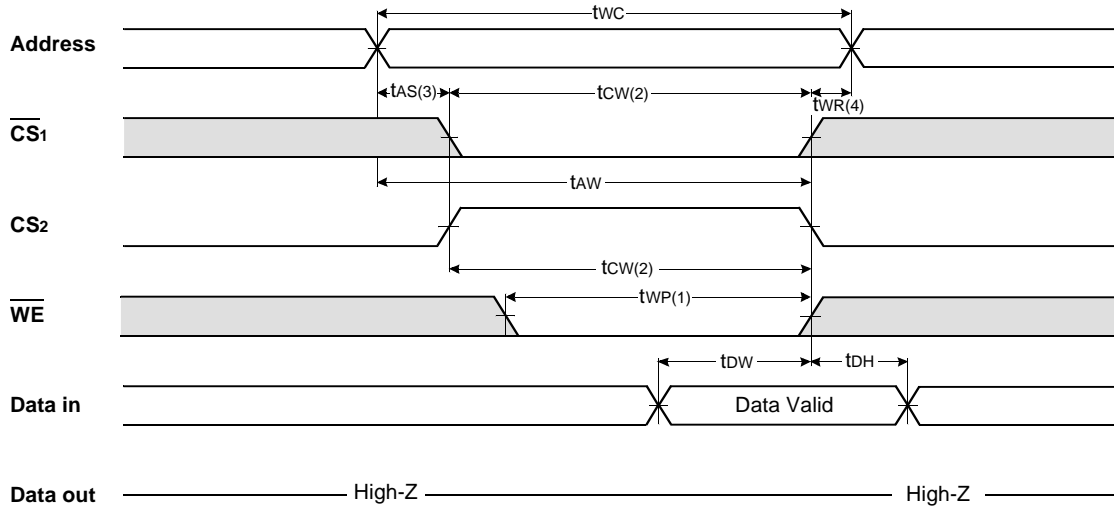
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)

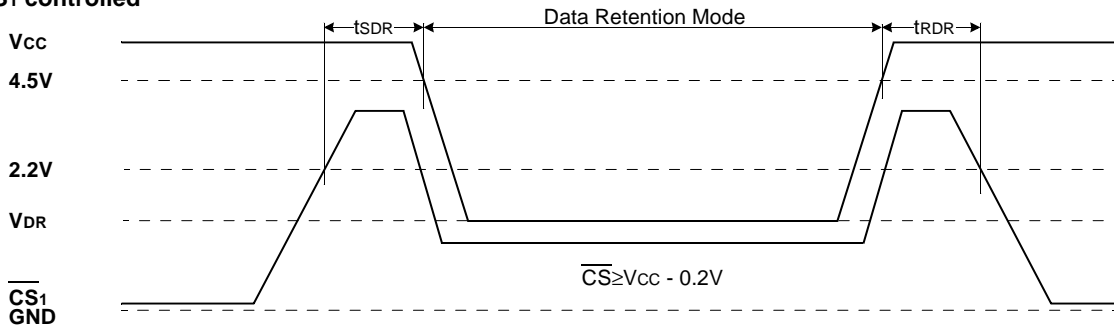


NOTES (WRITE CYCLE)

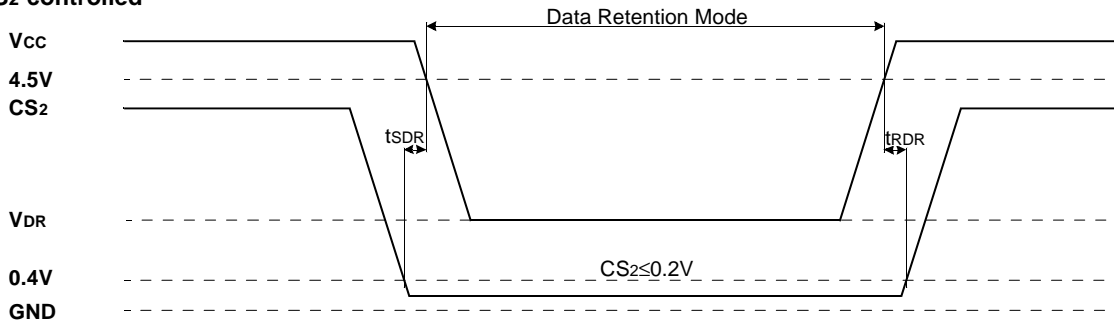
1. A write occurs during the overlap of a low \overline{CS}_1 , a high CS_2 and a low \overline{WE} . A write begins at the latest transition among \overline{CS}_1 goes low, CS_2 going high and \overline{WE} going low : A write end at the earliest transition among CS_1 going high, CS_2 going low and \overline{WE} going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the CS_1 going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as \overline{CS}_1 or \overline{WE} going high t_{WR2} applied in case a write ends as CS_2 going to low.

DATA RETENTION WAVE FORM

CS₁ controlled



CS₂ controlled



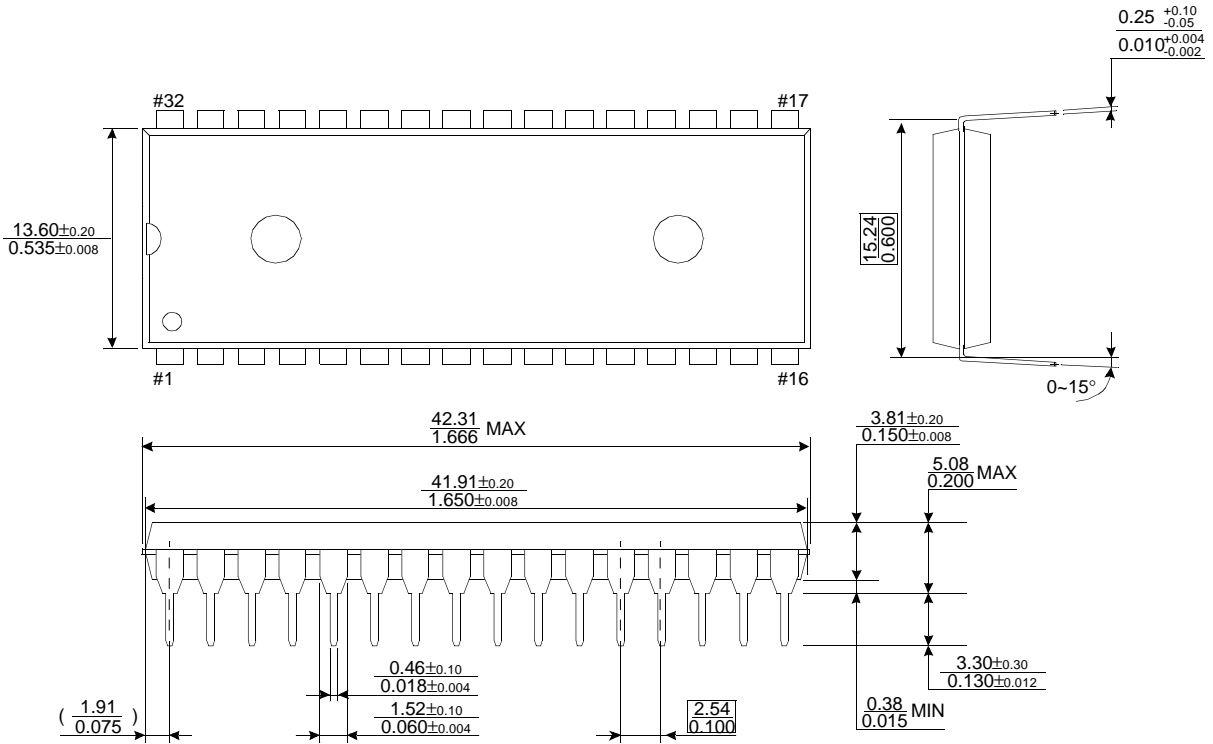
KM681000E Family

CMOS SRAM

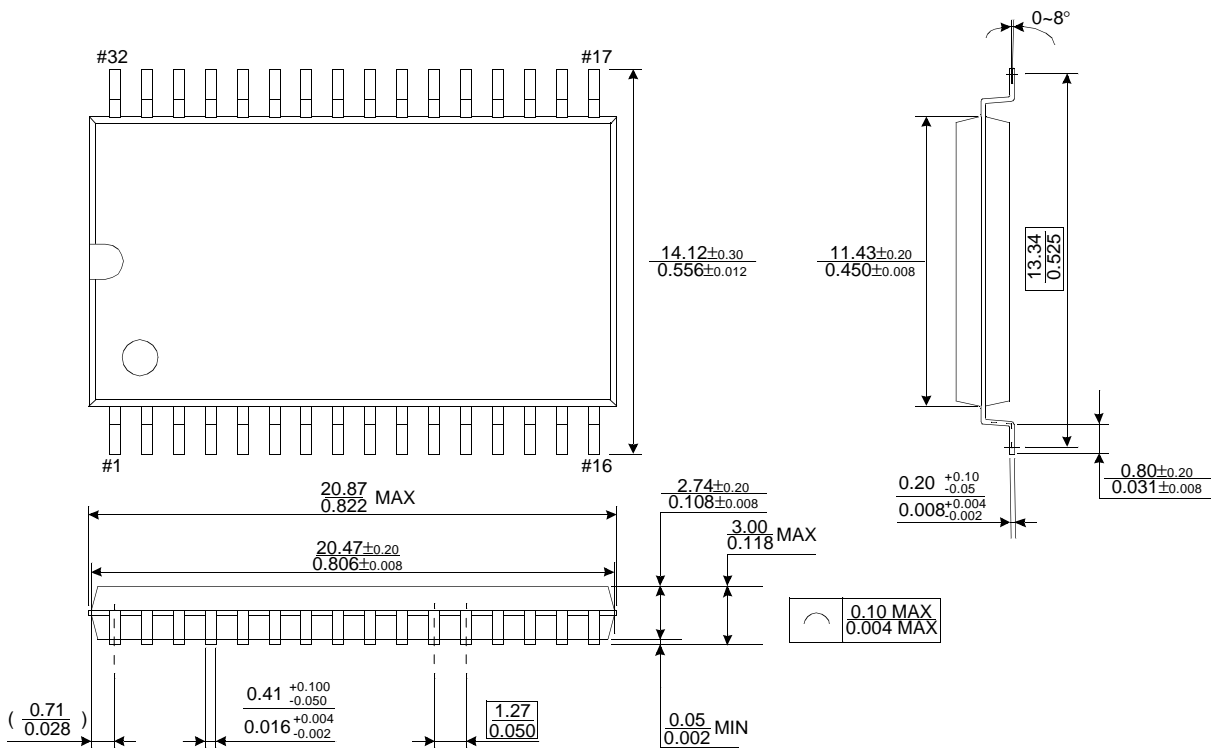
PACKAGE DIMENSIONS

32 DUAL INLINE PACKAGE (600mil)

Units: millimeters(inches)



32 PLASTIC SMALL OUTLINE PACKAGE (525mil)



PACKAGE DIMENSIONS

Units: millimeters(inches)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)

