



CYPRESS

CY29940-1

2.5V or 3.3V, 200-MHz 1:18 Clock Distribution Buffer

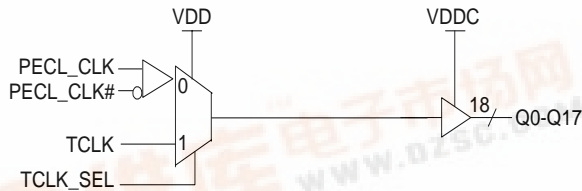
Features

- 200-MHz clock support
- LVPECL or LVCMOS/LVTTL clock input
- LVCMOS/LVTTL-compatible inputs
- 18 clock outputs: drive up to 36 clock lines
- 150 ps max. output-to-output skew
- 23Ω output impedance
- Dual or single supply operation:
 - 3.3V core and 3.3V outputs
 - 3.3V core and 2.5V outputs
 - 2.5V core and 2.5V outputs
- Pin-compatible with MPC940L, MPC9109
- Available in commercial and industrial temperature ranges
- 32-pin TQFP package

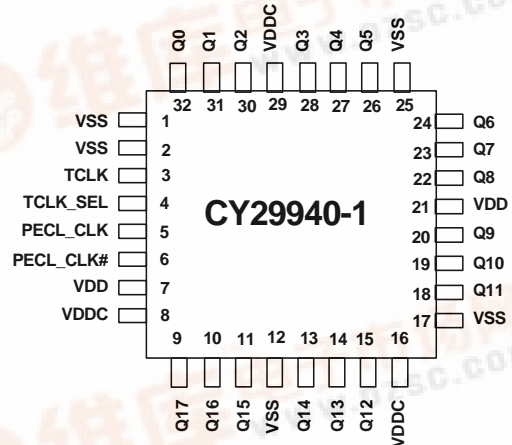
Description

The CY29940-1 is a low-voltage 200-MHz clock distribution buffer with the capability to select either a differential LVPECL- or a LVCMOS/LVTTL-compatible input clock. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL-compatible. The eighteen outputs are 2.5V or 3.3V LVCMOS/LVTTL-compatible and can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:36. Low output-to-output skews make the CY29940-1 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

Block Diagram



Pin Configuration



Pin Description^[1]

| Pin | Name | PWR | I/O | Description |
|---|-----------|------|-------|---|
| 5 | PECL_CLK | | I, PU | PECL Input Clock |
| 6 | PECL_CLK# | | I, PD | PECL Input Clock |
| 3 | TCLK | | I, PD | External Reference/Test Clock Input |
| 9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32 | Q(17:0) | VDDC | O | Clock Outputs |
| 4 | TCLK_SEL | | I, PD | Clock Select Input. When LOW, PECL clock is selected and when HIGH TCLK is selected. |
| 8, 16, 29 | VDDC | | | 3.3V or 2.5V Power Supply for Output Clock Buffers |
| 7, 21 | VDD | | | 3.3V or 2.5V Power Supply |
| 1, 2, 12, 17, 25 | VSS | | | Common Ground |

Note:

1. PD = Internal Pull-down; PU = Internal Pull-up.

Absolute Maximum Conditions

Maximum Input Voltage Relative to V_{SS} : $V_{SS} - 0.3V$
 Maximum Input Voltage Relative to V_{DD} : $V_{DD} + 0.3V$
 Storage Temperature: $-65^{\circ}C$ to $+150^{\circ}C$
 Operating Temperature: $-40^{\circ}C$ to $+85^{\circ}C$
 Maximum ESD Protection 2 kV
 Maximum Power Supply: 5.5V
 Maximum Input Current: ± 20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Electrical Specifications: $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{DDC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$

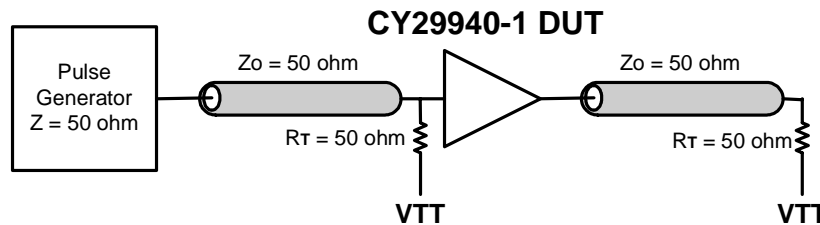
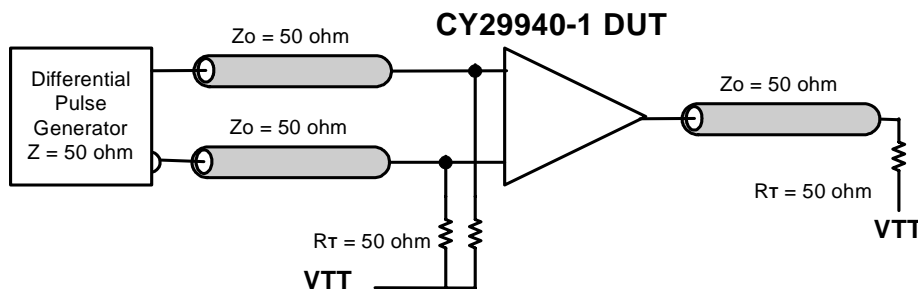
| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|-----------|--|--|----------------|------|----------------|----------|
| V_{IL} | Input Low Voltage | | V_{SS} | | 0.8 | V |
| V_{IH} | Input High Voltage | | 2.0 | | V_{DD} | V |
| I_{IL} | Input Low Current ^[2] | | | | -200 | μA |
| I_{IH} | Input High Current ^[2] | | | | 200 | μA |
| V_{PP} | Peak-to-Peak Input Voltage PECL_CLK | | 500 | | 1000 | mV |
| V_{CMR} | Common Mode Range ^[3] PECL_CLK | $V_{DD} = 3.3V$ | $V_{DD} - 1.4$ | | $V_{DD} - 0.6$ | V |
| | | $V_{DD} = 2.5V$ | $V_{DD} - 1.0$ | | $V_{DD} - 0.6$ | V |
| V_{OL} | Output Low Voltage ^[4,5,6] | $I_{OL} = 20$ mA, $V_{DDC} = 3.3V$ | | | 0.5 | V |
| | | $I_{OL} = 16$ mA, $V_{DDC} = 2.5V$ | | | | V |
| V_{OH} | Output High Voltage ^[4,5,6] | $I_{OH} = -20$ mA, $V_{DDC} = 3.3V$ | 2.4 | | | V |
| | | $I_{OH} = -16$ mA, $V_{DDC} = 2.5V$ | 1.8 | | | V |
| I_{DDQ} | Quiescent Supply Current | | | 5 | 7 | mA |
| I_{DD} | Dynamic Supply Current | $V_{DD} = 3.3V$, Outputs @ 150 MHz, $CL=10$ pF | | 285 | | mA |
| | | $V_{DD} = 3.3V$, Outputs @ 200 MHz, $CL=10$ pF | | 335 | | mA |
| | | $V_{DD} = 2.5V$, Outputs @ 150 MHz, $CL=10$ pF | | 200 | | mA |
| | | $V_{DD} = 2.5V$, Outputs @ 200 MHz, $CL=10$ pF | | 240 | | mA |
| Z_{out} | Output Impedance | | 18 | 23 | 28 | Ω |
| C_{in} | Input Capacitance | | | 4 | | pF |

Notes:

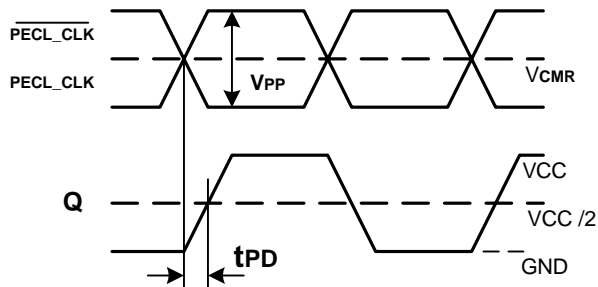
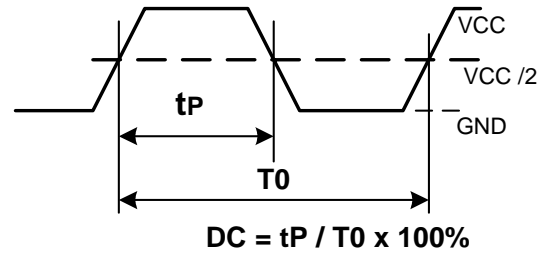
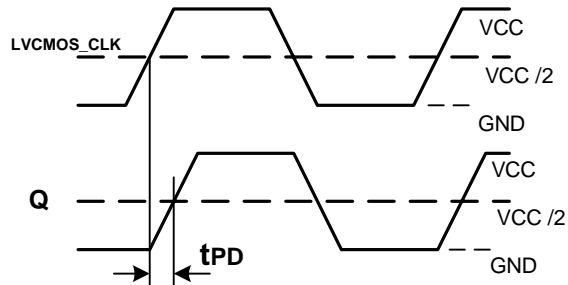
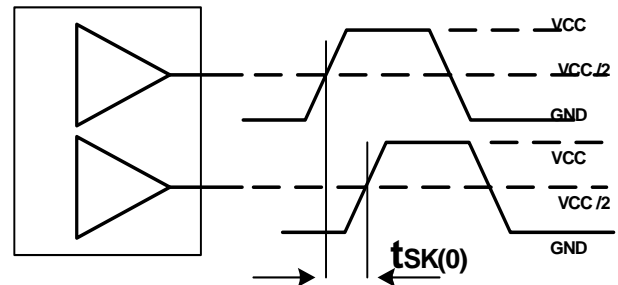
2. Inputs have pull-up/pull-down resistors that effect input current.
3. The V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the V_{CMR} range and the input lies within the V_{PP} specification. Driving series or parallel terminated 50 Ω (or 50 Ω to $V_{DD}/2$) transmission lines.
4. Outputs driving 50 Ω transmission lines.
5. See *Figure 1* and *Figure 2*.
6. 50% input duty cycle.

AC Electrical Specifications ($V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{DDC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$)^[7]

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------------|--|--|------|------|------|------|
| F _{max} | Input Frequency | LVC MOS Input | | | 200 | MHz |
| | | LVPECL Input | | | 180 | |
| T _{PD} | PECL_CLK to Q Delay ^[4,5,10] </ =150 MHz | V _{DD} = 3.3V | 2.0 | | 4.0 | ns |
| | | V _{DD} = 2.5V | 2.6 | | 5.2 | |
| | LVC MOS to Q Delay ^[4,5,10] </ =150 MHz | V _{DD} = 3.3V | 1.8 | | 3.4 | |
| | | V _{DD} = 2.5V | 2.3 | | 4.0 | |
| F _{outDC} | Output Duty Cycle ^[4,5,6] | FCLK < 134 MHz | 45 | | 55 | % |
| | | FCLK > 134 MHz | 40 | | 60 | |
| T _{skew} | Output-to-Output Skew ^[4,5] | | | | 150 | ps |
| T _{skew(pp)} | Part-to-Part Skew ^[8] | PECL, V _{DDC} = 3.3V | | | 1.4 | ns |
| | | PECL, V _{DDC} = 2.5V | | | 2.2 | |
| T _{skew(pp)} | Part-to-Part Skew ^[8] | TCLK, V _{DDC} = 3.3V | | | 1.2 | ns |
| | | TCLK, V _{DDC} = 2.5V | | | 1.7 | |
| T _{skew(pp)} | Part to Part Skew ^[9] | PECL_CLK | | | 850 | ps |
| | | TCLK | | | 750 | |
| t _R /t _F | Output Clocks Rise/Fall Time ^[4,5] | 0.7V to 2.0V, V _{DDC} = 3.3V | 0.3 | | 1.1 | ns |
| | | 0.5V to 1.8V, V _{DDC} = 2.5V | 0.3 | | 1.3 | |


Figure 1. LVC MOS_CLK CY29940-1 Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

Figure 2. PECL_CLK CY29940-1 Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V
Notes:

7. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
8. Across temperature and voltage ranges, includes output skew.
9. For a specific temperature and voltage, includes output skew.
10. Parameters tested @ 150 MHz.

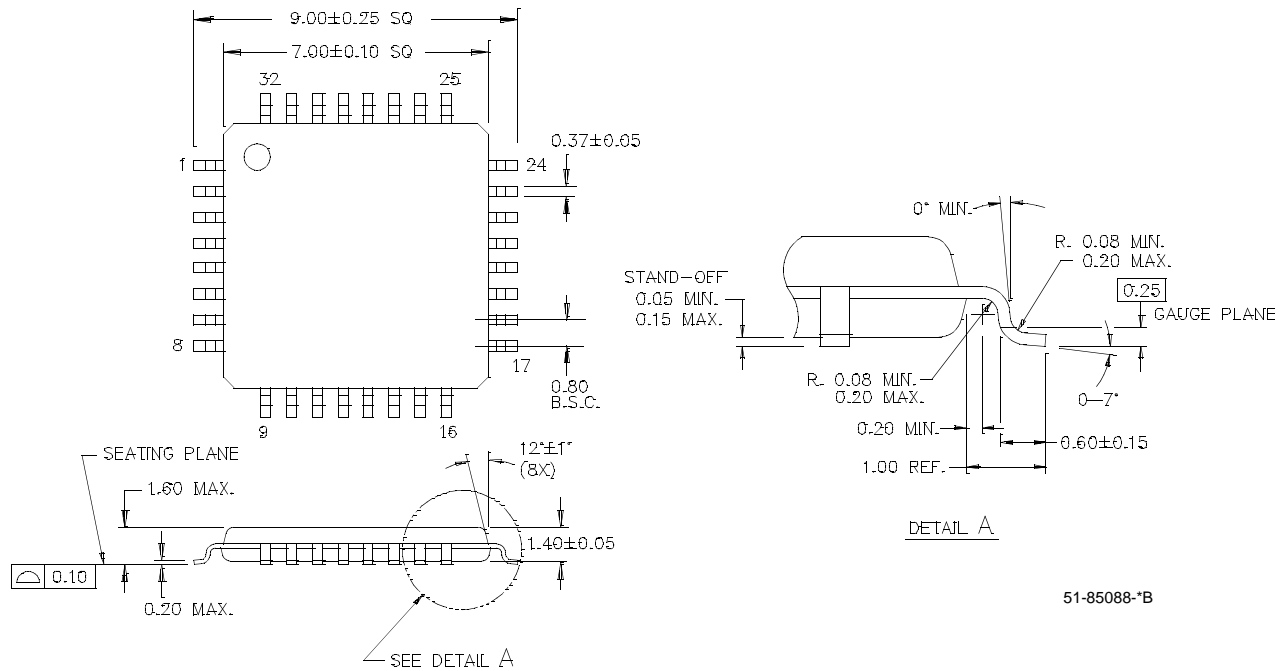

Figure 3. Propagation Delay (TPD) Test Reference

Figure 5. Output Duty Cycle (FoutDC)

Figure 4. LVCMOS Propagation Delay (TPD) Test Reference

Figure 6. Output-to-Output Skew tsk(0)

Ordering Information

| Part Number | Package Type | Production Flow |
|--------------|-----------------------------|----------------------------|
| CY29940AC-1 | 32-pin TQFP | Commercial, 0°C to 70°C |
| CY29940AC-1T | 32-pin TQFP – Tape and Reel | Commercial, 0°C to 70°C |
| CY29940AI-1 | 32-pin TQFP | Industrial, -40°C to +85°C |
| CY29940AI-1T | 32-pin TQFP – Tape and Reel | Industrial, -40°C to +85°C |

Package Drawing and Dimensions

32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.4 mm A32.14



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Document History Page

| Document Title: CY29940-1 2.5V or 3.3V, 200-MHz 1:18 Clock Distribution Buffer Document Number: 38-07487 | | | | |
|---|----------------|-------------------|------------------------|------------------------------|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 119820 | 01/29/03 | BRK | New Data Sheet |