



June 2002

ADC12H030/ADC12H032/ADC12H034/ADC12H038, ADC12030/ADC12032/ADC12034/ADC12038 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converters with MUX and Sample/Hold

General Description

The ADC12030, and ADC12H030 families are 12-bit plus sign successive approximation A/D converters with serial I/O and configurable input multiplexers. The ADC12032/ADC12H032, ADC12034/ADC12H034 and ADC12038/ADC12H038 have 2, 4 and 8 channel multiplexers, respectively. The differential multiplexer outputs and A/D inputs are available on the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 pins. The ADC12030/ADC12H030 has a two channel multiplexer with the multiplexer outputs and A/D inputs internally connected. The ADC12030 family is tested with a 5 MHz clock, while the ADC12H030 family is tested with an 8 MHz clock. On request, these A/Ds go through a self calibration process that adjusts linearity, zero and full-scale errors to less than ± 1 LSB each.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. A fully differential unipolar analog input range (0V to +5V) can be accommodated with a single +5V supply. In the differential modes, valid outputs are obtained even when the negative inputs are greater than the positive because of the 12-bit plus sign output data format.

The serial I/O is configured to comply with the NSC MICROWIRE. For voltage references see the LM4040 or LM4041.

Applications

- Medical instruments
- Process control systems
- Test equipment

Features

- Serial I/O (MICROWIRE Compatible)
- 2, 4, or 8 channel differential or single-ended multiplexer
- Analog input sample/hold function
- Power down mode
- Variable resolution and conversion rate
- Programmable acquisition time
- Variable digital output word length and format
- No zero or full scale adjustment required
- Fully tested and guaranteed with a 4.096V reference
- 0V to 5V analog input range with single 5V power supply
- No Missing Codes over temperature

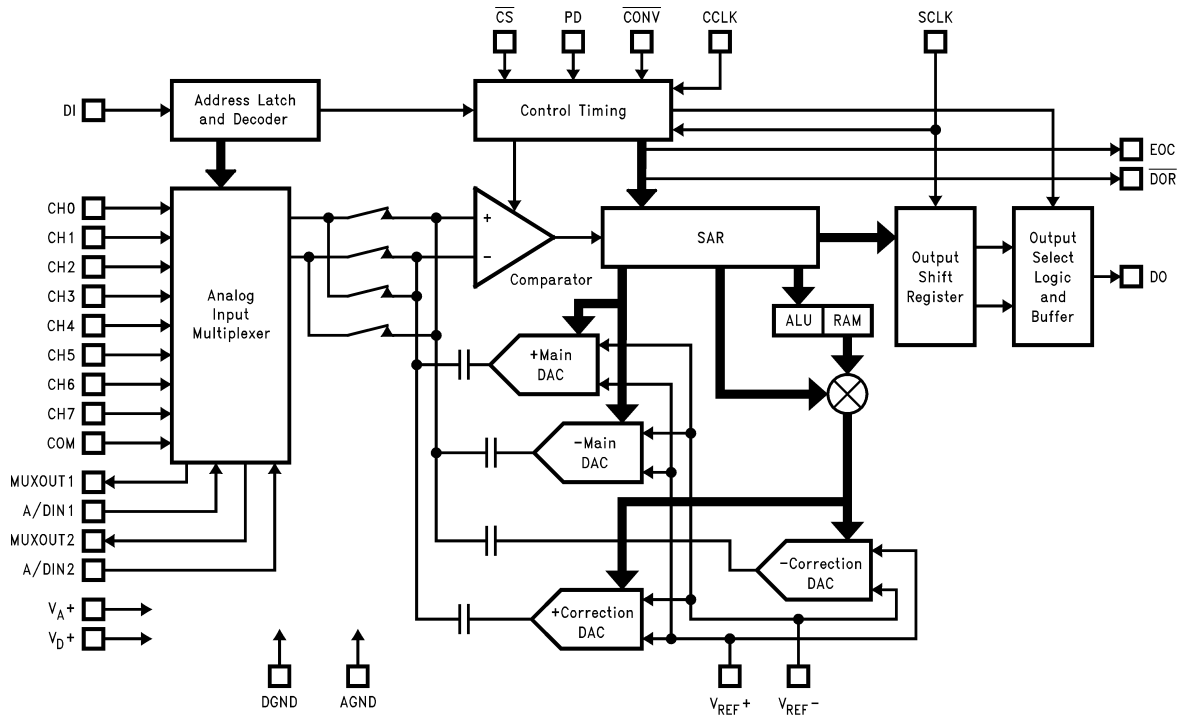
Key Specifications

■ Resolution	12-bit plus sign
■ 12-bit plus sign conversion time	
– ADC12H30 family	5.5 μ s (max)
– ADC12030 family	8.8 μ s (max)
■ 12-bit plus sign throughput time	
– ADC12H30 family	8.6 μ s (max)
– ADC12030 family	14 μ s (max)
■ Integral linearity error	± 1 LSB (max)
■ single supply	5V $\pm 10\%$
■ Power consumption	33 mW (max)
– Power down	100 μ W (typ)

ADC12H030/ADC12H032/ADC12H034/ADC12H038, ADC12030/ADC12032/ADC12034/ADC12038 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converters with MUX and Sample/Hold



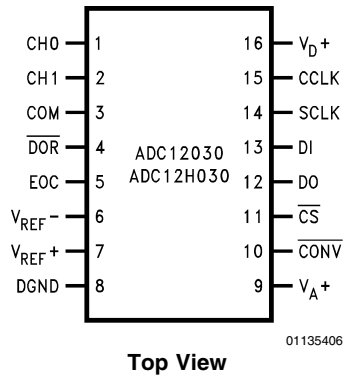
ADC12038 Simplified Block Diagram



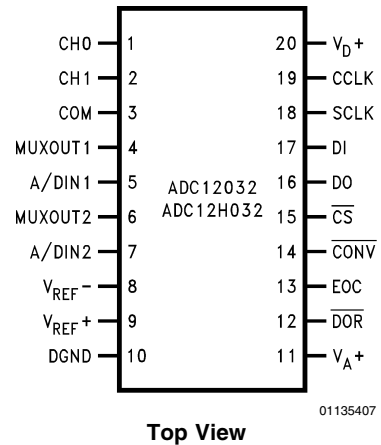
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Connection Diagrams

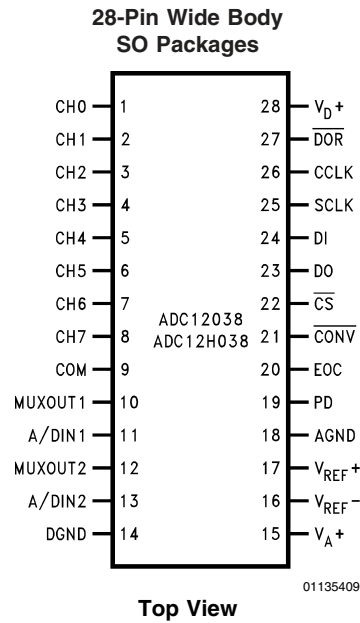
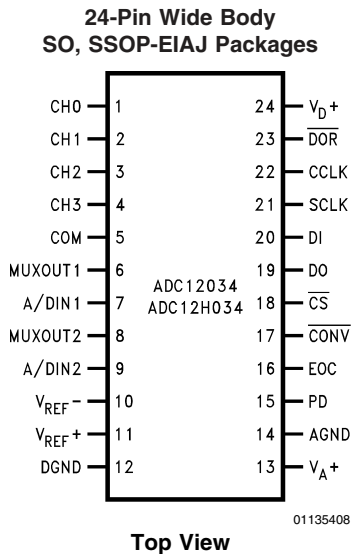
16-Pin Wide Body SO Packages



20-Pin Wide Body SO Packages



Connection Diagrams (Continued)



Ordering Information

Industrial Temperature Range -40°C ≤ T _A ≤ +85°C	Package
ADC12H030CIWM, ADC12030CIWM	M16B
ADC12H032CIWM, ADC12032CIWM	M20B
ADC12H034CIN, ADC12034CIN	N24C
ADC12H034CIWM, ADC12034CIWM	M24B
ADC12H034CIMSA	MSA24
ADC12H038CIWM, ADC12038CIWM	M28B

Pin Descriptions

CCLK	The clock applied to this input controls the successive approximation conversion time interval and the acquisition time. The rise and fall times of the clock edges should not exceed 1 μs.		
SCLK	This is the serial data clock input. The clock applied to this input controls the rate at which the serial data exchange occurs. The rising edge loads the information on the DI pin into the multiplexer address and mode select shift register. This address controls which channel of the analog input multiplexer (MUX) is selected and the mode of operation for the A/D. With \overline{CS} low the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When \overline{CS} is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When \overline{CS} is toggled the falling edge of \overline{CS} always clocks out the first bit of data. \overline{CS} should be brought low when SCLK is low. The rise and fall times of the clock edges should not exceed	DI	1 μs. This is the serial data input pin. The data applied to this pin is shifted by the rising edge of SCLK into the multiplexer address and mode select register. <i>Table 2</i> through <i>Table 5</i> show the assignment of the multiplexer address and the mode select data.
		DO	The data output pin. This pin is an active push/pull output when \overline{CS} is low. When \overline{CS} is high, this output is TRI-STATE. The A/D conversion result (D0–D12) and converter status data are clocked out by the falling edge of SCLK on this pin. The word length and format of this result can vary (see <i>Table 7</i>). The word length and format are controlled by the data shifted into the multiplexer address and mode select register (see <i>Table 5</i>).
		EOC	This pin is an active push/pull output and indicates the status of the ADC12030/2/4/8. When low, it signals that the A/D is busy with a conversion, auto-calibration, auto-zero or power down cycle. The rising edge of EOC signals the end of one of these cycles.
		\overline{CS}	This is the chip select pin. When a logic low

Pin Descriptions (Continued)

<p>is applied to this pin, the rising edge of SCLK shifts the data on DI into the address register. This low also brings DO out of TRI-STATE. With \overline{CS} low the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When \overline{CS} is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When \overline{CS} is toggled the falling edge of \overline{CS} always clocks out the first bit of data. \overline{CS} should be brought low when SCLK is low. The falling edge of \overline{CS} resets a conversion in progress and starts the sequence for a new conversion. When \overline{CS} is brought back low during a conversion, that conversion is prematurely terminated. The data in the output latches may be corrupted. Therefore, when \overline{CS} is brought back low during a conversion in progress the data output at that time should be ignored. \overline{CS} may also be left continuously low. In this case it is imperative that the correct number of SCLK pulses be applied to the ADC in order to remain synchronous. After the ADC supply power is applied it expects to see 13 clock pulses for each I/O sequence. The number of clock pulses the ADC expects is the same as the digital output word length. This word length can be modified by the data shifted in on the DO pin. <i>Table 5</i> details the data required.</p>	<p>\overline{DOR}</p> <p>This is the data output ready pin. This pin is an active push/pull output. It is low when the conversion result is being shifted out and goes high to signal that all the data has been shifted out.</p>	<p>\overline{CONV}</p> <p>A logic low is required on this pin to program any mode or change the ADC's configuration as listed in the Mode Programming <i>Table 5</i> such as 12-bit conversion, 8-bit conversion, Auto Cal, Auto Zero etc. When this pin is high the ADC is placed in the read data only mode. While in the read data only mode, bringing \overline{CS} low and pulsing SCLK will only clock out on DO any data stored in the ADCs output shift register. The data on DI will be neglected. A new conversion will not be started and the ADC will remain in the mode and/or configuration previously programmed. Read data only cannot be per-</p>	<p>formed while a conversion, Auto-Cal or Auto-Zero are in progress.</p>
<p>PD</p>	<p>CH0–CH7</p>	<p>COM</p>	<p>This is the power down pin. When PD is high the A/D is powered down; when PD is low the A/D is powered up. The A/D takes a maximum of 250 μs to power up after the command is given.</p> <p>These are the analog inputs of the MUX. A channel input is selected by the address information at the DI pin, which is loaded on the rising edge of SCLK into the address register (See <i>Tables 2, 3, 4</i>).</p> <p>The voltage applied to these inputs should not exceed V_{A+} or go below GND. Exceeding this range on an unselected channel will corrupt the reading of a selected channel.</p> <p>This pin is another analog input pin. It is used as a pseudo ground when the analog multiplexer is single-ended.</p>
<p>MUXOUT1,</p>	<p>MUXOUT2</p>	<p>A/DIN1, /DIN2</p>	<p>These are the multiplexer output pins.</p> <p>These are the converter input pins. MUXOUT1 is usually tied to A/DIN1. MUXOUT2 is usually tied to A/DIN2. If external circuitry is placed between MUXOUT1 and A/DIN1, or MUXOUT2 and A/DIN2 it may be necessary to protect these pins. The voltage at these pins should not exceed V_{A+} or go below AGND (see <i>Figure 5</i>).</p>
<p>V_{REF+}</p>	<p>V_{REF-}</p>	<p>V_{A+}, V_{D+}</p>	<p>This is the positive analog voltage reference input. In order to maintain accuracy, the voltage range of V_{REF} ($V_{REF} = V_{REF+} - V_{REF-}$) is 1 V_{DC} to 5.0 V_{DC} and the voltage at V_{REF+} cannot exceed V_{A+}. See <i>Figure 6</i> for recommended bypassing.</p> <p>The negative voltage reference input. In order to maintain accuracy, the voltage at this pin must not go below GND or exceed V_{A+}. (See <i>Figure 6</i>).</p> <p>These are the analog and digital power supply pins. V_{A+} and V_{D+} are not connected together on the chip. These pins should be tied to the same power supply and bypassed separately (see <i>Figure 6</i>). The operating voltage range of V_{A+} and V_{D+} is 4.5 V_{DC} to 5.5 V_{DC}.</p>
<p>DGND</p>	<p>AGND</p>	<p>DGND</p> <p>AGND</p>	<p>This is the digital ground pin (see <i>Figure 6</i>).</p> <p>This is the analog ground pin (see <i>Figure 6</i>).</p>

Converter Electrical Characteristics (Continued)

The following specifications apply for $V^+ = V_{A^+} = V_{D^+} = +5.0 V_{DC}$, $V_{REF^+} = +4.096 V_{DC}$, $V_{REF^-} = 0 V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 8$ MHz for the ADC12H030, ADC12H032, ADC12H034 and ADC12H038, $f_{CK} = f_{SK} = 5$ MHz for the ADC12030, ADC12032, ADC12034 and ADC12038, $R_S = 25\Omega$, source impedance for V_{REF^+} and $V_{REF^-} \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX} ; all other limits $T_A = T_J = 25^\circ C$.** (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
+INL	Positive Integral Linearity Error	8-bit + sign mode (Note 12)		$\pm 1/2$	LSB (max)
-INL	Negative Integral Linearity Error	8-bit + sign mode (Note 12)		$\pm 1/2$	LSB (max)
DNL	Differential Non-Linearity	8-bit + sign mode		$\pm 3/4$	LSB (max)
	Positive Full-Scale Error	8-bit + sign mode (Note 12)		$\pm 1/2$	LSB (max)
	Negative Full-Scale Error	8-bit + sign mode (Note 12)		$\pm 1/2$	LSB (max)
	Offset Error	8-bit + sign mode, after Auto-Zero (Note 13) $V_{IN(+)} = V_{IN(-)} = + 2.048V$		$\pm 1/2$	LSB (max)
TUE	Total Unadjusted Error	8-bit + sign mode after Auto-Zero (Notes 12, 13, 14)		$\pm 3/4$	LSB (max)
	Multiplexer Channel to Channel Matching		± 0.05		LSB
	Power Supply Sensitivity	$V^+ = +5V \pm 10\%$ $V_{REF} = +4.096V$			
	Offset Error		± 0.5	± 1	LSB (max)
	+ Full-Scale Error		± 0.5	± 1.5	LSB (max)
	- Full-Scale Error		± 0.5	± 1.5	LSB (max)
	+ Integral Linearity Error		± 0.5		LSB
	- Integral Linearity Error		± 0.5		LSB
	Output Data from "12-Bit Conversion of Offset" (see Table 5)	(Note 20)		+10 -10	LSB (max) LSB (min)
	Output Data from "12-Bit Conversion of Full-Scale" (see Table 5)	(Note 20)		4095 4093	LSB (max) LSB (min)
UNIPOLAR DYNAMIC CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$f_{IN} = 1$ kHz, $V_{IN} = 5 V_{PP}$, $V_{REF^+} = 5.0V$ $f_{IN} = 20$ kHz, $V_{IN} = 5 V_{PP}$, $V_{REF^+} = 5.0V$ $f_{IN} = 40$ kHz, $V_{IN} = 5 V_{PP}$, $V_{REF^+} = 5.0V$	69.4 68.3 65.7		dB dB dB
	-3 dB Full Power Bandwidth	$V_{IN} = 5 V_{PP}$, where S/(N+D) drops 3 dB	31		kHz
DIFFERENTIAL DYNAMIC CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$f_{IN} = 1$ kHz, $V_{IN} = \pm 5V$, $V_{REF^+} = 5.0V$ $f_{IN} = 20$ kHz, $V_{IN} = \pm 5V$, $V_{REF^+} = 5.0V$ $f_{IN} = 40$ kHz, $V_{IN} = \pm 5V$, $V_{REF^+} = 5.0V$	77.0 73.9 67.0		dB dB dB
	-3 dB Full Power Bandwidth	$V_{IN} = \pm 5V$, where S/(N+D) drops 3 dB	40		kHz
REFERENCE INPUT, ANALOG INPUTS AND MULTIPLEXER CHARACTERISTICS					
C_{REF}	Reference Input Capacitance		85		pF
$C_{A/D}$	A/DIN1 and A/DIN2 Analog Input Capacitance		75		pF
	A/DIN1 and A/DIN2 Analog Input Leakage Current	$V_{IN} = +5.0V$ or $V_{IN} = 0V$	± 0.1	± 1.0	μA (max)
	CH0-CH7 and COM Input Voltage			GND - 0.05 $V_{A^+} + 0.05$	V (min) V (max)

Converter Electrical Characteristics (Continued)

The following specifications apply for $V^+ = V_{A+} = V_{D+} = +5.0 V_{DC}$, $V_{REF+} = +4.096 V_{DC}$, $V_{REF-} = 0 V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 8$ MHz for the ADC12H030, ADC12H032, ADC12H034 and ADC12H038, $f_{CK} = f_{SK} = 5$ MHz for the ADC12030, ADC12032, ADC12034 and ADC12038, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ C$. (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
REFERENCE INPUT, ANALOG INPUTS AND MULTIPLEXER CHARACTERISTICS					
C_{CH}	CH0–CH7 and COM Input Capacitance		10		pF
C_{MUXOUT}	MUX Output Capacitance		20		pF
	Off Channel Leakage (Note 16) CH0–CH7 and COM Pins	On Channel = 5V and Off Channel = 0V	-0.01	-0.3	μA (min)
		On Channel = 0V and Off Channel = 5V	0.01	0.3	μA (max)
	On Channel Leakage (Note 16) CH0–CH7 and COM Pins	On Channel = 5V and Off Channel = 0V	0.01	0.3	μA (max)
		On Channel = 0V and Off Channel = 5V	-0.01	-0.3	μA (min)
	MUXOUT1 and MUXOUT2 Leakage Current	$V_{MUXOUT} = 5.0V$ or $V_{MUXOUT} = 0V$	0.01	0.3	μA (max)
R_{ON}	MUX On Resistance	$V_{IN} = 2.5V$ and $V_{MUXOUT} = 2.4V$	850	1150	Ω (max)
	R_{ON} Matching Channel to Channel	$V_{IN} = 2.5V$ and $V_{MUXOUT} = 2.4V$	5		%
	Channel to Channel Crosstalk	$V_{IN} = 5 V_{PP}$, $f_{IN} = 40$ kHz	-72		dB
	MUX Bandwidth		90		kHz

DC and Logic Electrical Characteristics

The following specifications apply for $V^+ = V_{A+} = V_{D+} = +5.0 V_{DC}$, $V_{REF+} = +4.096 V_{DC}$, $V_{REF-} = 0 V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 8$ MHz for the ADC12H030, ADC12H032, ADC12H034 and ADC12H038, $f_{CK} = f_{SK} = 5$ MHz for the ADC12030, ADC12032, ADC12034 and ADC12038, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ C$. (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
CCLK, CS, CONV, DI, PD AND SCLK INPUT CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V^+ = 5.5V$		2.0	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V^+ = 4.5V$		0.8	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5.0V$	0.005	1.0	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	-0.005	-1.0	μA (min)
DO, EOC AND DOR DIGITAL OUTPUT CHARACTERISTICS					
$V_{OUT(1)}$	Logical "1" Output Voltage	$V^+ = 4.5V$, $I_{OUT} = -360 \mu A$		2.4	V (min)
		$V^+ = 4.5V$, $I_{OUT} = -10 \mu A$		4.25	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V^+ = 4.5V$, $I_{OUT} = 1.6$ mA		0.4	V (max)
I_{OUT}	TRI-STATE® Output Current	$V_{OUT} = 0V$	-0.1	-3.0	μA (max)
		$V_{OUT} = 5V$	0.1	3.0	μA (max)
$+I_{SC}$	Output Short Circuit Source Current	$V_{OUT} = 0V$	14	6.5	mA (min)
$-I_{SC}$	Output Short Circuit Sink Current	$V_{OUT} = V_{D+}$	16	8.0	mA (min)
POWER SUPPLY CHARACTERISTICS					
I_{D+}	Digital Supply Current ADC12030, ADC12032, ADC12034	Awake	1.6	2.5	mA (max)
		$\overline{CS} = \text{HIGH}$, Powered Down, CCLK on	600		μA

DC and Logic Electrical Characteristics (Continued)

The following specifications apply for $V^+ = V_{A^+} = V_{D^+} = +5.0 V_{DC}$, $V_{REF^+} = +4.096 V_{DC}$, $V_{REF^-} = 0 V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 8$ MHz for the ADC12H030, ADC12H032, ADC12H034 and ADC12H038, $f_{CK} = f_{SK} = 5$ MHz for the ADC12030, ADC12032, ADC12034 and ADC12038, $R_S = 25\Omega$, source impedance for V_{REF^+} and $V_{REF^-} \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Bold-face limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ C$. (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
POWER SUPPLY CHARACTERISTICS					
	and ADC12038	$\overline{CS} = \text{HIGH}$, Powered Down, CCLK off	20		μA
	Digital Supply Current	Awake	2.3	3.2	mA
	ADC12H030, ADC12H032, ADC12H034 and ADC12H038	$\overline{CS} = \text{HIGH}$, Powered Down, CCLK on	0.9		mA
		$\overline{CS} = \text{HIGH}$, Powered Down, CCLK off	20		μA
I_{A^+}	Positive Analog Supply Current	Awake	2.7	4.0	mA (max)
		$\overline{CS} = \text{HIGH}$, Powered Down, CCLK on	10		μA
		$\overline{CS} = \text{HIGH}$, Powered Down, CCLK off	0.1		μA
I_{REF}	Reference Input Current	Awake	70		μA
		$\overline{CS} = \text{HIGH}$, Powered Down	0.1		μA

AC Electrical Characteristics

The following specifications apply for $V^+ = V_{A^+} = V_{D^+} = +5.0 V_{DC}$, $V_{REF^+} = +4.096 V_{DC}$, $V_{REF^-} = 0 V_{DC}$, 12-bit + sign conversion mode, $t_r = t_f = 3$ ns, $f_{CK} = f_{SK} = 8$ MHz for the ADC12H030, ADC12H032, ADC12H034 and ADC12H038, $f_{CK} = f_{SK} = 5$ MHz for the ADC12030, ADC12032, ADC12034 and ADC12038, $R_S = 25\Omega$, source impedance for V_{REF^+} and $V_{REF^-} \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Bold-face limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ C$. (Note 17)

Symbol	Parameter	Conditions	Typical (Note 10)	ADC12H030/2/4/8	ADC12030/2/4/8	Units (Limits)
				Limits (Note 11)	Limits (Note 11)	
f_{CK}	Conversion Clock (CCLK) Frequency		10	8	5	MHz (max)
			1			MHz (min)
f_{SK}	Serial Data Clock SCLK Frequency		10	8	5	MHz (max)
			0			Hz (min)
	Conversion Clock Duty Cycle			40	40	% (min)
				60	60	% (max)
	Serial Data Clock Duty Cycle			40	40	% (min)
				60	60	% (max)
t_C	Conversion Time	12-Bit + Sign or 12-Bit	44(t_{CK})	44(t_{CK})	44(t_{CK})	(max)
				5.5	8.8	μs (max)
		8-Bit + Sign or 8-Bit	21(t_{CK})	21(t_{CK})	21(t_{CK})	(max)
				2.625	4.2	μs (max)

AC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = V_{A+} = V_{D+} = +5.0 V_{DC}$, $V_{REF+} = +4.096 V_{DC}$, $V_{REF-} = 0 V_{DC}$, 12-bit + sign conversion mode, $t_r = t_f = 3 \text{ ns}$, $f_{CK} = f_{SK} = 8 \text{ MHz}$ for the ADC12H030, ADC12H032, ADC12H034 and ADC12H038, $f_{CK} = f_{SK} = 5 \text{ MHz}$ for the ADC12030, ADC12032, ADC12034 and ADC12038, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Bold-face limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ\text{C}$. (Note 17)

Symbol	Parameter	Conditions	Typical (Note 10)	ADC12H030/2/4/8	ADC12030/2/4/8	Units (Limits)	
				Limits (Note 11)	Limits (Note 11)		
t_A	Acquisition Time (Note 19)	6 Cycles Programmed	$6(t_{CK})$	6(t_{CK})	6(t_{CK})	(min)	
				7(t_{CK})	7(t_{CK})	(max)	
			0.75	1.2	μs (min)		
			0.875	1.4	μs (max)		
			10 Cycles Programmed	$10(t_{CK})$	10(t_{CK})	10(t_{CK})	(min)
					11(t_{CK})	11(t_{CK})	(max)
				1.25	2.0	μs (min)	
				1.375	2.2	μs (max)	
		18 Cycles Programmed	$18(t_{CK})$	18(t_{CK})	18(t_{CK})	(min)	
				19(t_{CK})	19(t_{CK})	(max)	
				2.25	3.6	μs (min)	
				2.375	3.8	μs (max)	
34 Cycles Programmed	$34(t_{CK})$	34(t_{CK})	34(t_{CK})	(min)			
		35(t_{CK})	35(t_{CK})	(max)			
		4.25	6.8	μs (min)			
		4.375	7.0	μs (max)			
t_{CKAL}	Self-Calibration Time		$4944(t_{CK})$	4944(t_{CK})	4944(t_{CK})	(max)	
				618.0	988.8	μs (max)	
t_{AZ}	Auto-Zero Time		$76(t_{CK})$	76(t_{CK})	76(t_{CK})	(max)	
				9.5	15.2	μs (max)	
t_{SYNC}	Self-Calibration or Auto-Zero Synchronization Time from DOR		$2(t_{CK})$	2(t_{CK})	2(t_{CK})	(min)	
				3(t_{CK})	3(t_{CK})	(max)	
			0.250	0.40	μs (min)		
			0.375	0.60	μs (max)		
$\overline{t_{DOR}}$	DOR High Time when \overline{CS} is Low Continuously for Read Data and Software Power Up/Down		$9(t_{SK})$	9(t_{SK})	9(t_{SK})	(max)	
				1.125	1.8	μs (max)	
$\overline{t_{CONV}}$	CONV Valid Data Time		$8(t_{SK})$	8(t_{SK})	8(t_{SK})	(max)	
				1.0	1.6	μs (max)	

AC Electrical Characteristics

The following specifications apply for $V^+ = V_{A+} = V_{D+} = +5.0 V_{DC}$, $V_{REF+} = +4.096 V_{DC}$, $V_{REF-} = 0 V_{DC}$, 12-bit + sign conversion mode, $t_r = t_f = 3 \text{ ns}$, $f_{CK} = f_{SK} = 8 \text{ MHz}$ for the ADC12H030, ADC12H032, ADC12H034 and ADC12H038, $f_{CK} = f_{SK} = 5 \text{ MHz}$ for the ADC12030, ADC12032, ADC12034 and ADC12038, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Bold-face limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ\text{C}$. (Note 17)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
t_{HPU}	Hardware Power-Up Time, Time from PD Falling Edge to EOC Rising Edge		140	250	μs (max)
t_{SPU}	Software Power-Up Time, Time from Serial Data Clock Falling Edge to		140	250	μs (max)

AC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = V_{A+} = V_{D+} = +5.0 V_{DC}$, $V_{REF+} = +4.096 V_{DC}$, $V_{REF-} = 0 V_{DC}$, 12-bit + sign conversion mode, $t_r = t_f = 3 \text{ ns}$, $f_{CK} = f_{SK} = 8 \text{ MHz}$ for the ADC12H030, ADC12H032, ADC12H034 and ADC12H038, $f_{CK} = f_{SK} = 5 \text{ MHz}$ for the ADC12030, ADC12032, ADC12034 and ADC12038, $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.048V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Bold-face limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J = 25^\circ\text{C}$. (Note 17)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
	EOC Rising Edge				
t_{ACC}	Access Time Delay from \overline{CS} Falling Edge to DO Data Valid		20	50	ns (max)
t_{SET-UP}	Set-Up Time of \overline{CS} Falling Edge to Serial Data Clock Rising Edge			30	ns (min)
t_{DELAY}	Delay from SCLK Falling Edge to \overline{CS} Falling Edge		0	5	ns (min)
t_{1H}, t_{0H}	Delay from \overline{CS} Rising Edge to DO TRI-STATE	$R_L = 3k, C_L = 100 \text{ pF}$	40	100	ns (max)
t_{HDI}	DI Hold Time from Serial Data Clock Rising Edge		5	15	ns (min)
t_{SDI}	DI Set-Up Time from Serial Data Clock Rising Edge		5	10	ns (min)
t_{HDO}	DO Hold Time from Serial Data Clock Falling Edge	$R_L = 3k, C_L = 100 \text{ pF}$	25	50 5	ns (max) ns (min)
t_{DDO}	Delay from Serial Data Clock Falling Edge to DO Data Valid		35	50	ns (max)
t_{RDO}	DO Rise Time, TRI-STATE to High DO Rise Time, Low to High	$R_L = 3k, C_L = 100 \text{ pF}$	10 10	30 30	ns (max) ns (max)
t_{FDO}	DO Fall Time, TRI-STATE to Low DO Fall Time, High to Low	$R_L = 3k, C_L = 100 \text{ pF}$	12 12	30 30	ns (max) ns (max)
t_{CD}	Delay from \overline{CS} Falling Edge to \overline{DOR} Falling Edge		25	45	ns (max)
t_{SD}	Delay from Serial Data Clock Falling Edge to \overline{DOR} Rising Edge		25	45	ns (max)
C_{IN}	Capacitance of Logic Inputs		10		pF
C_{OUT}	Capacitance of Logic Outputs		20		pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

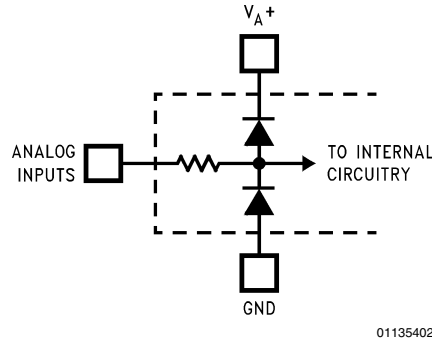
Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies ($V_{IN} < GND$ or $V_{IN} > V_{A+}$ or V_{D+}), the current at that pin should be limited to 30 mA. The 120 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 30 mA to four.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} , θ_{JA} and the ambient temperature, T_A . The maximum allowable power dissipation at any temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 150^\circ\text{C}$. The typical thermal resistance (θ_{JA}) of these parts when board mounted follow:

Part Number	Thermal Resistance θ_{JA}
ADC12H030CIWM, ADC12030CIWM	70°C/W
ADC12H032CIWM, ADC12032CIWM	64°C/W
ADC12H034CIN, ADC12034CIN	42°C/W
ADC12H034CIWM, ADC12034CIWM	57°C/W
ADC12H034CIMSA	97°C/W
ADC12H038CIWM, ADC12038CIWM	50°C/W

- Note 5:** The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.
- Note 6:** See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.
- Note 7:** Two on-chip diodes are tied to each analog input through a series resistor as shown below. Input voltage magnitude up to 5V above V_{A+} or 5V below GND will not damage this device. However, errors in the A/D conversion can occur (if these diodes are forward biased by more than 50 mV) if the input voltage magnitude of selected or unselected analog input go above V_{A+} or below GND by more than 50 mV. As an example, if V_{A+} is 4.5 V_{DC} , full-scale input voltage must be $\leq 4.5 V_{DC}$ to ensure accurate conversions.



- Note 8:** To guarantee accuracy, it is required that the V_{A+} and V_{D+} be connected together to the same power supply with separate bypass capacitors at each V^+ pin.
- Note 9:** With the test condition for V_{REF} ($V_{REF+} - V_{REF-}$) given as +4.096V, the 12-bit LSB is 1.0 mV and the 8-bit LSB is 16.0 mV.
- Note 10:** Typicals are at $T_J = T_A = 25^\circ\text{C}$ and represent most likely parametric norm.
- Note 11:** Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
- Note 12:** Positive integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative integral linearity error, the straight line passes through negative full-scale and zero (see Figures 2, 3).
- Note 13:** Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the worst-case value of the code transitions between 1 to 0 and 0 to +1 (see Figure 4).
- Note 14:** Total unadjusted error includes offset, full-scale, linearity and multiplexer errors.
- Note 15:** The DC common-mode error is measured in the differential multiplexer mode with the assigned positive and negative input channels shorted together.
- Note 16:** Channel leakage current is measured after the channel selection.
- Note 17:** Timing specifications are tested at the TTL logic levels, $V_{IL} = 0.4\text{V}$ for a falling edge and $V_{IH} = 2.4\text{V}$ for a rising edge. TRI-STATE output voltage is forced to 1.4V.
- Note 18:** The ADC12030 family's self-calibration technique ensures linearity and offset errors as specified, but noise inherent in the self-calibration process will result in a maximum repeatability uncertainty of 0.2 LSB.
- Note 19:** If SCLK and CCLK are driven from the same clock source, then t_A is 6, 10, 18 or 34 clock periods minimum and maximum.
- Note 20:** The "12-Bit Conversion of Offset" and "12-Bit Conversion of Full-Scale" modes are intended to test the functionality of the device. Therefore, the output data from these modes are not an indication of the accuracy of a conversion result.

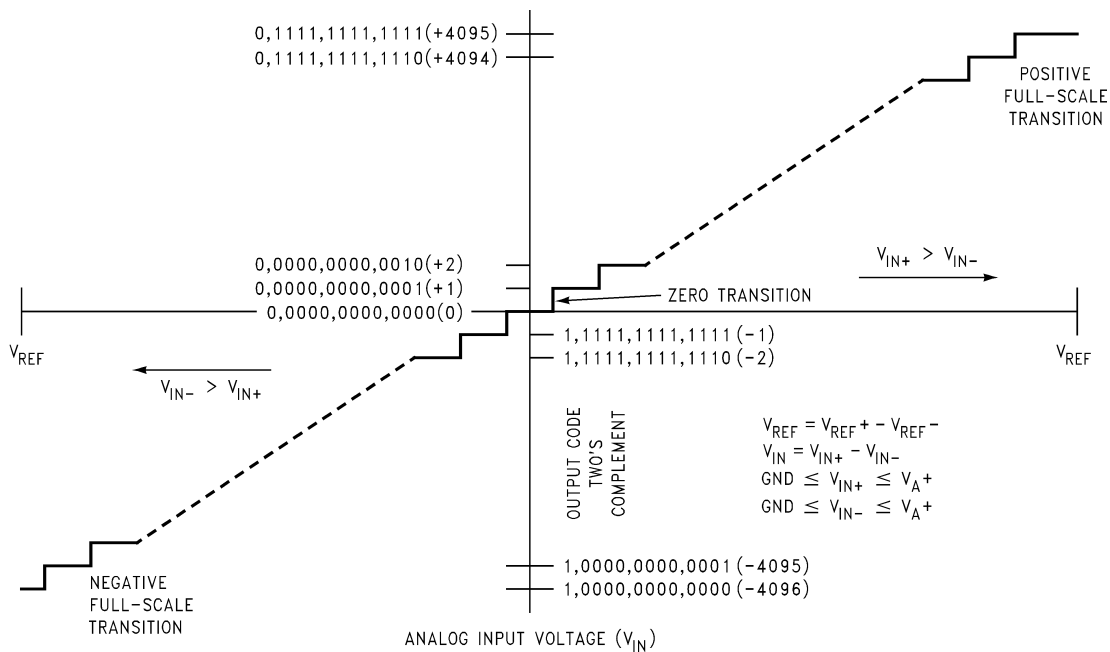
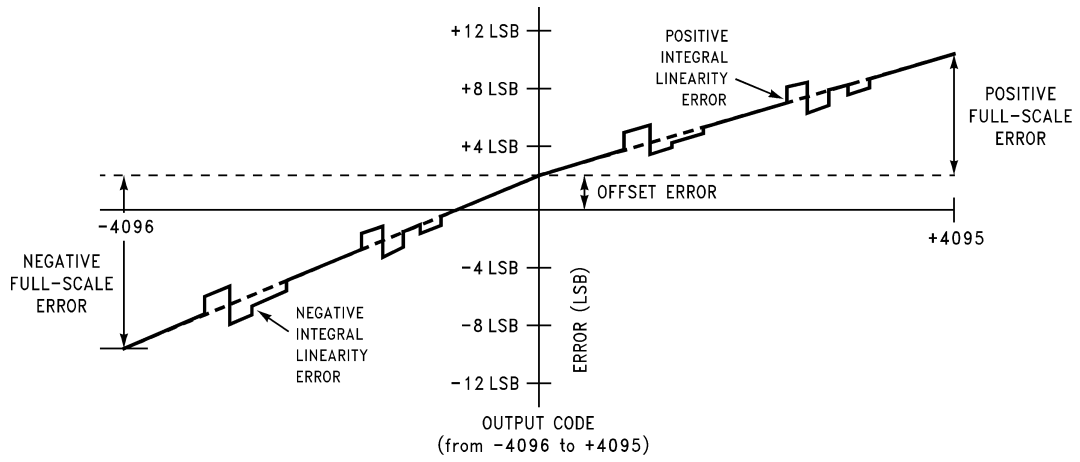
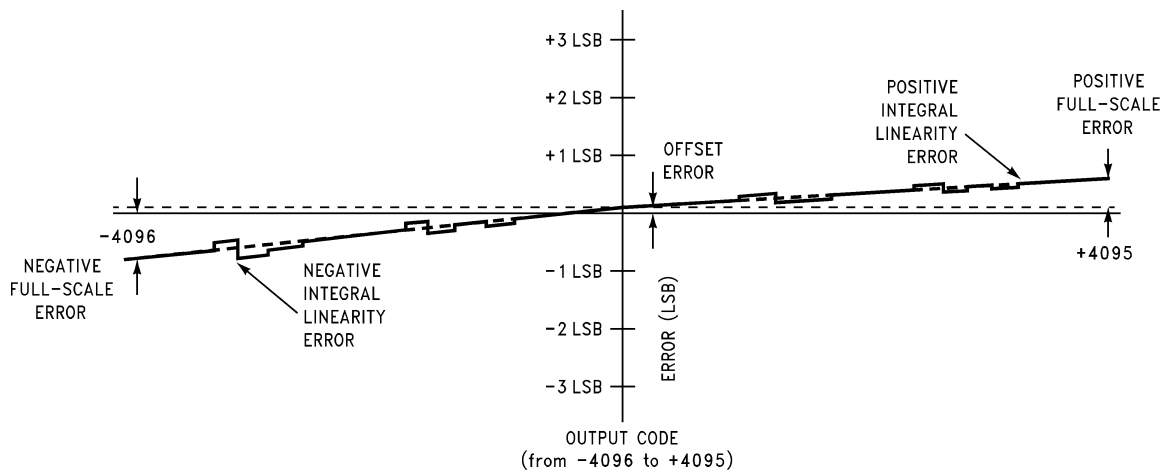


FIGURE 1. Transfer Characteristic



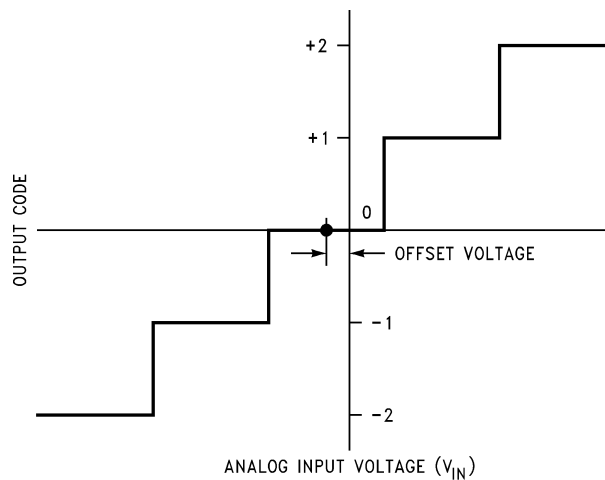
01135411

FIGURE 2. Simplified Error Curve vs Output Code without Auto-Calibration or Auto-Zero Cycles



01135412

FIGURE 3. Simplified Error Curve vs Output Code after Auto-Calibration Cycle

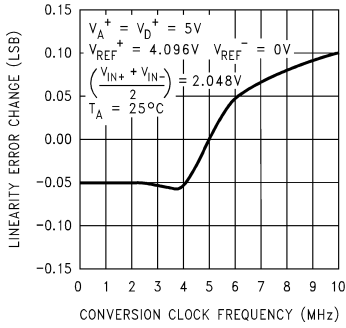


01135413

FIGURE 4. Offset or Zero Error Voltage

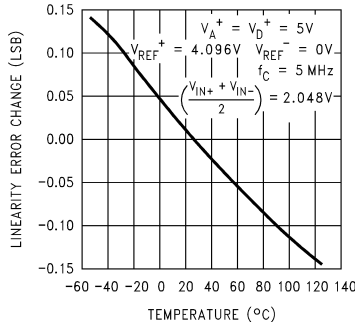
Typical Performance Characteristics The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign mode is equal to or better than shown. (Note 9)

Linearity Error Change vs Clock Frequency



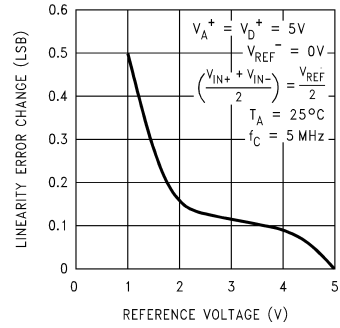
01135453

Linearity Error Change vs Temperature



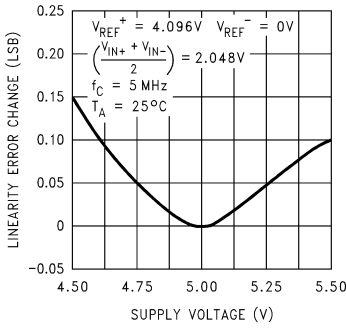
01135454

Linearity Error Change vs Reference Voltage



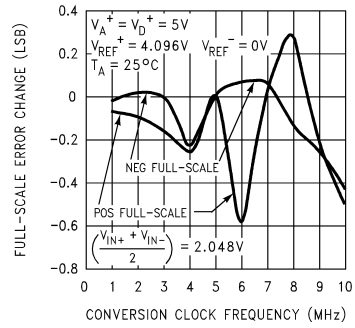
01135455

Linearity Error Change vs Supply Voltage



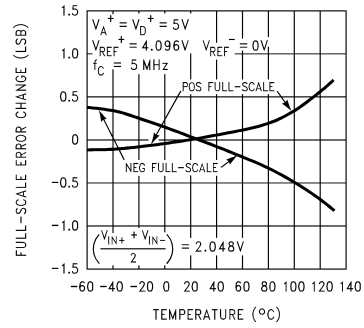
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Full-Scale Error Change vs Clock Frequency



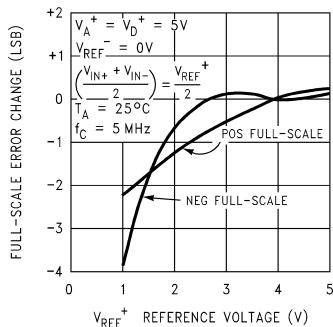
01135457

Full-Scale Error Change vs Temperature



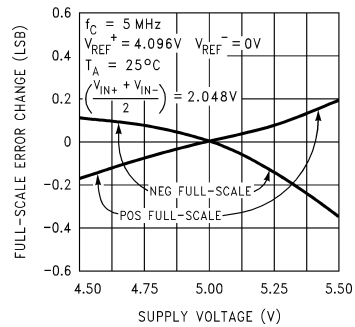
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Full-Scale Error Change vs Reference Voltage



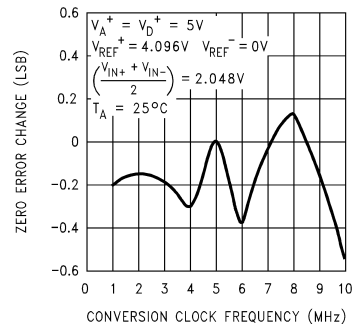
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Full-Scale Error Change vs Supply Voltage



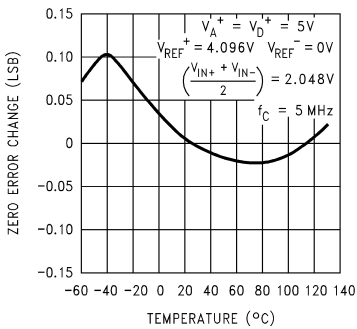
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Zero Error Change vs Clock Frequency



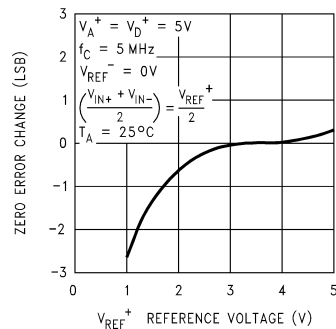
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Zero Error Change vs Temperature



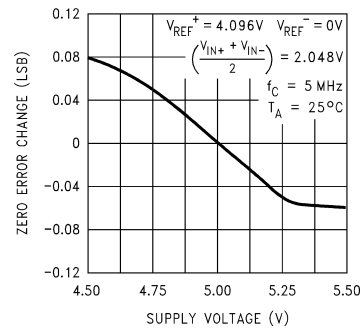
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Zero Error Change vs Reference Voltage



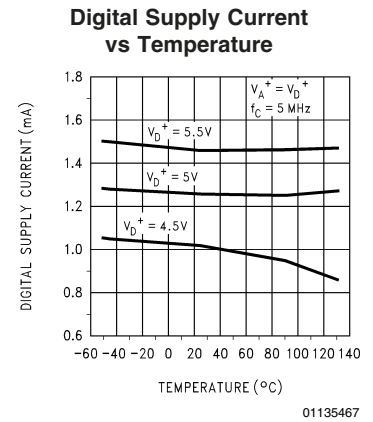
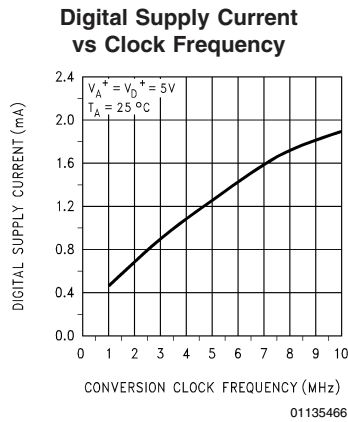
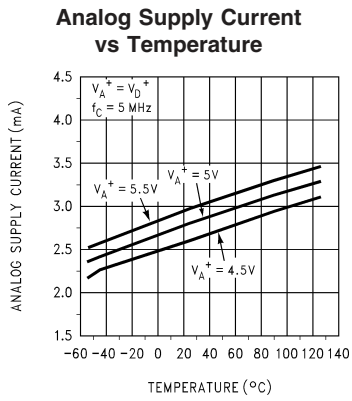
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Zero Error Change vs Supply Voltage

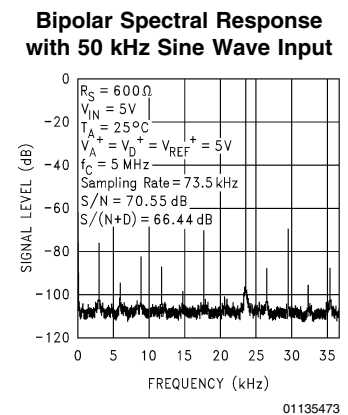
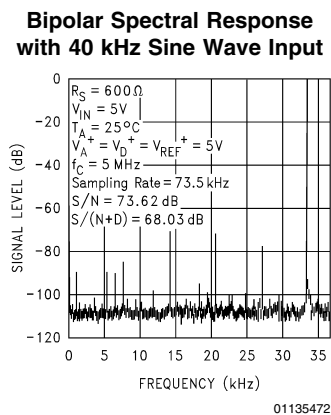
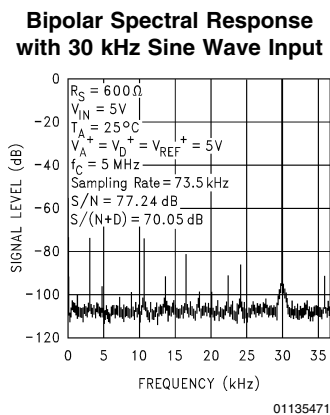
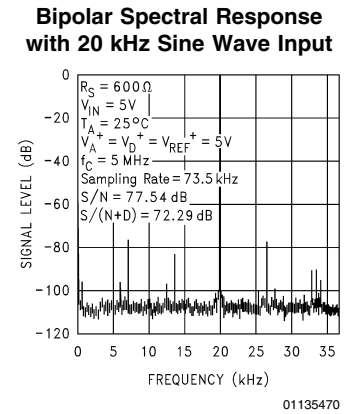
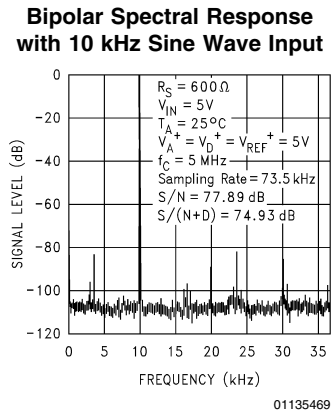
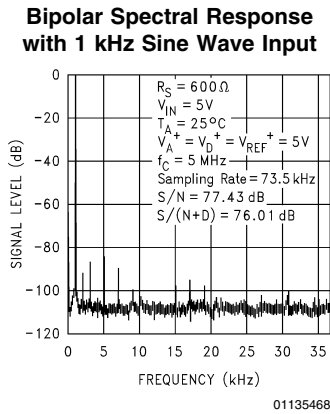


01135464

Typical Performance Characteristics The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign mode is equal to or better than shown. (Note 9) (Continued)

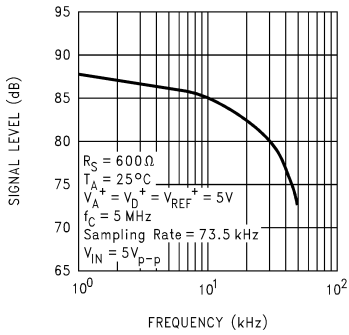


Typical Dynamic Performance Characteristics The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified.

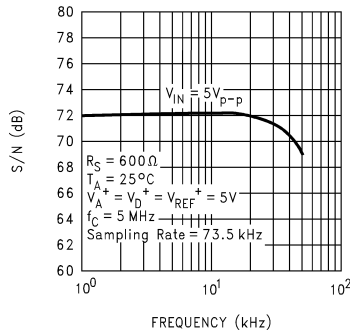


Typical Dynamic Performance Characteristics The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. (Continued)

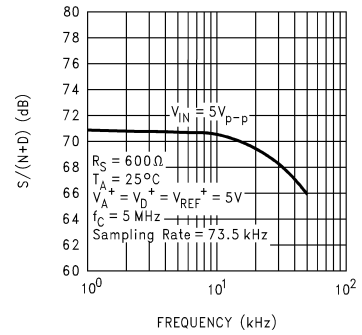
Bipolar Spurios Free Dynamic Range



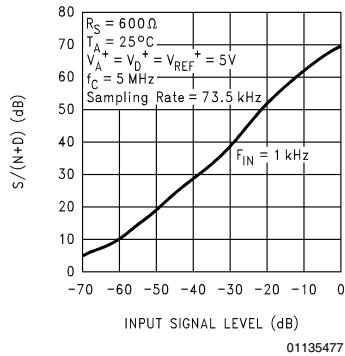
Unipolar Signal-to-Noise Ratio vs Input Frequency



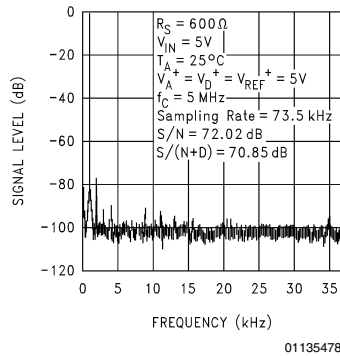
Unipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



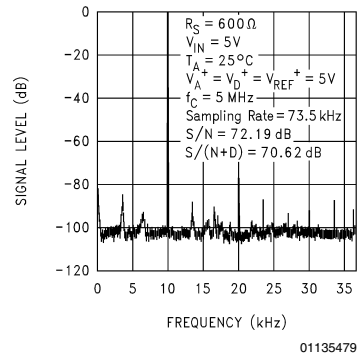
Unipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



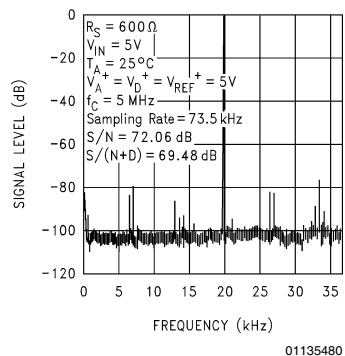
Unipolar Spectral Response with 1 kHz Sine Wave Input



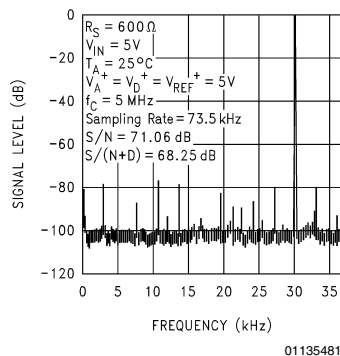
Unipolar Spectral Response with 10 kHz Sine Wave Input



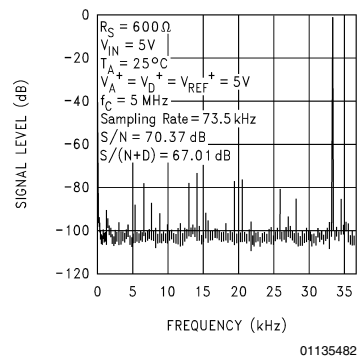
Unipolar Spectral Response with 20 kHz Sine Wave Input



Unipolar Spectral Response with 30 kHz Sine Wave Input

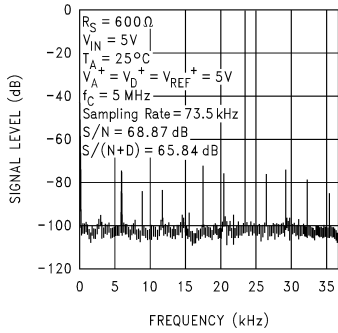


Unipolar Spectral Response with 40 kHz Sine Wave Input



Typical Dynamic Performance Characteristics The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. (Continued)

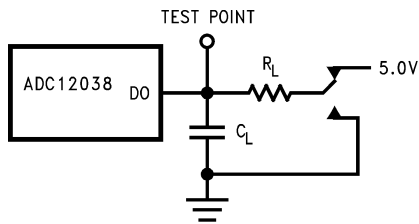
Unipolar Spectral Response with 50 kHz Sine Wave Input



01135483

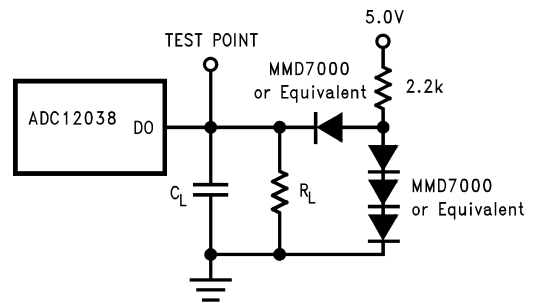
Test Circuits

DO "TRI-STATE" (t_{1H} , t_{0H})



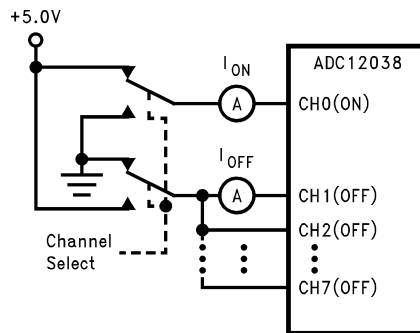
01135403

DO except "TRI-STATE"



01135404

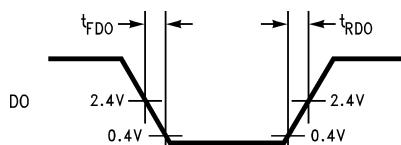
Leakage Current



01135405

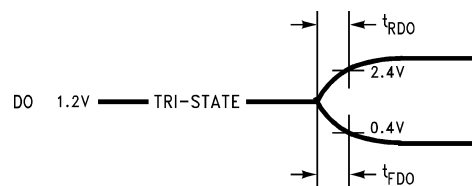
Timing Diagrams

DO Falling and Rising Edge



01135418

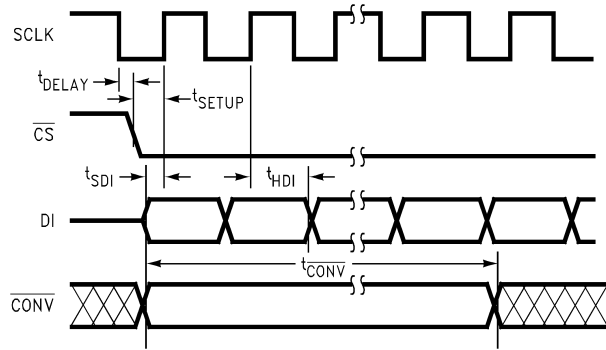
DO "TRI-STATE" Falling and Rising Edge



01135419

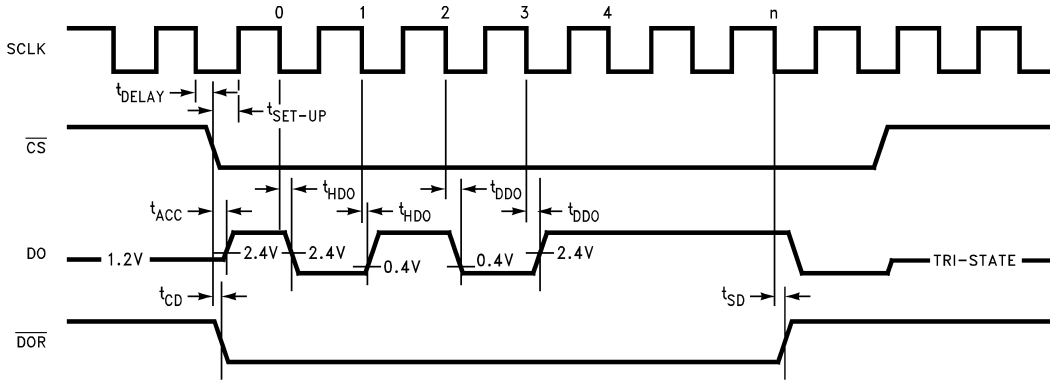
Timing Diagrams (Continued)

DI Data Input Timing



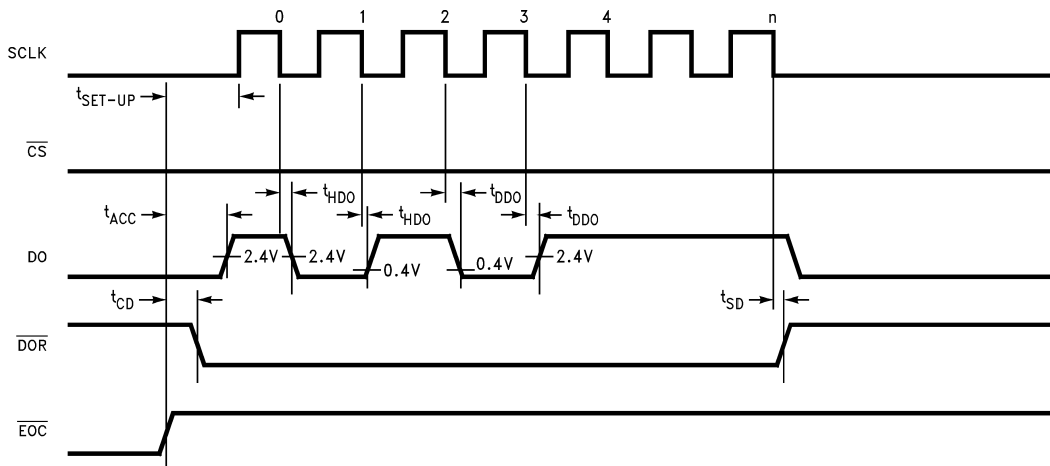
01135420

DO Data Output Timing Using CS



01135421

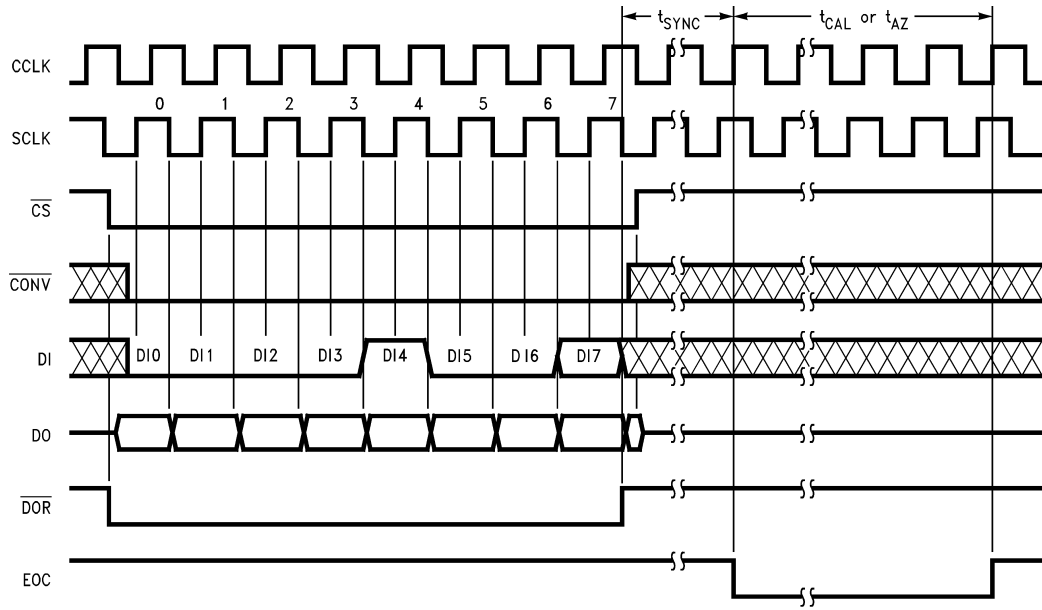
DO Data Output Timing with CS Continuously Low



01135422

Timing Diagrams (Continued)

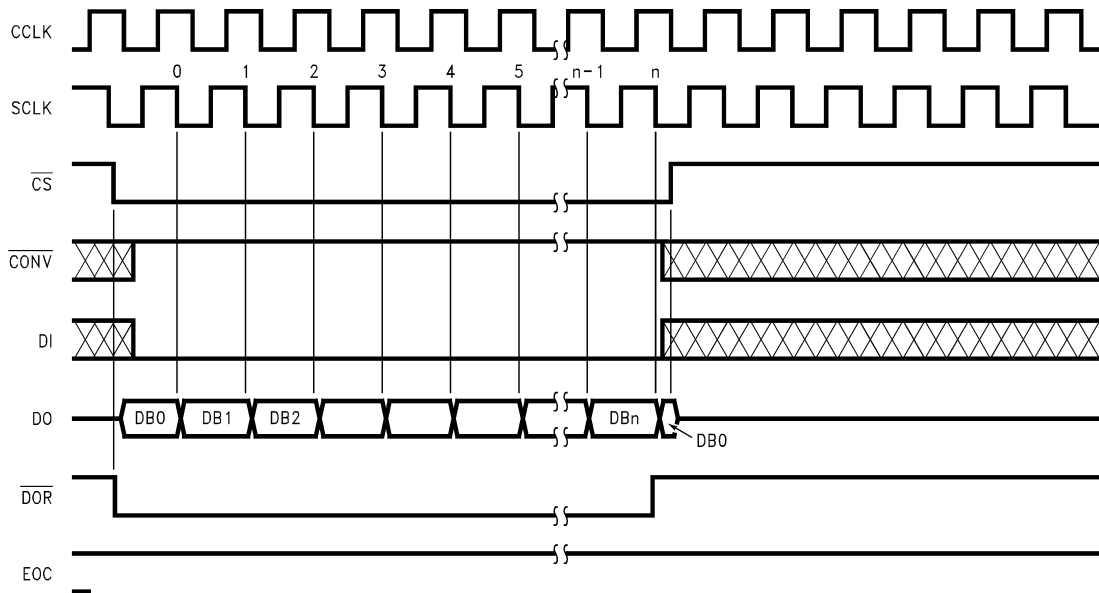
ADC12038 Auto Cal or Auto Zero



01135423

Note: DO output data is not valid during this cycle.

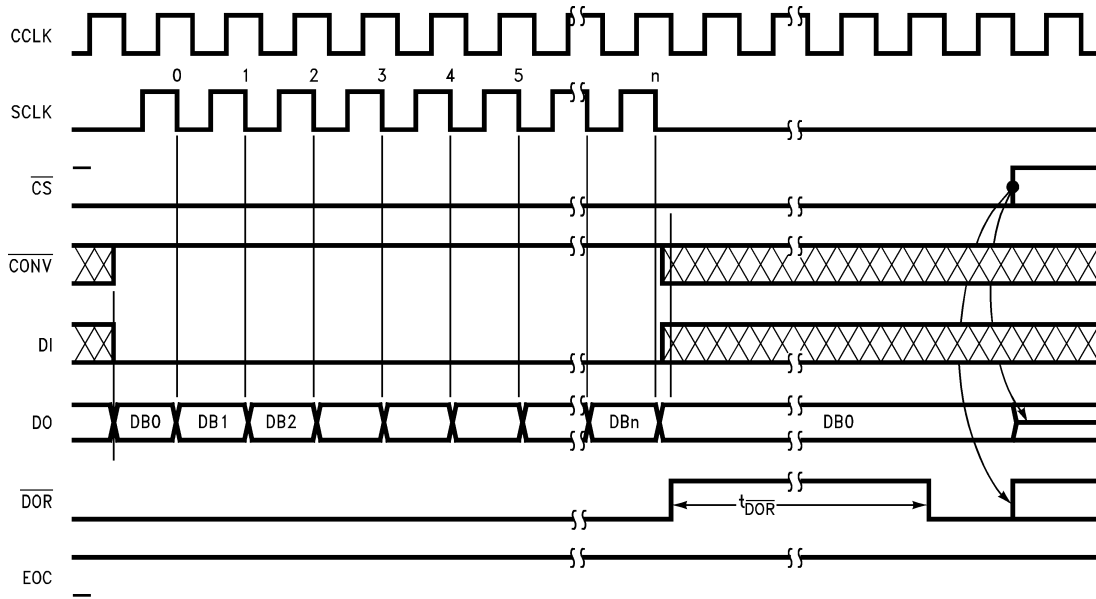
ADC12038 Read Data without Starting a Conversion Using CS



01135424

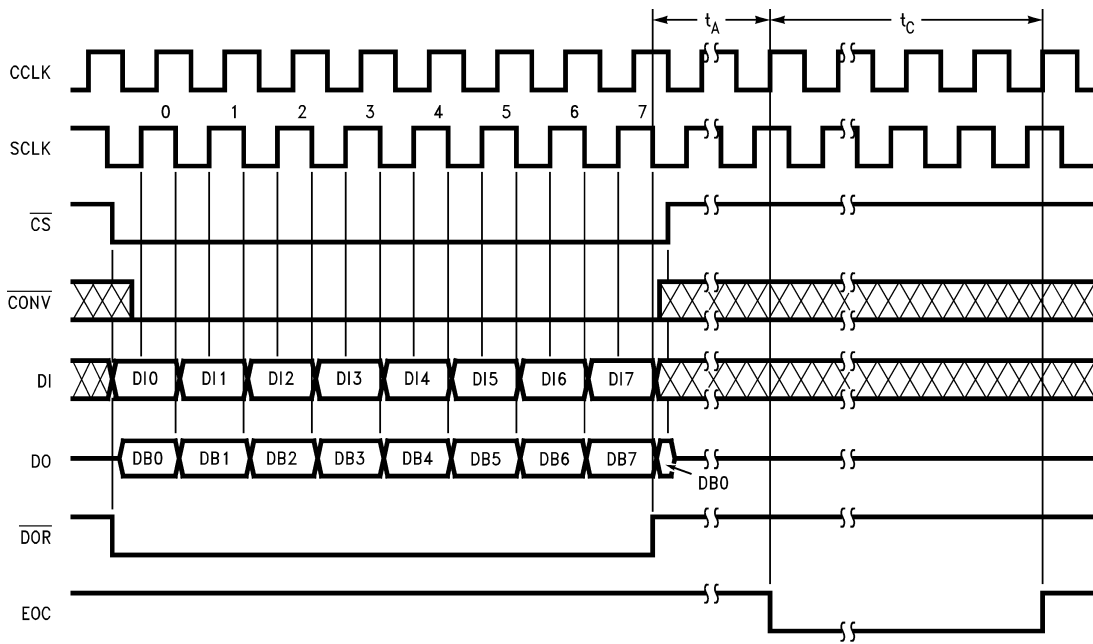
Timing Diagrams (Continued)

ADC12038 Read Data without Starting a Conversion with \overline{CS} Continuously Low



01135425

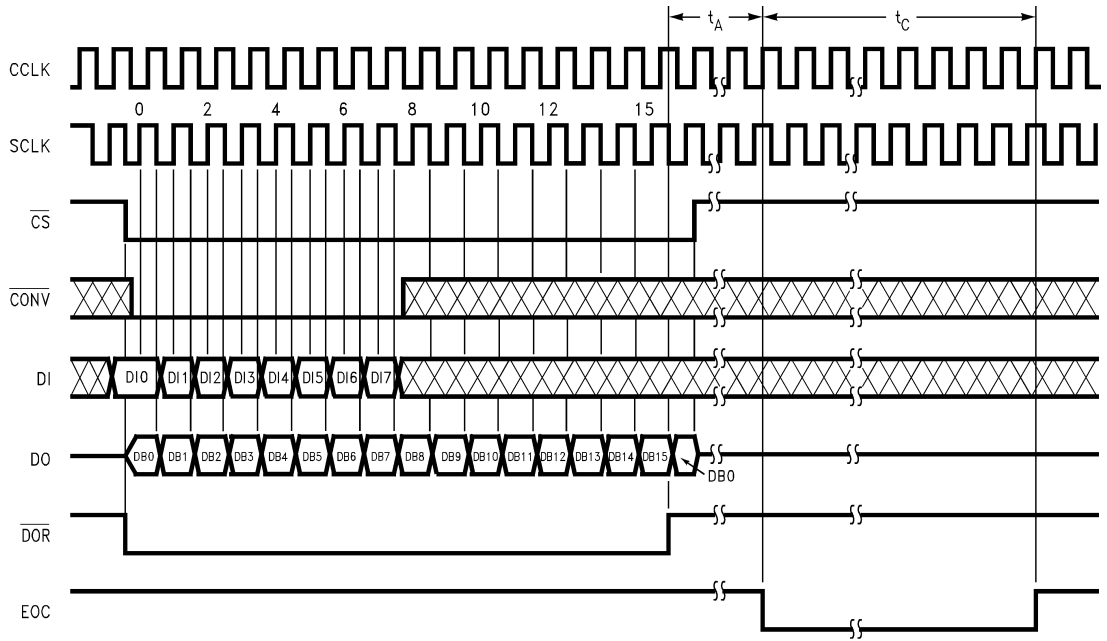
ADC12038 Conversion Using \overline{CS} with 8-Bit Digital Output Format



01135426

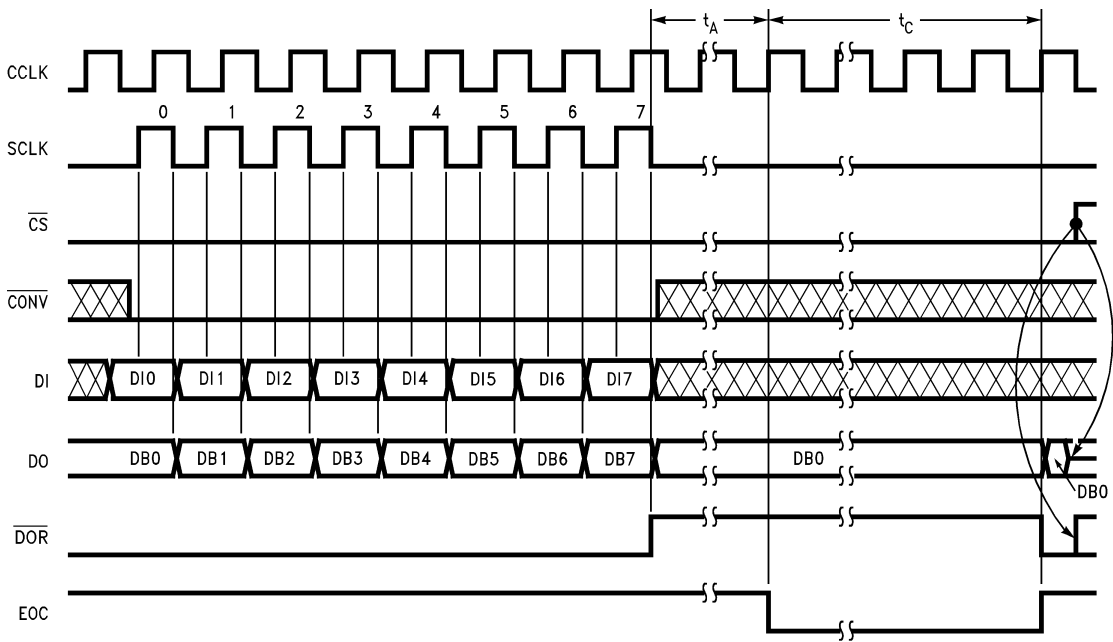
Timing Diagrams (Continued)

ADC12038 Conversion Using \overline{CS} with 16-Bit Digital Output Format



01135451

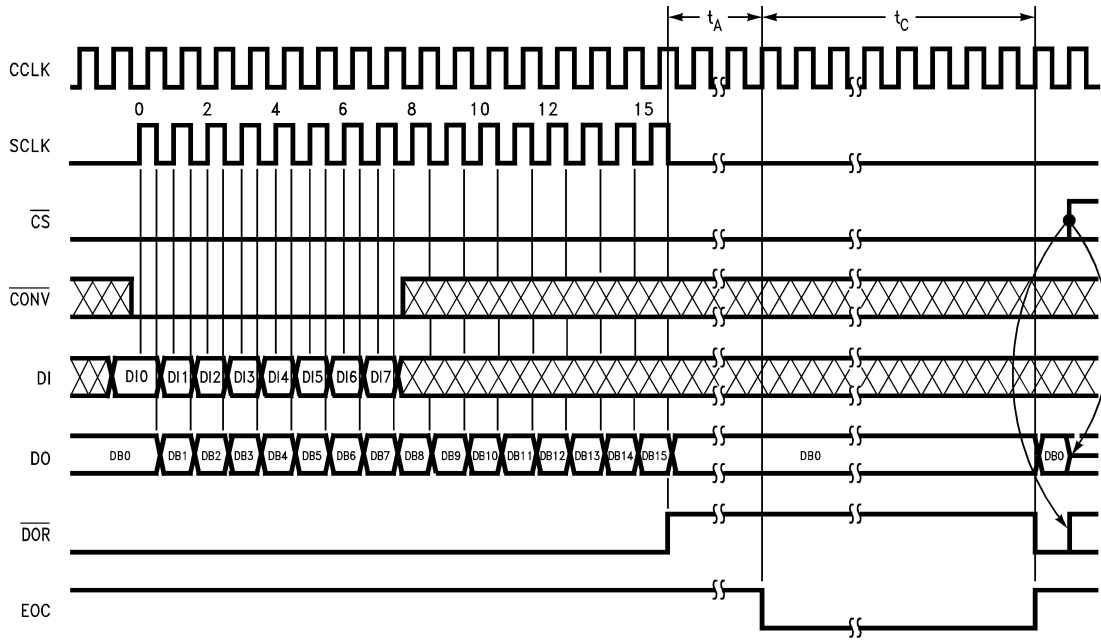
ADC12038 Conversion with \overline{CS} Continuously Low and 8-Bit Digital Output Format



01135428

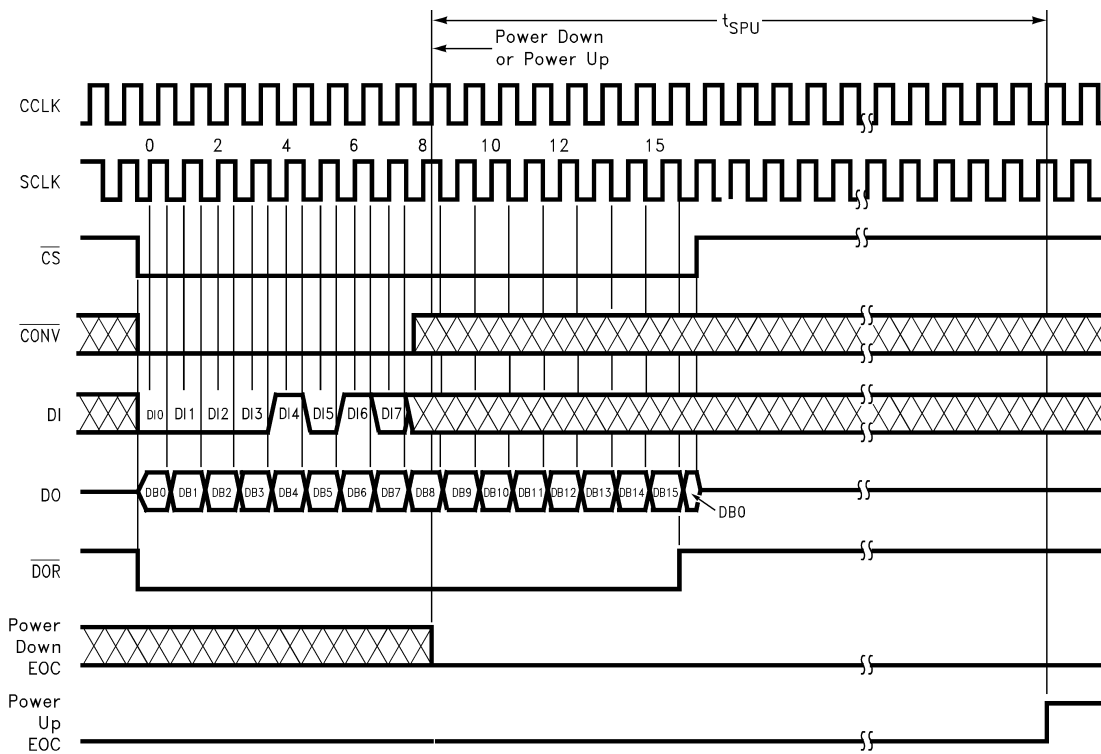
Timing Diagrams (Continued)

ADC12038 Conversion with \overline{CS} Continuously Low and 16-Bit Digital Output Format



01135429

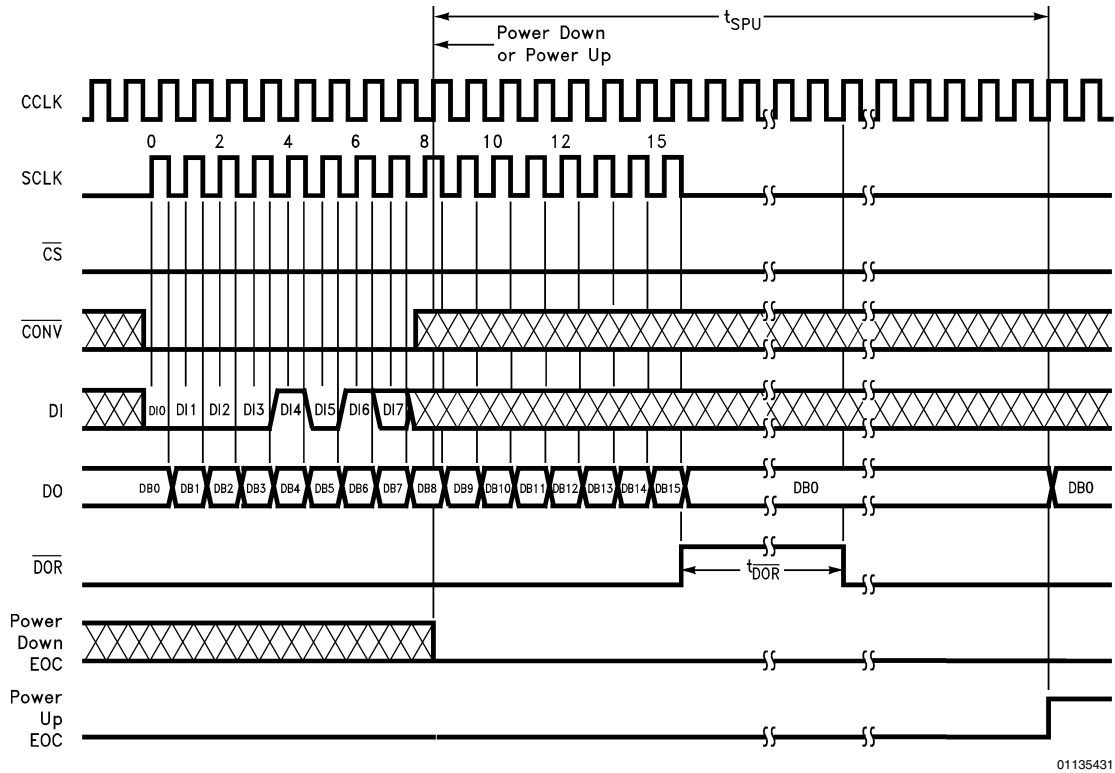
ADC12038 Software Power Up/Down Using \overline{CS} with 16-Bit Digital Output Format



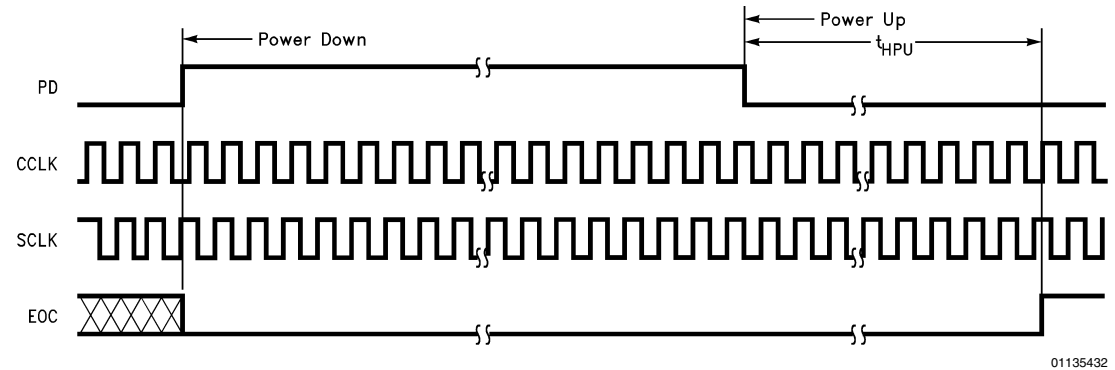
01135452

Timing Diagrams (Continued)

ADC12038 Software Power Up/Down with \overline{CS} Continuously Low and 16-Bit Digital Output Format



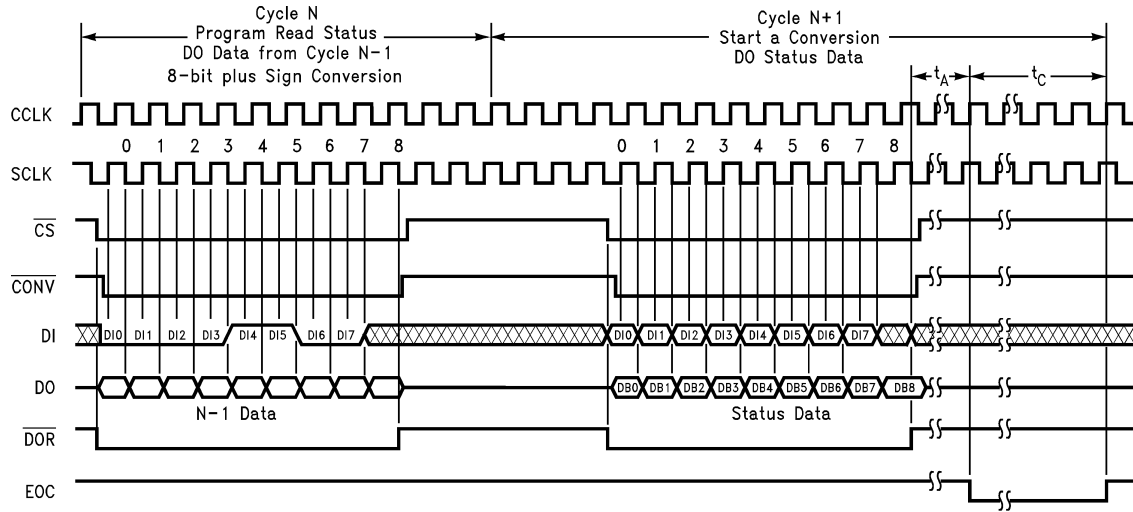
ADC12038 Hardware Power Up/Down



Note: Hardware power up/down may occur at any time. If PD is high while a conversion is in progress that conversion will be corrupted and erroneous data will be stored in the output shift register.

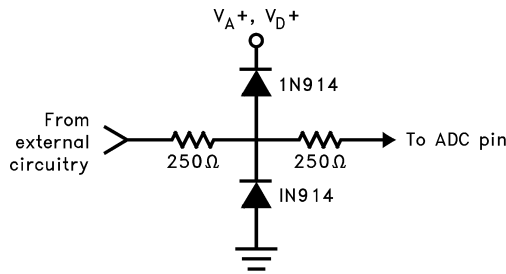
Timing Diagrams (Continued)

ADC12038 Configuration Modification—Example of a Status Read



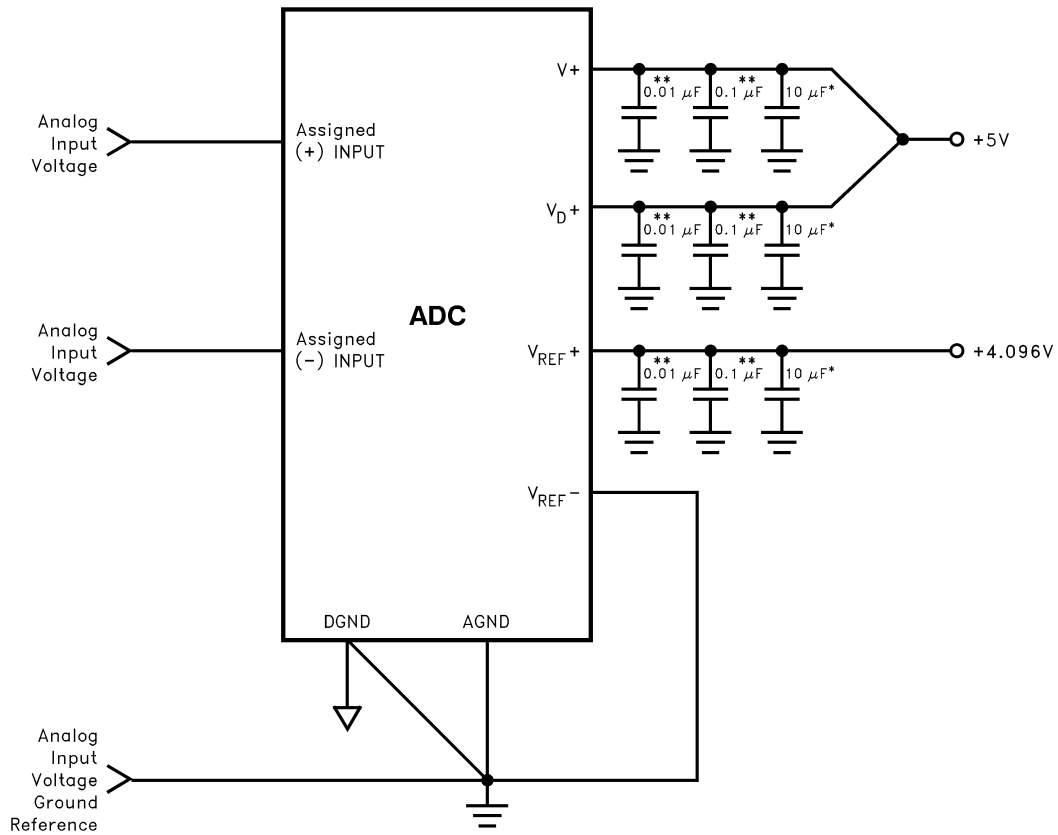
01135433

Note: In order for all 9 bits of Status Information to be accessible, the last conversion programmed before Cycle N needs to have a resolution of 8 bits plus sign, 12 bits, 12 bits plus sign, or greater.



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FIGURE 5. Protecting the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 Analog Pins



*Tantalum
 **Monolithic Ceramic or better

01135435

FIGURE 6. Recommended Power Supply Bypassing and Grounding

Tables

TABLE 1. Data Out Formats

DO Formats		DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15	DB16
with Sign	17 Bits	X	X	X	X	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB
	13 Bits	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB				
	9 Bits	Sign	MSB	6	5	4	3	2	1	LSB								
LSB First	17 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign	X	X	X	X
	13 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign				
	9 Bits	LSB	1	2	3	4	5	6	MSB	Sign								

Tables (Continued)

TABLE 1. Data Out Formats (Continued)

DO Formats			DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15	DB16	
without Sign	MSB First	16 Bits	0	0	0	0	MSB	10	9	8	7	6	5	4	3	2	1	LSB		
		12 Bits	MSB	10	9	8	7	6	5	4	3	2	1	LSB						
		8 Bits	MSB	6	5	4	3	2	1	LSB										
	LSB First	16 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	0	0	0	0		
		12 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB						
		8 Bits	LSB	1	2	3	4	5	6	MSB										

X = High or Low state.

TABLE 2. ADC12038 Multiplexer Addressing

MUX Address				Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2									A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
D10	D11	D12	D13	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM	A/DIN1	A/DIN2	MUXOUT1	MUXOUT2	
L	L	L	L	+	-								+	-	CH0	CH1	Differential
L	L	L	H			+	-						+	-	CH2	CH3	
L	L	H	L					+	-				+	-	CH4	CH5	
L	L	H	H							+	-		+	-	CH6	CH7	
L	H	L	L	-	+								-	+	CH0	CH1	
L	H	L	H			-	+						-	+	CH2	CH3	
L	H	H	L					-	+				-	+	CH4	CH5	
L	H	H	H							-	+		-	+	CH6	CH7	
H	L	L	L	+								-	+	-	CH0	COM	Single-Ended
H	L	L	H			+						-	+	-	CH2	COM	
H	L	H	L					+				-	+	-	CH4	COM	
H	L	H	H							+		-	+	-	CH6	COM	
H	H	L	L		+							-	+	-	CH1	COM	
H	H	L	H				+					-	+	-	CH3	COM	
H	H	H	L						+			-	+	-	CH5	COM	
H	H	H	H							+		-	+	-	CH7	COM	

TABLE 3. ADC12034 Multiplexer Addressing

MUX Address			Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2					A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	DI2	CH0	CH1	CH2	CH3	COM	A/DIN1	A/DIN2	MUXOUT1	MUXOUT2	
L	L	L	+	-				+	-	CH0	CH1	Differential
L	L	H			+	-		+	-	CH2	CH3	
L	H	L	-	+				-	+	CH0	CH1	
L	H	H			-	+		-	+	CH2	CH3	
H	L	L	+				-	+	-	CH0	COM	Single-Ended
H	L	H			+		-	+	-	CH2	COM	
H	H	L		+			-	+	-	CH1	COM	
H	H	H				+	-	+	-	CH3	COM	

TABLE 4. ADC12032 and ADC12030 Multiplexer Addressing

MUX Address		Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2			A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	DI1	CH0	CH1	COM	A/DIN1	A/DIN2	MUXOUT1	MUXOUT2	
L	L	+	-		+	-	CH0	CH1	Differential
L	H	-	+		-	+	CH0	CH1	
H	L	+		-	+	-	CH0	COM	Single-Ended
H	H		+	-	+	-	CH1	COM	

Note: ADC12030 and ADC12H030 do not have A/DIN1, A/DIN2, MUXOUT1 and MUXOUT2 pins.

TABLE 5. Mode Programming

ADC12038	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7	Mode Selected (Current)	DO Format (next Conversion Cycle)
ADC12034	DI0	DI1	DI2		DI3	DI4	DI5	DI6		
ADC12030 and ADC12032	DI0	DI1			DI2	DI3	DI4	DI5		
	See Tables 2, 3 or Table 4				L	L	L	L	12 Bit Conversion	12 or 13 Bit MSB First
	See Tables 2, 3 or Table 4				L	L	L	H	12 Bit Conversion	16 or 17 Bit MSB First
	See Tables 2, 3 or Table 4				L	L	H	L	8 Bit Conversion	8 or 9 Bit MSB First
	L	L	L	L	L	L	H	H	12 Bit Conversion of Full-Scale	12 or 13 Bit MSB First
	See Tables 2, 3 or Table 4				L	H	L	L	12 Bit Conversion	12 or 13 Bit LSB First
	See Tables 2, 3 or Table 4				L	H	L	H	12 Bit Conversion	16 or 17 Bit LSB First
	See Tables 2, 3 or Table 4				L	H	H	L	8 Bit Conversion	8 or 9 Bit LSB First
	L	L	L	L	L	H	H	H	12 Bit Conversion of Offset	12 or 13 Bit LSB First
	L	L	L	L	H	L	L	L	Auto Cal	No Change
	L	L	L	L	H	L	L	H	Auto Zero	No Change
	L	L	L	L	H	L	H	L	Power Up	No Change
	L	L	L	L	H	L	H	H	Power Down	No Change
	L	L	L	L	H	H	L	L	Read Status Register	No Change
	L	L	L	L	H	H	L	H	Data Out without Sign	No Change
	H	L	L	L	H	H	L	H	Data Out with Sign	No Change
	L	L	L	L	H	H	H	L	Acquisition Time—6 CCLK Cycles	No Change
	L	H	L	L	H	H	H	L	Acquisition Time—10 CCLK Cycles	No Change
	H	L	L	L	H	H	H	L	Acquisition Time—18 CCLK Cycles	No Change

TABLE 5. Mode Programming (Continued)

ADC12038	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7	Mode Selected (Current)	DO Format (next Conversion Cycle)
ADC12034	DI0	DI1	DI2		DI3	DI4	DI5	DI6		
ADC12030 and ADC12032	DI0	DI1			DI2	DI3	DI4	DI5		
	H	H	L	L	H	H	H	L	Acquisition Time—34 CCLK Cycles	No Change
	L	L	L	L	H	H	H	H	User Mode	No Change
	H	X	X	X	H	H	H	H	Test Mode (CH1–CH7 become Active Outputs)	No Change

Note: The A/D powers up with no Auto Cal, no Auto Zero, 10 CCLK acquisition time, 12-bit + sign conversion, power up, 12- or 13-bit MSB first, and user mode.
X = Don't Care

TABLE 6. Conversion/Read Data Only Mode Programming

\overline{CS}	\overline{CONV}	PD	Mode
L	L	L	See Table 5 for Mode
L	H	L	Read Only (Previous DO Format). No Conversion.
H	X	L	Idle
X	X	H	Power Down

X = Don't Care

TABLE 7. Status Register

Status Bit Location	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8
Status Bit	PU	PD	Cal	8 or 9	12 or 13	16 or 17	Sign	Justification	Test Mode
Function	Device Status			DO Output Format Status					
	“High” indicates a Power Up Sequence is in progress	“High” indicates a Power Down Sequence is in progress	“High” indicates an Auto-Cal Sequence is in progress	“High” indicates an 8 or 9 bit format	“High” indicates a 12 or 13 bit format	“High” indicates a 16 or 17 bit format	“High” indicates that the sign bit is included. When “Low” the sign bit is not included.	When “High” the conversion result will be output MSB first. When “Low” the result will be output LSB first.	When “High” the device is in test mode. When “Low” the device is in user mode.

Application Hints

1.0 DIGITAL INTERFACE

1.1 Interface Concepts

The example in *Figure 7* shows a typical sequence of events after the power is applied to the ADC12030/2/4/8:

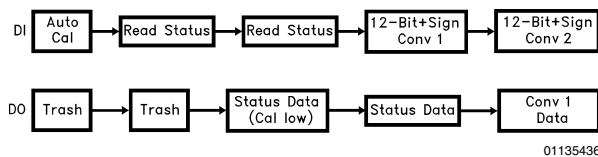


FIGURE 7. Typical Power Supply Power Up Sequence

The first instruction input to the A/D via DI initiates Auto Cal. The data output on DO at that time is meaningless and is completely random. To determine whether the Auto Cal has been completed, a read status instruction is issued to the A/D. Again the data output at that time has no significance

since the Auto Cal procedure modifies the data in the output shift register. To retrieve the status information, an additional read status instruction is issued to the A/D. At this time the status data is available on DO. If the Cal signal in the status word, is low Auto Cal has been completed. Therefore, the next instruction issued can start a conversion. The data output at this time is again status information. To keep noise from corrupting the A/D conversion, status can not be read during a conversion. If \overline{CS} is strobed and is brought low during a conversion, that conversion is prematurely ended. EOC can be used to determine the end of a conversion or the A/D controller can keep track in software of when it would be appropriate to communicate to the A/D again. Once it has been determined that the A/D has completed a conversion, another instruction can be transmitted to the A/D. The data from this conversion can be accessed when the next instruction is issued to the A/D.

Note, when \overline{CS} is low continuously it is important to transmit the exact number of SCLK cycles, as shown in the timing diagrams. Not doing so will desynchronize the serial communication to the A/D. (See Section 1.3.)

Application Hints (Continued)

1.2 Changing Configuration

The configuration of the ADC12030/2/4/8 on power up defaults to 12-bit plus sign resolution, 12- or 13-bit MSB First, 10 CCLK acquisition time, user mode, no Auto Cal, no Auto Zero, and power up mode. Changing the acquisition time and turning the sign bit on and off requires an 8-bit instruction to be issued to the ADC. This instruction will not start a conversion. The instructions that select a multiplexer address and format the output data do start a conversion. *Figure 8* describes an example of changing the configuration of the ADC12030/2/4/8.

During I/O sequence 1, the instruction on DI configures the ADC12030/2/4/8 to do a conversion with 12-bit +sign resolution. Notice that when the 6 CCLK Acquisition and Data Out without Sign instructions are issued to the ADC, I/O sequences 2 and 3, a new conversion is not started. The data output during these instructions is from conversion N which was started during I/O sequence 1. The Configuration Modification timing diagram describes in detail the sequence of events necessary for a Data Out without Sign, Data Out with Sign, or 6/10/18/34 CCLK Acquisition time mode selection. *Table 5* describes the actual data necessary to be input to the ADC to accomplish this configuration modification. The next instruction, shown in *Figure 8*, issued to the A/D starts conversion N+1 with 8 bits of resolution formatted MSB first. Again the data output during this I/O cycle is the data from conversion N.

The number of SCLKs applied to the A/D during any conversion I/O sequence should vary in accord with the data out word format chosen during the previous conversion I/O sequence. The various formats and resolutions available are shown in *Table 1*. In *Figure 8*, since 8-bit without sign MSB first format was chosen during I/O sequence 4, the number of SCLKs required during I/O sequence 5 is 8. In the following I/O sequence the format changes to 12-bit without sign MSB first; therefore the number of SCLKs required during I/O sequence 6 changes accordingly to 12.

1.3 \overline{CS} Low Continuously Considerations

When \overline{CS} is continuously low, it is important to transmit the exact number of SCLK pulses that the ADC expects. Not doing so will desynchronize the serial communications to the ADC. When the supply power is first applied to the ADC, it will expect to see 13 SCLK pulses for each I/O transmission. The number of SCLK pulses that the ADC expects to see is the same as the digital output word length. The digital output word length is controlled by the Data Out (DO) format. The DO format maybe changed any time a conversion is started or when the sign bit is turned on or off. The table below details out the number of clock periods required for different DO formats:

DO Format		Number of SCLKs Expected
8-Bit MSB or LSB First	SIGN OFF	8
	SIGN ON	9
12-Bit MSB or LSB First	SIGN OFF	12
	SIGN ON	13
16-Bit MSB or LSB first	SIGN OFF	16
	SIGN ON	17

If erroneous SCLK pulses desynchronize the communications, the simplest way to recover is by cycling the power supply to the device. Not being able to easily resynchronize the device is a shortcoming of leaving \overline{CS} low continuously. The number of clock pulses required for an I/O exchange may be different for the case when \overline{CS} is left low continuously vs the case when \overline{CS} is cycled. Take the I/O sequence detailed in *Figure 7* (Typical Power Supply Sequence) as an example. The table below lists the number of SCLK pulses required for each instruction:

Instruction	\overline{CS} Low Continuously	\overline{CS} Strobed
Auto Cal	13 SCLKs	8 SCLKs
Read Status	13 SCLKs	8 SCLKs
Read Status	13 SCLKs	8 SCLKs
12-Bit + Sign Conv 1	13 SCLKs	8 SCLKs
12-Bit + Sign Conv 2	13 SCLKs	13 SCLKs

1.4 Analog Input Channel Selection

The data input on DI also selects the channel configuration for a particular A/D conversion (see *Tables 2, 3, 4* and *Table 5*). In *Figure 8* the only times when the channel configuration could be modified would be during I/O sequences 1, 4, 5 and 6. Input channels are reselected before the start of each new conversion. Shown below is the data bit stream required on DI, during I/O sequence number 4 in *Figure 8*, to set CH1 as the positive input and CH0 as the negative input for the different versions of ADCs:

Part Number	DI Data							
	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7
ADC12H030 ADC12030	L	H	L	L	H	L	X	X
ADC12H032 ADC12032	L	H	L	L	H	L	X	X
ADC12H034 ADC12034	L	H	L	L	L	H	L	X
ADC12H038 ADC12038	L	H	L	L	L	L	H	L

Where X can be a logic high (H) or low (L).

1.5 Power Up/Down

The ADC may be powered down at any time by taking the PD pin HIGH or by the instruction input on DI (see *Tables 5, 6*, and the Power Up/Down timing diagrams). When the ADC is powered down in this way, the circuitry necessary for an A/D conversion is deactivated. The circuitry necessary for digital I/O is kept active. Hardware power up/down is controlled by the state of the PD pin. Software power-up/down is controlled by the instruction issued to the ADC. If a software power up instruction is issued to the ADC while a hardware power down is in effect (PD pin high) the device will remain in the power-down state. If a software power down instruction is issued to the ADC while a hardware power up is in effect (PD pin low), the device will power down. When the device is powered down by software, it may be powered up by either issuing a software power up instruction or by taking PD pin high and then low. If the power down command is issued during an A/D conversion, that conversion is disrupted. Therefore, the data output after power up cannot be relied upon.

Application Hints (Continued)

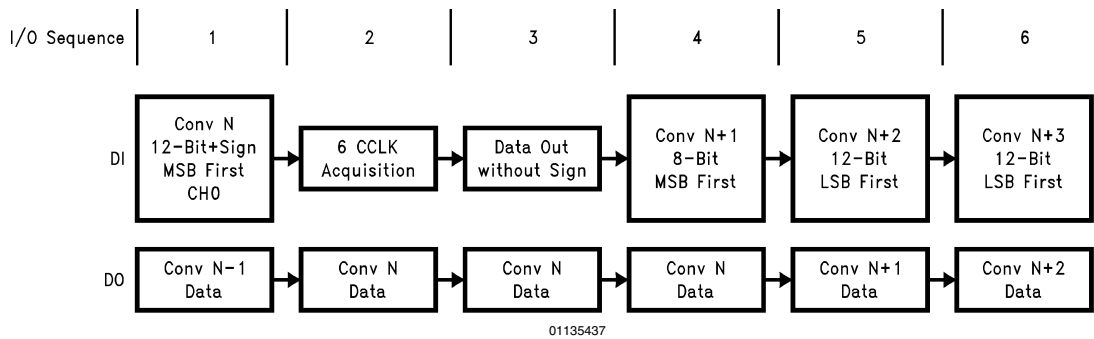


FIGURE 8. Changing the ADC's Conversion Configuration

1.6 User Mode and Test Mode

An instruction may be issued to the ADC to put it into test mode. Test mode is used by the manufacturer to verify complete functionality of the device. During test mode CH0–CH7 become active outputs. If the device is inadvertently put into the test mode with \overline{CS} continuously low, the serial communications may be desynchronized. Synchronization may be regained by cycling the power supply voltage to the device. Cycling the power supply voltage will also set the device into user mode. If \overline{CS} is used in the serial interface, the ADC may be queried to see what mode it is in. This is done by issuing a “read STATUS register” instruction to the ADC. When bit 9 of the status register is high, the ADC is in test mode; when bit 9 is low the ADC, is in user mode. As an alternative to cycling the power supply, an instruction sequence may be used to return the device to user mode. This instruction sequence must be issued to the ADC using \overline{CS} . The following table lists the instructions required to return the device to user mode:

Instruction	DI Data							
	DI0	DI1	DI2	DI3	DI4	DI5	DI6	DI7
TEST MODE	H	X	X	X	H	H	H	H
Reset	L	L	L	L	H	H	H	L
Test Mode Instructions	L	L	L	L	H	L	H	L
USER MODE	L	L	L	L	H	H	H	H
Power Up	L	L	L	L	H	L	H	L
Set DO with or without Sign	H or L	L	L	L	H	H	L	H
Set Acquisition Time	H or L	H or L	L	L	H	H	H	L
Start a Conversion	H or L	H or L	H or L	H or L	L	H or L	H or L	H or L

X = Don't Care

After returning to user mode with the user mode instruction the power up, data with or without sign, and acquisition time instructions need to be resent to ensure that the ADC is in the required state before a conversion is started.

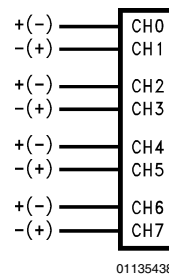
1.7 Reading the Data Without Starting a Conversion

The data from a particular conversion may be accessed without starting a new conversion by ensuring that the \overline{CONV} line is taken high during the I/O sequence. See the Read Data timing diagrams. *Table 6* describes the operation of the \overline{CONV} pin.

2.0 DESCRIPTION OF THE ANALOG MULTIPLEXER

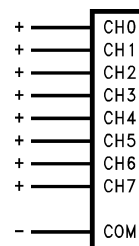
For the ADC12038, the analog input multiplexer can be configured with 4 differential channels or 8 single ended channels with the COM input as the zero reference or any combination thereof (see *Figure 9*). The difference between the voltages on the V_{REF+} and V_{REF-} pins determines the input voltage span (V_{REF}). The analog input voltage range is 0 to V_A+ . Negative digital output codes result when $V_{IN-} > V_{IN+}$. The actual voltage at V_{IN-} or V_{IN+} cannot go below AGND.

4 Differential Channels



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8 Single-Ended Channels with COM as Zero Reference



01135439

FIGURE 9.

Application Hints (Continued)

CH0, CH2, CH4, and CH6 can be assigned to the MUXOUT1 pin in the differential configuration, while CH1, CH3, CH5, and CH7 can be assigned to the MUXOUT2 pin. In the differential configuration, the analog inputs are paired as follows: CH0 with CH1, CH2 with CH3, CH4 with CH5 and CH6 with CH7. The A/DIN1 and A/DIN2 pins can be assigned positive or negative polarity.

With the single-ended multiplexer configuration CH0 through CH7 can be assigned to the MUXOUT1 pin. The COM pin is always assigned to the MUXOUT2 pin. A/DIN1 is assigned as the positive input; A/DIN2 is assigned as the negative input. (See Figure 10).

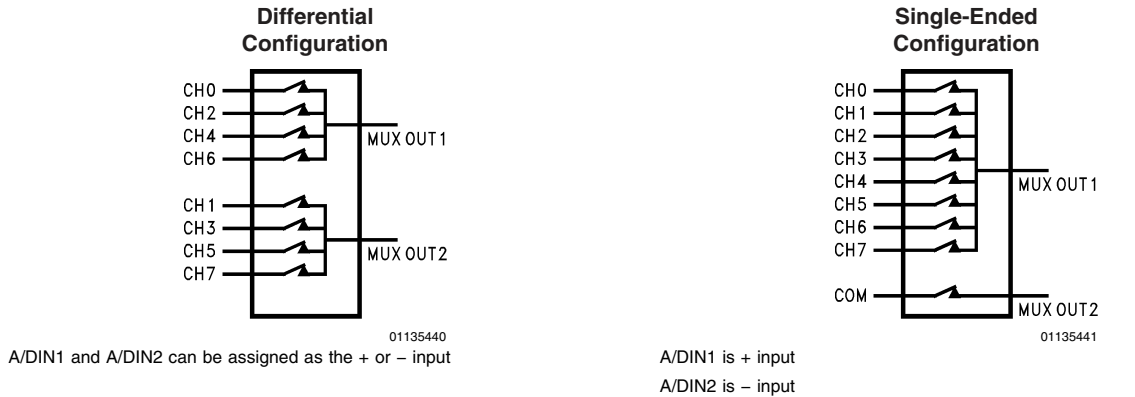


FIGURE 10.

The Multiplexer assignment tables for the ADC12030,2,4,8 (Tables 2, 3, 4) summarize the aforementioned functions for the different versions of A/Ds.

2.1 Biasing for Various Multiplexer Configurations

Figure 11 is an example of biasing the device for single-ended operation. The sign bit is always low. The digital output range is 0 0000 0000 0000 to 0 1111 1111 1111. One LSB is equal to 1 mV (4.1V/4096 LSBs).

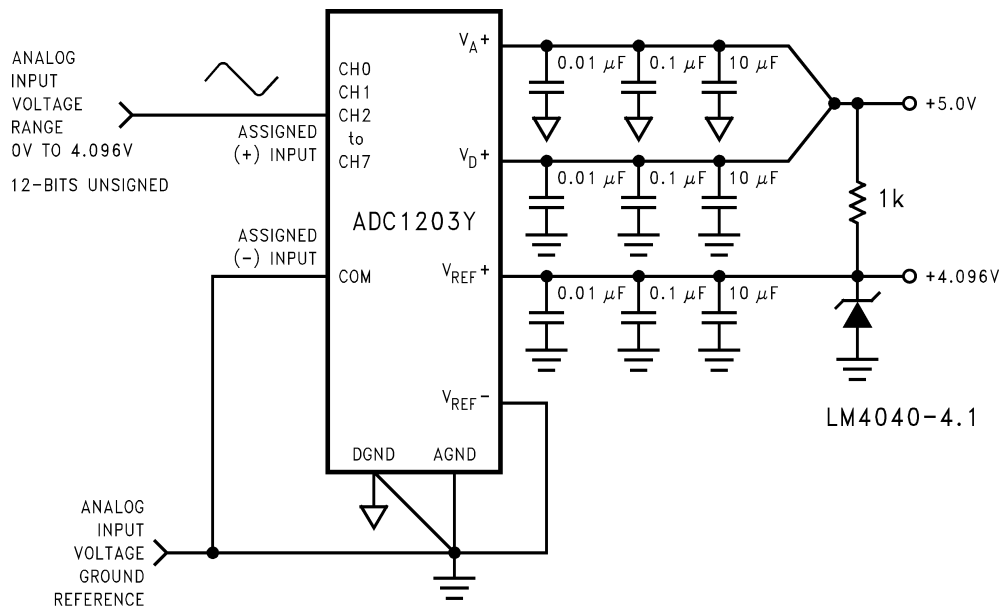


FIGURE 11. Single-Ended Biasing

Application Hints (Continued)

For pseudo-differential signed operation, the biasing circuit shown in *Figure 12* shows a signal AC coupled to the ADC. This gives a digital output range of -4096 to $+4095$. With a 2.5V reference, as shown, 1 LSB is equal to $610\ \mu\text{V}$. Although, the ADC is not production tested with a 2.5V reference, linearity error typically will not change more than 0.1 LSB (see the curves in the Typical Electrical Characteristics Section). With the ADC set to an acquisition time of 10 clock

periods, the input biasing resistor needs to be $600\ \Omega$ or less. Notice though that the input coupling capacitor needs to be made fairly large to bring down the high pass corner. Increasing the acquisition time to 34 clock periods (with a $5\ \text{MHz}$ CCLK frequency) would allow the $600\ \Omega$ to increase to 6k , which with a $1\ \mu\text{F}$ coupling capacitor would set the high pass corner at $26\ \text{Hz}$. Increasing R_1 to 6k would allow R_2 to be 2k .

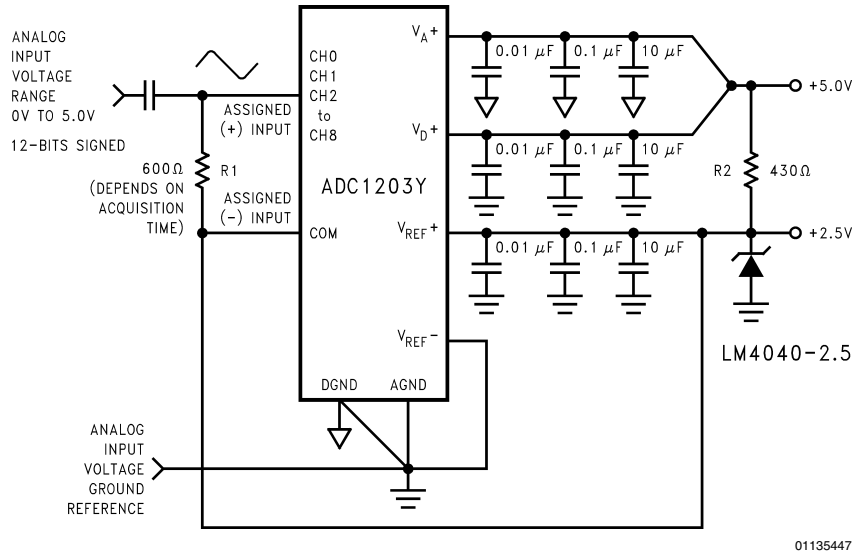


FIGURE 12. Pseudo-Differential Biasing with the Signal Source AC Coupled Directly into the ADC

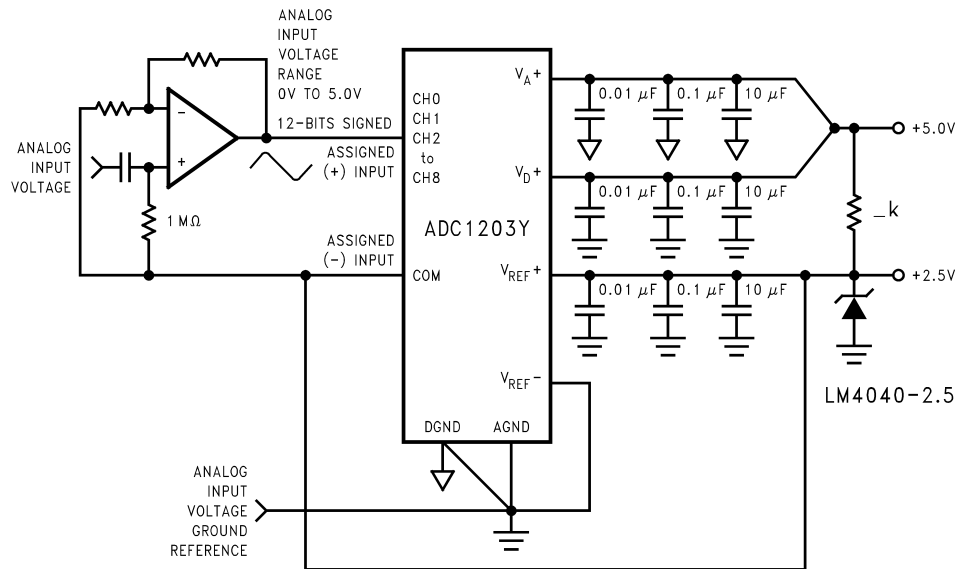
An alternative method for biasing pseudo-differential operation is to use the $+2.5\text{V}$ from the LM4040 to bias any amplifier circuits driving the ADC as shown in *Figure 13*. The value of the resistor pull-up biasing the LM4040-2.5 will depend upon the current required by the op amp biasing circuitry.

In the circuit of *Figure 13* some voltage range is lost since the amplifier will not be able to swing to $+5\text{V}$ and GND with a single $+5\text{V}$ supply. Using an adjustable version of the

LM4041 to set the full scale voltage at exactly 2.048V and a lower grade LM4040D-2.5 to bias up everything to 2.5V as shown in *Figure 14* will allow the use of all the ADC's digital output range of -4096 to $+4095$ while leaving plenty of head room for the amplifier.

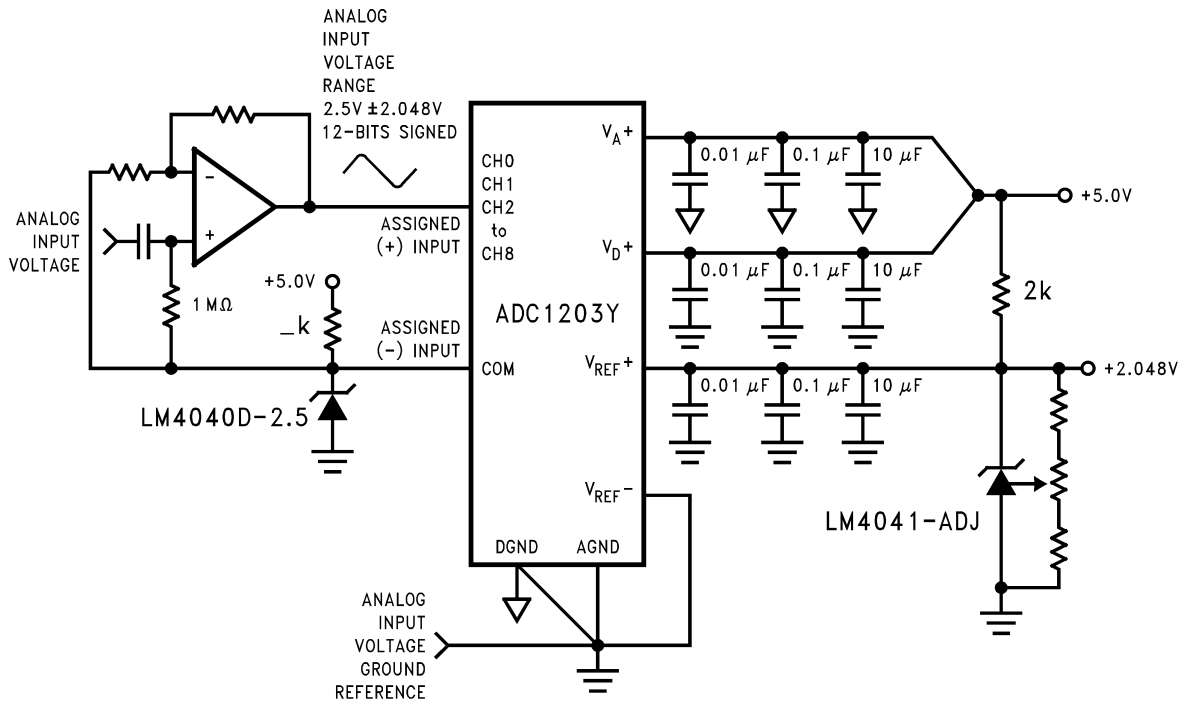
Fully differential operation is shown in *Figure 15*. One LSB for this case is equal to $(4.1\text{V}/4096) = 1\ \text{mV}$.

Application Hints (Continued)



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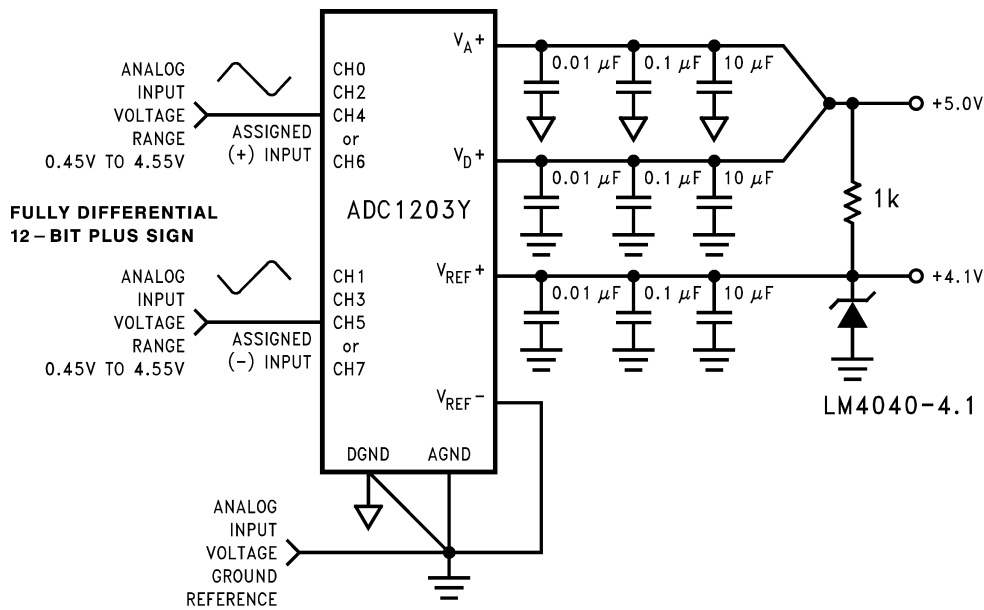
FIGURE 13. Alternative Pseudo-Differential Biasing



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FIGURE 14. Pseudo-Differential Biasing without the Loss of Digital Output Range

Application Hints (Continued)

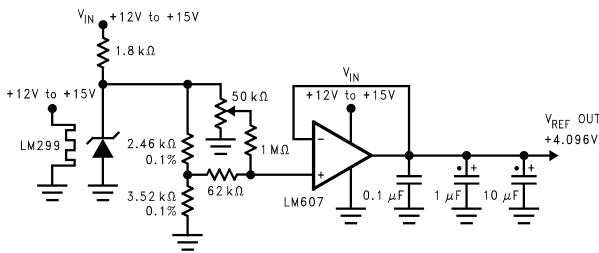


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FIGURE 15. Fully Differential Biasing

3.0 REFERENCE VOLTAGE

The difference in the voltages applied to the V_{REF+} and V_{REF-} defines the analog input span (the difference between the voltage applied between two multiplexer inputs or the voltage applied to one of the multiplexer inputs and analog ground), over which 4095 positive and 4096 negative codes exist. The voltage sources driving V_{REF+} or V_{REF-} must have very low output impedance and noise. The circuit in *Figure 16* is an example of a very stable reference appropriate for use with the device.



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FIGURE 16. Low Drift Extremely Stable Reference Circuit

The ADC 12030/2/4/8 can be used in either ratiometric or absolute reference applications. In ratiometric systems, the analog input voltage is proportional to the voltage used for the ADC's reference voltage. When this voltage is the system power supply, the V_{REF+} pin is connected to V_A+ and V_{REF-} is connected to ground. This technique relaxes the system reference stability requirements because the analog input voltage and the ADC reference voltage move together. This maintains the same output code for given input conditions. For absolute accuracy, where the analog input voltage

varies between very specific voltage limits, a time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage's magnitude will require an initial adjustment to null reference voltage induced full-scale errors.

Below are recommended references along with some key specifications.

Part Number	Output Voltage Tolerance	Temperature Coefficient
LM4041CI-Adj	±0.5%	±100ppm/°C
LM4040AI-4.1	±0.1%	±100ppm/°C
LM4120AI-4.1	±0.2%	±50ppm/°C
LM4121AI-4.1	±0.2%	±50ppm/°C
LM4050AI-4.1	±0.1	±50ppm/°C
LM4030AI-4.1	±0.05%	±10ppm/°C
LM4031AI	±2.2	±26ppm/°C
LM4031AC	±0.4	±46ppm/°C
LM4140AC-4.1	±0.1%	±3.0ppm/°C
Circuit of Figure 16	Adjustable	±2ppm/°C

The reference voltage inputs are not fully differential. The ADC12030/2/4/8 will not generate correct conversions or comparisons if V_{REF+} is taken below V_{REF-} . Correct conversions result when V_{REF+} and V_{REF-} differ by 1V and remain, at all times, between ground and V_A+ . The V_{REF} common mode range, $(V_{REF+} + V_{REF-})/2$ is restricted to $(0.1 \times V_A+)$ to $(0.6 \times V_A+)$. Therefore, with $V_A+ = 5V$ the center of the reference ladder should not go below 0.5V or above 3.0V. *Figure 17* is a graphic representation of the voltage restrictions on V_{REF+} and V_{REF-} .

Application Hints (Continued)

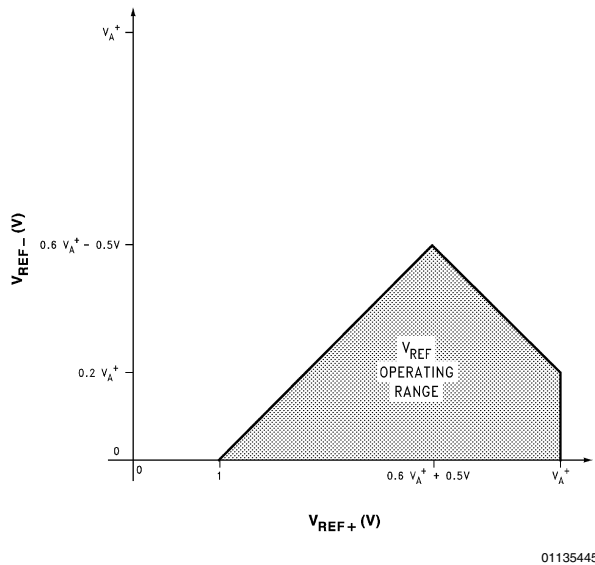


FIGURE 17. V_{REF} Operating Range

4.0 ANALOG INPUT VOLTAGE RANGE

The ADC12030/2/4/8's fully differential ADC generate a two's complement output that is found by using the equations shown below:

for (12-bit) resolution the Output Code =

$$\frac{(V_{IN}^+ - V_{IN}^-) (4096)}{(V_{REF}^+ - V_{REF}^-)}$$

for (8-bit) resolution the Output Code =

$$\frac{(V_{IN}^+ - V_{IN}^-) (256)}{(V_{REF}^+ - V_{REF}^-)}$$

Round off to the nearest integer value between -4096 to 4095 for 12-bit resolution and between -256 to 255 for 8-bit resolution if the result of the above equation is not a whole number.

Examples are shown in the table below:

V_{REF}^+	V_{REF}^-	V_{IN}^+	V_{IN}^-	Digital Output Code
+2.5V	+1V	+1.5V	0V	0,1111,1111,1111
+4.096V	0V	+3V	0V	0,1011,1011,1000
+4.096V	0V	+2.499V	+2.500V	1,1111,1111,1111
+4.096V	0V	0V	+4.096V	1,0000,0000,0000

5.0 INPUT CURRENT

At the start of the acquisition window (t_A) a charging current flows into or out of the analog input pins (A/DIN1 and A/DIN2) depending on the input voltage polarity. The analog input pins are CH0-CH7 and COM when A/DIN1 is tied to MUXOUT1 and A/DIN2 is tied to MUXOUT2. The peak value of this input current will depend on the actual input voltage

applied, the source impedance and the internal multiplexer switch on resistance. With MUXOUT1 tied to A/DIN1 and MUXOUT2 tied to A/DIN2 the internal multiplexer switch on resistance is typically 1.6 k Ω . The A/DIN1 and A/DIN2 mux on resistance is typically 750 Ω .

6.0 INPUT SOURCE RESISTANCE

For low impedance voltage sources (<600 Ω), the input charging current will decay, before the end of the S/H's acquisition time of 2 μ s (10 CCLK periods with $f_C = 5$ MHz), to a value that will not introduce any conversion errors. For high source impedances, the S/H's acquisition time can be increased to 18 or 34 CCLK periods. For less ADC resolution and/or slower CCLK frequencies the S/H's acquisition time may be decreased to 6 CCLK periods. To determine the number of clock periods (N_C) required for the acquisition time with a specific source impedance for the various resolutions the following equations can be used:

$$12 \text{ Bit + Sign } N_C = [R_S + 2.3] \times f_C \times 0.824$$

$$8 \text{ Bit + Sign } N_C = [R_S + 2.3] \times f_C \times 0.57$$

Where f_C is the conversion clock (CCLK) frequency in MHz and R_S is the external source resistance in k Ω . As an example, operating with a resolution of 12 Bits+sign, a 5 MHz clock frequency and maximum acquisition time of 34 conversion clock periods the ADC's analog inputs can handle a source impedance as high as 6 k Ω . The acquisition time may also be extended to compensate for the settling or response time of external circuitry connected between the MUXOUT and A/DIN pins.

The acquisition time t_A is started by a falling edge of SCLK and ended by a rising edge of CCLK (see timing diagrams). If SCLK and CCLK are asynchronous one extra CCLK clock period may be inserted into the programmed acquisition time for synchronization. Therefore with asynchronous SCLK and CCLKs the acquisition time will change from conversion to conversion.

7.0 INPUT BYPASS CAPACITANCE

External capacitors (0.01 μ F-0.1 μ F) can be connected between the analog input pins, CH0-CH7, and analog ground to filter any noise caused by inductive pickup associated with long input leads. These capacitors will not degrade the conversion accuracy.

8.0 NOISE

The leads to each of the analog multiplexer input pins should be kept as short as possible. This will minimize input noise and clock frequency coupling that can cause conversion errors. Input filtering can be used to reduce the effects of the noise sources.

9.0 POWER SUPPLIES

Noise spikes on the V_A^+ and V_D^+ supply lines can cause conversion errors; the comparator will respond to the noise. The ADC is especially sensitive to any power supply spikes that occur during the auto-zero or linearity correction. The minimum power supply bypassing capacitors recommended are low inductance tantalum capacitors of 10 μ F or greater paralleled with 0.1 μ F monolithic ceramic capacitors. More or different bypassing may be necessary depending on the overall system requirements. Separate bypass capacitors should be used for the V_A^+ and V_D^+ supplies and placed as close as possible to these pins.

Application Hints (Continued)

10.0 GROUNDING

The ADC12030/2/4/8's performance can be maximized through proper grounding techniques. These include the use of separate analog and digital ground planes. The digital ground plane is placed under all components that handle digital signals, while the analog ground plane is placed under all components that handle analog signals. The digital and analog ground planes are connected together at only one

point, either the power supply ground or at the pins of the ADC. This greatly reduces the occurrence of ground loops and noise.

Shown in *Figure 18* is the ideal ground plane layout for the ADC12038 along with ideal placement of the bypass capacitors. The circuit board layout shown in *Figure 18* uses three bypass capacitors: 0.01 μF (C1) and 0.1 μF (C2) surface mount capacitors and 10 μF (C3) tantalum capacitor.

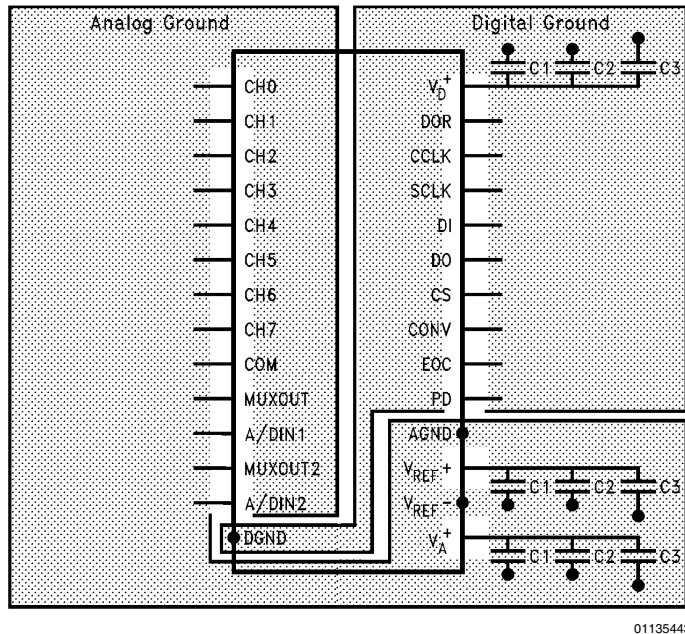


FIGURE 18. Ideal Ground Plane

11.0 CLOCK SIGNAL LINE ISOLATION

The ADC12030/2/4/8's performance is optimized by routing the analog input/output and reference signal conductors as far as possible from the conductors that carry the clock signals to the CCLK and SCLK pins. Ground traces parallel to the clock signal traces can be used on printed circuit boards to reduce clock signal interference on the analog input/output pins.

12.0 THE CALIBRATION CYCLE

A calibration cycle needs to be started after the power supplies, reference, and clock have been given enough time to stabilize after initial turn-on. During the calibration cycle, correction values are determined for the offset voltage of the sampled data comparator and any linearity and gain errors. These values are stored in internal RAM and used during an analog-to-digital conversion to bring the overall full-scale, offset, and linearity errors down to the specified limits. Full-scale error typically changes ± 0.4 LSB over temperature and linearity error changes even less; therefore it should be necessary to go through the calibration cycle only once after power up if the Power Supply Voltage and the ambient temperature do not change significantly (see the curves in the Typical Performance Characteristics).

13.0 THE AUTO-ZERO CYCLE

To correct for any change in the zero (offset) error of the A/D, the auto-zero cycle can be used. It may be necessary to do an auto-zero cycle whenever the ambient temperature or the power supply voltage change significantly. (See the curves titled "Zero Error Change vs Ambient Temperature" and "Zero Error Change vs Supply Voltage" in the Typical Performance Characteristics.)

14.0 DYNAMIC PERFORMANCE

Many applications require the A/D converter to digitize AC signals, but the standard DC integral and differential nonlinearity specifications will not accurately predict the A/D converter's performance with AC input signals. The important specifications for AC applications reflect the converter's ability to digitize AC signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise (S/N), signal-to-noise + distortion ratio (S/(N + D)), effective bits, full power bandwidth, aperture time and aperture jitter are quantitative measures of the A/D converter's capability.

An A/D converter's AC performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. S/(N + D) and S/N are calculated from the resulting FFT data, and a spectral plot may also be obtained. Typical values for S/N

Application Hints (Continued)

are shown in the table of Electrical Characteristics, and spectral plots of S/(N + D) are included in the typical performance curves.

The A/D converter's noise and distortion levels will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. This can be seen in the S/(N + D) versus frequency curves.

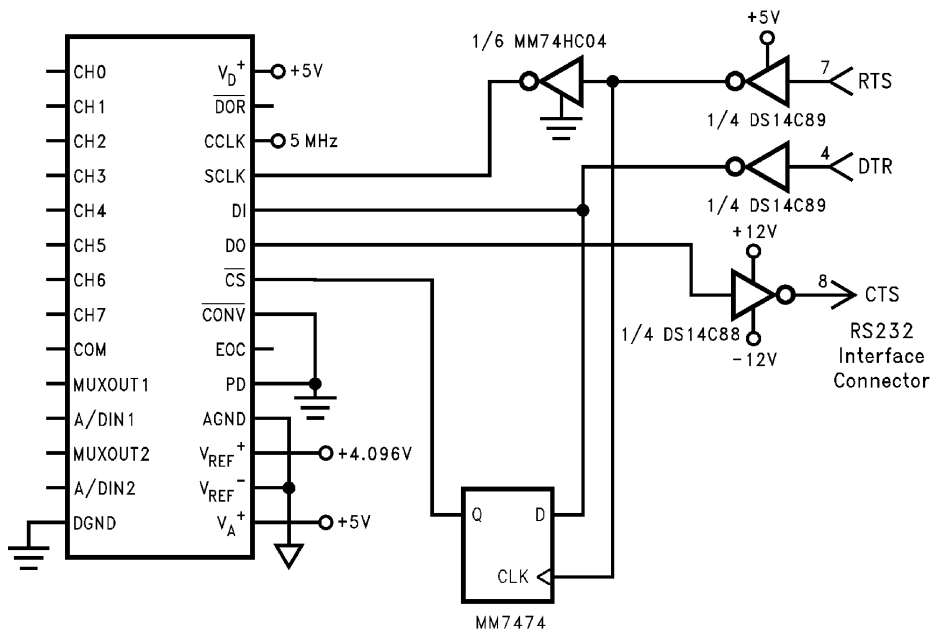
Effective number of bits can also be useful in describing the A/D's noise performance. An ideal A/D converter will have some amount of quantization noise, determined by its resolution, which will yield an optimum S/N ratio given by the following equation:

$$S/N = (6.02 \times n + 1.76) \text{ dB}$$

where n is the A/D's resolution in bits.

S/(N + D) (or SINAD) is a combination of S/N (or SNR) and distortion and is considered to be an overall measure of an A/D converter performance. S/(N + D) is defined as:

$$\text{SINAD} = -20 * \log \sqrt{10^{\frac{-\text{SNR}}{10}} + 10^{\frac{\text{THD}}{10}}}$$



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Note: V_A⁺, V_D⁺, and V_{REF}⁺ on the ADC12038 each have 0.01 μF and 0.1 μF chip caps, and 10 μF tantalum caps. All logic devices are bypassed with 0.1 μF caps.

The assignment of the RS232 port is shown below

			B7	B6	B5	B4	B3	B2	B1	B0
COM1	Input Address	3FE	X	X	X	CTS	X	X	X	X
	Output Address	3FC	X	X	X	0	X	X	RTS	DTR

A sample program, written in Microsoft QuickBasic, is shown on the next page. The program prompts for data mode select instruction to be sent to the A/D. This can be found from the Mode Programming table shown earlier. The data should be entered in "1"s and "0"s as shown in the table with DI0 first. Next the program prompts for the number of SCLKs required for the programmed mode select instruction. For instance, to send all "0"s to the A/D, selects CH0 as the +input, CH1 as

and the effective number of Bits (ENOB) is defined as:

$$\text{ENOB} = \frac{S/(N + D) \text{ (dB)} - 1.76}{6.02}$$

As an example, this device with a differential signed 5V, 1 kHz sine wave input signal will typically have a S/(N + D) of 77 dB, which is equivalent to 12.5 effective bits.

15.0 AN RS232 SERIAL INTERFACE

Shown on the following page is a schematic for an RS232 interface to any IBM and compatible PCs. The DTR, RTS, and CTS RS232 signal lines are buffered via level translators and connected to the ADC12038's DI, SCLK, and DO pins, respectively. The D flip flop drives the $\overline{\text{CS}}$ control line.

Application Hints (Continued)

Power Down instructions do not change these default settings. The following power up sequence should be followed:

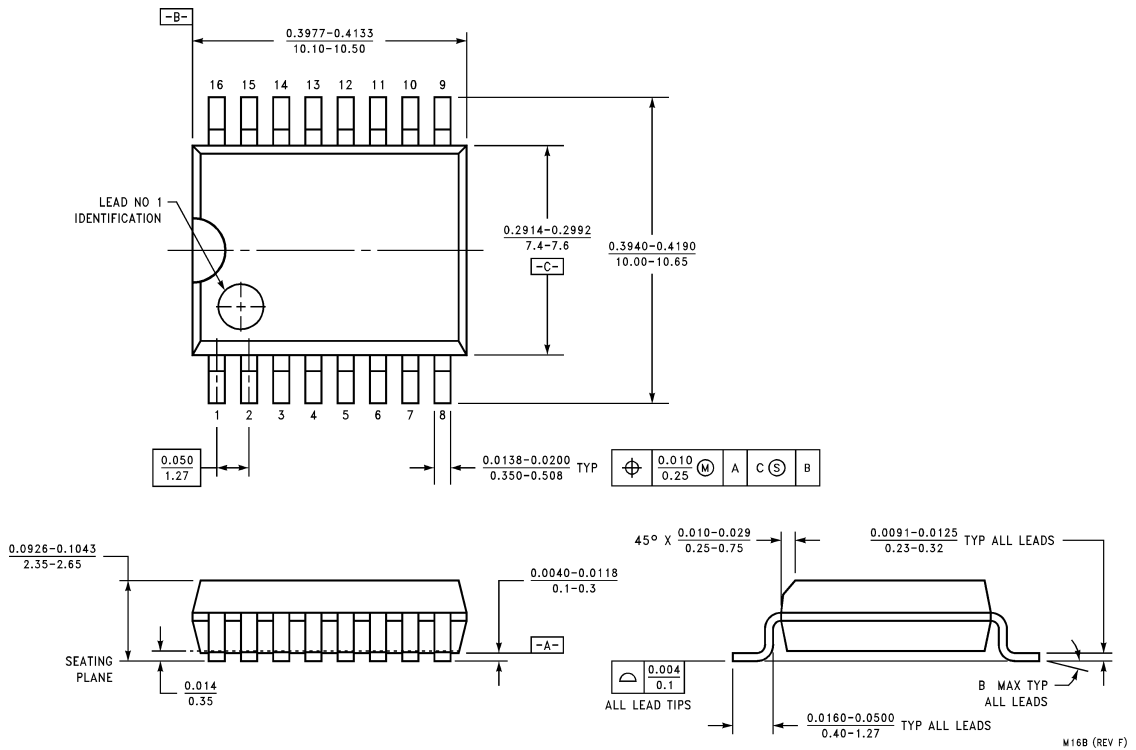
1. Run the program
2. Prior to responding to the prompt apply the power to the ADC12038
3. Respond to the program prompts

It is recommended that the first instruction issued to the ADC12038 be Auto Cal (see Section 1.1).

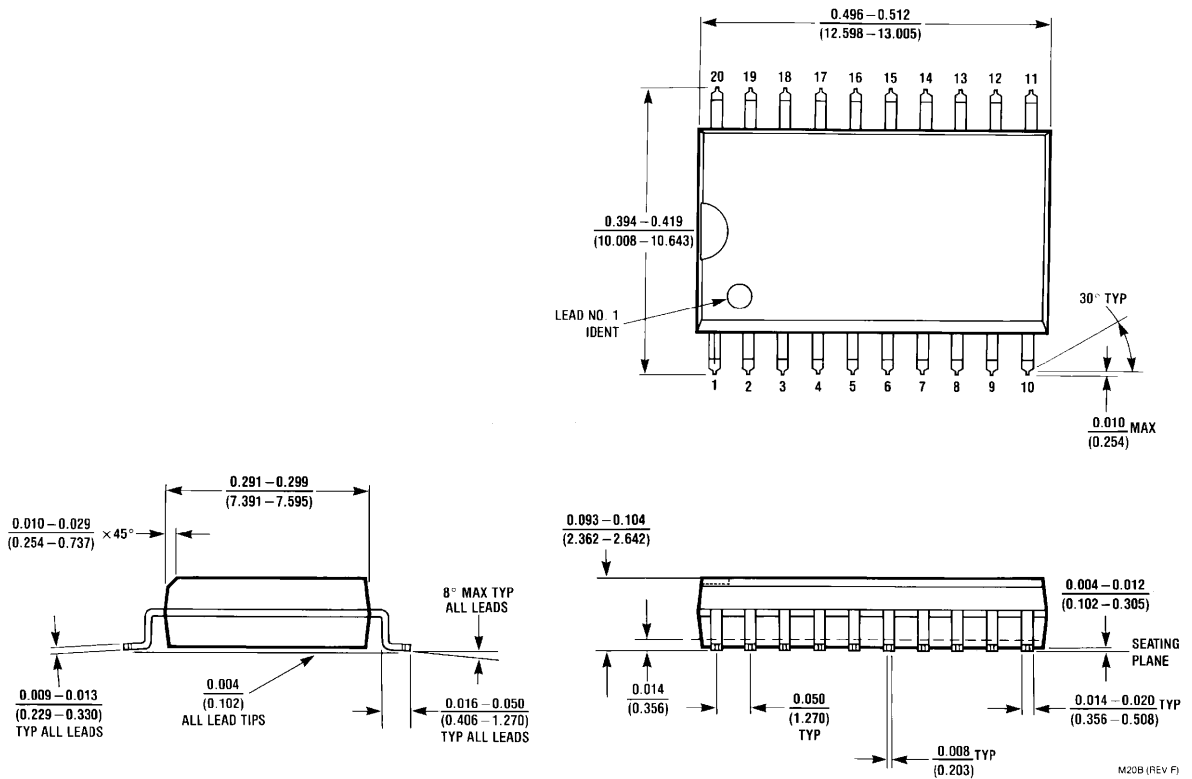
```
'variables DOL=Data Out word length,
=>DI=Data string for A/D DI input,
'          DO=A/D result string
'SET CS# HIGH
OUT  &H3FC, (&H2 OR INP (&H3FC))      'set
=>RTS HIGH
OUT  &H3FC, (&HFE AND INP(&H3FC))      'set
=>DTR LOW
OUT  &H3FC, (&HFD AND INP(&H3FC))      'set
=>RTS LOW
OUT  &H3FC, (&HEF AND INP(&H3FC))      'set
=>B4 low
10
LINE INPUT <"DI data for ADC12038 (see
=>Mode Table on data sheet)"; DI$
INPUT <"ADC12038 output word length
=>(8,9,12,13,16 or 17)"; DOL
20
'SET CS# HIGH
OUT  &H3FC, (&H2 OR INP (&H3FC))      'set
=>RTS HIGH
OUT  &H3FC, (&HFE AND INP(&H3FC))      'set
=>DTR LOW
OUT  &H3FC, (&HFD AND INP(&H3FC))      'set
=>RTS LOW
'SET CS# LOW
OUT  &H3FC, (&H2 OR INP (&H3FC))      'set
=>RTS HIGH
OUT  &H3FC, (&H1 OR INP(&H3FC))      'set
=>DTR HIGH
OUT  &H3FC, (&HFD AND INP(&H3FC))      'set
=>RTS LOW
DO$=
=> <" "
=>DO variable
    OUT  &H3FC, (&H1 OR INP(&H3FC))      'SET
=>DTR HIGH
    OUT  &H3FC, (&HFD AND
=>INP (&H3FC))      'SCLK low
```

```
FOR N=1 TO 8
    Temp$=MID$(DI$,N,1)
    IF Temp$=<">0" THEN
        OUT &H3FC, (&H1 OR INP(&H3FC))
    ELSE OUT &H3FC, (&HFE AND INP(&H3FC))
    END IF
'out
=>DI
    OUT &H3FC, (&H2 OR
=>INP (&H3FC))      'SCLK high
    IF (INP(&H3FE) AND 16)=16 THEN
        DO$=DO$+<">0"
    ELSE
        DO$=DO$+<">1"
    END
=>IF
'input
=>DO
    OUT &H3FC, (&H1 OR INP(&H3FC))      'SET
=>DTR HIGH
    OUT &H3FC, (&HFD AND
=>INP (&H3FC))      'SCLK low
NEXT N
IF DOL>8 THEN
    FOR N=9 TO DOL
        OUT &H3FC, (&H1 OR INP(&H3FC))      'SET
=>DTR HIGH
        OUT &H3FC, (&HFD AND
=>INP (&H3FC))      'SCLK low
        OUT &H3FC, (&H2 OR
=>INP (&H3FC))      'SCLK high
        IF (INP(&H3FE) AND &H10)=&H10 THEN
            DO$=DO$+<">0"
        ELSE
            DO$=DO$+<">1"
        END IF
    NEXT N
END IF
OUT  &H3FC, (&HFA AND
=>INP (&H3FC))      'SCLK low and DI high
FOR N=1 TO 500
NEXT N
PRINT DO$
INPUT <"Enter <">C" to convert
=>else <">RETURN" to alter DI data"; s$
IF s$=<">C" OR s$=<">c" THEN
'reset GOTO 20
ELSE
    GOTO 10
END IF
END
```

Physical Dimensions inches (millimeters)
unless otherwise noted

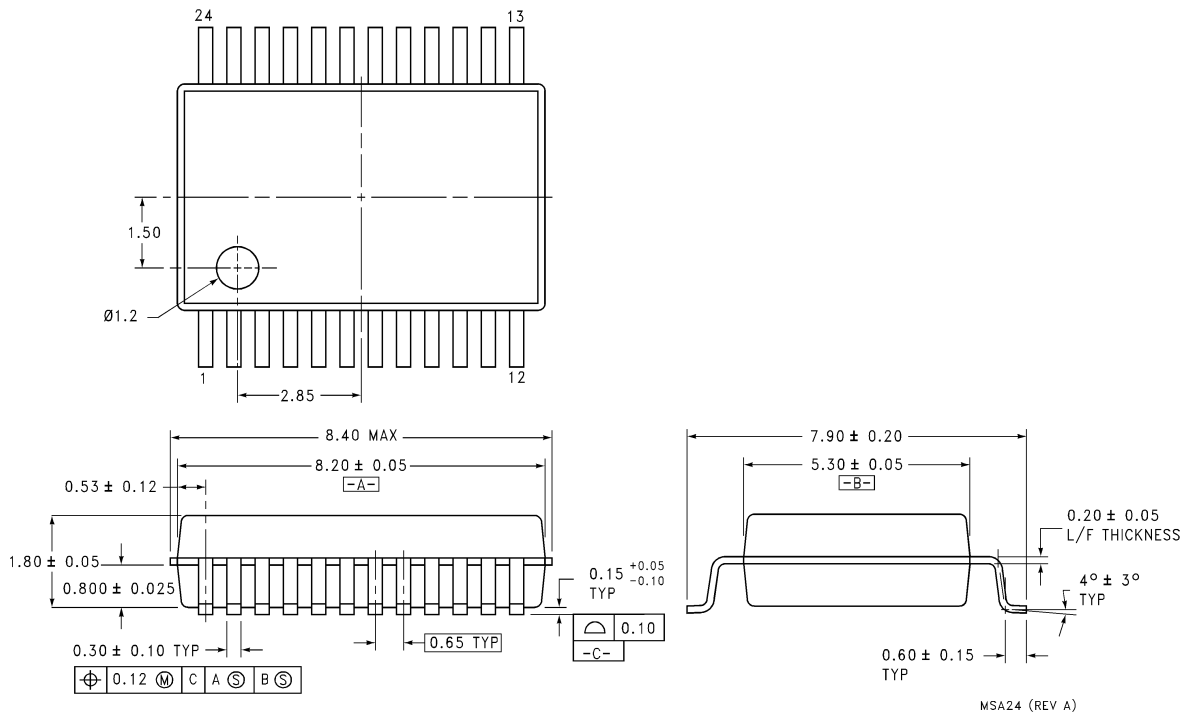
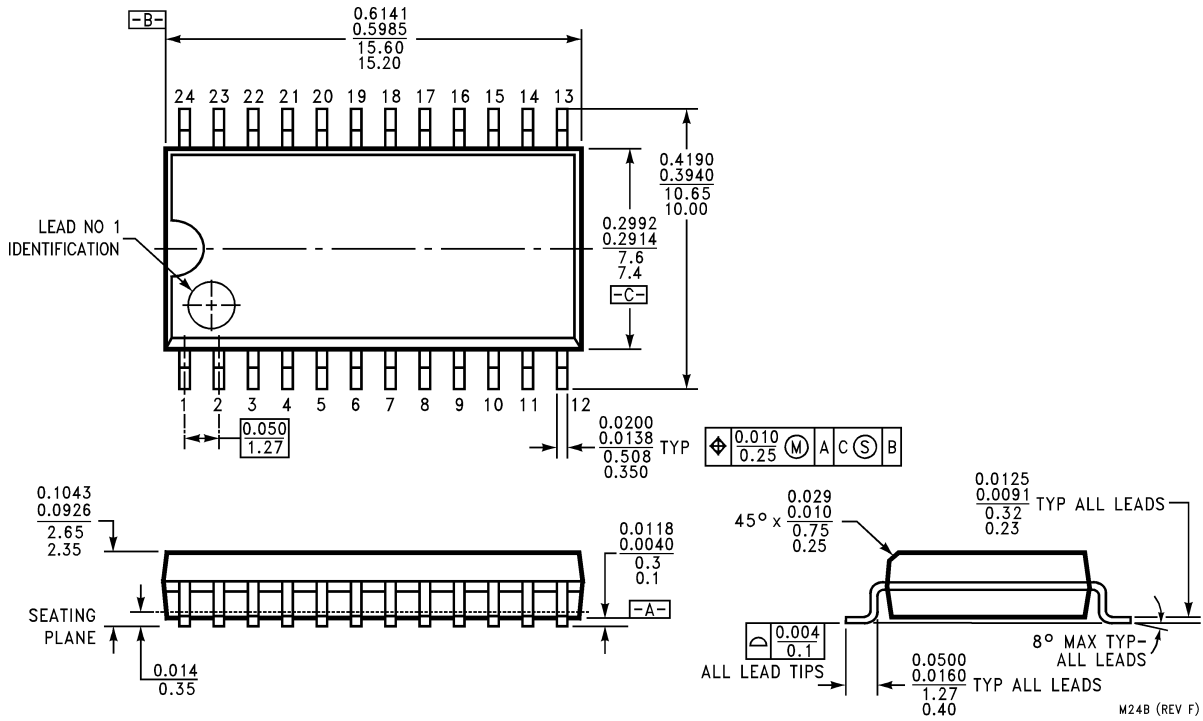


Order Number ADC12030CIWM or ADC12H030CIWM
NS Package Number M16B

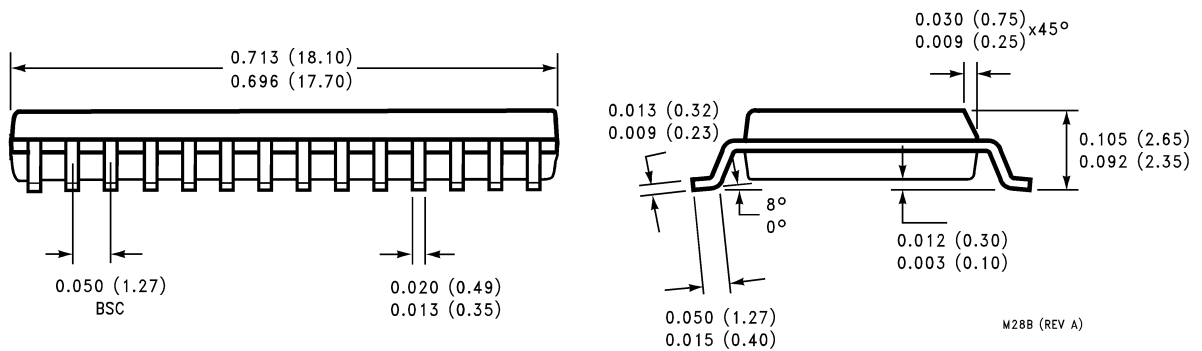
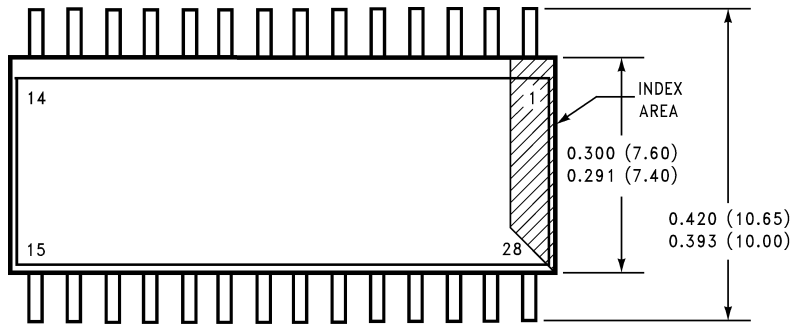


Order Number ADC12032CIWM or ADC12H032CIWM
NS Package Number M20B

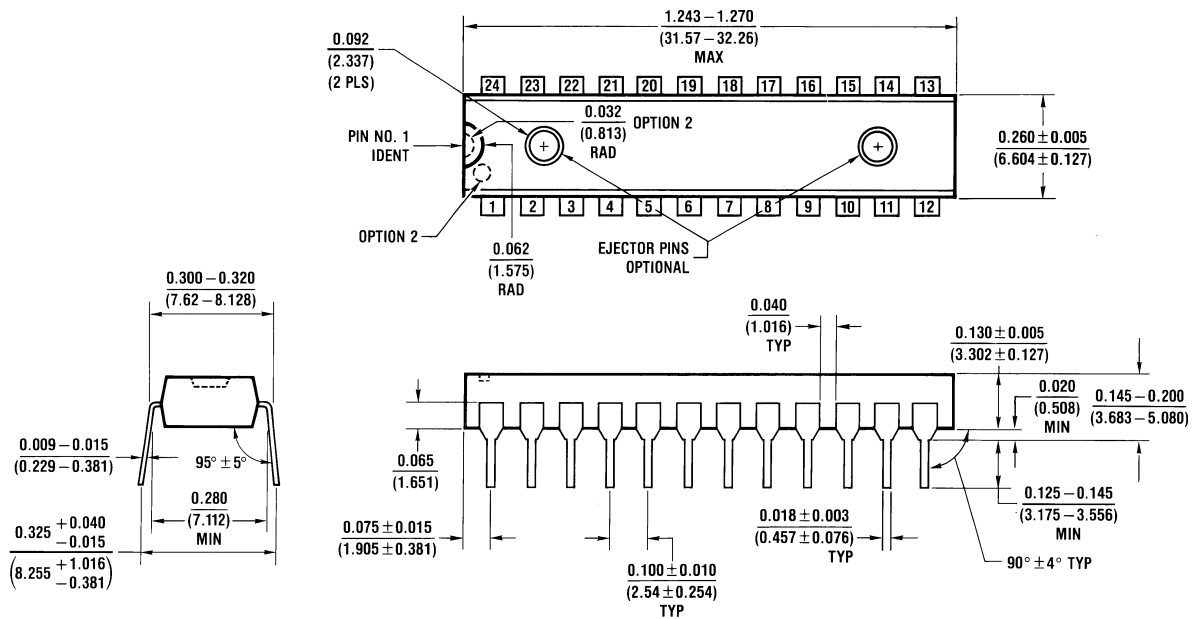
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**Order Number ADC12038CIWM or ADC12H038CIWM
NS Package Number M28B**



**Order Number ADC12034CIN or ADC12H034CIN
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