

18-30GHz Low Noise Amplifier

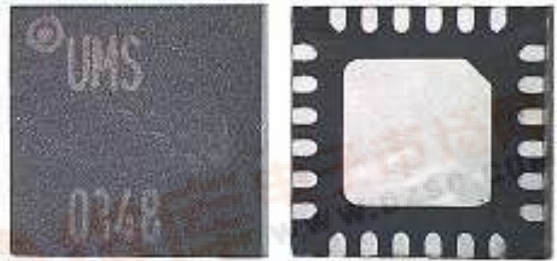
GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA2069-QDG is a three-stage self-biased wide band monolithic low noise amplifier. Typical applications range from telecommunication (point to point, point to multi-point, VSAT) to ISM and military markets.

The circuit is manufactured with a standard pHEMT process: 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

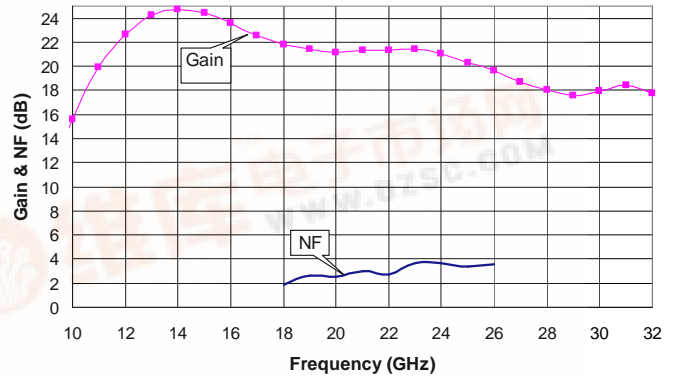
It is supplied in lead-free SMD package.



Main Features

- Broadband performance 18-30GHz
- 3dB noise figure
- 20dB gain
- 65 mA Low DC power consumption.
- 20dBm 3rd order intercept point (high current configuration).
- 24L-QFN4x4 SMD package

Gain and NF @ high current config. (BCF grounded)



Main Characteristics

Tamb = +25°C, Vd = +4,5V Pads: VgB, VgC, VgF=GND (High current configuration)

Symbol	Parameter	Min	Typ	Max	Unit
NF	Noise figure, 18-26GHz		3	4	dB
G	Gain	17	20		dB
IP3	3rd order intercept point (Pout/tone=-5dBm) 18-26 GHz	18	20		dBm

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!



Electrical Characteristics (low current configuration)

Tamb = +25°C, Vd = +4.5V Pads: VgB, VgD, VgE=GND

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	18		30	GHz
G	Gain	16.5	19.5		dB
ΔG	Gain flatness		± 2	± 2.5	dB
NF	Noise figure (18 – 26.5GHz)		3	4	dB
IS11I	Input return loss (18 – 26.5GHz)		-5	-3	dB
IS22I	Ouput return loss (18 – 26.5GHz)		-7	-3	dB
IP3	3rd order intercept point (Pout/tone=-5dBm) 18-26GHz	16.5	18.5		dBm
P1dB	Output power at 1dB gain compression 18-26GHz	9.0	10.5		dBm
Id	Drain bias current		65		mA

These values are representative of onboard measurements as defined on the drawing 95541 (see below).

Performances can be optimized thanks to external matching (refer to the “Sub-band enhancement” section below).

Electrical Characteristics (high current configuration)

Tamb = +25°C, Vd = +4,5V Pads: VgB, VgC, VgF=GND

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	18		30	GHz
G	Gain	17	20		dB
ΔG	Gain flatness		± 2	± 2.5	dB
NF	Noise figure (18 – 26.5GHz)		3	4	dB
IS11I	Input return loss (18 – 26.5GHz)		-5	-3	dB
IS22I	Ouput return loss (18 – 26.5GHz)		-7	-3	dB
IP3	3rd order intercept point (Pout/tone=-5dBm) 18-26 GHz	18	20		dBm
P1dB	Output power at 1dB gain compression 18-26 GHz	12	13.5		dBm
Id	Drain bias current		85		mA

These values are representative of onboard measurements as defined on the drawing 95541 (see below).

Performances can be optimized thanks to external matching (refer to the “Sub-band enhancement” section below).

Absolute Maximum Ratings (1)

Tamb = +25°C

Symbol	Parameter (1)	Values	Unit
Vd	Drain bias voltage	5	V
Pin	Maximum input power overdrive	-7.0	dBm
Rth_BDE	Thermal Resistance channel to ground paddle (2)	130	°C/W
Rth_BCF	Thermal Resistance channel to ground paddle (2)	120	°C/W
Top	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these paramaters may cause permanent damage.

(2) Thermal resistance for Tamb. = +85°C and a Tj max = +175°C.

Typical Package Sij parameters for low current configuration

Tamb = +25°C, Vd = +4,5V Pads: B, D, E grounded.

F (GHz)	S11	S11	S12	S12	S21	S21	S22	S22
	dB	/°	dB	/°	dB	/°	dB	/°
2	-0.1	-58.7	-95.2	-85.6	-57.5	-2.4	-0.6	-148.4
3	-0.1	-89.3	-68.8	63.3	-77.6	-24.4	-0.9	157.1
4	-0.1	-123.5	-63.2	93.4	-52.9	62.8	-0.9	112.4
5	-0.2	-160.8	-62.9	47.1	-37.4	145.3	-1.3	72.0
6	-0.4	156.1	-58.1	11.4	-18.1	93.6	-1.7	39.9
7	-0.6	107.6	-67.5	-59.7	-4.4	28.0	-2.0	8.4
8	-1.2	58.9	-68.1	93.7	4.4	-52.1	-3.0	-20.2
9	-1.8	13.5	-61.6	-9.2	9.6	-122.4	-3.9	-38.6
10	-2.8	-26.1	-60.0	-42.6	14.7	176.1	-4.4	-69.5
11	-4.0	-58.0	-55.1	171.8	19.0	109.4	-8.3	-92.5
12	-5.7	-89.1	-53.4	87.2	21.7	41.3	-13.4	-92.8
13	-8.8	-122.0	-49.6	14.1	23.3	-24.1	-17.0	-67.1
14	-15.8	-173.9	-50.5	-42.8	24.0	-86.8	-12.6	-36.0
15	-17.4	24.9	-48.2	-120.3	23.5	-146.2	-8.3	-46.7
16	-10.9	-20.6	-48.3	171.6	22.4	162.0	-6.3	-65.3
17	-8.5	-47.1	-49.6	133.4	21.5	116.9	-5.9	-85.2
18	-7.0	-65.5	-47.3	121.9	20.9	75.8	-5.9	-99.8
19	-6.2	-82.8	-44.9	92.5	20.8	34.2	-6.1	-116.0
20	-5.8	-98.4	-42.5	57.3	20.7	-6.5	-7.2	-130.1
21	-4.9	-110.8	-43.2	20.1	20.9	-48.3	-7.9	-137.3
22	-4.7	-125.9	-45.3	14.9	20.9	-90.8	-9.2	-142.4
23	-4.3	-138.7	-43.3	-0.5	20.9	-135.3	-8.7	-139.3
24	-3.9	-152.2	-43.7	-14.8	20.4	178.7	-7.6	-141.9
25	-3.8	-163.2	-44.2	-36.7	19.6	135.8	-6.3	-148.5
26	-3.3	-173.7	-45.4	-48.5	18.8	92.8	-4.4	-156.9
27	-3.0	175.5	-46.5	-43.8	17.8	52.7	-3.7	-169.0
28	-2.5	166.4	-43.7	-45.2	17.1	13.2	-3.0	-179.9
29	-2.5	155.4	-43.2	-59.5	16.8	-26.3	-2.7	171.2
30	-2.8	146.3	-42.0	-81.7	17.3	-69.6	-2.7	161.4
31	-3.9	144.4	-46.4	-112.7	18.0	-123.9	-2.6	156.1
32	-2.8	154.3	-47.9	-148.6	17.2	168.4	-2.5	150.5

Refer to the "definition of the Sij reference planes" section below.

Typical Package Sij parameters for high current configuration

Tamb = +25°C, Vd = +4,5V Pads: B, C, F grounded.

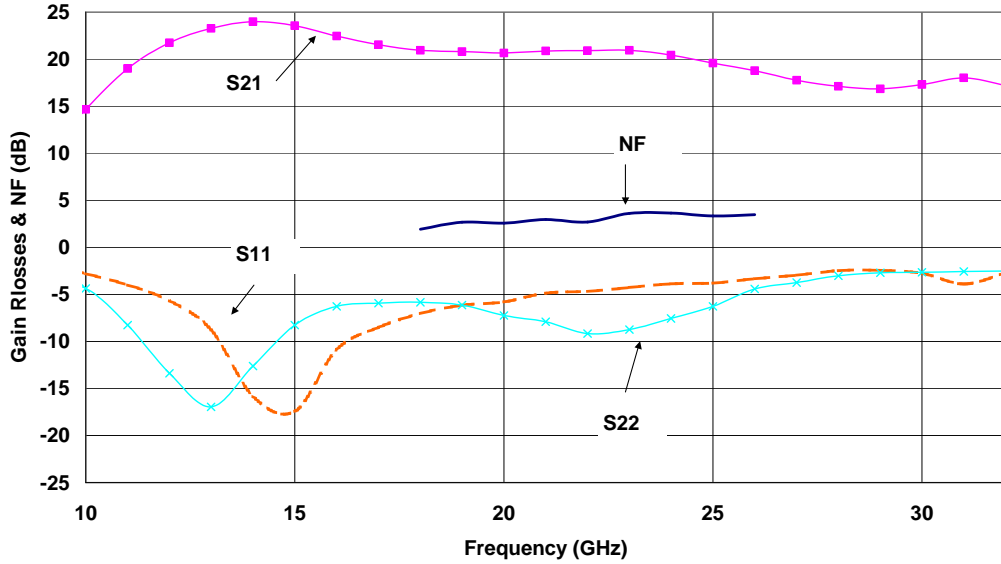
F (GHz)	S11	S11	S12	S12	S21	S21	S22	S22
	dB	∠°	dB	∠°	dB	∠°	dB	∠°
2	-0.1	-58.5	-92.2	81.8	-57.9	0.4	-0.7	-146.6
3	-0.1	-88.9	-67.1	55.2	-69.1	-41.4	-1.1	159.3
4	-0.1	-122.6	-62.8	100.3	-51.5	77.3	-1.0	114.1
5	-0.2	-159.2	-63.0	51.4	-37.2	145.1	-1.5	73.0
6	-0.4	158.4	-56.6	15.4	-17.7	97.4	-1.9	40.1
7	-0.7	110.4	-64.5	-49.7	-3.8	31.4	-2.2	8.3
8	-1.3	60.8	-67.3	88.2	5.3	-49.4	-3.4	-21.8
9	-1.8	13.6	-61.5	-7.6	10.6	-120.9	-4.6	-40.0
10	-2.9	-27.8	-59.6	-45.7	15.6	177.2	-4.8	-68.3
11	-4.0	-60.9	-54.4	176.7	19.9	110.8	-8.5	-89.9
12	-5.6	-92.1	-53.9	99.3	22.7	43.0	-12.5	-90.4
13	-8.5	-123.1	-50.6	22.2	24.2	-22.2	-16.3	-76.8
14	-14.6	-169.0	-52.1	-32.8	25.1	-84.9	-13.8	-40.8
15	-19.5	26.2	-50.3	-120.6	24.8	-145.6	-8.9	-46.4
16	-11.3	-23.8	-49.4	165.3	23.6	161.3	-6.5	-65.0
17	-8.5	-49.1	-50.9	132.8	22.6	115.2	-6.0	-86.1
18	-6.9	-67.5	-46.9	122.6	21.8	73.8	-5.8	-101.6
19	-6.1	-83.9	-44.9	88.3	21.5	32.7	-6.1	-119.7
20	-5.6	-97.1	-43.0	53.7	21.2	-7.8	-7.0	-134.2
21	-4.6	-109.1	-44.1	21.4	21.3	-48.7	-7.6	-144.5
22	-4.4	-123.2	-45.4	19.8	21.3	-90.2	-9.0	-153.5
23	-4.1	-135.7	-43.9	7.2	21.4	-133.4	-9.4	-152.7
24	-3.7	-149.8	-43.4	-10.0	21.0	-178.9	-8.8	-151.9
25	-3.8	-162.0	-44.3	-34.6	20.3	138.4	-7.6	-155.6
26	-3.5	-173.4	-44.5	-42.2	19.7	94.7	-5.5	-161.7
27	-3.3	174.4	-47.4	-45.9	18.7	53.4	-4.5	-172.3
28	-3.0	164.8	-44.8	-39.0	18.0	12.8	-3.6	177.3
29	-2.9	153.8	-43.6	-43.1	17.6	-27.1	-3.0	168.4
30	-2.9	143.4	-41.7	-66.2	18.0	-70.8	-2.6	158.1
31	-3.8	138.2	-44.6	-91.4	18.4	-123.8	-2.6	150.7
32	-2.7	145.3	-49.9	-140.7	17.8	169.5	-2.6	144.6

Refer to the “definition of the Sij reference planes” section below.

Typical PCB Measured Performance

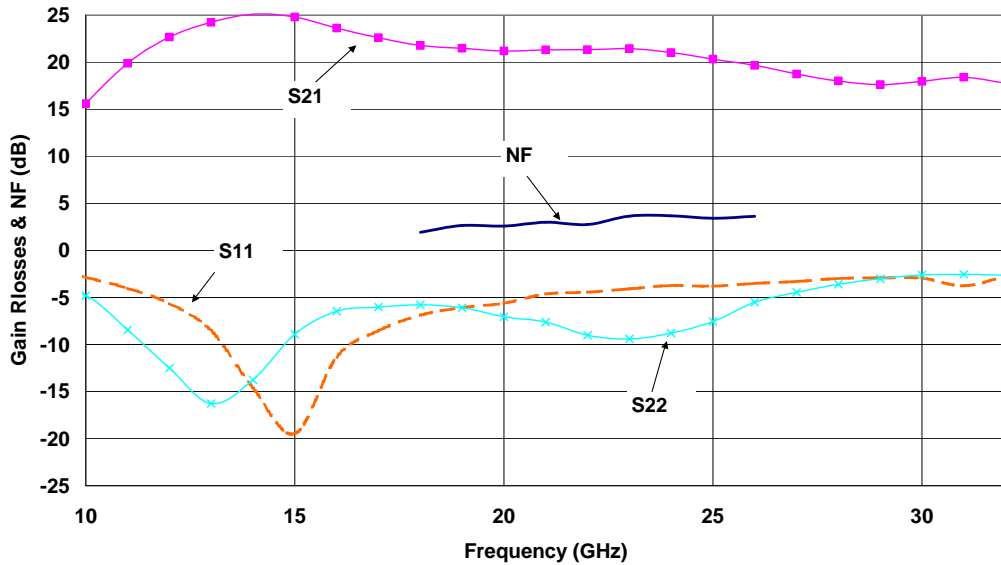
Tamb = +25°C, Vd = +4,5V

Gain / Return losses and NF @ low current config. (BDE grounded)



NF Gain and Losses in the package access planes, using the proposed land pattern & board 95541.

Gain / Return losses and NF @ high current config. (BCF grounded)

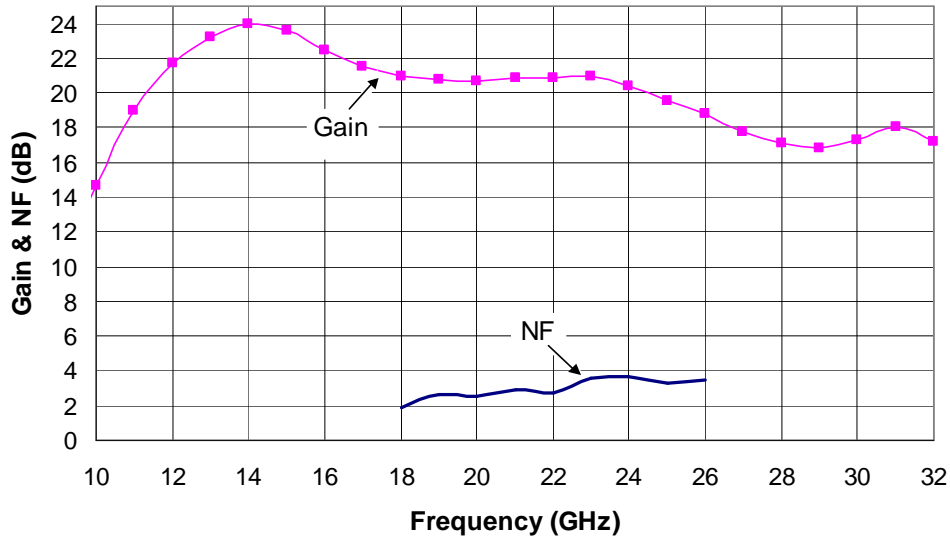


NF Gain and Losses in the package access planes, using the proposed land pattern & board 95541

Typical PCB Measured Performance

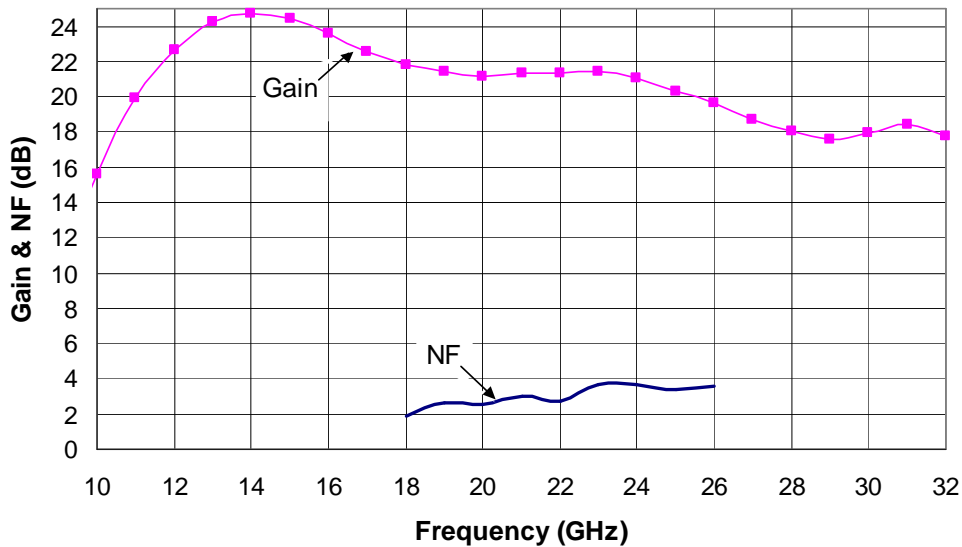
Tamb = +25°C, Vd = +4,5V

Gain and NF @ low current config. (BDE grounded)



NF and Gain in the package access planes, using the proposed land pattern & board 95541

Gain and NF @ high current config. (BCF grounded)

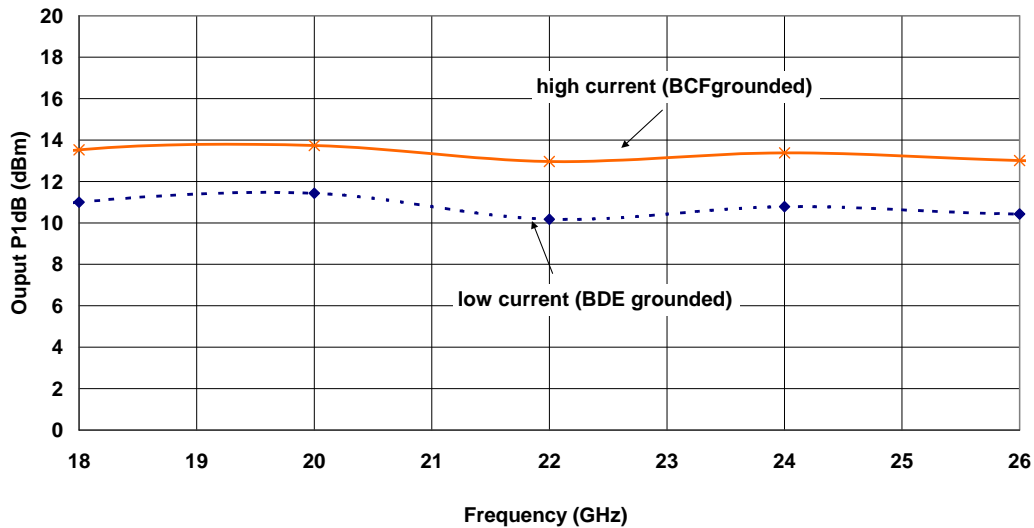


NF and Gain in the package access planes, using the proposed land pattern & board 95541

Typical PCB Measured Performance

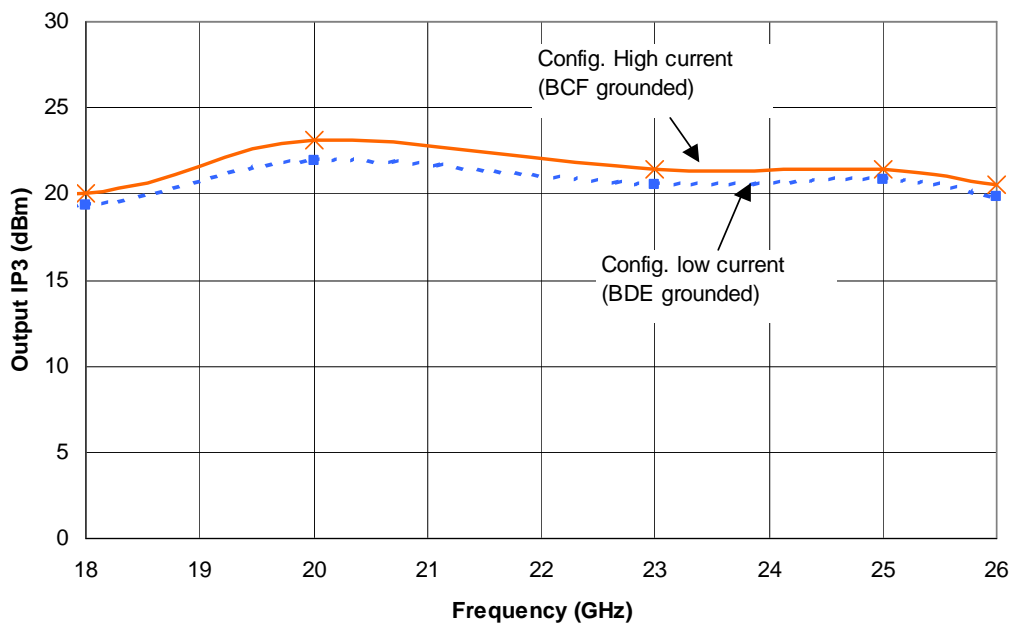
Tamb = +25°C, Vd = +4,5V

Typical Output 1 dB compression



Typical Pout -1dB in the package, using the proposed land pattern & board 95541.

Typical Output IP3 vs Frequency @ Pout/tone=-5 dBm

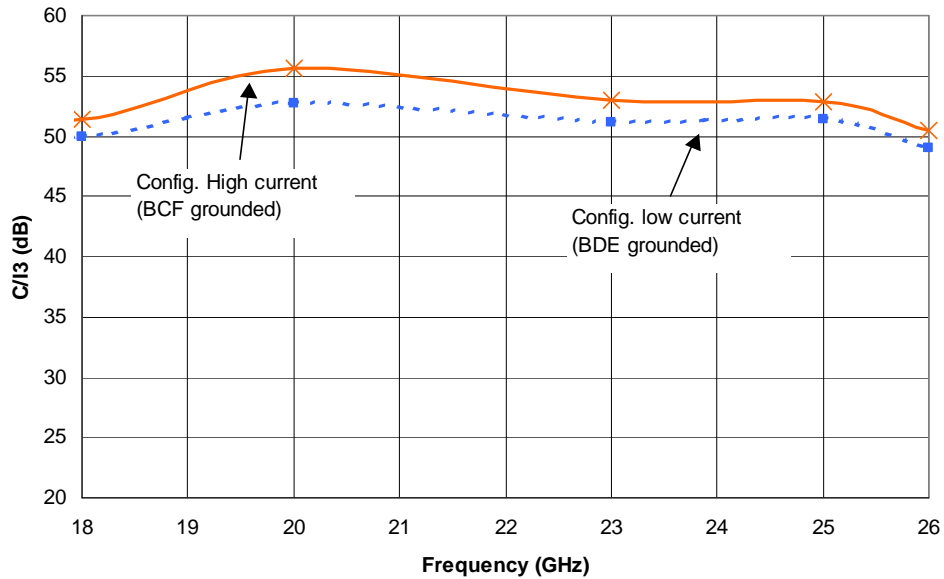


Typical Output IP3 in the package, using the proposed land pattern & board 95541.

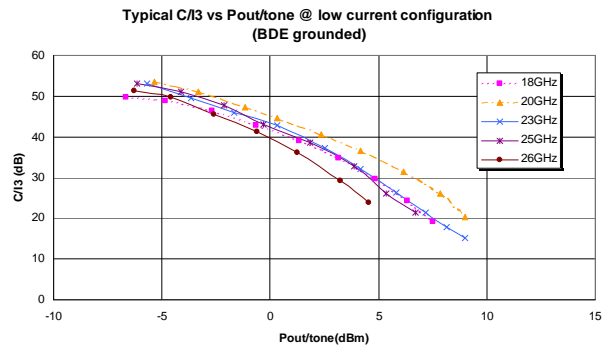
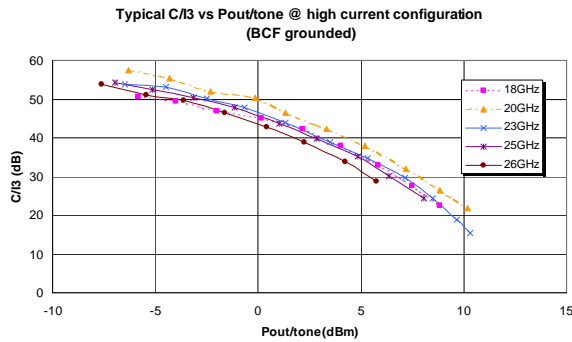
Typical PCB Measured Performance

Tamb = +25°C, Vd = +4,5V

Typical C/I3 vs Frequency @ Pout/tone=-5 dBm



Typical C/I3 versus frequency, using the proposed land pattern & board 95541.

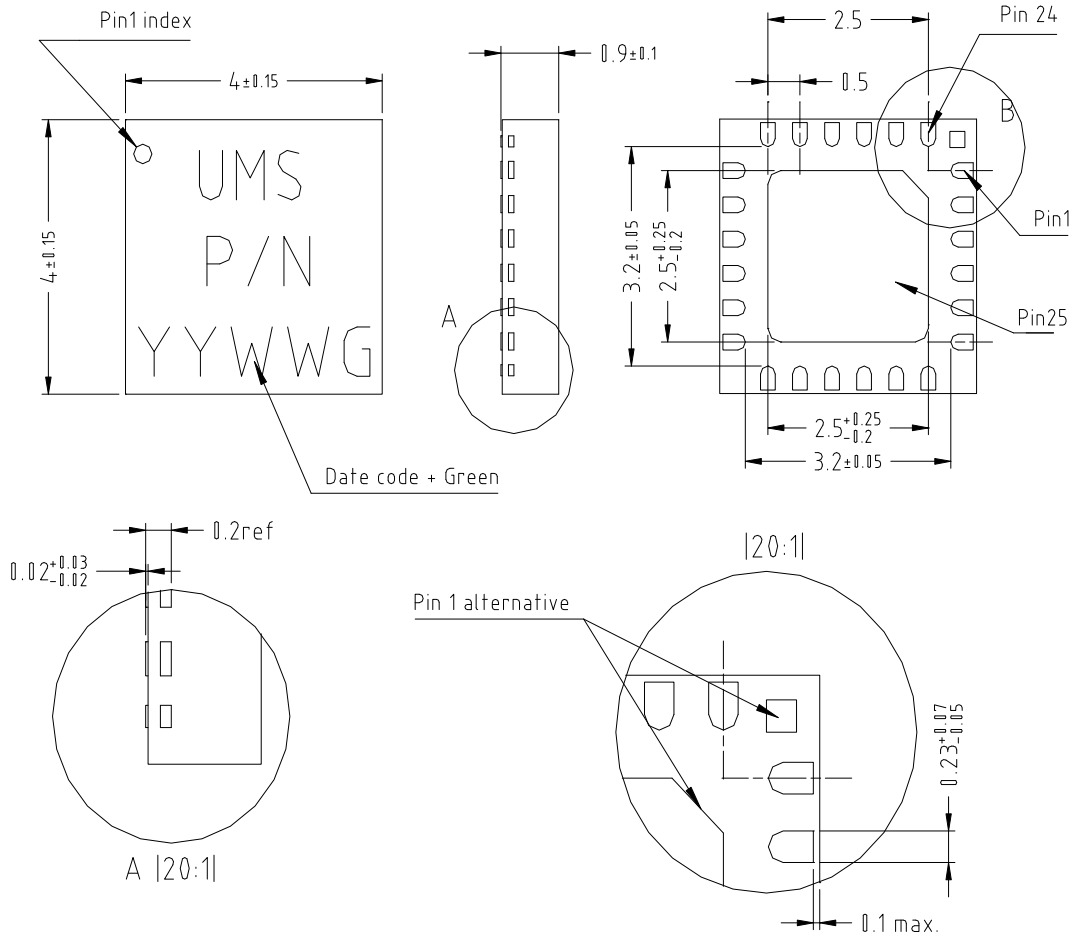


Typical C/I3 versus output power, using the proposed land pattern & board 95541.

CHA2069-QDG

18-30GHz Low Noise Amplifier

Package outline:



Matt tin, Lead Free

(Green)

Units

mm

From the standard

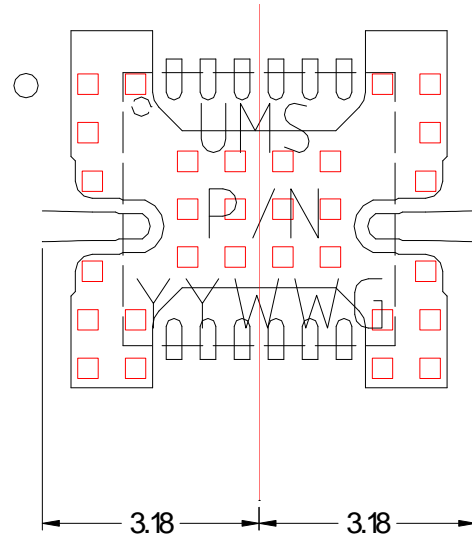
JEDEC MO-220

25- GND

1- NC	9- D	17- NC
2- NC	10- NC	18- NC
3- GND	11- E	19- Vd1,2,3
4- RF in	12- F	20- Vd1,2,3
5- GND	13- NC	21- Vg3
6- NC	14- GND	22- Vg2
7- B	15- RF out	23- Vg1
8- C	16- GND	24- NC

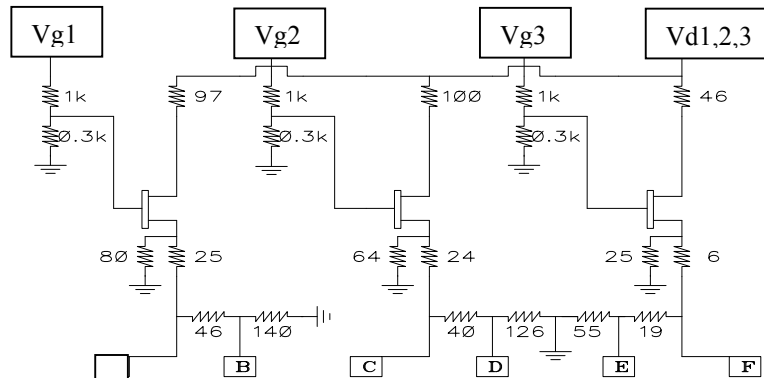
Definition of the Sij reference planes

The reference planes are defined from the footprint of the recommended characterization board 95541 shown below. The reference is the symmetrical axis of the package. The input and output reference planes are located at 3.18mm offset (input wise and output wise respec.) from this axis. Then, the given Sij incorporates this land pattern.



Circuit Biasing options

This circuit is self-biased, and flexibility is provided by the access to number of pads. the internal DC electrical schematic is given in order to use these pads in a safe way.



The two requirements are:

N°1: Not exceed $V_{ds} = 3.5V$ (internal Drain to S ource voltage).

N°2: Not biased in such a way that Vgs becomes positive. (Internal Gate to Source voltage)

We propose two standard biasing:
Low Noise and low consumption:

$V_d = 4.5V$ and B, D, E grounded.
All the other pads non connected (NC).
 $I_{dd} = 65mA$ & $P_{out-1dB} = 10.5dBm$ Typical.

(Equivalent to B, C, D, E, F: non connected and $V_d=4.5V$; $V_{g1}=V_{g2}=V_{g3}=+1. V$).

Low Noise and higher output power

$V_d = 4.5V$ and B, C, F grounded.
All the other pads non connected (NC).
 $I_{dd} = 85mA$ & $P_{out-1dB} = 13.5dBm$ Typical..

Application note

The design of the motherboard has a strong impact on the overall performance since the transition from the motherboard to the package is comparably large. In case of the SMD type packages of United Monolithic Semiconductors the motherboard should be designed according to the information given in the following to achieve good performance. Other configurations are also possible but can lead to different results. If you need advice please contact United Monolithic Semiconductors for further information.

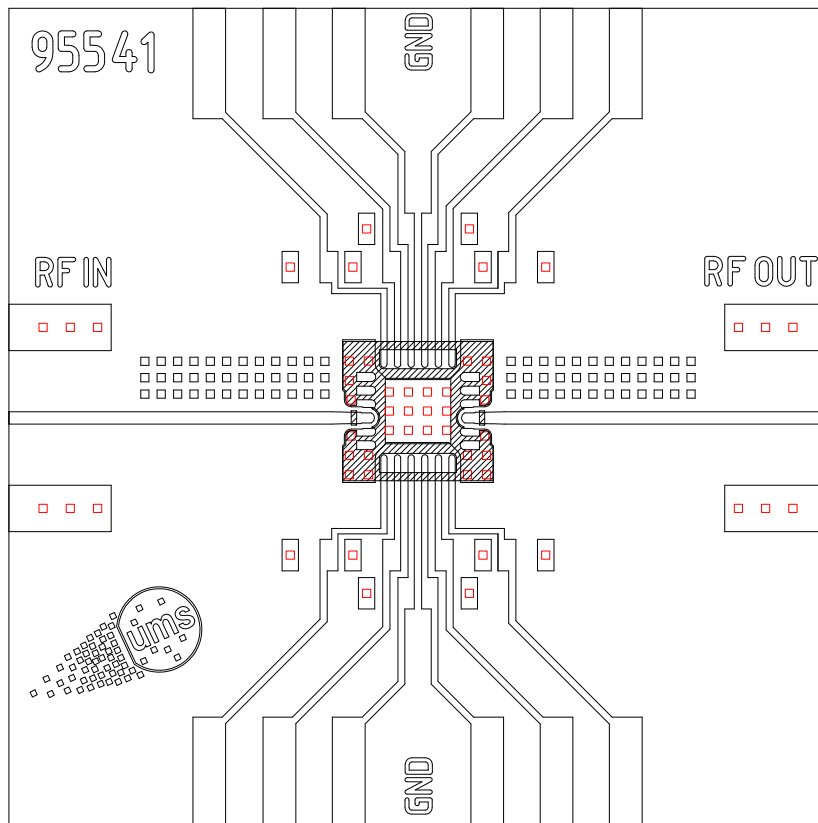
SMD type packages of UMS should allow design and fabrication of micro- and mm-wave modules at low cost. Therefore, a suitable motherboard environment has been chosen. All tests and verifications have been performed on Rogers RO4003. This material exhibits a permittivity of 3.38 and has been used with a thickness of 200 μ m [8 mils] and a 1/2oz or less copper cladding. The corresponding 50Ohm transmission line has a strip width of about 460 μ m [approx. 18 mils].

The contact areas on the motherboard for the package connections should be designed according to the footprint given below. The proper via structure under the ground pad is very important in order to achieve a good RF and lifetime performance. All tests have been done by using a grid of plated through vias with a diameter of less than 300 μ m [12 mils] and a spacing of less than 700 μ m [28 mils] from the centres of two adjacent vias. The via grid should cover the whole space under the ground pad and the vias closest to the RF ports should be located near the edge of the pad to allow a good RF ground connection. Since the vias are important for heat transfer, a proper via filling should be guaranteed during the mounting procedure to get a low thermal resistance between package and heat sink. For power devices the use of heat slugs in the motherboard instead of a grid of vias is recommended.

For the mounting process the SMD type package can be handled as a standard surface mount component. The use of either solder or conductive epoxy is possible. The solder thickness after reflow should be typical 50 μ m [2 mils] and the lateral alignment between the package and the motherboard should be within 50 μ m [2 mils]. Caution should be taken to obtain a good and reliable contact over the whole pad areas. Voids or other improper connections, in particular, between the ground pads of motherboard and package will lead to a deterioration of the RF performance and the heat dissipation. The latter effect can reduce drastically reliability and lifetime of the product.

Proposed Assembly board "95941" for the 24L-QFN4x4 products characterization.

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



Sub-band enhancement

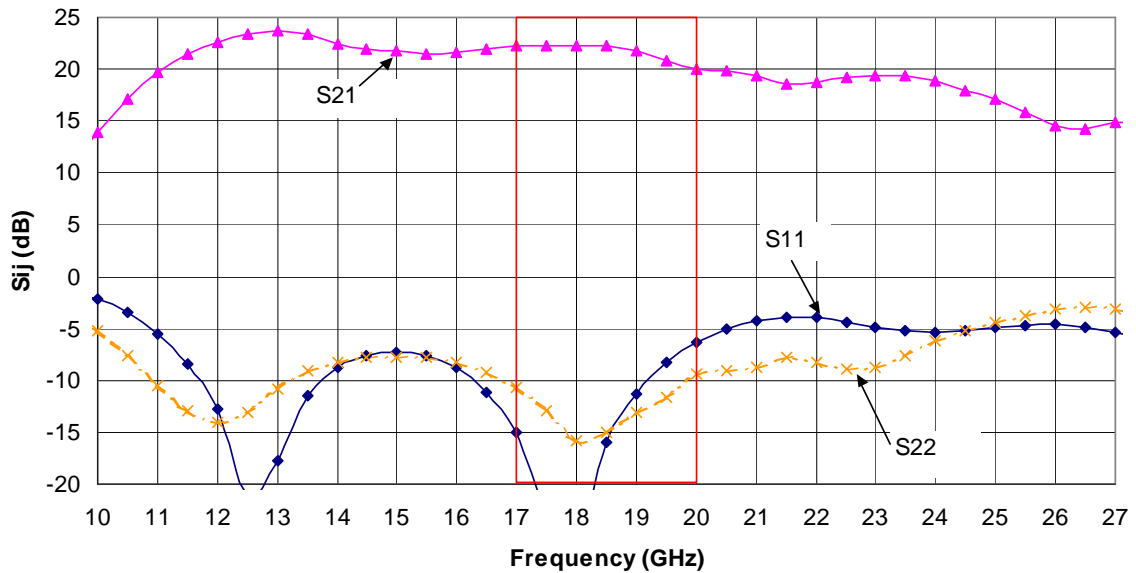
The performances of this product can be enhanced in sub-bands using external matching components such as very simple combination of micro-strip stubs. For some sub-bands, matching networks have been implemented and some typical results are shown below. For further details see the application notes listed below.

Matched Sub-band	Application note reference
17-20GHz	AN0010_CHA2069QDG_17-20
21-24GHz	AN0011_CHA2069QDG_21-24
24.5-26.5GHz	AN0012_CHA2069QDG_24_5-26_5

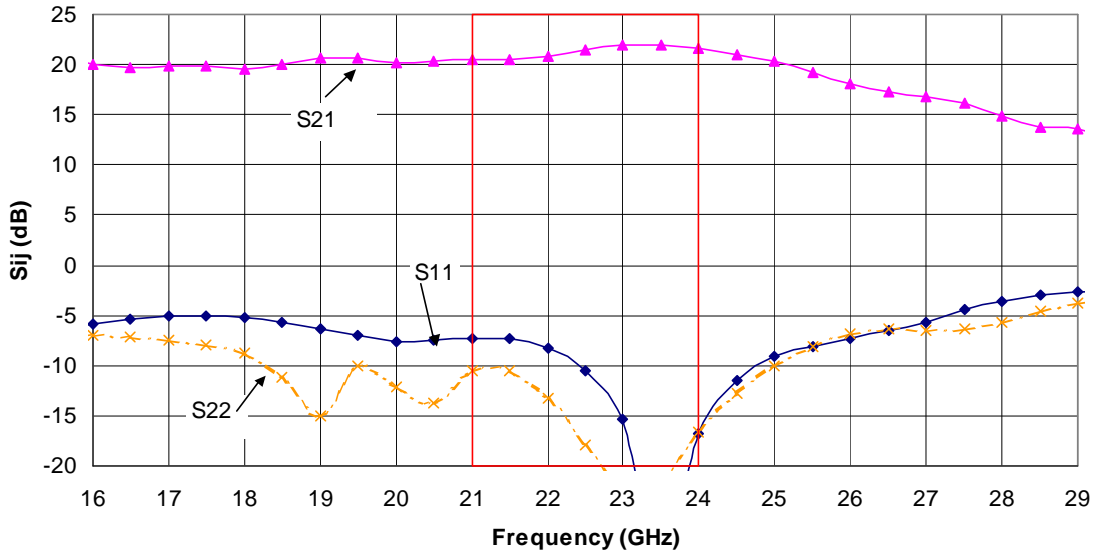
Of course, based on the S_{ij} matrix given previously, more accurate, or dedicated frequency boards may be derived.

The following graphs show S parameters obtained thanks to the external matching networks described in the application notes quoted in the list above.

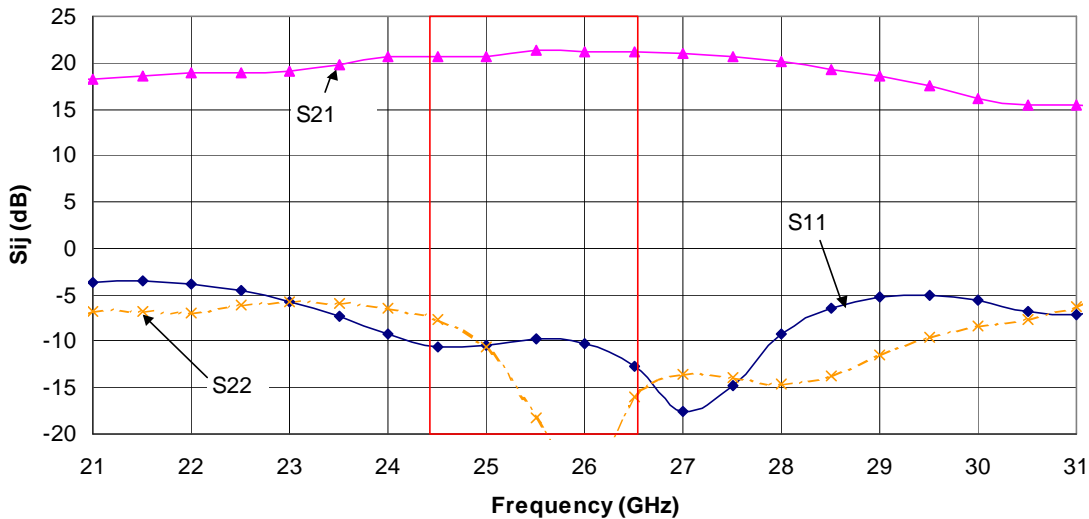
**Typical S parameters with matching network for the 17-20GHz band
Config. High current (BCFgrounded)**



Typical S parameters with matching network for the 21-24GHz band
 Config. High current (BCFgrounded)



Typical S parameters with matching network
 for the 24.5-26.5GHz band
 Config. High current (BCFgrounded)



Ordering Information

QFN 4x4 RoHS compliant package: CHA2069-QDG/XY
Stick: XY = 20 Tape & reel: XY = 21

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