GENERAL DESCRIPTION

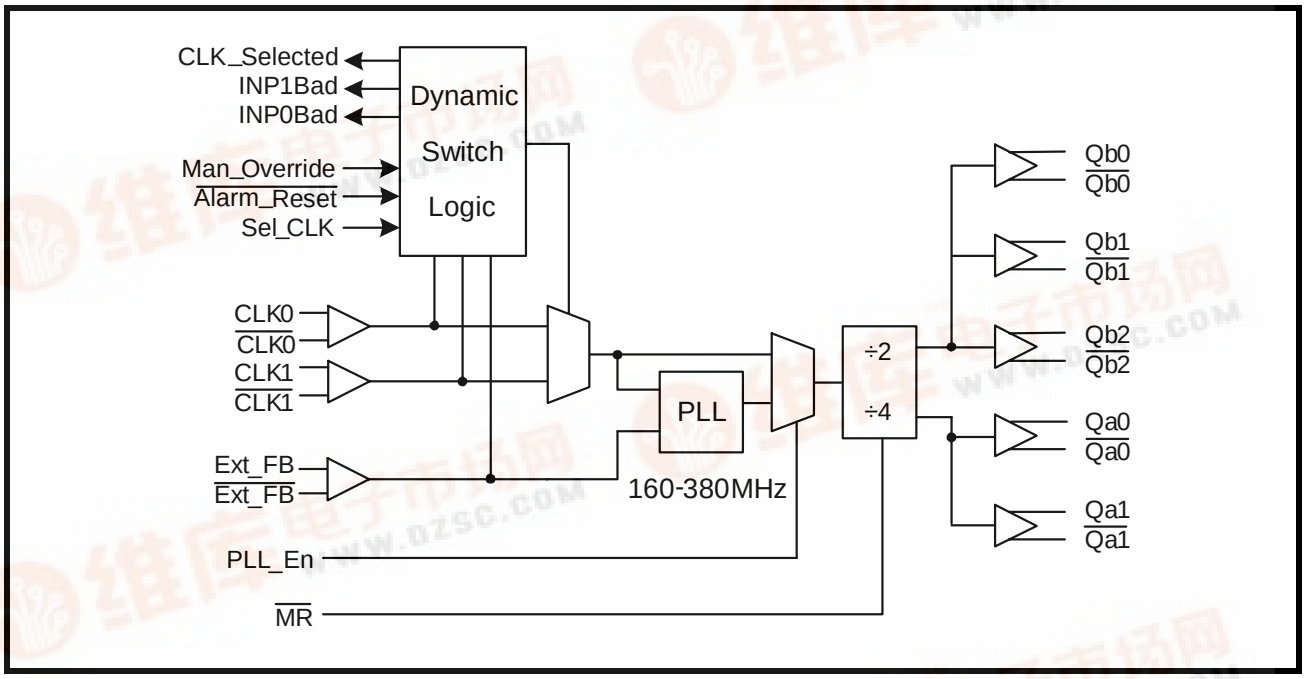
The XRK799J93 is a PLL clock driver designed specifically for redundant clock tree designs. The device receives two differential LVPECL clock signals from which it generates 5 new differential LVPECL clock outputs. Two of the output pairs regenerate the input signals frequency and phase while the other three pairs generate 2x, phase aligned clock outputs. External PLL feedback is used to also provide zero delay buffer performance.

The XRK799J93 Intelligent Dynamic Clock Switch circuit continuously monitors both input CLK signals. Upon detection of a failure (CLK stuck HIGH or LOW for at least 1 period), the INP_BAD for that CLK will be latched (H). If that CLK is the primary clock, the device will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance. The typical phase bump caused by a failed clock is eliminated.

FEATURES

- Fully Integrated PLL
- Intelligent Dynamic Clock Switch
- LVPECL Clock Outputs
- LVCMOS Control I/O
- 3.3V Operation
- 32-Lead TQFP Packaging

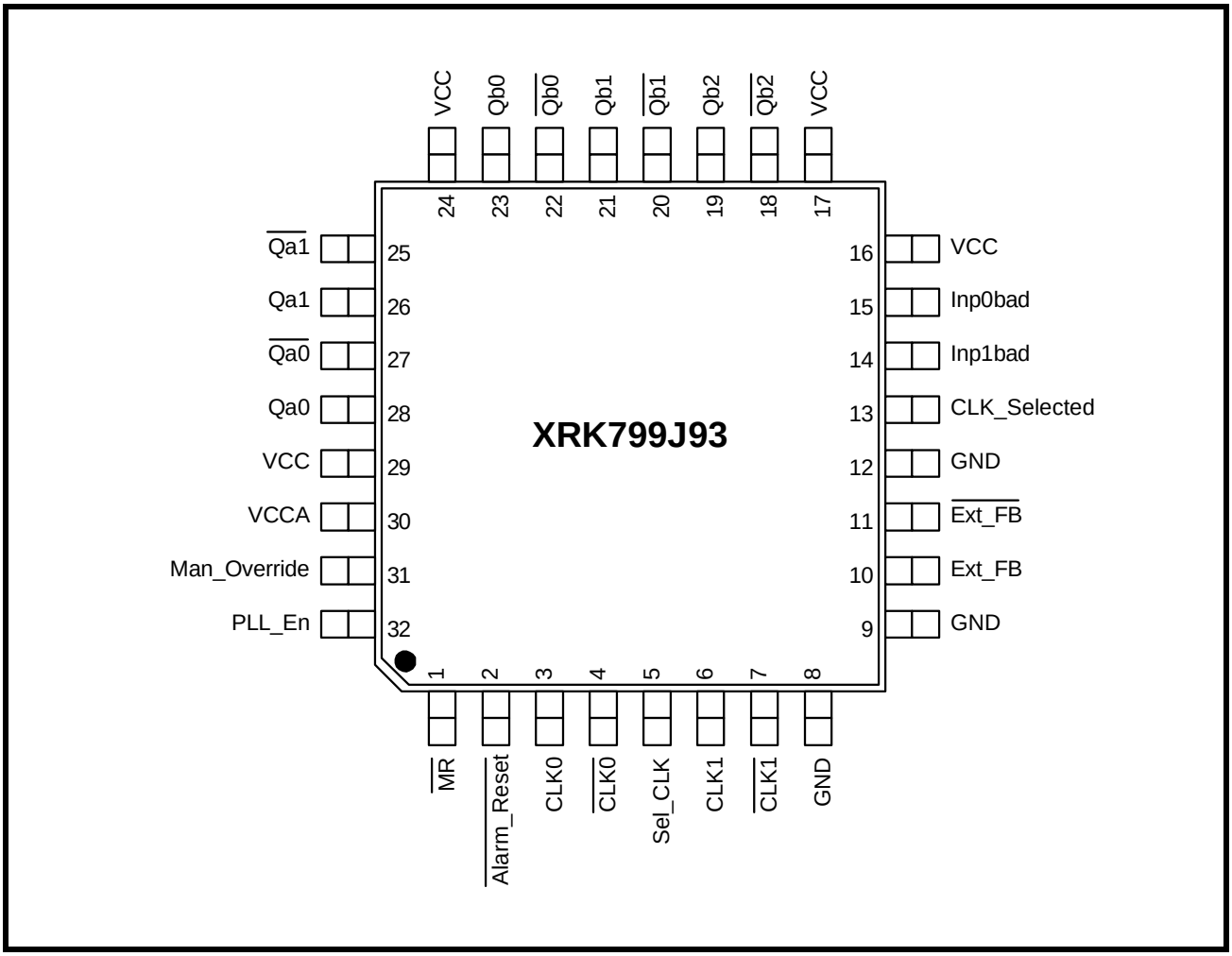
FIGURE 1. BLOCK DIAGRAM OF THE XRK799J93



PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRK799J93IQ	32-Lead TQFP	-40°C to +85°C

FIGURE 2. PIN OUT OF THE XRK799J93



PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$	LVPECL Input LVPECL Input	Clock 0 - Differential PLL clock reference (CLK0 pulldown, $\overline{\text{CLK0}}$ pulldown) Clock 1 - Differential PLL clock reference (CLK1 pulldown, $\overline{\text{CLK1}}$ pulldown)
Ext_FB, $\overline{\text{Ext\_FB}}$	LVPECL Input	Differential PLL feedback clock (Ext_FB pulldown, $\overline{\text{Ext\_FB}}$ pulldown)
Qa[1:0], $\overline{\text{Qa[1:0]}}$	LVPECL Output	Differential 1x output pairs, connect one QaX pair to Ext_FB
Qb[2:0], $\overline{\text{Qb[2:0]}}$	LVPECL Output	Differential 2x output pairs
Inp0bad	LVCMOS Output	Indicates detection of a bad input reference Clock 0 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted.
Inp1bad	LVCMOS Output	Indicates detection of a bad input reference Clock 1 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted.
CLK_Selected	LVCMOS Output	0 - if CLK0 is selected 1 - if CLK1 is selected
$\overline{\text{Alarm\_Reset}}$	LVCMOS Input	0 - will reset the input bad flags and align CLK_Selected with Sel_CLK. The input is one-shotted 1 - normal operation (50KΩ pullup).
Sel_CLK	LVCMOS Input	0 - selects CLK0 1 - selects CLK1 (50kΩ pulldown)
Man_Override	LVCMOS Input	0 - normal operation 1 - disables internal clock switch circuitry (50KΩ pulldown).
PLL_En	LVCMOS Input	0 - bypasses the phase-locked loop, input CLKx directly drives divider block 1 - selected input reference applied to PLL (50KΩ pullup).
$\overline{\text{MR}}$	LVCMOS Input	0 - resets the internal dividers forcing outputs LOW. Asynchronous to the clock 1 - normal operation (50KΩ pullup).
VCCA	Power Supply	PLL power supply
VCC	Power Supply	Digital power supply
GNDA	Power Supply	PLL Ground
GND	Power Supply	Digital Ground

ABSOLUTE MAXIMUM RATINGS[a]

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT	CONDITION
V_{CC}	Supply Voltage	-0.3	3.9	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3		V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

GENERAL SPECIFICATIONS

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	CONDITION
V_{TT}	Output termination voltage		V_{CC}-2		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	Thermal resistance junction to ambient JESD 51-3, single layer test board JESD 51-6, multilayer test board			 62.0 47	 °C/W °C/W	Natural convection
θ_{JC}	Thermal resistance junction to case			14	°C/W	
	Operating junction temperature			115	°C	

DC CHARACTERISTICS (V_{CC}= 3.3 ± 5%, T_A= -40°C TO +85°C)

SYMBOL	CHARACTERISTICS		MIN	TYP	MAX	UNIT	CONDITION
LVCMOS control inputs ($\overline{MR}$, PLL_En, Sel_CLK, Man_Override, $\overline{Alarm\_Reset}$)							
V_{IH}	Input voltage high		2.0		VCC+0.3	V	
V_{IL}	Input voltage low				0.8	V	
I_{IN}	Input Current	Man_Override, Sel_CLK (pull down)			100	µA	V_{IN}=V_{CC}
		PLL_En, $\overline{MR}$, $\overline{Alarm\_Reset}$ (pull up)	-100			µA	V_{IN}=GND
LVCMOS Control Outputs							
V_{OH}	Output High Voltage		2.0			V	I_{OH}=-10mA
V_{OL}	Output Low Voltage				0.55	V	I_{OL}=10mA
LVPECL clock inputs (CLK, $\overline{CLK}$)[b]							
I_{IN}	Input current				±100	µA	V_{IN} =V_{CC} or V_{IN} =GND
LVPECL clock outputs (Qa[1:0], $\overline{Qa[1:0]}$, Qb[2:0], $\overline{Qb[2:0]}$)							
V_{OH}	Output high voltage		V_{CC}-1.2		V_{CC}-0.7	V	Termination 50Ω to V_{TT}
V_{OL}	Output low voltage		V_{CC}-1.9		V_{CC}-1.45	V	Termination 50Ω to V_{TT}
Supply Current							
I_{GND}	Maximum ground supply current - gnd pins				180	mA	GND pins
I_{CCPLL}	Maximum PLL power supply - VCC_PLL pin				15	mA	V_{CCPLL} pin

a. Inputs have internal pullup/pulldown resistors which affect the input current.

b. Clock inputs driven by LVPECL compatible signals.

AC CHARACTERISTICS (V_{CC}= 3.3 ± 5%, T_A= -40°C TO +85°C) [f]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
f_{ref}	Input Reference Frequency ÷4 feedback	40		95	MHz	Locked
f_{VCO}	PLL VCO Lock Range	160		380	MHz	Qa output used for feedback
f_{MAX}	Output Frequency Qa[1:0] Qb[2:0]	40 80		95 190	MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_{pd}	Propagation Delay CLKn to Ext_FB (SPO) [c] CLKn to Q (Bypass)	-150		 150 5	 ps ns	 PLL_En=1 PLL_En=0
V_{PP}	Differential peak-to-peak input voltage [g]	0.25		1.3	V	
V_{CMR}	Differential input crosspoint voltage [h]	V_{CC}-1.7		V_{CC}-0.3	V	
t_{skew}	Output-to-Output Skew Within Qa[1:0] or Qb[2:0] All outputs			 50 80	 ps	
$\Delta_{per/cycle}$	Rate of change of periods Qa[1:0] [d] Qb[2:0] [d] Qa[1:0] [e] Qb[2:0] [e]			 50 25 400 200	 ps/ cycle	
DC	Output duty cycle	45		55	%	
t_{jitter}	Cycle-to-cyle jitter, Standard deviation (RMS)			40	ps	@ f_{ref} =75MHZ
t_{lock}	Maximum PLL lock time			10	ms	
t_r/t_f	Output Rise/Fall time	50		700	ps	

c. Static phase offset between the selected reference clock and the feedback signal.

d. Specification holds for a clock switch between two signals no greater than 400ps out of phase. Delta period change per cycle is averaged over the clock switch excursion. (See Applications Information section for more detail)

e. Specification holds for a clock switch between two signals no greater than ±π out of phase. Delta period change per cycle is averaged over the clock switch excursion.

f. PECL output termination is 50 ohms to VCC – 2.0V.

g. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristic including SPO, device and part-to-part skew. Applicable to CLK0, CLK1 and Ext_FB.

h. V_{CMR} is the crosspoint of the differential input signal. Normal operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} specification. Violation of V_{CMR} or V_{PP} impacts the SPO, device and part-to-part skew. Applicable to CLK0, CLK1 and Ext_FB.

APPLICATIONS INFORMATION

The XRK799J93 is a dual clock PLL with on–chip Intelligent Dynamic Clock Switch circuitry.

DEFINITIONS

primary clock: The input CLK selected by Sel_Clk.

secondary clock: The input CLK NOT selected by Sel_Clk.

PLL reference signal: The CLK selected as the PLL reference signal by Sel_Clk or the Intelligent Dynamic Clock Switch. The Intelligent Dynamic Clock Switch can override Sel_Clk.

STATUS FUNCTIONS

Clk_Selected: Clk_Selected (L) indicates CLK0 is selected as the PLL reference signal. Clk_Selected (H) indicates CLK1 is selected as the PLL reference signal.

Inp0bad, Inp1bad: Inp0bad is latched (H) when CLK0 is stuck (H) or (L) for at least one Ext_FB period, or if one of the inputs CLK0 or $\overline{CLK0}$ is floating. Inp1bad is latched (H) when CLK1 is stuck (H) or (L) for at least one Ext_FB period, or if one of the inputs CLK1 or $\overline{CLK1}$ is floating. Both Inp0bad and Inp1bad are latched (H) when Ext_FB is stuck (H) or (L) for at least one Qa period, or if one of the inputs Ext_FB or $\overline{Ext\_FB}$ is floating. Both Inp0bad and Inp1bad are cleared (L) on assertion of $\overline{Alarm\_Reset}$. The status functions Inp0bad and Inp1bad are active for Man_Override (H) or (L).

CONTROL FUNCTIONS

Sel_Clk: Sel_Clk (L) selects CLK0 as the primary clock. Sel_Clk (H) selects CLK1 as the primary clock.

$\overline{Alarm\_Reset}$*:* Asserted by a negative edge. Generates a one–shot reset pulse that clears INPUT_BAD latches and Clk_Selected latch.

PLL_En: While (L), the PLL reference signal is substituted for the VCO output.

$\overline{MR}$*:* While (L), internal dividers are held in reset which holds all Q outputs LOW.

MAN OVERRIDE (H)

(IDCS is disabled, PLL functions normally). PLL reference signal (as indicated by Clk_Selected) will always be the CLK selected by Sel_Clk. If Ext_FB misses at least one pulse, Qa and Qb outputs will drop to a minimum frequency (~20MHz) for 1-uS, or until Ext_FB shows any activity, whichever is longer. This prevents the Qa and Qb frequencies from rising due the PLL incorrectly interpreting an intermittent Ext_FB as a VCO running too slow.

MAN OVERRIDE (L)

Intelligent Dynamic Clock Switch is enabled. The first CLK to fail will latch it's INP_BAD (H) status flag and select the other input as the Clk_Selected for the PLL reference clock. Once latched, the Clk_Selected and INP_BAD remain latched until assertion of Alarm_Reset which clears all latches (INP_BADs are cleared and Clk_Selected = Sel_Clk).

If both Inp0bad and Inp1bad are (H), either due to both CLK0 and CLK1 having missed at least 1 pulse each or Ext_FB having missed at least 1 pulse, then Qa and Qb outputs will drop to a minimum frequency (~20MHz) until such time as Alarm_Reset_b is asserted.

NOTE: *If both CLKs are bad when Alarm_Reset is asserted, both INP_BADs will be latched (H) after one Ext_FB period and Clk_Selected will be latched (L) indicating CLK0 is the PLL reference signal. While neither INP_BAD is latched (H), the Clk_Selected can be freely changed with Sel_Clk. Whenever a CLK switch occurs, (manually or by the Intelligent Dynamic Clock Switch), following the next negative edge of the newly selected PLL reference signal, the next positive edge pair of Ext_FB and the newly selected PLL reference signal will slew to alignment.*

To calculate the overall uncertainty between the input CLKs and the outputs from multiple XRK799J93's, the following procedure should be used. Assuming that the input CLKs to all XRK799J93's are exactly in phase, the total uncertainty will be the sum of the static phase offset, max I/O jitter, and output to output skew.

During a dynamic switch, the output phase between two devices may be increased for a short period of time. If the two input CLKs are 400ps out of phase, a dynamic switch of an XRK799J93 will result in an instantaneous phase change of 400ps to the PLL reference signal without a corresponding change in the output phase (due to the limited response of the PLL). As a result, the I/O phase of a device, undergoing this switch, will initially

be 400ps and diminish as the PLL slews to its new phase alignment. This transient timing issue should be considered when analyzing the overall skew budget of a system.

HOT INSERTION AND WITHDRAWAL

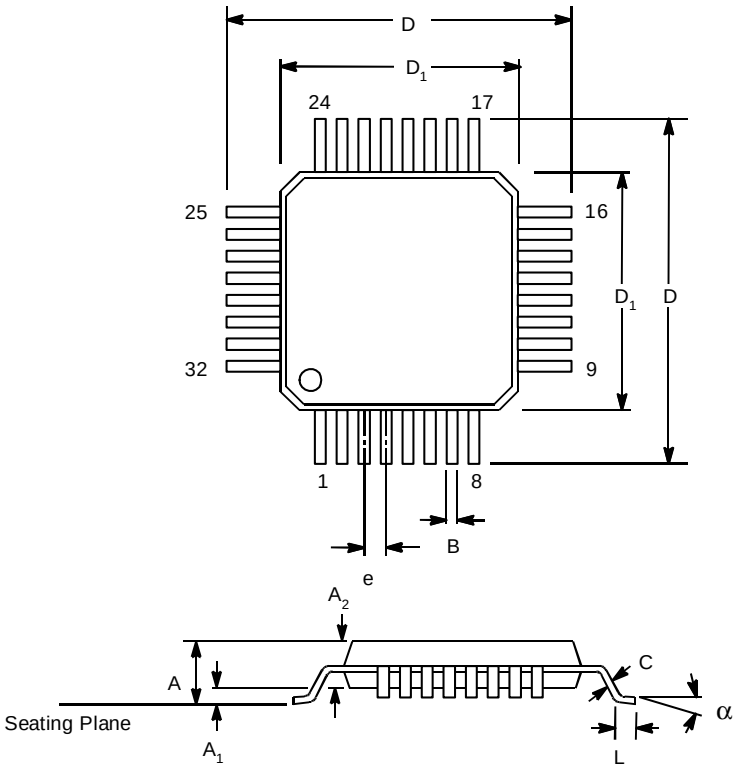
In PECL applications, a powered up driver will experience a low impedance path through an XRK799J93 input to its powered down VCC pins. In this case, a 100 ohm series resistance should be used in front of the input pins to limit the driver current. The resistor will have minimal impact on the rise and fall times of the input signals.

ACQUIRING FREQUENCY LOCK

1. While the XRK799J93 is receiving a valid CLK signal, assert Man_Override HIGH.
2. The PLL will phase and frequency lock within the specified lock time.
3. Apply a HIGH to LOW transition to $\overline{\text{Alarm\_Reset}}$ to reset Input Bad flags.
4. De–assert Man_Override LOW to enable Intelligent Dynamic Clock Switch mode.

PACKAGE DIMENSIONS

32 LEAD THIN QUAD FLAT PACK
(7 x 7 x 1.4 mm TQFP)
rev. 2.00



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
1.0.0	June 14, 2005	Initial release.
1.0.1	December 15, 2006	Edit block diagram and update pull-up resistors.