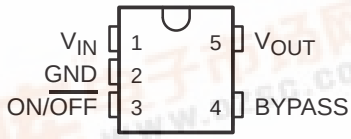
LP2985LV
150-mA LOW-NOISE, LOW-DROPOUT REGULATOR WITH SHUTDOWN FOR OUTPUT VOLTAGES <2.3 V

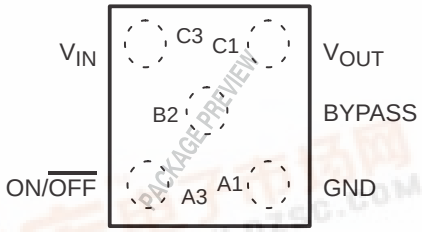
SLVS552 – OCTOBER 2004

- Available in the Texas Instruments NanoStar™ and NanoFree™ Wafer Chip Scale Packages
- Output Tolerance of:
  - 1% (A Grade)
  - 1.5% (Standard Grade)
- Ultra Low Dropout, Typically 280 mV at Full Load of 150 mA
- Wide V_{IN} Range . . . 16 V (Max)
- Low I_Q . . . 850 µA at Full Load at 150 mA
- Shutdown Current . . . 0.01 µA Typ
- Low Noise . . . 30 μV_{RMS} With 10-nF Bypass Capacitor
- Stable With Low ESR Capacitors, Including Ceramic
- Over-Current and Thermal Protection
- High Peak Current Capability
- For V_{OUT} Options ≥2.5 V, See LP2985 Data Sheet
- Portable Applications
  - Cellular Phones
  - Palmtop and Laptop Computers
  - Personal Digital Assistants (PDAs)
  - Digital Cameras and Camcorders
  - CD Players
  - MP3 Players

DBV (SOT-23) PACKAGE
(TOP VIEW)



YEQ, YEU, YZQ, OR YZU (WCSP) PACKAGE
(TOP VIEW)



description/ordering information

The LP2985LV family of fixed-output, low-dropout regulators offers exceptional, cost-effective performance for both portable and nonportable applications. Available in voltages of 1.25 V, 1.35 V, 1.5 V, 1.7 V, 1.8 V, and 2 V, the family has an output tolerance of 1% for the A version (1.5% for the non-A version), and is capable of delivering 150-mA continuous load current. Standard regulator features, such as over-current and over-temperature protection, are included.

The LP2985LV has a host of features that makes the regulator an ideal candidate for a variety of portable applications:

- Low dropout: A PNP pass element allows a typical dropout of 280 mV at 150-mA load current.
- Low quiescent current: The use of a vertical PNP process allows for quiescent currents that are considerably lower than those associated with traditional lateral PNP regulators.
- Shutdown: A shutdown feature is available, allowing the regulator to consume only 0.01 µA when the ON/$\overline{\text{OFF}}$ pin is pulled low.
- Low-ESR-capacitor friendly: The regulator is stable with low ESR capacitors, allowing for the use of small, inexpensive ceramic capacitors in cost-sensitive applications.

description/ordering information (continued)

- Low noise: The BYPASS pin allows for low noise operation, with a typical output noise of 30 μV (RMS) with the use of a 10-nF bypass capacitor.
- Small packaging: For the most space-constraint needs, the regulator is available in SOT-23 package, as well as NanoStar™ wafer chip scale packaging, offering an even smaller size with improved thermal and electrical characteristics. NanoStar package technology is a major breakthrough in IC packaging concepts, using the die as the package.

ORDERING INFORMATION

T_J	PART GRADE	V_{OUT} (NOM)	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 125°C	A grade: 1% tolerance	1.25 V	SOT23-5 (DBV)	Reel of 3000	LP2985A-12DBVR	PREVIEW
				Reel of 250	LP2985A-12DBVT	
		1.35 V		Reel of 3000	LP2985A-13DBVR	PREVIEW
				Reel of 250	LP2985A-13DBVT	
		1.5 V		Reel of 3000	LP2985A-15DBVR	PREVIEW
				Reel of 250	LP2985A-15DBVT	
		1.7 V		Reel of 3000	LP2985A-17DBVR	PREVIEW
				Reel of 250	LP2985A-17DBVT	
		1.8 V		Reel of 3000	LP2985A-18DBVR	LPT_
				Reel of 250	LP2985A-18DBVT	
		2 V		Reel of 3000	LP2985A-20DBVR	PREVIEW
				Reel of 250	LP2985A-20DBVT	
		1.25 V	NanoStar™ − WCSP 0.17-mm Bump (YEQ)	Reel of 3000	LP2985A-12YEQR	PREVIEW
		1.35 V			LP2985A-13YEQR	PREVIEW
		1.5 V			LP2985A-15YEQR	PREVIEW
		1.7 V			LP2985A-17YEQR	PREVIEW
		1.8 V			LP2985A-18YEQR	PREVIEW
		2 V			LP2985A-20YEQR	PREVIEW
		1.25 V	NanoFree™ − WCSP 0.17-mm Bump (YZQ, Pb-free)	Reel of 3000	LP2985A-12YZQR	PREVIEW
		1.35 V			LP2985A-13YZQR	PREVIEW
		1.5 V			LP2985A-15YZQR	PREVIEW
		1.7 V			LP2985A-17YZQR	PREVIEW
		1.8 V			LP2985A-18YZQR	PREVIEW
		2 V			LP2985A-20YZQR	PREVIEW
		1.25 V	NanoStar™ − WCSP 0.30-mm Bump (YEU)	Reel of 3000	LP2985A-12YEUR	PREVIEW
		1.35 V			LP2985A-13YEUR	PREVIEW
		1.5 V			LP2985A-15YEUR	PREVIEW
		1.7 V			LP2985A-17YEUR	PREVIEW
		1.8 V			LP2985A-18YEUR	PREVIEW
		2 V			LP2985A-20YEUR	PREVIEW
		1.25 V	NanoFree™ − WCSP 0.30-mm Bump (YZU, Pb-free)	Reel of 3000	LP2985A-12YZUR	PREVIEW
		1.35 V			LP2985A-13YZUR	PREVIEW
		1.5 V			LP2985A-15YZUR	PREVIEW
		1.7 V			LP2985A-17YZUR	PREVIEW
		1.8 V			LP2985A-18YZUR	PREVIEW
		2 V			LP2985A-20YZUR	PREVIEW

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV: The actual top-side marking has one additional character that designates the assembly/test site.
YEQ/YZQ, YEU/YZU: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

description/ordering information (continued)

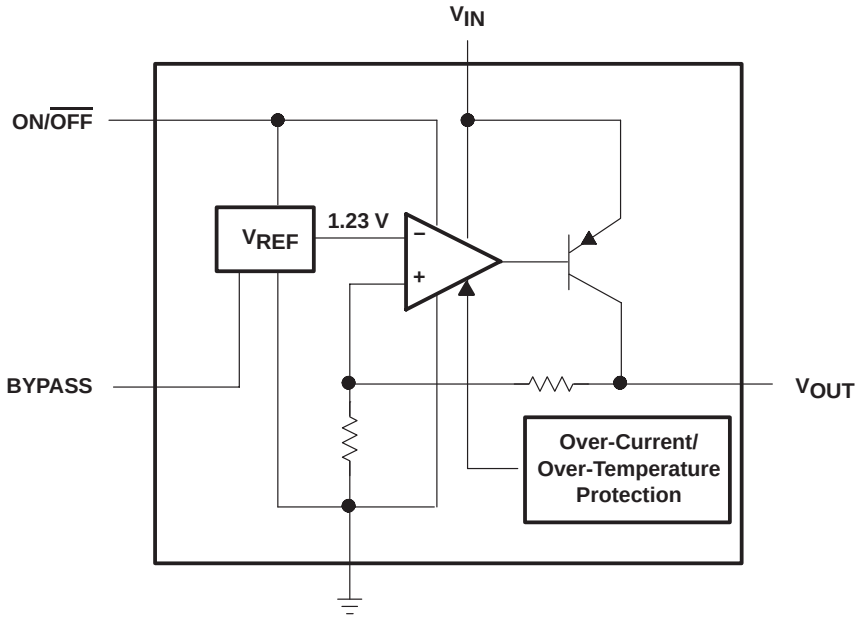
ORDERING INFORMATION

T_J	PART GRADE	V_{OUT} (NOM)	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 125°C	Standard grade: 1.5% tolerance	1.25 V	SOT-23 (DBV)	Reel of 3000	LP2985-12DBVR	PREVIEW
				Reel of 250	LP2985-12DBVT	
		1.35 V		Reel of 3000	LP2985-13DBVR	PREVIEW
				Reel of 250	LP2985-13DBVT	
		1.5 V		Reel of 3000	LP2985-15DBVR	PREVIEW
				Reel of 250	LP2985-15DBVT	
		1.7 V		Reel of 3000	LP2985-17DBVR	PREVIEW
				Reel of 250	LP2985-17DBVT	
		1.8 V		Reel of 3000	LP2985-18DBVR	LPH_
				Reel of 250	LP2985-18DBVT	
		2 V		Reel of 3000	LP2985-20DBVR	PREVIEW
				Reel of 250	LP2985-20DBVT	
		1.25 V	NanoStar™ – WCSP 0.17-mm Bump (YEQ)	Reel of 3000	LP2985-12YEQR	PREVIEW
		1.35 V			LP2985-13YEQR	PREVIEW
		1.5 V			LP2985-15YEQR	PREVIEW
		1.7 V			LP2985-17YEQR	PREVIEW
		1.8 V			LP2985-18YEQR	PREVIEW
		2 V			LP2985-20YEQR	PREVIEW
		1.25 V	NanoFree™ – WCSP 0.17-mm Bump (YZQ, Pb free)	Reel of 3000	LP2985-12YZQR	PREVIEW
		1.35 V			LP2985-13YZQR	PREVIEW
		1.5 V			LP2985-15YZQR	PREVIEW
		1.7 V			LP2985-17YZQR	PREVIEW
		1.8 V			LP2985-18YZQR	PREVIEW
		2 V			LP2985-20YZQR	PREVIEW
		1.25 V	NanoStar™ – WCSP 0.30-mm Bump (YEU)	Reel of 3000	LP2985-12YEUR	PREVIEW
		1.35 V			LP2985-13YEUR	PREVIEW
		1.5 V			LP2985-15YEUR	PREVIEW
		1.7 V			LP2985-17YEUR	PREVIEW
		1.8 V			LP2985-18YEUR	PREVIEW
		2 V			LP2985-20YEUR	PREVIEW
		1.25 V	NanoFree™ – WCSP 0.30-mm Bump (YZQ, Pb free)	Reel of 3000	LP2985-12YZUR	PREVIEW
		1.35 V			LP2985-13YZUR	PREVIEW
		1.5 V			LP2985-15YZUR	PREVIEW
		1.7 V			LP2985-17YZUR	PREVIEW
		1.8 V			LP2985-18YZUR	PREVIEW
		2 V			LP2985-20YZUR	PREVIEW

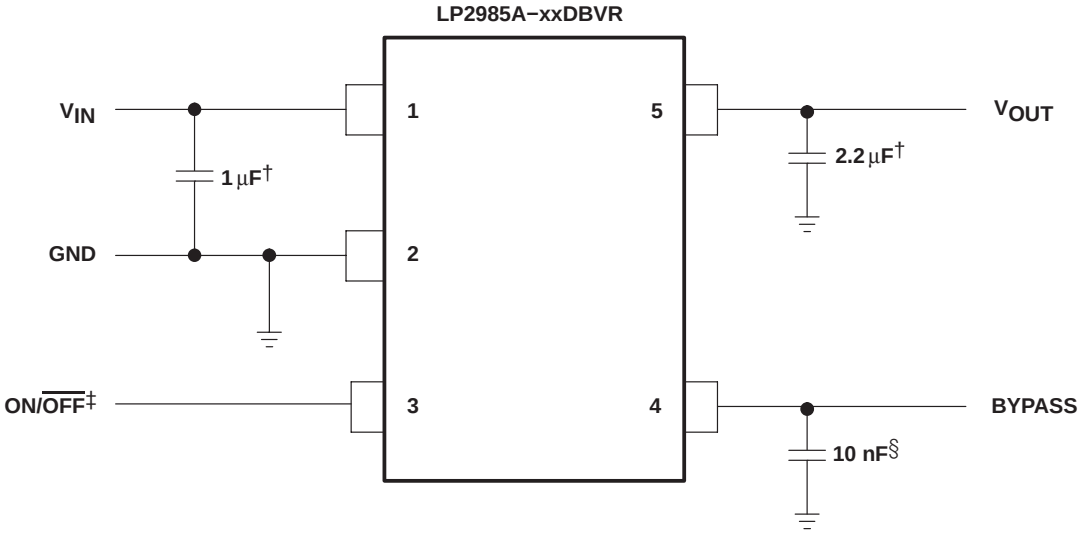
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV: The actual top-side marking has one additional character that designates the assembly/test site.
YEQ/YZQ, YEU/YZU: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

functional block diagram



basic application circuit



† Minimum C_{OUT} value for stability (can be increased without limit for improved stability and transient response)
‡ ON/OFF must be actively terminated. Connect to V_{IN} if shutdown feature is not used.
§ Optional BYPASS capacitor for low noise operation

absolute maximum ratings over the virtual junction temperature range (unless otherwise noted)†

Continuous input voltage range . . . . . −0.3 V to 16 V
ON/$\overline{\text{OFF}}$ input voltage range . . . . . −0.3 V to 16 V
Output voltage range (see Note 1) . . . . . −0.3 V to 9 V
Input/output voltage differential, V_{IN}-V_{OUT} (see Note 2) . . . . . −0.3 V to 16 V
Output current, I_O (see Note 3) . . . . . Internally limited (short-circuit protected)
Package thermal impedance, θ_{JA} (see Notes 3 and 4): DBV package . . . . . 206°C/W
YEQ/YZQ package . . . . . TBD°C/W
YEU/YZU package . . . . . TBD°C/W
Operating virtual junction temperature . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. If load is returned to a negative power supply in a dual supply system, the output must be diode clamped to GND.
2. The PNP pass transistor has a parasitic diode connected between the input and output. This diode is normally reversed bias ($V_{IN} > V_{OUT}$) but will be forward biased if the output voltage exceeds the input voltage by a diode drop (see Application Information for more details).
3. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{IN}	Supply input voltage	2.2	16	V
$V_{ON/\overline{OFF}}$	ON/$\overline{\text{OFF}}$ input voltage	−0.3	V_{IN}	V
I_{OUT}	Output current		150	mA
T_J	Virtual junction temperature	−40	125	°C

electrical characteristics at specified virtual junction temperature range, V_{IN} = V_{OUT} (nominal) + 1 V, $V_{ON/\overline{OFF}}$ = 2 V, C_{IN} = 1 µF, I_L = 1 mA, C_{OUT} = 4.7 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	LP2985A−XX			LP2985−XX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_{OUT}	Output voltage tolerance	I_L = 1mA	25°C	−1		1	−1.5		1.5	%V_{NOM}
		1 mA ≤ I_L ≤ 50 mA	25°C	−1.5		1.5	−2.5		2.5	
			−40°C to 125°C	−2.5		2.5	−3.5		3.5	
		1 mA ≤ I_L ≤ 150 mA	25°C	−2.5		2.5	−3.0		3.0	
			−40°C to 125°C	−3.5		3.5	−4.0		4.0	
	Line regulation	V_{IN} = [$V_{OUT(NOM)}$ + 1 V] to 16 V	25°C		0.007	0.014		0.007	0.014	%/V
			−40°C to 125°C			0.032			0.032	
$V_{IN(MIN)}$	Minimum V_{IN} to maintain output regulation (see Note 5)		25°C		2.05			2.05		V
			−40°C to 125°C			2.2			2.2	
V_{IN}-V_{OUT}	Dropout voltage (see Note 5)	I_L = 50 mA	25°C		120	150		120	150	mV
			−40°C to 125°C			250			250	
		I_L = 150 mA	25°C		280	350		280	350	
			−40°C to 125°C			600			600	
I_{GND}	Ground pin current	I_L = 0	25°C		65	95		65	95	µA
			−40°C to 125°C			125			125	
		I_L = 1 mA	25°C		75	110		75	110	
			−40°C to 125°C			170			170	
		I_L = 10 mA	25°C		120	220		120	220	
			−40°C to 125°C			400			400	
		I_L = 50 mA	25°C		350	600		350	600	
			−40°C to 125°C			1000			1000	
		I_L = 150 mA	25°C		850	1500		850	1500	
			−40°C to 125°C			2500			2500	
		$V_{ON/\overline{OFF}}$ < 0.3 V (OFF)	25°C		0.01	0.8		0.01	0.8	
		$V_{ON/\overline{OFF}}$ < 0.15 V (OFF)	−40°C to 105°C		0.05	2		0.05	2	
			−40°C to 125°C			5			5	
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage (see Note 6)	$V_{ON/\overline{OFF}}$= HIGH → (ON)	25°C		1.4			1.4		V
			−40°C to 125°C	1.6			1.6			
		$V_{ON/\overline{OFF}}$ = LOW → (OFF)	25°C		0.55			0.55		
			−40°C to 125°C			0.15			0.15	
$I_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input current	$V_{ON/\overline{OFF}}$ = 0	25°C		0.01			0.01		µA
			−40°C to 125°C			−2			−2	
		$V_{ON/\overline{OFF}}$ = 5 V	25°C		5			5		
			−40°C to 125°C			15			15	

NOTES: 5. Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below the value measured with a 1-V differential. Dropout limits may not apply because V_{IN} must be the greater of a) 2.2 V, or b) $V_{OUT(nom)}$ + dropout voltage (Max) in order to maintain output regulation.

6. The ON/$\overline{OFF}$ input must be properly driven for reliable operation (see Application Information).

electrical characteristics at specified virtual junction temperature range, V_{IN} = V_{OUT} (nominal) + 1 V, $V_{ON/OFF}$ = 2 V, C_{IN} = 1 µF, I_L = 1 mA, C_{OUT} = 4.7 µF (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_J	LP2985A−XX			LP2985−XX			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_n	Output noise (RMS)	BW = 300 Hz to 50 kHz, C_{OUT} = 10 µF, C_{BYPASS} = 10 nF, V_{OUT} = 1.8 V	25°C		30			30		µV
$\Delta V_{OUT}/\Delta V_{IN}$	Ripple rejection	f = 1kHz, C_{OUT} = 10 µF, C_{BYPASS} = 10 nF	25°C		45			45		dB
$I_{OUT(PK)}$	Peak output current	$V_{OUT} \geq V_{O(NOM)}$ − 5%	25°C		350			350		mA
$I_{OUT(SC)}$	Short circuit current	R_L = 0 (steady state) (see Note 7)	25°C		400			400		mA

NOTE 7: See Typical Characteristics Curve, Short-Circuit Current vs. V_{OUT}

APPLICATION INFORMATION

capacitors

input capacitor (C_{IN})

A minimum value of 1 μF (over the entire operating temperature range) is required at the input of the LP2985LV. In addition, this input capacitor should be located within 1 cm of the input pin and connected to a clean analog ground. There are no Equivalent Series Resistance (ESR) requirements for this capacitor and the capacitance can be increased without limit.

output capacitor (C_{OUT})

As an advantage over other regulators, the LP2985LV permits the use of low ESR capacitors at the output, including ceramic capacitors that can have an ESR as low as 5 mΩ. Of course, tantalum and film capacitors can also be used if size and cost are not issues. The output capacitor should also be located within 1 cm of the output pin and be returned to a clean analog ground.

As with other PNP LDOs, stability conditions require the output capacitor to have a minimum capacitance and an ESR that falls within a certain range.

Minimum C_{OUT}: 2.2 μF (can be increased without limit to improve transient response stability margin)

ESR range: See Figures 1 and 2

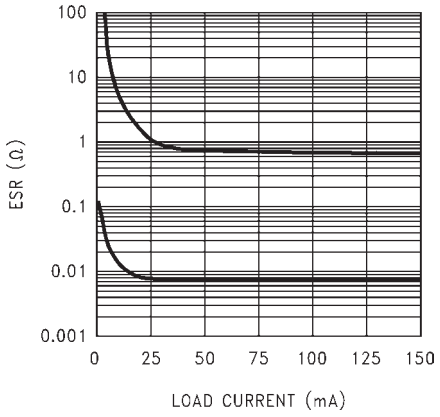


Figure 1. 2.2-μF Stable ESR Curves

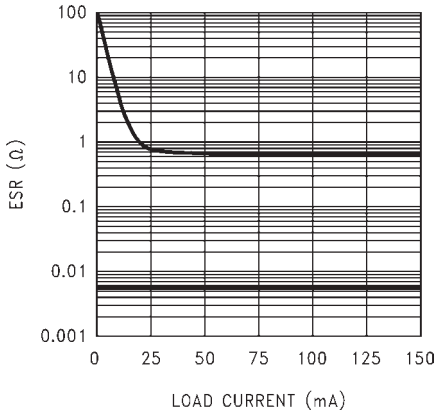


Figure 2. 4.7-μF Stable ESR Curves

APPLICATION INFORMATION

output capacitor (C_{OUT}) (continued)

It is critical that both the minimum capacitance and ESR requirement be met *over the entire operating temperature range*. Depending on the type of capacitors used, both these parameters can vary significantly with temperature (see Capacitor Characteristics section).

noise bypass capacitor (C_{BYPASS})

The LP2985LV allows for low noise performance with the use of a bypass capacitor that is connected to the internal band-gap reference via the BYPASS pin. This high-impedance band-gap circuitry is biased in the microampere range and, thus, cannot be loaded significantly, else its output − and correspondingly the output of the regulator − will change. Thus, for best output accuracy, dc leakage current through C_{BYPASS} should be minimized as much as possible and should never exceed 100 nA.

A 10-nF capacitor is recommended for C_{BYPASS}; ceramic and film capacitors are well suited for this purpose.

capacitor characteristics

ceramic

Ceramic capacitors are ideal choices for use on the output of the LP2985LV for several reasons. For capacitances in the range of 2.2 μF to 4.7 μF, ceramic capacitors have the lowest cost and the lowest ESR, making them choice candidates for filtering high-frequency noise. For instance, a typical 2.2-μF ceramic capacitor has an ESR in the range of 10 mΩ to 20 mΩ and satisfies minimum ESR requirements of the regulator.

Ceramic capacitors have one glaring disadvantage that must be taken into account − a poor temperature coefficient, where the capacitance can vary significantly with temperature. For instance, a large-value ceramic capacitor (≥2.2 μF) can lose more than half of its capacitance as temperature rises from 25°C to 85°C. Thus, a 2.2 μF at 25°C will drop well below the minimum C_{OUT} required for stability as ambient temperature rises. For this reason, select an output capacitor that maintains the minimum 2.2 μF required for stability over the *entire operating temperature range*. Note that there are some ceramic capacitors that can maintain a ±15% capacitance tolerance over temperature.

tantalum

Tantalum capacitors can be used at the output of the LP2985LV, but there are significant disadvantages that could prohibit their use.

- In the 1-μF to 4.7-μF range, tantalum capacitors are more expensive than ceramics of the equivalent capacitance and voltage ratings.
- Tantalum capacitors have higher ESRs than their equivalent-sized ceramic counterparts. Thus, to meet the ESR requirements, a higher-capacitance tantalum may be required, at the expense of larger size and higher cost.
- The ESR of a tantalum capacitor increases as temperature drops, as much as double from 25°C to −40°C. Thus, ESR margins must be maintained over the temperature range in order to prevent regulator instability.

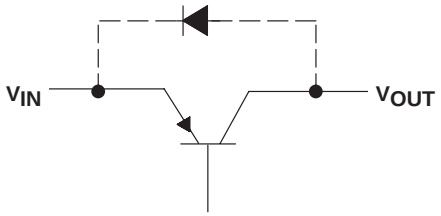
APPLICATION INFORMATION

ON/$\overline{\text{OFF}}$ operation

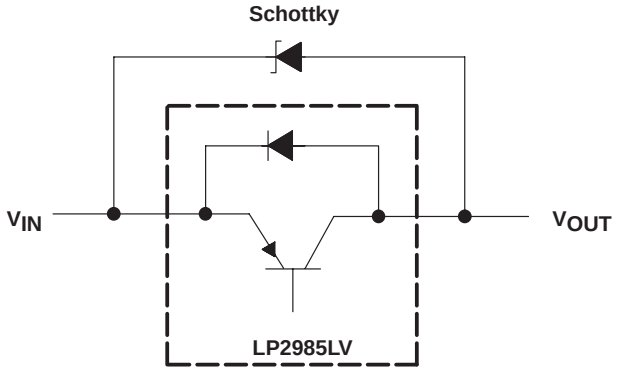
The LP2985LV allows for a shutdown mode via the ON/$\overline{\text{OFF}}$ pin. Driving the pin LOW (≤0.3 V) turns the device OFF, conversely, a HIGH (≥1.6 V) turns the device ON. If the shutdown feature is not used, the ON/$\overline{\text{OFF}}$ pin should be connected to the input to ensure that the regulator is on at all times. For proper operation, do not leave the ON/$\overline{\text{OFF}}$ pin unconnected and apply a signal with a slew rate of ≥40 mV/μs.

reverse input-output voltage

There is an inherent diode present across the PNP pass element of the LP2985LV.

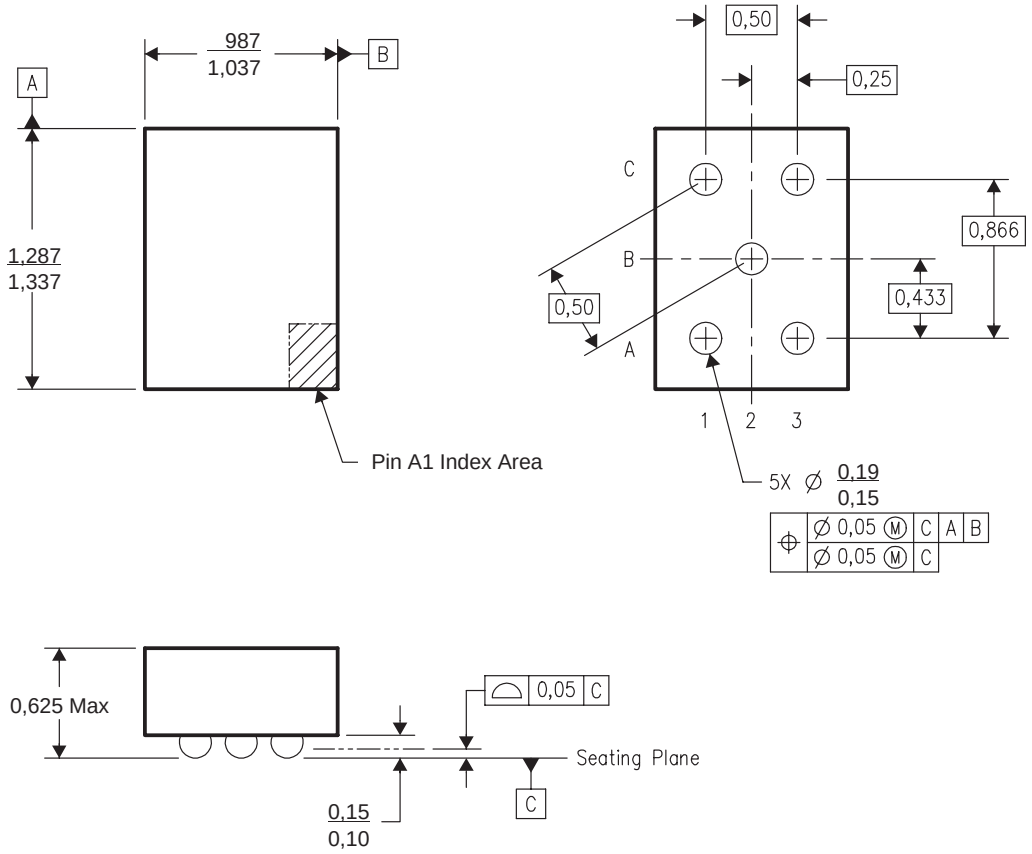


With the anode connected to the output, this diode is reverse biased during normal operation since the input voltage is higher than the output. However, if the output is pulled higher than the input for any reason, this diode will be forward biased and can cause a parasitic silicon-controlled rectifier (SCR) to latch, resulting in high current flowing from the output to the input. Thus, to prevent possible damage to the regulator in any application where the output may be pulled above the input, an external Schottky diode must be connected between the output and input. With the anode on output, this Schottky limits the reverse voltage across the output and input pins to ∼0.3 V, preventing the regulator's internal diode from forward biasing.



WAFER CHIP SCALE INFORMATION

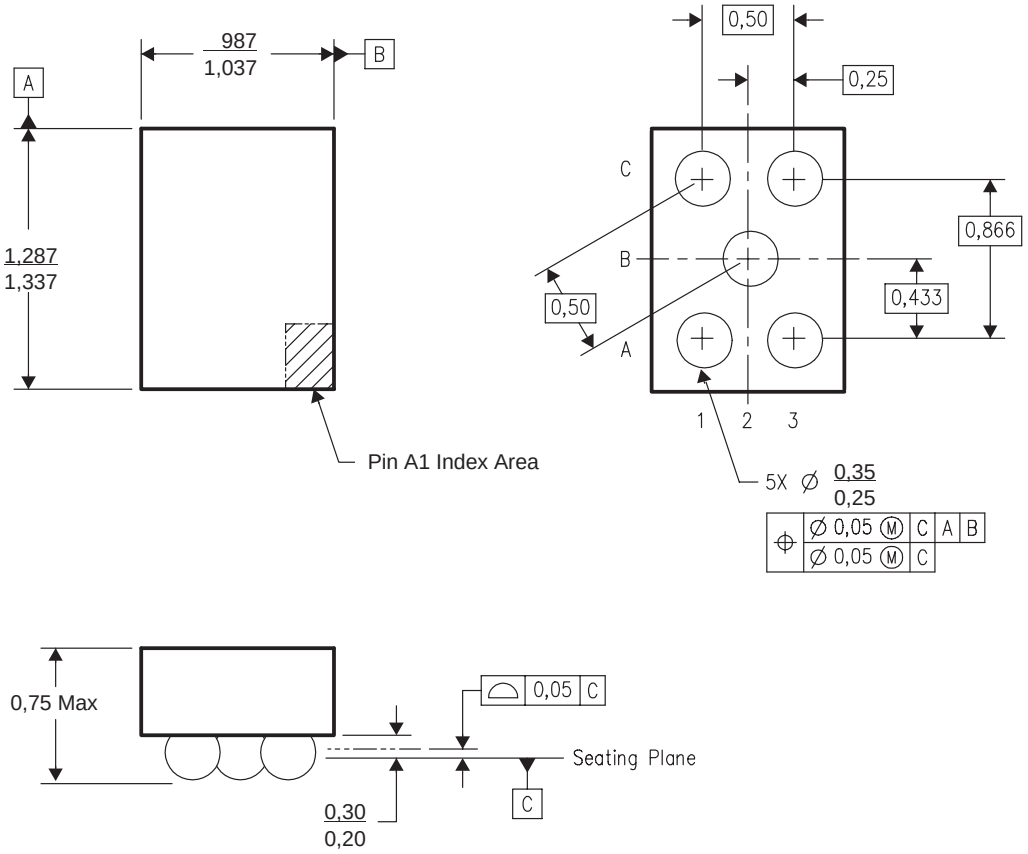
LP2985x-xxYEQ NanoStar (0.17-mm Bump)
LP2985x-xxYZQ NanoFree (0.17-mm Pb-Free Bump)



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar package configuration
D. This package is tin-lead (SnPb), consult the factory for availability of lead-free material.

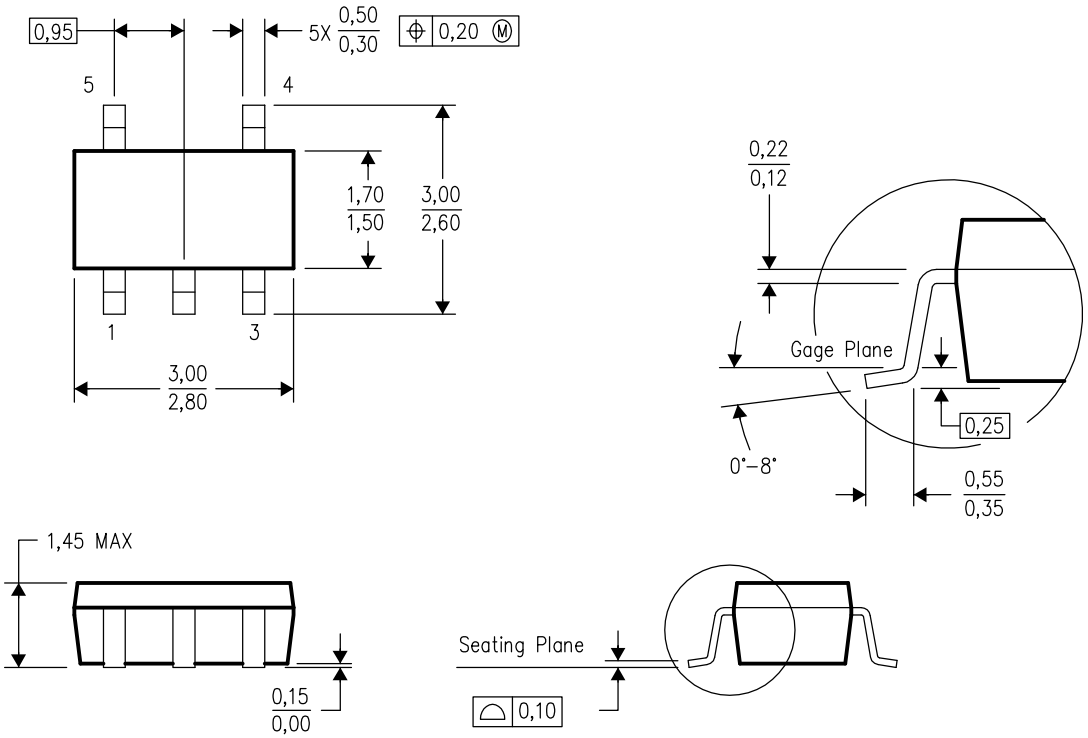
WAFER CHIP SCALE INFORMATION

LP2985x-xxYEU NanoStar (0.30-mm Bump)
LP2985x-xxYZU NanoFree (0.30-mm Pb-Free Bump)



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar package configuration
D. This package is tin-lead (SnPb), consult the factory for availability of lead-free material.

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–178 Variation AA.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265