ZARLINK SEMICONDUCTOR™

MT93L04
128-Channel Voice Echo Canceller

Data Sheet

January 2006

Features

- **MT93L04** is a Multi-chip Module (MCM) consisting of 4 **MT93L00** devices thus providing 128 channels of 64 msec Echo Cancellation
- Each device (MT93L00) is independent of the each other
- Each device has the capability of cancelling echo over 32 channels
- The MCM module provides more than 40% board space savings
- Each device (MT93L00) can be programmed independently in any mode e.g back to back or extended delay to provide capability of cancelling different echo tails
- Each device has the same Jtag identification code

Applications

- Voice over IP network gateways
- Voice over ATM, Frame Relay
- T1/E1/J1 multichannel echo cancellation
- Wireless base stations
- Echo Canceller pools
- DCME, satellite and multiplexer systems

Ordering Information

MT93L04AG	365 Ball BGA	Trays
MT93L04AG2	365 Ball BGA**	Trays

**Pb Free Tin/Silver/Copper

-40°C to +85°C

Description

The MT93L04 Voice Echo Canceller implements a cost effective solution for telephony voice-band echo cancellation conforming to ITU-T G.168 requirements. The MT93L04 architecture contains 64 groups of two echo cancellers (ECA and ECB) which can be configured to provide two channels of 64 milliseconds or one channel of 128 milliseconds echo cancellation. This provides 128 channels of 64 milliseconds to 64 channels of 128 milliseconds echo cancellation or any combination of the two configurations. The MT93L04 supports ITU-T G.165 and G.164 tone disable requirements.

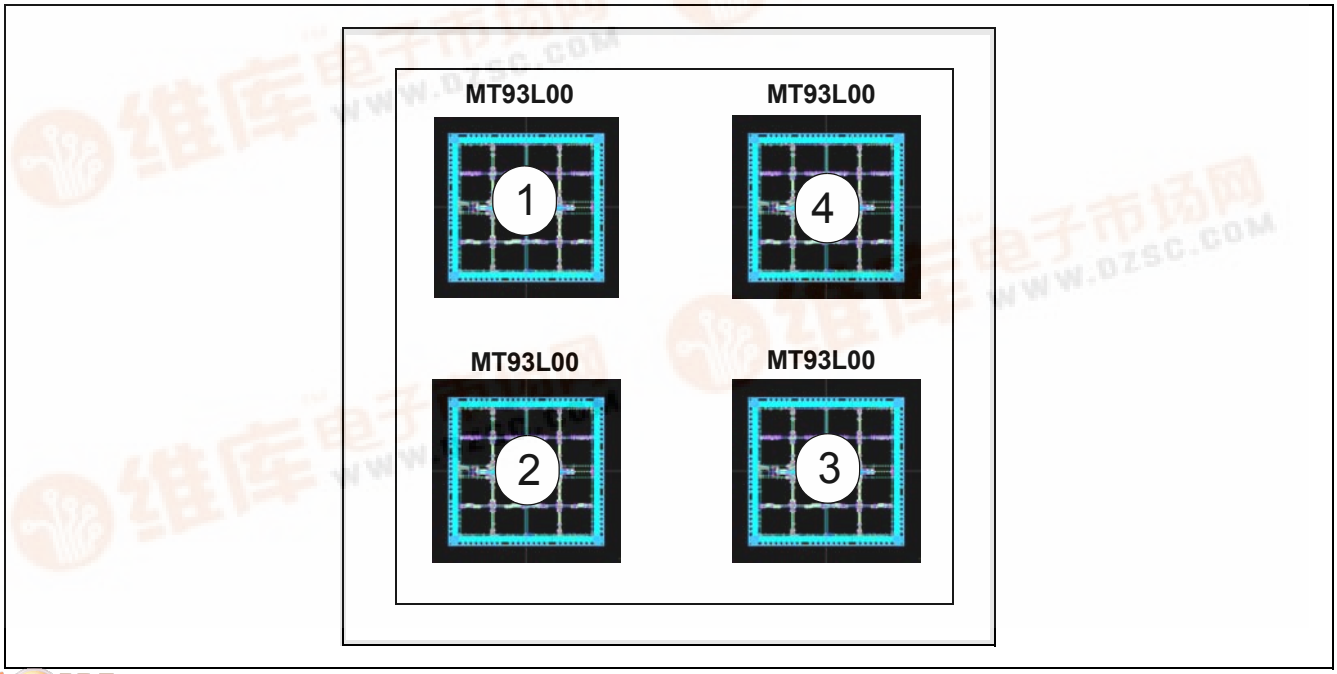


Figure 1 - MT93L04 is MULTI-CHIP Module Consisting of 4 MT93L00 Devices

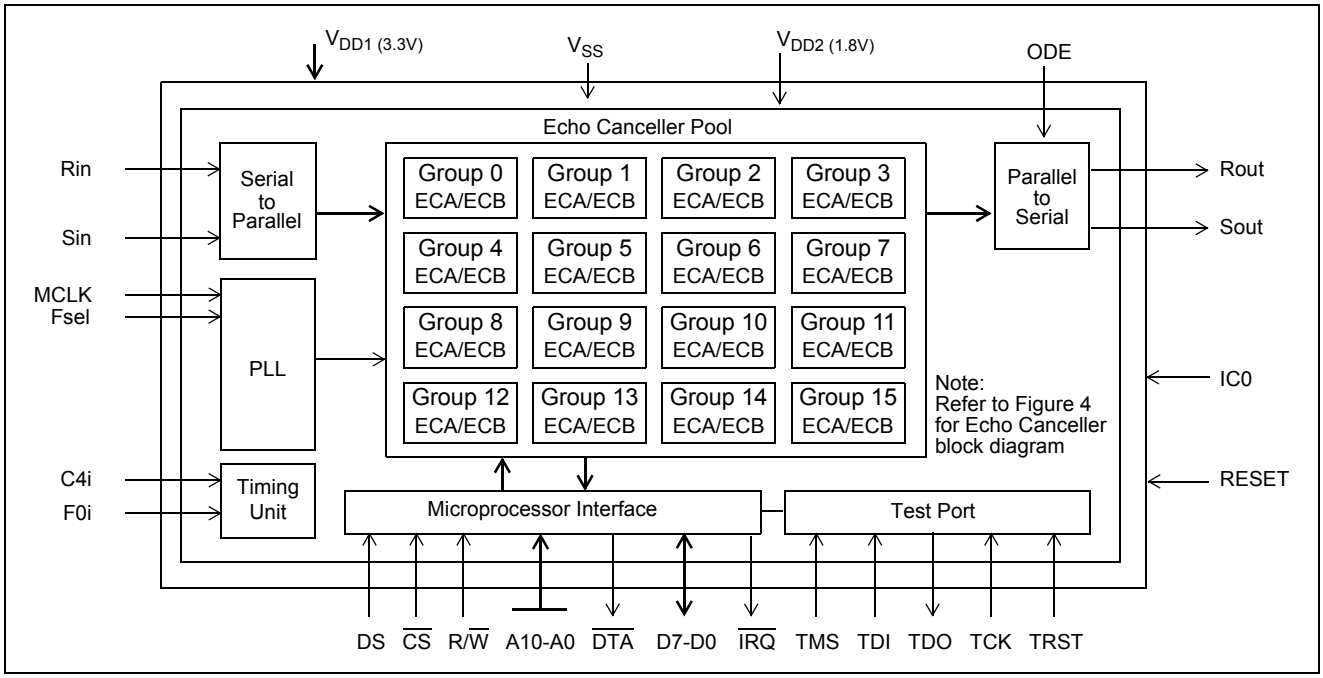


Figure 2 - Functional Block Diagram for Single MT93L00 (32 channels)

Features of Single MT93L00

- Independent multiple channels of echo cancellation; from 32 channels of 64 ms to 16 channels of 128 ms with the ability to mix channels at 128 ms or 64 ms in any combination
- Independent Power Down mode for each group of 2 channels for power management
- ITU-T G.165 and G.168 compliant
- Field proven, high quality performance
- Compatible to ST-BUS and GCI interface at 2 Mb/s serial PCM
- PCM coding, μ/A-Law ITU-T G.711 or sign magnitude
- Per channel Fax/Modem G.164 2100 Hz or G.165 2100 Hz phase reversal Tone Disable
- Per channel echo canceller parameters control
- Transparent data transfer and mute
- Fast reconvergence on echo path changes
- Non-Linear Processor with high quality subjective performance
- Protection against narrow band signal divergence
- Offset nulling of all PCM channels
- 10 MHz or 20 MHz master clock operation
- 3.3 V pads and 1.8 V Logic core operation with 5-Volt tolerant inputs
- No external memory required
- Non-multiplexed microprocessor interface
- IEEE-1149.1 (JTAG) Test Access Port

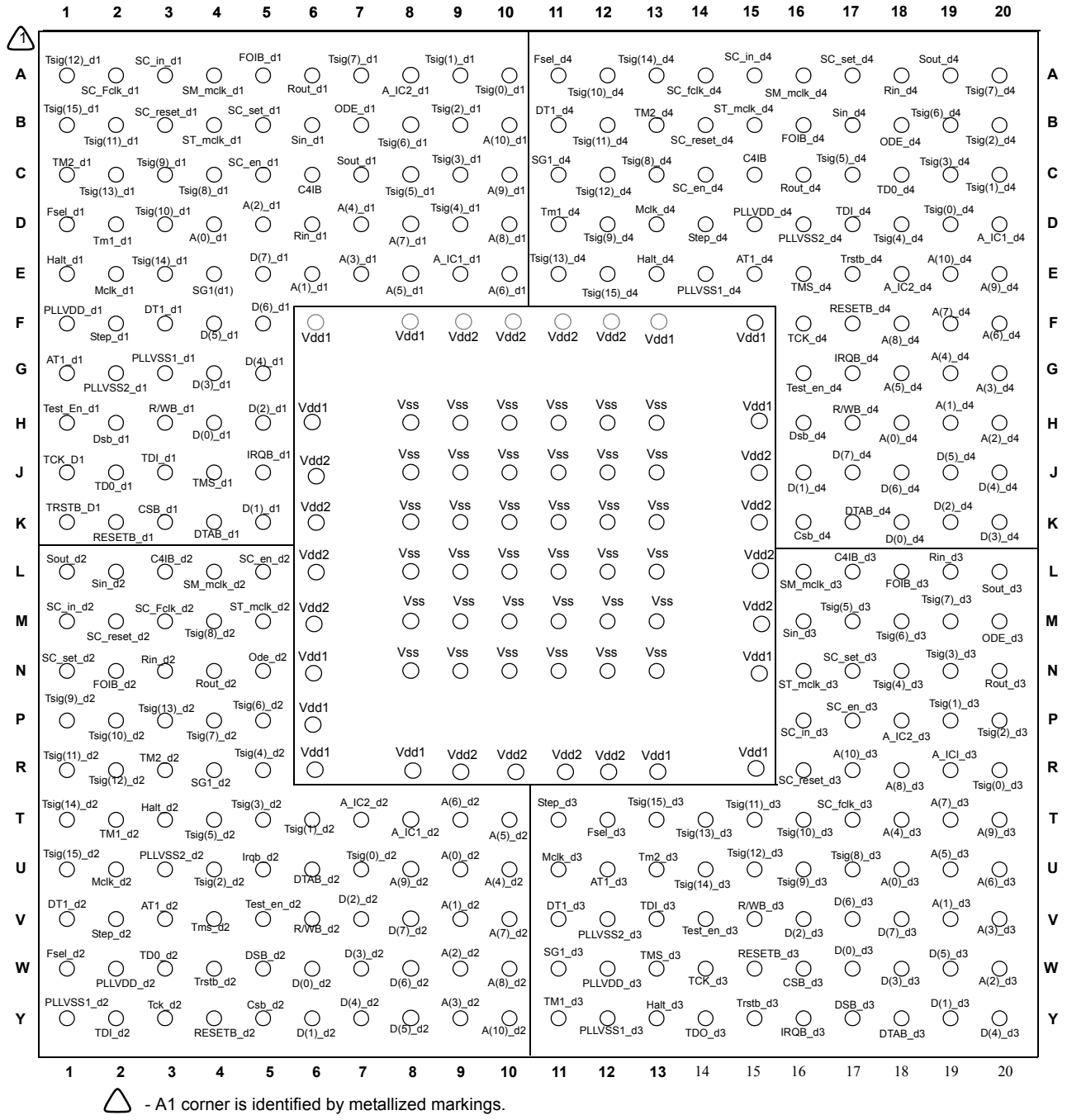


Figure 3 - 365 Ball BGA

Pin Description

Signal Name	Signal Type	BGA Ball #	Signal Description
V_{DD1} = 3.3V	Power	R6, R8, R13, R15, N15,H15, F15,F13,F8,F6,H6,N6, P6,	Positive Power Supply. Nominally 3.3 volt. V_{DD1} = I/O Voltage
V_{DD2} = 1.8V	Power	R9,R10,R11,R12,M15, L15,K15,J15,F12,F11, F10,F9,J6, K6, L6,M6,	Positive Power Supply. Nominally 1.8 volt. V_{DD2} = Core Voltage
VSS	Power	H8,H9,H10,H11,H12, H13, J8, J9,J10,J11, J12,J13,K8,K9,K10,K11,K12,K13 L8,L9,L10, L11,L12,L13,M8,M9,M10,M11,M12, M13, N8, N9,N10,N11,N12,N13	Ground
DEVICE 1			
TMS_d1	User Signal	J4	**Test Mode Select (3.3 V Input).** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up when not driven.
TDI_d1	User Signal	J3	**Test Serial Data In (3.3 V Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
TDO_d1	User Signal	J2	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
TCK_d1	User Signal	J1	**Test Clock (3.3 V Input).** Provides the clock to the JTAG test logic.
TRSTB_d1	User Signal	K1	**Test Reset (3.3 V Input).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up or held low, to ensure that the MT93L00 is in the normal functional mode. This pin is pulled by an internal pull-down when not driven.
Test_En_d1	ICO	H1	**Internal Connection.** Connected to VSS for normal operation
RESETB_d1	User Signal	K2	**Device Reset (Schmitt Trigger Input).** An active low resets the device and puts the MT93L00 into a low-power stand-by mode. When the RESET pin is returned to logic high and a clock is applied to the MCLK pin, the device will automatically execute initialization routines, which preset all the Control and Status Registers to their default power-up values.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
IRQB_d1	User Signal	J5	**Interrupt Request (Open Drain Output).** This output goes low when an interrupt occurs in any channel. IRQ returns high when all the interrupts have been read from the Interrupt FIFO Register. A pull-up resistor (1 K typical) is required at this output.
DSB_d1	User Signal	H2	**Data Strobe (Input).** This active low input works in conjunction with CS to enable the read and write operations.
CSB_d1	User Signal	K3	**Chip Select (Input).** This active low input is used by a microprocessor to activate the microprocessor port.
R/WB_d1	User Signal	H3	**Read/Write (Input).** This input controls the direction of the data bus lines (D7-D0) during a microprocessor access.
DTAB_d1	User Signal	K4	**Data Transfer Acknowledgment (Open Drain Output).** This active low output indicates that a data bus transfer is completed. A pull-up resistor (1 K typical) is required at this output.
D(0)_d1	User Signal	H4	**Data Bus D0 - D7 (Bidirectional).** These pins form the 8-bit bidirectional data bus of the microprocessor port.
D(1)_d1	User Signal	K5	
D(2)_d1	User Signal	H5	
D(3)_d1	User Signal	G4	
D(4)_d1	User Signal	G5	
D(5)_d1	User Signal	F4	
D(6)_d1	User Signal	F5	
D(7)_d1	User Signal	E5	
A(0)_d1	User Signal	D4	**Address A0 to A10 (Input).** These inputs provide the A10 - A0 address lines to the internal registers.
A(1)_d1	User Signal	E6	
A(2)_d1	User Signal	D5	
A(3)_d1	User Signal	E7	
A(4)_d1	User Signal	D7	
A(5)_d1	User Signal	E8	
A(6)_d1	User Signal	E10	
A(7)_d1	User Signal	D8	
A(8)_d1	User Signal	D10	
A(9)_d1	User Signal	C10	
A(10)_d1	User Signal	B10	

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
A_IC1_d1	ICO	E9	**Internal Connection.** Connected to VSS for normal operation
A_IC2_d1	ICO	A8	**Internal Connection.** Connected to VSS for normal operation
Tsig(0)_d1	NC	A10	**No connection.** The pin must be left open for normal operation.
Tsig(1)_d1	NC	A9	**No connection.** The pin must be left open for normal operation.
Tsig(2)_d1	NC	B9	**No connection.** The pin must be left open for normal operation.
Tsig(3)_d1	NC	C9	**No connection.** The pin must be left open for normal operation.
Tsig(4)_d1	NC	D9	**No connection.** The pin must be left open for normal operation.
Tsig(5)_d1	NC	C8	**No connection.** The pin must be left open for normal operation.
Tsig(6)_d1	NC	B8	**No connection.** The pin must be left open for normal operation.
Tsig(7)_d1	NC	A7	**No connection.** The pin must be left open for normal operation.
ODE_d1	User Signal	B7	**Output Drive Enable (Input).** This input pin is logically AND'd with the ODE bit-6 of the Main Control Register. When both ODE bit and ODE input pin are high, the Rout and Sout ST-BUS outputs are enabled.When the ODE bit is low or the ODE input pin is low, the Rout and Sout ST-BUS outputs are high impedance.
Sout_d1	User Signal	C7	**Send PCM Signal Output (Output).** Port 1 TDM data output streams.Sout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rout_d1	User Signal	A6	**Receive PCM Signal Output (Output).** Port 2 TDM data output streams. Rout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Sin_d1	User Signal	B6	**Send PCM Signal Input (Input).** Port 2 TDM data input streams. Sin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rin_d1	User Signal	D6	**Receive PCM Signal Input (Input).** Port 1 TDM data input streams.Rin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
FOIb_d1	User Signal	A5	**Frame Pulse (Input).** This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS or GCI interface specifications.
C4IB_d1	User Signal	C6	**Serial Clock (Input).** 4.096 MHz serial clock for shifting data in/out on the serial streams (Rin, Sin, Rout, Sout).
SC_set_d1	ICO	B5	**Internal Connection.** Connected to VSS for normal operation
SM_mclk_d1	ICO	A4	**Internal Connection.** Connected to VSS for normal operation
ST_mclk_d1	ICO	B4	**Internal Connection.** Connected to VSS for normal operation
SC_en_d1	ICO	C5	**Internal Connection.** Connected to VSS for normal operation
SC_In_d1	ICO	A3	**Internal Connection.** Connected to VSS for normal operation
SC_Reset:_d1	ICO	B3	**Internal Connection.** Connected to VSS for normal operation
SC_Fclk_d1	ICO	A2	**Internal Connection.** Connected to VSS for normal operation
Tsig(8)_d1	NC	C4	**Internal Connection.** The pin must be left open for normal operation.
Tsig(9)_d1	NC	C3	**Internal Connection.** The pin must be left open for normal operation.
Tsig(10)_d1	NC	D3	**Internal Connection.** The pin must be left open for normal operation.
Tsig(11)_d1	NC	B2	**Internal Connection.** The pin must be left open for normal operation.
Tsig(12)_d1	NC	A1	**Internal Connection.** The pin must be left open for normal operation.
Tsig(13)_d1	NC	C2	**Internal Connection.** The pin must be left open for normal operation.
Tsig(14)_d1	NC	E3	**Internal Connection.** The pin must be left open for normal operation.
Tsig(15)_d1	NC	B1	**Internal Connection.** The pin must be left open for normal operation.
Tm1_d1	ICO	D2	**Internal Connection.** Connected to VSS for normal operation
Tm2_d1	ICO	C1	**Internal Connection.** Connected to VSS for normal operation

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
Sg1_d1	ICO	E4	**Internal Connection.** Connected to VSS for normal operation
DT1_d1	NC	F3	**No connection.** The pin must be left open for normal operation.
MCLK_d1	User Signal	E2	**Master Clock (Input).** Nominal 10 MHz or 20 MHz Master Clock input. May be connected to an asynchronous (relative to frame signal) clock source.
Fsel_d1	User Signal	D1	**Frequency select (Input).** This input selects the Master Clock frequency operation. When Fsel pin is low, nominal 19.2 MHz Master Clock input must be applied. When Fsel pin is high, nominal 9.6 MHz Master Clock input must be applied.
Halt_d1	ICO	E1	**Internal Connection.** Connected to VSS for normal operation
Step_d1	ICO	F2	**Internal Connection.** Connected to VSS for normal operation
PLLVSS1_d1	Power	G3	**PLL Ground.** Must be connected to VSS
PLLVDD_d1	Power	F1	**PLL Power Supply.** Must be connected to VDD2
PLLVSS2_d1	Power	G2	**PLL Ground.** Must be connected to VSS
AT1_d1	NC	G1	**No connection.** The pin must be left open for normal operation.
DEVICE 2			
TMS_d2	Signal	V4	**Test Mode Select (3.3 V Input).** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up when not driven.
TDI_d2	Signal	Y2	**Test Serial Data In (3.3 V Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
TDO_d2	Signal	W3	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
TCK_d2	Signal	Y3	**Test Clock (3.3 V Input).** Provides the clock to the JTAG test logic.
TRSTB_d2	Signal	W4	**Test Reset (3.3 V Input).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up or held low, to ensure that the MT93L00 is in the normal functional mode. This pin is pulled by an internal pull-down when not driven.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
Test_En_d2	ICO	V5	**Internal Connection.** Connected to VSS for normal operation
RESETB_d2	Signal	Y4	**Device Reset (Schmitt Trigger Input).** An active low resets the device and puts the MT93L00 into a low-power stand-by mode. When the RESET pin is returned to logic high and a clock is applied to the MCLK pin, the device will automatically execute initialization routines, which preset all the Control and Status Registers to their default power-up values.
IRQB_d2	Signal	U5	**Interrupt Request (Open Drain Output).** This output goes low when an interrupt occurs in any channel. IRQ returns high when all the interrupts have been read from the Interrupt FIFO Register. A pull-up resistor (1 K typical) is required at this output.
DSB_d2	Signal	W5	**Data Strobe (Input).** This active low input works in conjunction with CS to enable the read and write operations.
CSB_d2	Signal	Y5	**Chip Select (Input).** This active low input is used by a microprocessor to activate the microprocessor port.
R/WB_d2	Signal	V6	**Read/Write (Input).** This input controls the direction of the data bus lines (D7-D0) during a microprocessor access.
DTAB_d2	Signal	U6	**Data Transfer Acknowledgment (Open Drain Output).** This active low output indicates that a data bus transfer is completed. A pull-up resistor (1 K typical) is required at this output.
D(0)_d2	Signal	W6	**Data Bus D0 - D7 (Bidirectional).** These pins form the 8-bit bidirectional data bus of the microprocessor port.
D(1)_d2	Signal	Y6	
D(2)_d2	Signal	V7	
D(3)_d2	Signal	W7	
D(4)_d2	Signal	Y7	
D(5)_d2	Signal	Y8	
D(6)_d2	Signal	W8	
D(7)_d2	Signal	V8	

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
A(0)_d2	Signal	U9	**Address A0 to A10 (Input).** These inputs provide the A10 - A0 address lines to the internal registers.
A(1)_d2	Signal	V9	
A(2)_d2	Signal	W9	
A(3)_d2	Signal	Y9	
A(4)_d2	Signal	U10	
A(5)_d2	Signal	T10	
A(6)_d2	Signal	T9	
A(7)_d2	Signal	V10	
A(8)_d2	Signal	W10	
A(9)_d2	Signal	U8	
A(10)_d2	Signal	Y10	
A_IC1_d2	ICO	T8	**Internal Connection.** Connected to VSS for normal operation
A_IC2_d2	ICO	T7	**Internal Connection.** Connected to VSS for normal operation
Tsig(0)_d2	NC	U7	**No connection.** The pin must be left open for normal operation.
Tsig(1)_d2	NC	T6	**No connection.** The pin must be left open for normal operation.
Tsig(2)_d2	NC	U4	**No connection.** The pin must be left open for normal operation.
Tsig(3)_d2	NC	T5	**No connection.** The pin must be left open for normal operation.
Tsig(4)_d2	NC	R5	**No connection.** The pin must be left open for normal operation.
Tsig(5)_d2	NC	T4	**No connection.** The pin must be left open for normal operation.
Tsig(6)_d2	NC	P5	**No connection.** The pin must be left open for normal operation.
Tsig(7)_d2	NC	P4	**No connection.** The pin must be left open for normal operation.
ODE_d2	Signal	N5	**Output Drive Enable (Input).** This input pin is logically AND'd with the ODE bit-6 of the Main Control Register. When both ODE bit and ODE input pin are high, the Rout and Sout ST-BUS outputs are enabled.When the ODE bit is low or the ODE input pin is low, the Rout and Sout ST-BUS outputs are high impedance.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
Sout_d2	Signal	L1	**Send PCM Signal Output (Output).** Port 1 TDM data output streams.Sout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rout_d2	Signal	N4	**Receive PCM Signal Output (Output).** Port 2 TDM data output streams. Rout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Sin_d2	Signal	L2	**Send PCM Signal Input (Input).** Port 2 TDM data input streams. Sin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rin_d2	Signal	N3	**Receive PCM Signal Input (Input).** Port 1 TDM data input streams.Rin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
FOIb_d2	Signal	N2	**Frame Pulse (Input).** This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS or GCI interface specifications.
C4IB_d2	Signal	L3	**Serial Clock (Input).** 4.096 MHz serial clock for shifting data in/out on the serial streams (Rin, Sin, Rout, Sout).
SC_set_d2	ICO	N1	**Internal Connection.** Connected to VSS for normal operation
SM_mclk_d2	ICO	L4	**Internal Connection.** Connected to VSS for normal operation
ST_mclk_d2	ICO	M5	**Internal Connection.** Connected to VSS for normal operation
SC_en_d2	ICO	L5	**Internal Connection.** Connected to VSS for normal operation
SC_In_d2	ICO	M1	**Internal Connection.** Connected to VSS for normal operation
SC_Reset:_d2	ICO	M2	**Internal Connection.** Connected to VSS for normal operation
SC_Fclk_d2	ICO	M3	**Internal Connection.** Connected to VSS for normal operation
Tsig(8)_d2	NC	M4	**No connection.** The pin must be left open for normal operation.
Tsig(9)_d2	NC	P1	**No connection.** The pin must be left open for normal operation.
Tsig(10)_d2	NC	P2	**No connection.** The pin must be left open for normal operation.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
Tsig(11)_d2	NC	R1	**No connection.** The pin must be left open for normal operation.
Tsig(12)_d2	NC	R2	**No connection.** The pin must be left open for normal operation.
Tsig(13)_d2	NC	P3	**No connection.** The pin must be left open for normal operation.
Tsig(14)_d2	NC	T1	**No connection.** The pin must be left open for normal operation.
Tsig(15)_d2	NC	U1	**No connection.** The pin must be left open for normal operation.
Tm1_d2	ICO	T2	**Internal Connection.** Connected to VSS for normal operation
Tm2_d2	ICO	R3	**Internal Connection.** Connected to VSS for normal operation
Sg1_d2	ICO	R4	**Internal Connection.** Connected to VSS for normal operation
DT1_d2	NC	V1	**No connection.** The pin must be left open for normal operation.
MCLK_d2	Signal	U2	**Master Clock (Input).** Nominal 10 MHz or 20 MHz Master Clock input. May be connected to an asynchronous (relative to frame signal) clock source.
Fsel_d2	Signal	W1	**Frequency select (Input).** This input selects the Master Clock frequency operation. When Fsel pin is low, nominal 19.2 MHz Master Clock input must be applied. When Fsel pin is high, nominal 9.6 MHz Master Clock input must be applied.
Halt_d2	ICO	T3	**Internal Connection.** Connected to VSS for normal operation
Step_d2	ICO	V2	I**nternal Connection.** Connected to VSS for normal operation
PLLVSS1_d2	Power	Y1	**PLL Ground.** Must be connected to VSS
PLLVDD_d2	Power	W2	**PLL Power Supply**. Must be connected to VDD2
PLLVSS2_d2	Power	U3	**PLL Ground.** Must be connected to VSS
AT1_d2	NC	V3	**No connection.** The pin must be left open for normal operation.
DEVICE 3			
TMS_d3	Signal	W13	**Test Mode Select (3.3 V Input).** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up when not driven.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
TDI_d3	Signal	V13	**Test Serial Data In (3.3 V Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
TDO_d3	Signal	Y14	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
TCK_d3	Signal	W14	**Test Clock (3.3 V Input).** Provides the clock to the JTAG test logic.
TRSTB_d3	Signal	Y15	**Test Reset (3.3 V Input).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up or held low, to ensure that the MT93L00 is in the normal functional mode. This pin is pulled by an internal pull-down when not driven.
Test_En_d3	ICO	V14	**Internal Connection.** Connected to VSS for normal operation
RESETB_d3	Signal	W15	**Device Reset (Schmitt Trigger Input).** An active low resets the device and puts the MT93L00 into a low-power stand-by mode. When the RESET pin is returned to logic high and a clock is applied to the MCLK pin, the device will automatically execute initialization routines, which preset all the Control and Status Registers to their default power-up values.
IRQB_d3	Signal	Y16	**Interrupt Request (Open Drain Output).** This output goes low when an interrupt occurs in any channel. IRQ returns high when all the interrupts have been read from the Interrupt FIFO Register. A pull-up resistor (1 K typical) is required at this output.
DSB_d3	Signal	Y17	**Data Strobe (Input).** This active low input works in conjunction with CS to enable the read and write operations.
CSB_d3	Signal	W16	**Chip Select (Input).** This active low input is used by a microprocessor to activate the microprocessor port.
R/WB_d3	Signal	V15	**Read/Write (Input).** This input controls the direction of the data bus lines (D7-D0) during a microprocessor access.
B_d3	Signal	Y18	**Data Transfer Acknowledgment (Open Drain Output).** This active low output indicates that a data bus transfer is completed. A pull-up resistor (1 K typical) is required at this output.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
D(0)_d3	Signal	W17	**Data Bus D0 - D7 (Bidirectional).** These pins form the 8-bit bidirectional data bus of the microprocessor port.
D(1) _d3	Signal	Y19	
D(2)_d3	Signal	V16	
D(3)_d3	Signal	W18	
D(4)_d3	Signal	Y20	
D(5)_d3	Signal	W19	
D(6)_d3	Signal	V17	
D(7)_d3	Signal	V18	
A(0)_d3	Signal	U18	**Address A0 to A10 (Input).** These inputs provide the A10 - A0 address lines to the internal registers.
A(1)_d3	Signal	V19	
A(2)_d3	Signal	W20	
A(3)_d3	Signal	V20	
A(4)_d3	Signal	T18	
A(5)_d3	Signal	U19	
A(6)_d3	Signal	U20	
A(7)_d3	Signal	T19	
A(8)_d3	Signal	R18	
A(9)_d3	Signal	T20	
A(10)_d3	Signal	R17	
A_IC1_d3	ICO	R19	**Internal Connection.** Connected to VSS for normal operation
A_IC2_d3	ICO	P18	**Internal Connection.** Connected to VSS for normal operation
Tsig(0)_d3	NC	R20	**No connection.** The pin must be left open for normal operation.
Tsig(1)_d3	NC	P19	**No connection.** The pin must be left open for normal operation.
Tsig(2)_d3	NC	P20	**No connection.** The pin must be left open for normal operation.
Tsig(3)_d3	NC	N19	**No connection.** The pin must be left open for normal operation.
Tsig(4)_d3	NC	N18	**No connection.** The pin must be left open for normal operation.
Tsig(5)_d3	NC	M17	**No connection.** The pin must be left open for normal operation.
Tsig(6)_d3	NC	M18	**No connection.** The pin must be left open for normal operation.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
Tsig(7)_d3	NC	M19	**No connection.** The pin must be left open for normal operation.
ODE_d3	Signal	M20	**Output Drive Enable (Input).** This input pin is logically AND'd with the ODE bit-6 of the Main Control Register. When both ODE bit and ODE input pin are high, the Rout and Sout ST-BUS outputs are enabled.When the ODE bit is low or the ODE input pin is low, the Rout and Sout ST-BUS outputs are high impedance.
Sout_d3	Signal	L20	**Send PCM Signal Output (Output).** Port 1 TDM data output streams.Sout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rout_d3	Signal	N20	**Receive PCM Signal Output (Output).** Port 2 TDM data output streams. Rout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Sin_d3	Signal	M16	**Send PCM Signal Input (Input).** Port 2 TDM data input streams. Sin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rin_d3	Signal	L19	**Receive PCM Signal Input (Input).** Port 1 TDM data input streams.Rin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
FOIb_d3	Signal	L18	**Frame Pulse (Input).** This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS or GCI interface specifications.
C4IB_d3	Signal	L17	**Serial Clock (Input).** 4.096 MHz serial clock for shifting data in/out on the serial streams (Rin, Sin, Rout, Sout).
SC_set_d3	ICO	N17	**Internal Connection.** Connected to VSS for normal operation
SM_mclk_d3	ICO	L16	**Internal Connection.** Connected to VSS for normal operation
ST_mclk_d3	ICO	N16	**Internal Connection.** Connected to VSS for normal operation
SC_en_d3	ICO	P17	**Internal Connection.** Connected to VSS for normal operation
SC_In_d3	ICO	P16	**Internal Connection**. Connected to VSS for normal operation
SC_Reset:_d3	ICO	R16	**Internal Connection.** Connected to VSS for normal operation

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
SC_Fclk_d3	ICO	T17	**Internal Connection.** Connected to VSS for normal operation
Tsig(8)_d3	NC	U17	**No connection.** The pin must be left open for normal operation.
Tsig(9)_d3	NC	U16	**No connection.** The pin must be left open for normal operation.
Tsig(10)_d3	NC	T16	**No connection.** The pin must be left open for normal operation.
Tsig(11)_d3	NC	T15	**No connection.** The pin must be left open for normal operation.
Tsig(12)_d3	NC	U15	**No connection.** The pin must be left open for normal operation.
Tsig(13)_d3	NC	T14	**No connection.** The pin must be left open for normal operation.
Tsig(14)_d3	NC	U14	**No connection.** The pin must be left open for normal operation.
Tsig(15)_d3	NC	T13	**No connection.** The pin must be left open for normal operation.
Tm1_d3	ICO	Y11	**Internal Connection.** Connected to VSS for normal operation
Tm2_d3	ICO	U13	**Internal Connection.** Connected to VSS for normal operation
Sg1_d3	ICO	W11	**Internal Connection.** Connected to VSS for normal operation
DT1_d3	NC	V11	**No connection.** The pin must be left open for normal operation.
MCLK_d3	Signal	U11	**Master Clock (Input).** Nominal 10 MHz or 20 MHz Master Clock input. May be connected to an asynchronous (relative to frame signal) clock source.
Fsel_d3	Signal	T12	**Frequency select (Input).** This input selects the Master Clock frequency operation. When Fsel pin is low, nominal 19.2 MHz Master Clock input must be applied. When Fsel pin is high, nominal 9.6 MHz Master Clock input must be applied.
Halt_d3	ICO	Y13	**Internal Connection.** Connected to VSS for normal operation
Step_d3	ICO	T11	**Internal Connection.** Connected to VSS for normal operation
PLLVSS1_d3	Power	Y12	**PLL Ground.** Must be connected to VSS
PLLVDD_d3	Power	W12	**PLL Power Supply.** Must be connected to VDD2

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
PLLVSS2_d3	Power	V12	**PLL Ground.** Must be connected to VSS
AT1_d3	NC	U12	**No connection.** The pin must be left open for normal operation.
DEVICE 4			
TMS_d4	Signal	E16	**Test Mode Select (3.3 V Input).** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up when not driven.
TDI_d4	Signal	D17	**Test Serial Data In (3.3 V Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
TDO_d4	Signal	C18	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
TCK_d4	Signal	F16	**Test Clock (3.3 V Input).** Provides the clock to the JTAG test logic.
TRSTB_d4	Signal	E17	**Test Reset (3.3 V Input).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up or held low, to ensure that the MT93L00 is in the normal functional mode. This pin is pulled by an internal pull-down when not driven.
Test_En_d4	ICO	G16	**Internal Connection.** Connected to VSS for normal operation
RESETB_d4	Signal	F17	**Device Reset (Schmitt Trigger Input).** An active low resets the device and puts the MT93L00 into a low-power stand-by mode. When the RESET pin is returned to logic high and a clock is applied to the MCLK pin, the device will automatically execute initialization routines, which preset all the Control and Status Registers to their default power-up values.
IRQB_d4	Signal	G17	**Interrupt Request (Open Drain Output).** This output goes low when an interrupt occurs in any channel. IRQ returns high when all the interrupts have been read from the Interrupt FIFO Register. A pull-up resistor (1 K typical) is required at this output.
DSB_d4	Signal	H16	**Data Strobe (Input).** This active low input works in conjunction with CS to enable the read and write operations.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
CSB_d4	Signal	K16	**Chip Select (Input).** This active low input is used by a microprocessor to activate the microprocessor port.
R/WB_d4	Signal	H17	**Read/Write (Input).** This input controls the direction of the data bus lines (D7-D0) during a microprocessor access.
DTAB_d4	Signal	K17	**Data Transfer Acknowledgment (Open Drain Output).** This active low output indicates that a data bus transfer is completed. A pull-up resistor (1 K typical) is required at this output.
D(0)_d4	Signal	K18	**Data Bus D0 - D7 (Bidirectional).** These pins form the 8-bit bidirectional data bus of the microprocessor port.
D(1)_d4	Signal	J16	
D(2)_d4	Signal	K19	
D(3)_d4	Signal	K20	
D(4)_d4	Signal	J20	
D(5)_d4	Signal	J19	
D(6)_d4	Signal	J18	
D(7)_d4	Signal	J17	
A(0)_d4	Signal	H18	**Address A0 to A10 (Input).** These inputs provide the A10 - A0 address lines to the internal registers.
A(1)_d4	Signal	H19	
A(2)_d4	Signal	H20	
A(3)_d4	Signal	G20	
A(4)_d4	Signal	G19	
A(5)_d4	Signal	G18	
A(6)_d4	Signal	F20	
A(7)_d4	Signal	F19	
A(8)_d4	Signal	F18	
A(9)_d4	Signal	E20	
A(10)_d4	Signal	E19	
A_IC1_d4	ICO	D20	**Internal Connection.** Connected to VSS for normal operation
A_IC2_d4	ICO	E18	**Internal Connection.** Connected to VSS for normal operation
Tsig(0)_d4	NC	D19	**No connection.** The pin must be left open for normal operation.
Tsig(1)_d4	NC	C20	**No connection.** The pin must be left open for normal operation.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
Tsig(2)_d4	NC	B20	**No connection.** The pin must be left open for normal operation.
Tsig(3)_d4	NC	C19	**No connection.** The pin must be left open for normal operation.
Tsig(4)_d4	NC	D18	**No connection.** The pin must be left open for normal operation.
Tsig(5)_d4	NC	C17	**No connection.** The pin must be left open for normal operation.
Tsig(6)_d4	NC	B19	**No connection.** The pin must be left open for normal operation.
Tsig(7)_d4	NC	A20	**No connection.** The pin must be left open for normal operation.
ODE_d4	Signal	B18	**Output Drive Enable (Input).** This input pin is logically AND'd with the ODE bit-6 of the Main Control Register. When both ODE bit and ODE input pin are high, the Rout and Sout ST-BUS outputs are enabled.When the ODE bit is low or the ODE input pin is low, the Rout and Sout ST-BUS outputs are high impedance.
Sout_d4	Signal	A19	**Send PCM Signal Output (Output).** Port 1 TDM data output streams.Sout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rout_d4	Signal	C16	**Receive PCM Signal Output (Output).** Port 2 TDM data output streams. Rout pin outputs serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Sin_d4	Signal	B17	**Send PCM Signal Input (Input).** Port 2 TDM data input streams. Sin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
Rin_d4	Signal	A18	**Receive PCM Signal Input (Input).** Port 1 TDM data input streams.Rin pin receives serial TDM data streams at 2.048 Mb/s with 32 channels per stream.
FOIb_d4	Signal	B16	**Frame Pulse (Input).** This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS or GCI interface specifications.
C4IB_d4	Signal	C15	**Serial Clock (Input).** 4.096 MHz serial clock for shifting data in/out on the serial streams (Rin, Sin, Rout, Sout).
SC_set_d4	ICO	A17	**Internal Connection.** Connected to VSS for normal operation

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
SM_mclk_d4	ICO	A16	**Internal Connection.** Connected to VSS for normal operation
ST_mclk_d4	ICO	B15	**Internal Connection.** Connected to VSS for normal operation
SC_en_d4	ICO	C14	**Internal Connection.** Connected to VSS for normal operation
SC_In_d4	ICO	A15	**Internal Connection.** Connected to VSS for normal operation
SC_Reset:_d4	ICO	B14	**Internal Connection.** Connected to VSS for normal operation
SC_Fclk_d4	ICO	A14	**Internal Connection.** Connected to VSS for normal operation
Tsig(8)_d4	NC	C13	**No connection.** The pin must be left open for normal operation.
Tsig(9)_d4	NC	D12	**No connection.** The pin must be left open for normal operation.
Tsig(10)_d4	NC	A12	**No connection.** The pin must be left open for normal operation.
Tsig(11)_d4	NC	B12	**No connection. T**he pin must be left open for normal operation.
Tsig(12)_d4	NC	C12	**No connection.** The pin must be left open for normal operation.
Tsig(13)_d4	NC	E11	**No connection.** The pin must be left open for normal operation.
Tsig(14)_d4	NC	A13	No connection. The pin must be left open for normal operation.
Tsig(15)_d4	NC	E12	**No connection.** The pin must be left open for normal operation.
Tm1_d4	ICO	D11	**Internal Connection.** Connected to VSS for normal operation
Tm2_d4	ICO	B13	**Internal Connection.** Connected to VSS for normal operation
Sg1_d4	ICO	C11	**Internal Connection.** Connected to VSS for normal operation
DT1_d4	NC	B11	**No connection.** The pin must be left open for normal operation.
MCLK_d4	Signal	D13	**Master Clock (Input).** Nominal 10 MHz or 20 MHz Master Clock input. May be connected to an asynchronous (relative to frame signal) clock source.

Pin Description (continued)

Signal Name	Signal Type	BGA Ball #	Signal Description
Fsel_d4	Signal	A11	**Frequency select (Input).** This input selects the Master Clock frequency operation. When Fsel pin is low, nominal 19.2 MHz Master Clock input must be applied. When Fsel pin is high, nominal 9.6 MHz Master Clock input must be applied.
Halt_d4	ICO	E13	**Internal Connection.** Connected to VSS for normal operation
Step_d4	ICO	D14	**Internal Connection.** Connected to VSS for normal operation
PLLVSS1_d4	Power	E14	**PLL Ground.** Must be connected to VSS
PLLVDD_d4	Power	D15	**PLL Power Supply.** Must be connected to VDD2
PLLVSS2_d4	Power	D16	**PLL Ground.** Must be connected to VSS
AT1_d4	NC	E15	**No connection.** The pin must be left open for normal operation.

Description of the Single MT93L00

Device Overview

The MT93L00 architecture contains 32 echo cancellers divided into 16 groups. Each group has two echo cancellers, Echo Canceller A and Echo Canceller B. Each group can be configured in Normal, Extended Delay or Back-to-Back configurations. In Normal configuration, a group of echo cancellers provides two channels of 64 ms echo cancellation, which run independently on different channels. In Extended Delay configuration, a group of echo cancellers achieves 128 ms of echo cancellation by cascading the two echo cancellers (A & B). In Back-to-Back configuration, the two echo cancellers from the same group are positioned to cancel echo coming from both directions in a single channel, providing full-duplex 64 ms echo cancellation.

Each echo canceller contains the following main elements (see Figure 4).

- Adaptive Filter for estimating the echo channel
- Subtractor for cancelling the echo
- Double-Talk detector for disabling the filter adaptation during periods of double-talk
- Path Change detector for fast reconvergence on major echo path changes
- Instability Detector to combat oscillation in very low ERL environments
- Non-Linear Processor for suppression of residual echo
- Disable Tone Detectors for detecting valid disable tones at send and receive path inputs
- Narrow-Band Detector for preventing Adaptive Filter divergence from narrow-band signals
- Offset Null filters for removing the DC component in PCM channels
- 12 dB attenuator for signal attenuation
- Parallel controller interface compatible with Motorola microcontrollers
- PCM encoder/decoder compatible with μ/A-Law ITU-T G.711 or Sign-Magnitude coding

Each echo canceller in the MT93L00 has four functional states: Mute, Bypass, Disable Adaptation and Enable Adaptation. These are explained in the section entitled Echo Canceller Functional States.

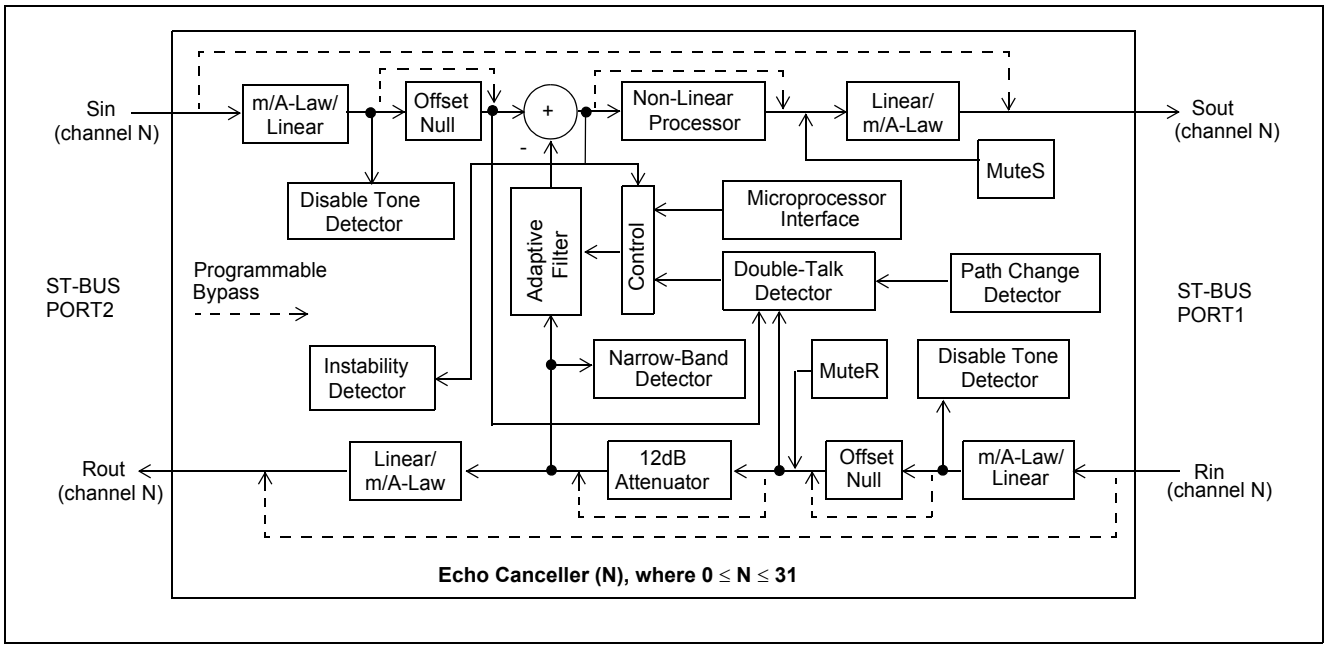


Figure 4 - Echo Canceller Functional Block Diagram

Adaptive Filter

The adaptive filter adapts to the echo path and generates an estimate of the echo signal. This echo estimate is then subtracted from Sin. For each group of echo cancellers, the adaptive filter is a 1024 tap FIR adaptive filter which is divided into two sections. Each section contains 512 taps providing 64 ms of echo estimation. In Normal configuration, the first section is dedicated to channel A and the second section to channel B. In Extended Delay configuration, both sections are cascaded to provide 128ms of echo estimation in channel A. In Back-to Back configuration, the first section is used in the receive direction and the second section is used in the transmit direction for the same channel.

Double-Talk Detector

Double-Talk is defined as those periods of time when signal energy is present in both directions simultaneously. When this happens, it is necessary to disable the filter adaptation to prevent divergence of the Adaptive Filter coefficients. Note that when double-talk is detected, the adaptation process is halted but the echo canceller continues to cancel echo using the previous converged echo profile.

A double-talk condition exists whenever the relative signal levels of Rin (Lrin) and Sin (Lsin) meet the following condition:

$$Lsin > Lrin + 20log10(DTDT)$$

where DTDT is the Double-Talk Detection Threshold.
Lsin and Lrin are signal levels expressed in dBm0.

A different method is used when it is uncertain whether Sin consists of a low level double-talk signal or an echo return. During these periods, the adaptation process is slowed down but it is not halted.

In G.168 standard, the echo return loss is expected to be at least 6 dB. This implies that the Double-Talk Detector Threshold (DTDT) should be set to 0.5 (-6 dB). However, in order to get additional guardband, the DTDT is set internally to 0.5625 (-5 dB).

In some applications the return loss can be higher or lower than 6 dB. The MT93L00 allows the user to change the detection threshold to suit each application's need. This threshold can be set by writing the desired threshold value into the DTDT register.

The DTDT register is 16 bits wide. The register value in hexadecimal can be calculated with the following equation:

$$DTDT(hex) = hex(DTDT(dec) * 32768)$$

$$where\ 0 < DTDT(dec) < 1$$

Example: For DTDT = 0.5625 (-5dB), the hexadecimal value becomes hex(0.5625 * 32768) = 4800h

Path Change Detector

Integrated into the MT93L00A is a Path Change Detector. This permits fast reconvergence when a major change occurs in the echo channel. Subtle changes in the echo channel are also tracked automatically once convergence is achieved, but at a much slower speed.

The Path Change Detector is activated by setting the PathDet bit in Control Register A3/B3 to "1". An optional path clearing feature can be enabled by setting the PathClr bit in Control Register A3/B3 to "1". With path clearing turned on, the existing echo channel estimate will also be cleared (i.e. the adaptive filter will be filled with zeroes) upon detection of a major path change.

Non-Linear Processor (NLP)

After echo cancellation, there is always a small amount of residual echo which may still be audible. The MT93L00 uses an NLP to remove residual echo signals which have a level lower than the Adaptive Suppression Threshold (TSUP in G.168). This threshold depends upon the level of the Rin (Lrin) reference signal as well as the programmed value of the Non-Linear Processor Threshold register (NLPTHR). TSUP can be calculated by the following equation:

$$TSUP = Lrin + 20\log10(NLPTHR)$$

where NLPTHR is the Non-Linear Processor Threshold register value
and Lrin is the relative power level expressed in dBm0.

When the level of residual error signal falls below TSUP, the NLP is activated further attenuating the residual signal by an additional 36 dB. To prevent a perceived decrease in background noise due to the activation of the NLP, a spectrally-shaped comfort noise, equivalent in power level to the background noise, is injected. This keeps the perceived noise level constant. Consequently, the user does not hear the activation and de-activation of the NLP.

The NLP processor can be disabled by setting the NLPDis bit to “1” in Control Register 2.

The NLPTHR register is 16 bits wide. The register value in hexadecimal can be calculated with the following equation:

$$NLPTHR(hex) = hex(NLPTHR(dec) * 32768)$$

$$where\ 0 < NLPTHR(dec) < 1$$

The comfort noise injector can be disabled by setting the INJDis bit to “1” in Control Register A1/B1. It should be noted that the NLPTHR is valid and the comfort noise injection is active only when the NLP is enabled.

If the comfort noise injector is unable to correctly match the level of the background noise (because of peculiar spectral characteristics, for example), the injected level can be fine-tuned using the Noise Scaling register. A neutral value of 80(hex) will prevent any scaling. Values less than 80(hex) will reduce the noise level, values greater than 80(hex) will increase the noise level. The scaling is done linearly.

Example: To decrease the comfort noise level by 3 dB, the register value would be 10 ^ (-3 / 20) • 128 = 0.71 • 128 = 91(dec) = 5B(hex)

The default factory setting for the Noise Scaling register should be adequate for most operating environments. It is unlikely that it will need to be changed. It has also been set to a value which will ensure G.168 compliance.

Disable Tone Detector

G.165 recommendation defines the disable tone as having the following characteristics: 2100 Hz (±21 Hz) sine wave, a power level between -6 to -31 dBm0, and a phase reversal of 180 degrees (± 25 degrees) every 450 ms (± 25 ms). If the disable tone is present for a minimum of one second with at least one phase reversal, the Tone Detector will trigger.

G.164 recommendation defines the disable tone as a 2100 Hz (±21 Hz) sine wave with a power level between 0 to -31 dBm0. If the disable tone is present for a minimum of 400 milliseconds, with or without phase reversal, the Tone Detector will trigger.

The MT93L00 has two Tone Detectors per channels (for a total of 64) in order to monitor the occurrence of a valid disable tone on both Rin and Sin. Upon detection of a disable tone, TD bit of the Status Register will indicate logic high and an interrupt is generated (i.e., IRQ pin low). Refer to Figure 5 and to the Interrupts section.

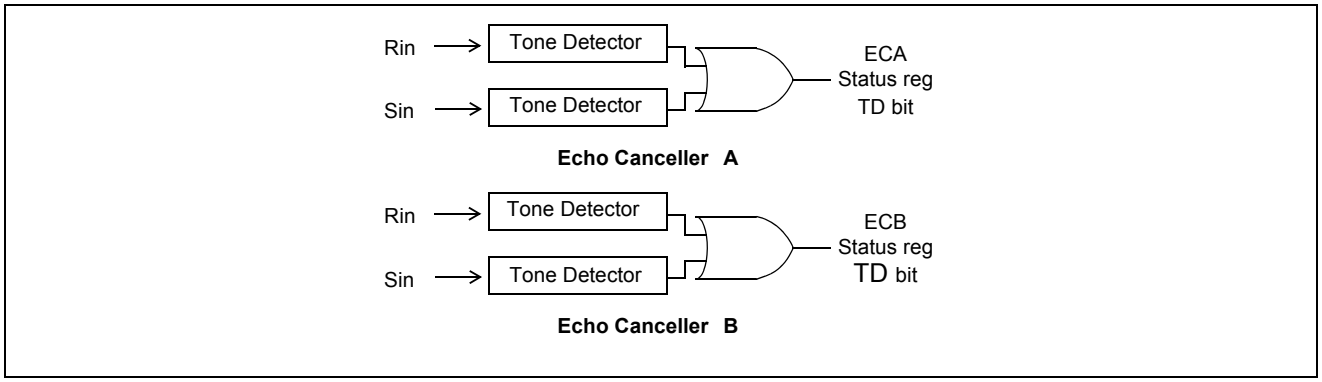


Figure 5 - Disable Tone Detection

Once a Tone Detector has been triggered, there is no longer a need for a valid disable tone (G.164 or G.165) to maintain Tone Detector status (i.e., TD bit high). The Tone Detector status will only release (i.e., TD bit low) if the signals Rin and Sin fall below -30 dBm0, in the frequency range of 390 Hz to 700 Hz, and below -34 dBm0, in the

frequency range of 700 Hz to 3400 Hz, for at least 400 ms. Whenever a Tone Detector releases, an interrupt is generated (i.e., IRQ pin low).

The selection between G.165 and G.164 tone disable is controlled by the PHDis bit in Control Register 2 on a per channel basis. When the PHDis bit is set to 1, G.164 tone disable requirements are selected.

In response to a valid disable tone, the echo canceller must be switched from the Enable Adaptation state to the Bypass state. This can be done in two ways, automatically or externally. In automatic mode, the Tone Detectors internally control the switching between Enable Adaptation and Bypass states. The automatic mode is activated by setting the AutoTD bit in Control Register 2 to high. In external mode, an external controller is needed to service the interrupts and poll the TD bits in the Status Registers. Following the detection of a disable tone (TD bit high) on a given channel, the external controller must switch the echo canceller from Enable Adaptation to Bypass state.

Instability Detector

In systems with very low echo channel return loss (ERL), there may be enough feedback in the loop to cause stability problems in the adaptive filter. This instability can result in variable pitched ringing or oscillation. Should this ringing occur, the Instability Detector will activate and suppress the oscillations.

The Instability Detector is activated by setting the RingClr bit in Control Register A3/B3 to "1".

Narrow Band Signal Detector (NBSD)

Single or dual frequency tones (i.e., DTMF tones) present in the receive input (Rin) of the echo canceller for a prolonged period of time may cause the Adaptive Filter to diverge. The Narrow Band Signal Detector (NBSD) is designed to prevent this by detecting single or dual tones of arbitrary frequency, phase, and amplitude. When narrow band signals are detected, adaptation is halted but the echo canceller continues to cancel echo.

The NBSD can be disabled by setting the NBDis bit to “1” in Control Register 2.

Offset Null Filter

Adaptive filters in general do not operate properly when a DC offset is present at any inputs. To remove the DC component, the MT93L00 incorporates Offset Null filters in both Rin and Sin inputs.

The offset null filters can be disabled by setting the HPFDis bit to “1” in Control Register 2.

ITU-T G.168 Compliance

The MT93L00 has been certified G.168 compliant in all 64 ms cancellation modes (i.e., Normal and Back-to-Back configurations) by in-house testing with the DSPG ECT-1 echo canceller tester.

It should be noted that G.168 compliance is not claimed for the 128 ms Extended Delay mode, although subjectively no difference can be noticed.

Device Configuration

The MT93L00 architecture contains 32 echo cancellers divided into 16 groups. Each group has two echo cancellers which can be individually controlled (Echo Canceller A and B). They can be set in three distinct configurations: Normal, Back-to-Back, and Extended Delay. See Figure 6.

Normal Configuration

In Normal configuration, the two echo cancellers (Echo Canceller A and B) are positioned in parallel, as shown in Figure 6a, providing 64 milliseconds of echo cancellation in two channels simultaneously.

Back-to-Back Configuration

In Back-to-Back configuration, the two echo cancellers from the same group are positioned to cancel echo coming from both directions in a single channel providing full-duplex 64 ms echo cancellation. See Figure 6c. This configuration uses only one timeslot on PORT1 and PORT2 and the second timeslot normally associated with ECB contains undefined data. Back-to-Back configuration allows a no-glue interface for applications where bidirectional echo cancellation is required.

Back-to-Back configuration is selected by writing “1” into the BBM bit of both Control Register A1 and Control Register B1 of a given group of echo cancellers. Table 2 shows the 16 groups of 2 cancellers that can be configured into Back-to-Back.

Examples of Back-to-Back configuration include positioning one group of echo cancellers between a CODEC and a transmission device or between two codecs for echo control on analog trunks.

Extended Delay configuration

In this configuration, the two echo cancellers from the same group are internally cascaded into one 128 milliseconds echo canceller. See Figure 6b. This configuration uses only one timeslot on PORT1 and PORT2 and the second timeslot normally associated with ECB contains undefined data.

Extended Delay configuration is selected by writing “1” into the ExtDl bit in Echo Canceller A, Control Register A1. For a given group, only Echo Canceller A, Control Register A1, has the ExtDl bit. Control Register B1, bit-0 must always be set to zero.

Table 2 shows the 16 groups of 2 cancellers that can each be configured into 64 ms or 128 ms echo tail capacity.

Echo Canceller Functional States

Each echo canceller has four functional states: Mute, Bypass, Disable Adaptation and Enable Adaptation.

Mute

In Normal and in Extended Delay configurations, writing a “1” into the MuteR bit replaces Rin with quiet code which is applied to both the Adaptive Filter and Rout. Writing a “1” into the MuteS bit replaces the Sout PCM data with quiet code.

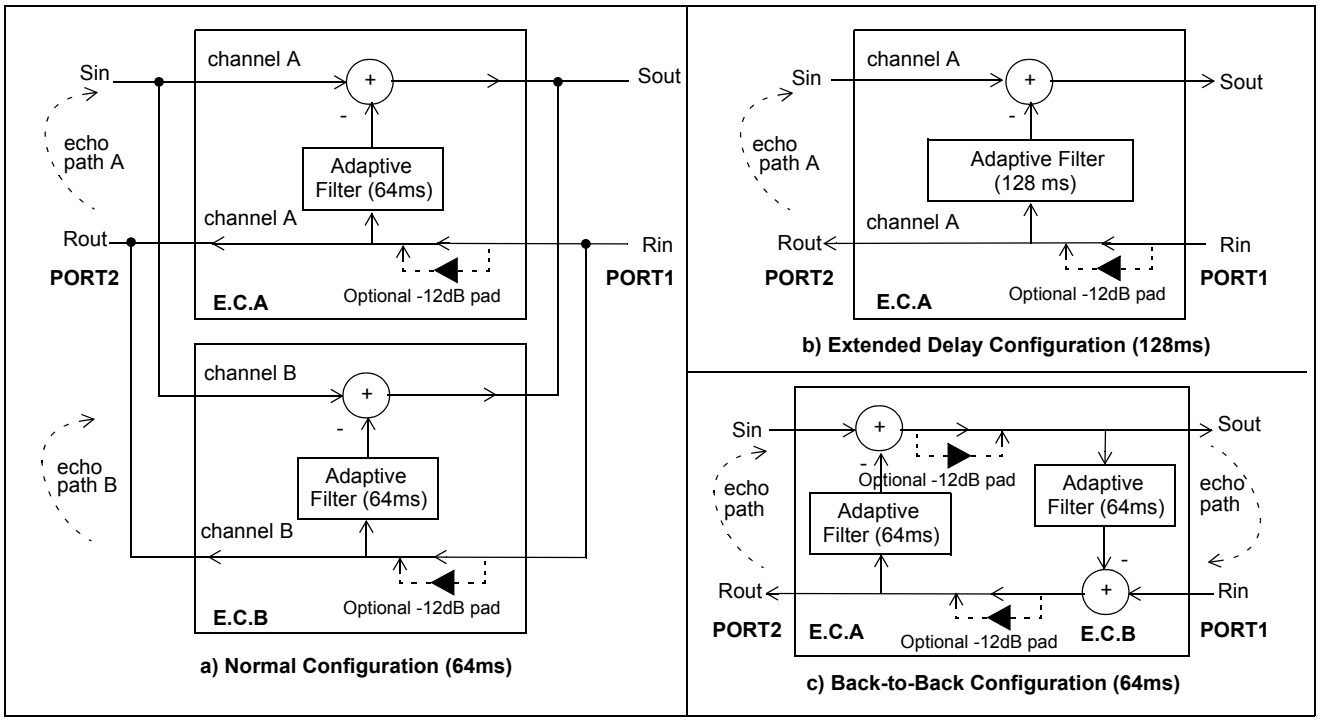


Figure 6 - Device Configuration

	LINEAR 16 bits 2's complement	SIGN/ MAGNITUDE μ-Law A-Law	CCITT (G.711)	
			μ-Law	A-Law
+Zero (quiet code)	0000h	80h	FFh	D5h

Table 1 - Quiet PCM Code Assignment

In Back-to-Back configuration, writing a "1" into the MuteR bit of Echo Canceller A, Control Register 2, causes quiet code to be transmitted on Rout. Writing a "1" into the MuteS bit of Echo Canceller A, Control Register 2, causes quiet code to be transmitted on Sout.

In Extended Delay and in Back -to -Back configurations, MuteR and MuteS bits of Echo Canceller B must always be "0". Refer to Figure 4 and to Control Register 2 for bit description.

Bypass

The Bypass state directly transfers PCM codes from Rin to Rout and from Sin to Sout. When Bypass state is selected, the Adaptive Filter coefficients are reset to zero. Bypass state must be selected for at least one frame (125 μs) in order to properly clear the filter.

Disable Adaptation

When the Disable Adaptation state is selected, the Adaptive Filter coefficients are frozen at their current value. The adaptation process is halted, however, the echo canceller continues to cancel echo.

Enable Adaptation

In Enable Adaptation state, the Adaptive Filter coefficients are continually updated. This allows the echo canceller to model the echo return path characteristics in order to cancel echo. This is the normal operating state.

The echo canceller functions are selected in Control Register A1/B1 and Control Register 2 through four control bits: MuteS, MuteR, Bypass and AdaptDis. Refer to the Registers Description for details.

MT93L00 Throughput Delay

The throughput delay of the MT93L00 varies according to the device configuration. For all device configurations, Rin to Rout has a delay of two frames and Sin to Sout has a delay of three frames. In Bypass state, the Rin to Rout and Sin to Sout paths have a delay of two frames.

Serial PCM I/O Channels

There are two sets of TDM I/O streams, each with channels numbered from 0 to 31. One set of input streams is for Receive (Rin) channels, and the other set of input streams is for Send (Sin) channels. Likewise, one set of output streams is for Rout pcm channels, and the other set is for Sout channels. See Figure 7 for channel allocation.

The arrangement and connection of PCM channels to each echo canceller is a 2 port I/O configuration for each set of PCM Send and Receive channels, as illustrated in Figure 4.

Serial Data Interface Timing

The MT93L00 provides ST-BUS and GCI interface timing. The Serial Interface clock frequency, C4i, is 4.096 MHz. The input and output data rate of the ST-Bus and GCI bus is 2.048 Mb/s.

The 8 KHz input frame pulse can be in either ST-BUS or GCI format. The MT93L00 automatically detects the presence of an input frame pulse and identifies it as either ST-BUS or GCI. In ST-BUS format, every second falling edge of the C4i clock marks a bit boundary, and the data is clocked in on the rising edge of C4i, three quarters of the way into the bit cell (See Figure 9). In GCI format, every second rising edge of the C4i clock marks the bit boundary, and data is clocked in on the second falling edge of C4i, half the way into the bit cell (see Figure 10).

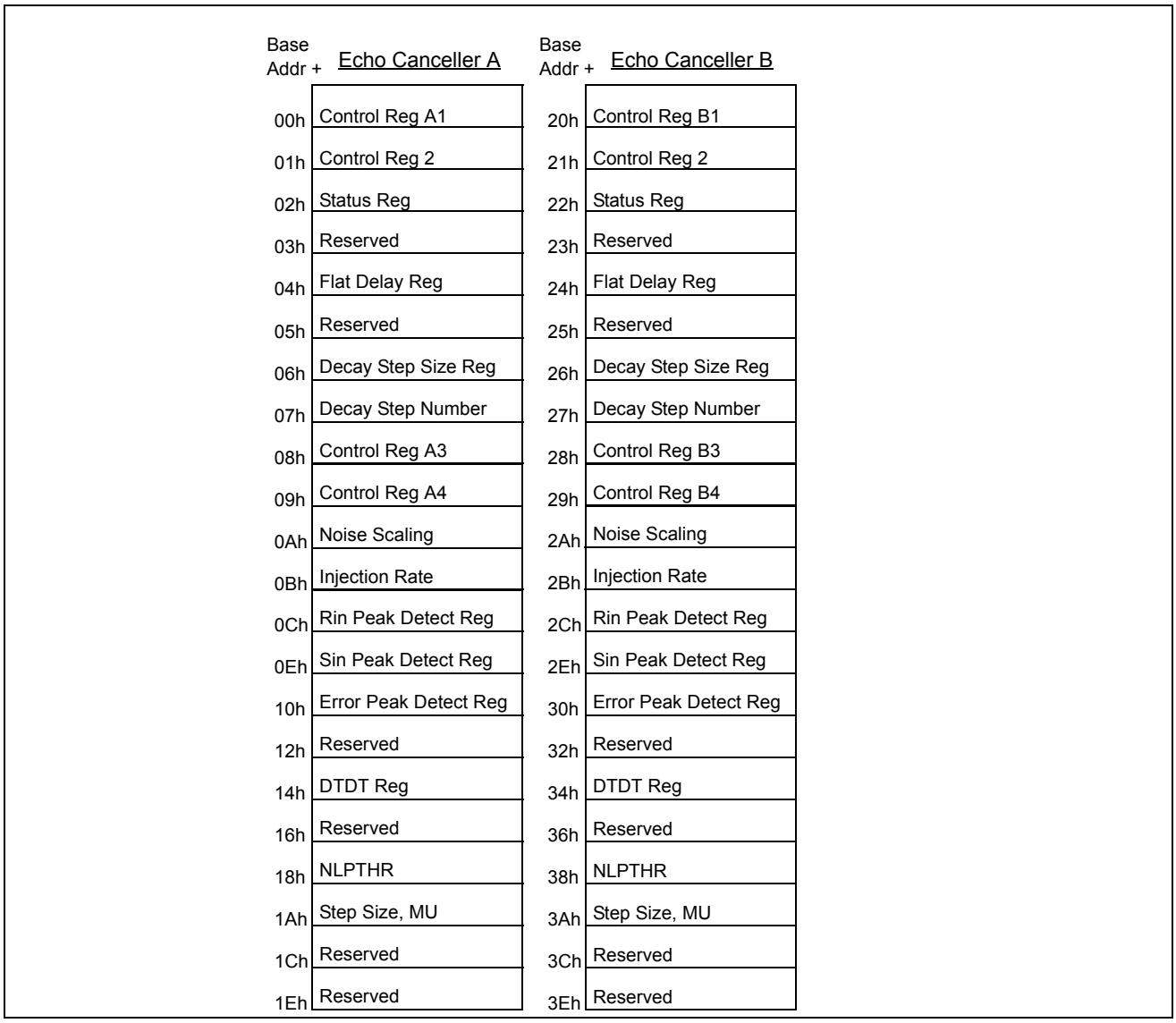


Figure 7 - Memory Mapping of per channel Control and Status Registers

Memory Mapped Control and Status registers

Internal memory and registers are memory mapped into the address space of the HOST interface. The internal dual ported memory is mapped into segments on a “per channel” basis to monitor and control each individual echo canceller and associated PCM channels. For example, in Normal configuration, echo canceller #5 makes use of Echo Canceller B from group 2. It occupies the internal address space from 0A0h to 0BFh and interfaces to PCM channel #5 on all serial PCM I/O streams.

As illustrated in Figure 7, the “per channel” registers provide independent control and status bits for each echo canceller. Figure 8 shows the memory map of the control/status register blocks for all echo cancellers.

When Extended Delay or Back-to-Back configuration is selected, Control Register A1/B1 and Control Register 2 of the selected group of echo cancellers require special care. Refer to the Register description section.

Table 2 is a list of the channels used for the 16 groups of echo cancellers when they are configured as Extended Delay or Back-to-Back

Normal Configuration

For a given group (group 0 to 15), 2 PCM I/O channels are used. For example, group 1 Echo Cancellers A and B, channels 2 and 3 are active.

Group	Channel	Group	Channel
0	0, 1	8	16, 17
1	2, 3	9	18, 19
2	4, 5	10	20, 21
3	6, 7	11	22, 23
4	8, 9	12	24, 25
5	10, 11	13	26, 27
6	12, 13	14	28, 29
7	14, 15	15	30, 31

Table 2 - Group and Channel Allocation

Extended Delay Configuration

For a given group (group 0 to 15), only one PCM I/O channel is active (Echo Canceller A) and the other channel carries don’t care data. For example, group 2, Echo Canceller A (Channel 4) will be active and Echo Canceller B (Channel 5) will carry don’t care data.

Back-to-Back Configuration

For a given group (group 0 to 15), only one PCM I/O channel is active (Echo Canceller A) and the other channel carries don’t care data. For example, group 5, Echo Canceller A (Channel 10) will be active and Echo Canceller B (Channel 11) will carry don’t care data.

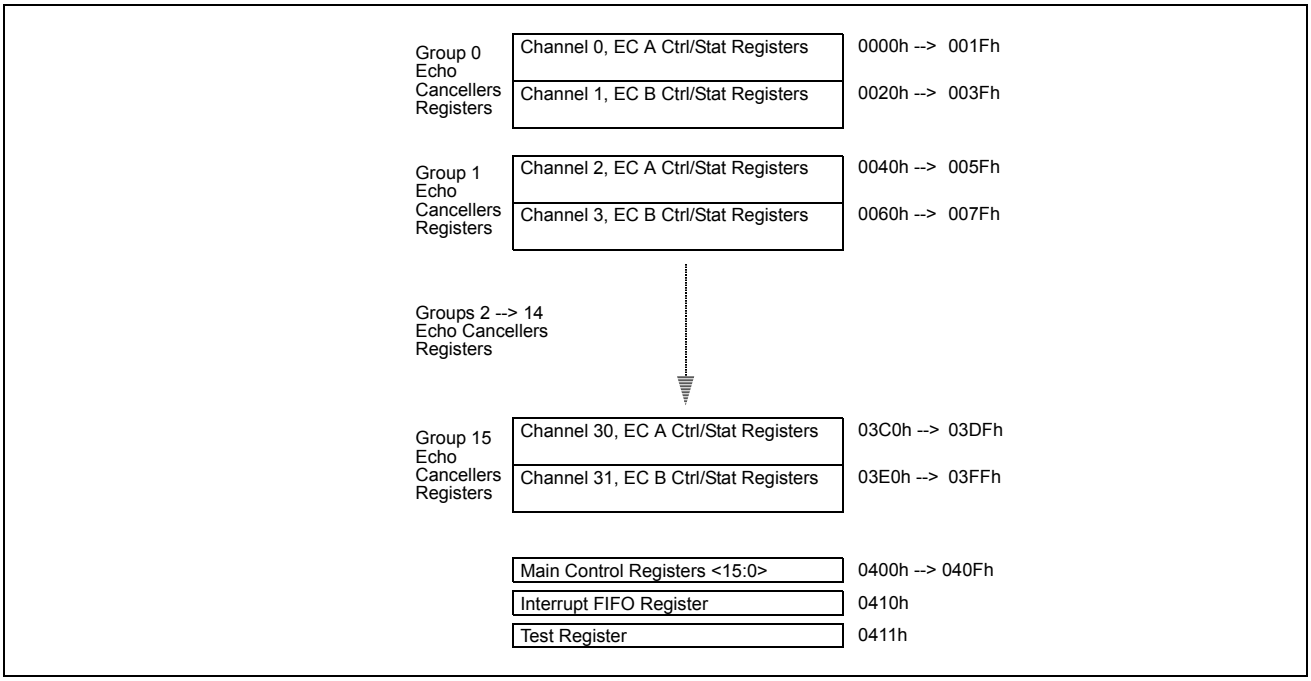


Figure 8 - Memory Mapping

Power Up Sequence

On power up, the RESET pin must be held low for 100µs. Forcing the RESET pin low will put the MT93L00 in power down state. In this state, all internal clocks are halted, D<7:0>, Sout, Rout, DTA and IRQ pins are tristated. The 16 Main Control Registers, the Interrupt FIFO Register and the Test Register are reset to zero.

When the RESET pin returns to logic high and a valid MCLK is applied, the user must wait 500µs for PLL to lock. C4i and F0i can be active during this period. Once the PLL has locked, the user must power up the 16 groups of echo cancellers individually, by writing a “1” into the PWUP bit in each group of echo canceller’s Main Control Register.

For each group of echo cancellers, when the PWUP bit toggles from zero to one, echo cancellers A and B execute their initialization routine. The initialization routine sets their registers, Base Address+00H to Base Address+3FH, to the default Reset Value and clears the Adaptive Filter coefficients. Two frames are necessary for the initialization routine to execute properly.

Once the initialization routine is executed, the user can set the per channel Control Registers, Base Address+00H to Base Address+3FH, for the specific application.

Power Management

Each group of echo cancellers can be placed in Power Down mode by writing a “0” into the PWUP bit in their respective Main Control Register. When a given group is in Power Down mode, the corresponding PCM data are bypassed from Rin to Rout and from Sin to Sout with two frames delay. Refer to the Main Control Register section for description.

The typical power consumption can be calculated with the following equation:

$$PC = 9 * Nb\_of\_groups + 3.6, \text{ in mW}$$

where $0 \leq Nb\_of\_groups \leq 16$

Call Initialization

To ensure fast initial convergence on a new call, it is important to clear the Adaptive filter. This is done by putting the echo canceller in bypass mode for at least one frame (125 μs) and then enabling adaptation.

Interrupts

The MT93L00 provides an interrupt pin (IRQ) to indicate to the HOST processor when a G.164 or G.165 Tone Disable is detected and released.

Although the MT93L00 may be configured to react automatically to tone disable status on any input PCM voice channels, the user may want for the external HOST processor to respond to Tone Disable information in an appropriate, application specific manner.

Each echo canceller will generate an interrupt when a Tone Disable occurs and will generate another interrupt when a Tone Disable releases.

Upon receiving an IRQ, the HOST CPU should read the Interrupt FIFO Register. This register is a FIFO memory containing the channel number of the echo canceller that has generated the interrupt.

All pending interrupts from any of the echo cancellers and their associated input channel number are stored in this FIFO memory. The IRQ always returns high after a read access to the Interrupt FIFO Register. The IRQ pin will toggle low for each pending interrupt.

After the HOST CPU has received the channel number of the interrupt source, the corresponding per channel Status Register can be read from internal memory to determine the cause of the interrupt (see Figure 7 for address mapping of Status register). The TD bit indicates the presence of a Tone Disable.

The MIRQ bit 5 in the Main Control Register 0 masks interrupts from the MT93L00. To provide more flexibility, the MTDBI (bit-4) and MTDAI (bit-3) bits in the Main Control Register<15:0> allow Tone Disable to be masked or unmasked, from generating an interrupt on a per channel basis. Refer to the Registers Description section.

JTAG Support

The MT93L00 JTAG interface conforms to the Boundary-Scan standard IEEE1149.1. This standard specifies a design-for-testability technique called Boundary-Scan test (BST). The operation of the Boundary Scan circuitry is controlled by an external Test Access Port (TAP) controller. JTAG inputs are 3.3 Volts compliant only.

Test Access Port (TAP)

The TAP provides access to many test functions of the MT93L00. It consists of three input pins and one output pin. The following pins are found on the TAP.

- Test Clock Input (TCK)

  The TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remains independent. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrent with the operation of the device and without interfering with the on-chip logic.

- Test Mode Select Input (TMS)

  The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to V_{DD1} when it is not driven from an external source.

- Test Data Input (TDI)

  Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to V_{DD1} when it is not driven from an external source

- Test Data Output (TDO)

  Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data from the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the Boundary Scan cells, the TDO driver is set to a high impedance state.

- Test Reset (TRST)

  This pin is used to reset the JTAG scan structure. This pin is internally pulled to V_{SS}.

Instruction Register

In accordance with the IEEE 1149.1 standard, the MT93L00 uses public instructions. The JTAG Interface contains a 3-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shifted-IR state. Subsequently, the instructions are decoded to achieve two basic functions: to select the test data register that will operate while the instruction is current, and to define the serial test data register path, which is used to shift data between TDI and TDO during data register scanning.

Test Data Registers

As specified in IEEE 1149.1, the MT93L00 JTAG Interface contains three test data registers:

- Boundary-Scan register

  The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the MT93L00 core logic.

- Bypass Register

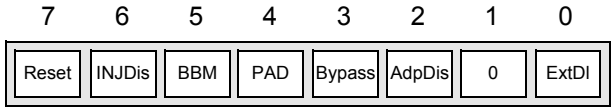
  The Bypass register is a single stage shift register that provides a one-bit path from TDI TDO.

- Device Identification register

  The Device Identification register provides access to the following encoded information:
  device version number, part number and manufacturer's name.

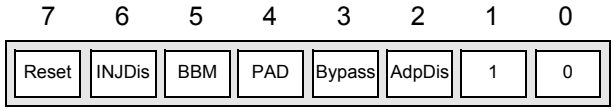
Register Descriptions

Echo Canceller A, Control Register A1 Read/Write Address: 00_H + Base Address



Reset Value: 00_H.

Echo Canceller B, Control Register B1 Read/Write Address: 20_H + Base Address

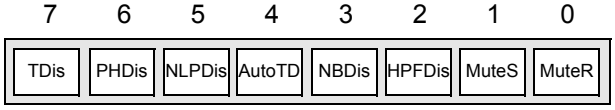


Reset Value: 02_H.

Bit	Name	Description
7	Reset	When high, the power-up initialization is executed which presets all register bits including this bit and clears the Adaptive Filter coefficients.
6	INJDis	When high, the noise injection process is disabled. When low noise injection is enabled.
5	BBM	When high the Back to Back configuration is enabled. When low the Normal configuration is enabled. Note: Do not enable Extended-Delay and BBM configurations at the same time. Always set **both** BBM bits of the two echo cancellers (Control Register A1 and Control Register B1) of the same group to the same logic value to avoid conflict.
4	PAD	When high, 12 dB of attenuation is inserted into the Rin to Rout path. When low the Rin to Rout path gain is 0 dB.
3	Bypass	When high, Sin data is by-passed to Sout and Rin data is by-passed to Rout. The Adaptive Filter coefficients are set to zero and the filter adaptation is stopped. When low, output data on both Sout and Rout is a function of the echo canceller algorithm.
2	AdpDis	When high, echo canceller adaptation is disabled. The MT93L00 cancels echo. When low, the echo canceller dynamically adapts to the echo path characteristics.
1	0 or 1	Bits marked as “1” or “0” are reserved bits and should be written as indicated.
0	ExtDl or 0	When high, Echo Cancellers A and B of the same group are internally cascaded into one 128 ms echo canceller. When low, Echo Cancellers A and B of the same group operate independently. Note: Do not enable both Extended-Delay and BBM configurations at the same time. Control Register B1 bit-0 is a reserved bit and should be written “0”.

Echo Canceller A, Control Register A2
Echo Canceller B, Control Register B2

Read/Write Address: 01_H + Base Address
Read/Write Address: 21_H + Base Address

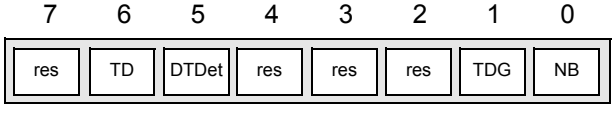


Reset Value: 00_H.

Bit	Name	Description
7	TDis	When high, tone detection is disabled. When low, tone detection is enabled. When both Echo Cancellers A and B TDis bits are high, Tone Disable processors are disabled entirely and are put into power down mode.
6	PHDis	When high, the tone detectors will trigger upon the presence of a 2100 Hz tone regardless of the presence/absence of periodic phase reversals. When low, the tone detectors will trigger only upon the presence of a 2100 Hz tone with periodic phase reversals.
5	NLPDis	When high, the non-linear processor is disabled. When low, the non-linear processors function normally. Useful for G.165 conformance testing.
4	AutoTD	When high, the echo canceller puts itself in Bypass mode when the tone detectors detect the presence of 2100 Hz tone. See PHDis for qualification of 2100 Hz tones. When low, the echo canceller algorithm will remain operational regardless of the state of the 2100 Hz tone detectors.
3	NBDis	When high, the narrow-band detector is disabled. When low, the narrow-band detector is enabled.
2	HPFDis	When high, the offset nulling high pass filters are bypassed in the Rin and Sin paths. When low, the offset nulling filters are active and will remove DC offsets on PCM input signals.
1	MuteS	When high, data on Sout is muted to quiet code. When low, Sout carries active code.
0	MuteR	When high, data on Rout is muted to quiet code. When low, Rout carries active code.

Echo Canceller A, Status Register
Echo Canceller B, Status Register

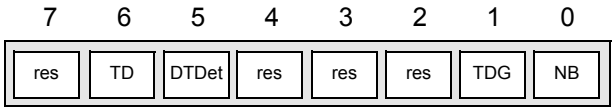
Read Address: 02_H + Base Address
Read Address: 22_H + Base Address



Reset Value: 00_H.

Bit	Name	Description
7	res	Reserved bit.
6	TD	Logic high indicates the presence of a 2100 Hz tone.

Echo Canceller A, Status Register Read Address: 02_H + Base Address
Echo Canceller B, Status Register Read Address: 22_H + Base Address



Reset Value: 00_H.

Bit	Name	Description
5	DTDet	Logic high indicates the presence of a double-talk condition.
4	res	Reserved bit.
3	res	Reserved bit.
2	res	Reserved bit.
1	TDG	Tone detection status bit gated with the AutoTD bit. Logic high indicates that AutoTD has been enabled and the tone detector has detected the presence of a 2100 Hz tone.
0	NB	Logic high indicates the presence of a narrow-band signal on Rin.

Echo Canceller A, Flat Delay Register (FD) Read/Write Address: 04h + Base Address
Echo Canceller B, Flat Delay Register (FD) Read/Write Address: 24h + Base Address

7	6	5	4	3	2	1	0
FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

Power Reset Value
00h

Echo Canceller A, Decay Step Number Register (NS) Read/Write Address: 07h + Base Address
Echo Canceller B, Decay Step Number Register (NS) Read/Write Address: 27h + Base Address

7	6	5	4	3	2	1	0
NS7	NS6	NS5	NS4	NS3	NS2	NS1	NS0

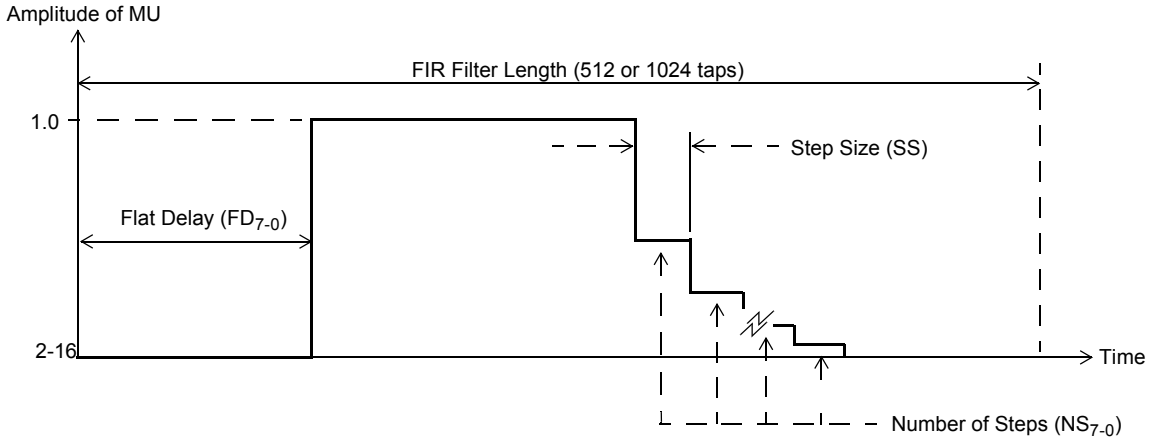
Power Reset Value
00h

Echo Canceller A, Decay Step Size Control Register (SSC) Read/Write Address: 06h + Base Address
Echo Canceller B, Decay Step Size Control Register (SSC) Read/Write Address: 26h + Base Address

7	6	5	4	3	2	1	0
0	0	0	0	0	SSC2	SSC1	SSC0

Power Reset Value
04h

Note: Bits marked with “0” are reserved bits and should be written “0”.



The Exponential Decay registers (Decay Step Number and Decay Step Size) and Flat Delay register allow the LMS adaptation step-size (MU) to be programmed over the length of the FIR filter. A programmable MU profile allows the performance of the echo canceller to be optimized for specific applications. For example, if the characteristic of the echo response is known to have a flat delay of several milliseconds and a roughly exponential decay of the echo impulse response, then the MU profile can be programmed to approximate this expected impulse response thereby improving the convergence characteristics of the Adaptive Filter. Note that in the following register descriptions, one tap is equivalent to 125 μs (64 ms/512 taps).

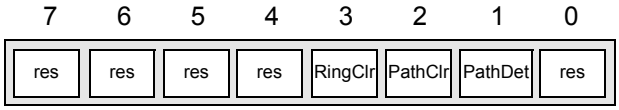
FD_{7-0} Flat Delay: This register defines the flat delay of the MU profile, (i.e., where the MU value is 2^{-16}). The delay is defined as FD_{7-0} x 8 taps. For example; if FD_{7-0} = 5, then MU=2^{-16} for the first 40 taps of the echo canceller FIR filter. The valid range of FD_{7-0} is: $0 \leq FD_{7-0} \leq 64$ in normal mode and $0 \leq FD_{7-0} \leq 128$ in extended-delay mode. The default value of FD_{7-0} is zero.

SSC_{2-0} Decay Step Size Control: This register controls the step size (SS) to be used during the exponential decay of MU. The decay rate is defined as a decrease of MU by a factor of 2 every SS taps of the FIR filter, where SS = 4 $x2^{SSC_{2-0}}$. For example; If SSC_{2-0} = 4, then MU is reduced by a factor of 2 every 64 taps of the FIR filter. The default value of SSC_{2-0} is 04h.NS_{7-0}Decay Step Number: This register defines the number of steps to be used for the decay of MU where each step has a period of SS taps (see SSC_{2-0}). The start of the exponential decay is defined as:

Filter Length (512 or 1024) - [Decay Step Number (NS_{7-0}) x Step Size (SS)] where SS = 4 $x2^{SSC_{2-0}}$.
For example, if NS_{7-0}=4 and SSC_{2-0}=4, then the exponential decay start value is 512 - [NS_{7-0} x SS] = 512 - [4 x ($4x2^4$)] = 256 taps for a filter length of 512 taps.

Echo Canceller A, Control Register A3
Echo Canceller B, Control Register B3

Read/Write Address: 08_H + Base Address
Read/Write Address: 28_H + Base Address

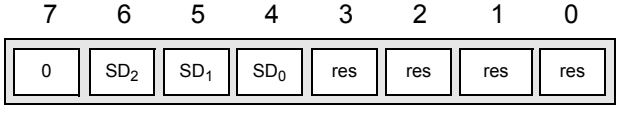


Reset Value: $0A_H$.

Bit	Name	Description
7-4	res	Reserved bits. Must always be set to zero for normal operation.
3	RingClr	When high, the instability detector is activated. When low, the instability detector is disabled
2	PathClr	When high, the current echo channel estimate will be cleared and the echo canceller will enter fast convergence mode upon detection of a path change. When low, the echo canceller will keep the current path estimate but revert to fast convergence mode upon detection of a path change. Note: this bit is ignored if PathDet is low.
1	PathDet	When high, the path change detector is activated. When low, the path change detector is disabled.
0	res	Reserved bit. Must always be set to zero for normal operation.

Echo Canceller A, Control Register A4
Echo Canceller B, Control Register B4

Read/Write Address: 09_H + Base Address
Read/Write Address: 29_H + Base Address



Reset Value: 50_H.

Bit	Name	Description
7	0	Must be set to zero.

Echo Canceller A, Control Register A4 Read/Write Address: 09_H + Base Address
Echo Canceller B, Control Register B4 Read/Write Address: 29_H + Base Address

7	6	5	4	3	2	1	0
0	SD_2	SD_1	SD_0	res	res	res	res

Reset Value: 50_H.

Bit	Name	Description
6-4	SupDec	These three bits control how long the echo canceller remains in a fast convergence state following a path change, Reset or Bypass operation. A value of zero will keep the echo canceller in fast convergence indefinitely.
3-0	res	Reserved bits. Must always be set to zero for normal operation.

Echo Canceller A, Noise Scaling (NS) Read/Write Address: 0Ah + Base Address
Echo Canceller B, Noise Scaling (NS) Read/Write Address: 2Ah + Base Address

7	6	5	4	3	2	1	0
NS7	NS6	NS5	NS4	NS3	NS2	NS1	NS0

Power Reset Value
74h

If the comfort noise level estimator is unable to correctly match the background noise level, this register can be used to scale the comfort noise up or down. A neutral value of 80h will prevent any scaling. Values less than 80h will scale the comfort noise level down. Values greater than 80h will scale the comfort noise level up. Scaling is done linearly, so to scale the comfort noise *down* by 1 dB, a value of 72h would be used (-1 dB = 89% of original level, $0.89_{(dec)}$ • 80h = 72h). Similarly, to scale up by 1 dB, use a value of 8Fh (1 dB = 112% of original level, $1.12_{(dec)}$ • 80h = 8Fh).

Echo Canceller A, Injection Rate (IR) Read/Write Address: 0Bh + Base Address
Echo Canceller B, Injection Rate (IR) Read/Write Address: 2Bh + Base Address

7	6	5	4	3	2	1	0
IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0

Power Reset Value
0Ch

The NLP ramps-in comfort noise during the initial background noise estimation stage. This register provides control over the ramp-in speed. Higher values will increase the ramp-in speed.

Echo Canceller A, Rin Peak Detect Register 2 (RP) Read Address: 0Dh + Base Address
Echo Canceller B, Rin Peak Detect Register 2 (RP) Read Address: 2Dh + Base Address

7	6	5	4	3	2	1	0
RP15	RP14	RP13	RP12	RP11	RP10	RP9	RP8

Power Reset Value
N/A

Echo Canceller A, Rin Peak Detect Register 1 (RP) Read Address: 0Ch + Base Address
Echo Canceller B, Rin Peak Detect Register 1 (RP) Read Address: 2Ch + Base Address

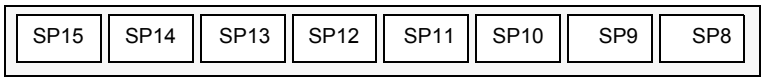
7	6	5	4	3	2	1	0
RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0

Power Reset Value
N/A

These peak detector registers allow the user to monitor the receive in signal (Rin) peak signal level. The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers for each echo canceller. The high byte is in Register 2 and the low byte is in Register 1.

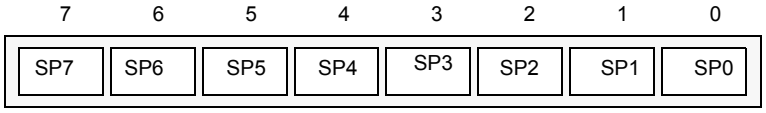
Echo Canceller A, Sin Peak Detect Register 2 (SP) Read Address: 0Fh + Base Address
Echo Canceller B, Sin Peak Detect Register 2 (SP) Read Address: 2Fh + Base Address

Power Reset Value
N/A



Echo Canceller A, Sin Peak Detect Register 1 (SP) Read Address: 0Eh + Base Address
Echo Canceller B, Sin Peak Detect Register 1 (SP) Read Address: 2Eh + Base Address

Power Reset Value
N/A



These peak detector registers allow the user to monitor the send in signal (Sin) peak signal level. The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers for each echo canceller. The high byte is in Register 2 and the low byte is in Register 1.

Main Control Register 1	(EC group 1)	Read/Write Address:	401_H
Main Control Register 2	(EC group 2)	Read/Write Address:	402_H
Main Control Register 3	(EC group 3)	Read/Write Address:	403_H
Main Control Register 4	(EC group 4)	Read/Write Address:	404_H
Main Control Register 5	(EC group 5)	Read/Write Address:	405_H
Main Control Register 6	(EC group 6)	Read/Write Address:	406_H
Main Control Register 7	(EC group 7)	Read/Write Address:	407_H
Main Control Register 8	(EC group 8)	Read/Write Address:	408_H
Main Control Register 9	(EC group 9)	Read/Write Address:	409_H
Main Control Register 10	(EC group 10)	Read/Write Address:	$40A_H$
Main Control Register 11	(EC group 11)	Read/Write Address:	$40B_H$
Main Control Register 12	(EC group 12)	Read/Write Address:	$40C_H$
Main Control Register 13	(EC group 13)	Read/Write Address:	$40D_H$
Main Control Register 14	(EC group 14)	Read/Write Address:	$40E_H$
Main Control Register 15	(EC group 15)	Read/Write Address:	$40F_H$

Echo Canceller A, Error Peak Detect Register 2 (EP) Read Address: 11h + Base Address
Echo Canceller B, Error Peak Detect Register 2 (EP) Read Address: 31h + Base Address

Power Reset Value
N/A

7	6	5	4	3	2	1	0
EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8

Echo Canceller A, Error Peak Detect Register 1 (EP) Read Address: 10h + Base Address
Echo Canceller B, Error Peak Detect Register 1 (EP) Read Address: 30h + Base Address

Power Reset Value
N/A

7	6	5	4	3	2	1	0
EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0

These peak detector registers allow the user to monitor the error signal peak level. The information is in 16-bit 2's complement linear coded format presented in two 8 bit registers for each echo canceller. The high byte is in Register 2 and the low byte is in Register 1.

Echo Canceller A, Double-Talk Detection Threshold Register 2 Read/Write Address: 15h + Base Address
Echo Canceller B, Double-Talk Detection Threshold Register 2 Read/Write Address: 35h + Base Address

Power Reset Value
48h

7	6	5	4	3	2	1	0	
DTDT15	DTDT14	DTDT13	DTDT12	DTDT11	DTDT10	DTDT9	DTDT8	**(DTDT)**

Echo Canceller A, Double-Talk Detection Threshold Register 1 Read/Write Address: 14h + Base Address
Echo Canceller B, Double-Talk Detection Threshold Register 1 Read/Write Address: 34h + Base Address

Power Reset Value
00h

7	6	5	4	3	2	1	0	
DTDT7	DTDT6	DTDT5	DTDT4	DTDT3	DTDT2	DTDT1	DTDT0	**(DTDT)**

This register allows the user to program the level of Double-Talk Detection Threshold (DTDT). The 16 bit 2's complement linear value defaults to 4800h= 0.5625 or -5 dB. The maximum value is 7FFFh = 0.9999 or 0 dB. The high byte is in Register 2 and the low byte is in Register 1.

Echo Canceller A, Non-Linear Processor Threshold Register 2 Read/Write Address: 19h + Base Address
Echo Canceller B, Non-Linear Processor Threshold Register 2 Read/Write Address: 39h + Base Address

7	6	5	4	3	2	1	0
NLP15	NLP14	NLP13	NLP12	NLP11	NLP10	NLP9	NLP8

(NLPTHR)

Power Reset Value 0Bh

Echo Canceller A, Non-Linear Processor Threshold Register 1 Read/Write Address: 18h + Base Address
Echo Canceller B, Non-Linear Processor Threshold Register 1 Read/Write Address: 38h + Base Address

7	6	5	4	3	2	1	0
NLP7	NLP6	NLP5	NLP4	NLP3	NLP2	NLP1	NLP0

(NLPTHR)

Power Reset Value 60h

This register allows the user to program the level of the Non-Linear Processor Threshold (NLPTHR). The 16 bit 2's complement linear value defaults to 0B60h = 0.0889 or -21.0 dB. The maximum value is 7FFFh = 0.9999 or 0 dB. The high byte is in Register 2 and the low byte is in Register 1.

Echo Canceller A, Adaptation Step Size (MU) Register 2 Read/Write Address: 1Bh + Base Address
Echo Canceller B, Adaptation Step Size (MU) Register 2 Read/Write Address: 3Bh + Base Address

7	6	5	4	3	2	1	0
MU15	MU14	MU13	MU12	MU11	MU10	MU9	MU8

(MU)

Power Reset Value 40h

Echo Canceller A, Adaptation Step Size (MU) Register 1 Read/Write Address: 1Ah + Base Address
Echo Canceller B, Adaptation Step Size (MU) Register 1 Read/Write Address: 3Ah + Base Address

7	6	5	4	3	2	1	0
MU7	MU6	MU5	MU4	MU3	MU2	MU1	MU0

(MU)

Power Reset Value 00h

This register allows the user to program the level of MU. MU is a 16 bit 2's complement value which defaults to 4000h = 1.0
The maximum value is 7FFFh or 1.9999 decimal. The high byte is in Register 2 and the low byte is in Register 1.

Main Control Register 0 (EC group 0) Read/Write Address: 400_H

7	6	5	4	3	2	1	0
WR_all	ODE	MIRQ	MTDBI	MTDAI	Format	LAW	PWUP

Reset Value: 00_H.

Bit	Name	Description
7	WR_all	Write all control bit: When high, Group 0-15 Echo Cancellers Registers are mapped into 0000h to 0003Fh which is Group 0 address mapping. Useful to initialize the 16 Groups of Echo Cancellers as per Group 0. When low, address mapping is per Figure 8. **Note:** Only the **Main Control Register 0** has the WR_all bit.

Main Control Register 0 (EC group 0) Read/Write Address: 400_H

7	6	5	4	3	2	1	0
WR_all	ODE	MIRQ	MTDBI	MTDAI	Format	LAW	PWUP

Reset Value: 00_H.

Bit	Name	Description
6	ODE	Output Data Enable: This control bit is logically AND'd with the ODE input pin. When both ODE bit and ODE input pin are high, the Rout and Sout outputs are enabled. When the ODE bit is low or the ODE input pin is low, the Rout and Sout outputs are high impedance. **Note:** Only the **Main Control Register 0** has the ODE bit.
5	MIRQ	Mask Interrupt: When high, all the interrupts from the Tone Detectors output are masked. The Tone Detectors operate as specified in their Echo Canceller B, Control Register 2. When low, the Tone Detectors Interrupts are active. **Note:** Only the **Main Control Register 0** has the MIRQ bit.
4	MTDBI	Mask Tone Detector B Interrupt: When high, the Tone Detector interrupt output from Echo Canceller B is masked. The Tone Detector operates as specified in Echo Canceller B, Control Register 2. When low, the Tone Detector B Interrupt is active.
3	MTDAI	Mask Tone Detector A Interrupt: When high, the Tone Detector interrupt output from Echo Canceller A is masked. The Tone Detector operates as specified in Echo Canceller A, Control Register 2. When low, the Tone Detector A Interrupt is active.
2	Format	ITU-T/Sign Mag: When high, both Echo Cancellers A and B for a given group, accept ITU-T (G.711) PCM code. When low, both Echo Cancellers A and B for a given group, accept sign-magnitude PCM code.
1	LAW	A/μ Law: When high, both Echo Cancellers A and B for a given group, accept A-Law companded PCM code. When low, both Echo Cancellers A and B for a given group, accept μ-Law companded PCM code.
0	PWUP	Power-UP: When high, both Echo Cancellers A and B and Tone Detectors for a given group, are active. When low, both Echo Cancellers A and B and Tone Detectors for a given group, are placed in Power Down mode. In this mode, the corresponding PCM data are bypassed from Rin to Rout and from Sin to Sout with two frames delay. When the PWUP bit toggles from zero to one, the echo canceller A and B execute their initialization routine which presets their registers, Base Address+00H to Base Address+3FH, to default Reset Value and clears the Adaptive Filter coefficients. Two frames are necessary for the initialization routine to execute properly. Once the initialization routine is executed, the user can set the per channel Control Registers for their specific application.

Bit	Name	Description
7-5	unused	Unused Bits.
4	MTDBI	Mask Tone Detector B Interrupt: When high, the Tone Detector interrupt output from Echo Canceller B is masked. The Tone Detector operates as specified in Echo Canceller B, Control Register 2. When low, the Tone Detector B Interrupt is active.
3	MTDAI	Mask Tone Detector A Interrupt: When high, the Tone Detector interrupt output from Echo Canceller A is masked. The Tone Detector operates as specified in Echo Canceller A, Control Register 2. When low, the Tone Detector A Interrupt is active.
2	Format	ITU-T/Sign Mag: When high, both Echo Cancellers A and B for a given group, select ITU-T (G.711) PCM code. When low, both Echo Cancellers A and B for a given group, select sign-magnitude PCM code.
1	LAW	A/μ Law: When high, both Echo Cancellers A and B for a given group, select A-Law companded PCM code. When low, both Echo Cancellers A and B for a given group, select m-Law companded PCM code.
0	PWUP	Power-UP: When high, both Echo Cancellers A and B and Tone Detectors for a given group, are active. When low, both Echo Cancellers A and B and Tone Detectors for a given group, are placed in Power Down mode. In this mode, the corresponding PCM data are bypassed from Rin to Rout and from Sin to Sout with two frames delay. When the PWUP bit toggles from zero to one, the echo cancellers A and B execute their initialization routine which presets their registers, Base Address+00H to Base Address+3FH, to default Reset Value and clears the Adaptive Filter coefficients. Two frames are necessary for the initialization routine to execute properly. Once the initialization routine is executed, the user can set the per channel Control Registers for their specific application.

Interrupt FIFO Register Read Address: 410_H (Read only)

7	6	5	4	3	2	1	0
IRQ	0	0	I4	I3	I2	I1	I0

Reset Value: 00_H.

Bit	Name	Description
7	IRQ	Logic high indicates an interrupt has occurred. IRQ bit is cleared after the Interrupt FIFO register is read. Logic Low indicates that no interrupt is pending and the FIFO is empty.
6:5	0	Unused bits. Always zero

Interrupt FIFO Register Read Address: 410_H (Read only)

7	6	5	4	3	2	1	0
IRQ	0	0	I4	I3	I2	I1	I0

Reset Value: 00_H.

Bit	Name	Description
4:0	I<4:0>	I<4:0> binary code indicates the channel number at which a Tone Detector state change has occurred. Note: Whenever a Tone Disable is detected or released, an interrupt is generated.

Test Register Read/Write Address: 411_H

7	6	5	4	3	2	1	0
res	res	res	res	res	res	res	Tirq

Reset Value: 00_H.

Bit	Name	Description
7:1	res	Reserved bits. Must always be set to zero for normal operation.
0	Tirq	Test IRQ: Useful for the application engineer to verify the interrupt service routine. When high, any change to MTDBI and MTDAI bits of the Main Control Register will cause an interrupt and its corresponding channel number will be available from the Interrupt FIFO Register. When low, normal operation is selected.

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	I/O Supply Voltage (V_{DD1})	V_{DD1}	-0.3	5.0	V
2	Core Supply Voltage (V_{DD2})	V_{DD2}	-0.3	2.5	V
3	Input on any I/O pins (other than supply pins)	V_{I3}	V_{SS} - 0.3	V_{DD1}+0.5	V
4	Input on any 5 V Tolerant I/O pins	V_{I5}	V_{SS} - 0.3	5.5	V
5	Continuous Current at digital outputs	I_o		20	mA
6	Package power dissipation	P_D		2.0	W
7	Storage temperature	T_S	-55	150	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - **Voltages are with respect to ground (Vss) unless otherwise stated.**

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		+85	°C	
2	I/O Supply Voltage	V_{DD1}	3.0	3.3	3.6	V	Device I/O voltage
3	Core Supply Voltage	V_{DD2}	1.6	1.8	1.9	V	Device core voltage
4	Input High Voltage on 3.3 V tolerant I/O	V_{IH3}	$0.7V_{DD1}$		V_{DD1}	V	
5	Input High Voltage on 5 V tolerant I/O	V_{IH5}	$0.7V_{DD1}$		5.5	V	
6	Input Low Voltage	V_{IL}			$0.3V_{DD1}$	V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

DC Electrical Characteristics† - Voltages are with respect to ground (V_{ss}) unless otherwise stated.

		Characteristics	Sym.	Min.	Ty.p‡	Max.	Units	Test Conditions
1		Static Supply Current***	I_{CC}			250	µA	$\overline{RESET}$ = 0
		IDD_IO (VDD1=3.3V)*** (single device)	I_{DD_IO}		10		mA	32 channels of **single** device are active
		IDD_CORE (single device) (VDD2 =1.8V)***	IDD_CORE		65		mA	32 channels of **single** device are active
2		Total Power Consumption for all 4 devices	P_C		600		mW	All devices and **all 128** channels are active
3	**INPUTS**	Input High Voltage	V_{IH}	$0.7V_{DD1}$			V	
4		Input Low Voltage	V_{IL}			$0.3V_{DD1}$	V	
5		Input Leakage Input Leakage on Pullup Input Leakage on Pulldown	I_{IH}/I_{IL} I_{LU} I_{LD}		 -30 30		µA µA µA	$V_{IN}=V_{SS\ to\ VDD1}$ or 5.5V $V_{IN}=V_{SS}$ $V_{IN}=V_{DD1}$ See Note 1
6		Input Pin Capacitance	C_I		3	10	pF	
7	**OUTPUTS**	Output High Voltage	V_{OH}	$0.8V_{DD1}$			V	I_{OH} = 10 mA
8		Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10 mA
9		High Impedance Leakage	I_{OZ}			10	µA	$V_{IN}=V_{SS\ to}$ 5.5V
10		Output Pin Capacitance	C_O		5	10	pF	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD1}=3.3 V and are for design aid only: not guaranteed and not subject to production testing.
* Note 1: Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (V_{IN}).
The *** specifications are for 1 MT93L00 device of the Multi-chip module.

AC Electrical Characteristics† - Timing Parameter Measurement Voltage Levels - Voltages are with respect to ground (V_{ss}) unless otherwise stated.

	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold	V_{TT}	$0.5V_{DD1}$	V	
2	CMOS Rise/Fall Threshold Voltage High	V_{HM}	$0.7V_{DD1}$	V	
3	CMOS Rise/Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD1}$	V	

† Characteristics are over recommended operating conditions unless otherwise stated

AC Electrical Characteristics† - Frame Pulse and $\overline{C4i}$

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Frame pulse width (ST-BUS, GCI)	t_{FPW}	20		2* tcP-20	ns	
2	Frame Pulse Setup time before $\overline{C4i}$ falling (ST-BUS or GCI)	t_{FPS}	10	122	150	ns	
3	Frame Pulse Hold Time from $\overline{C4i}$ falling (ST-BUS or GCI)	t_{FPH}	10	122	150	ns	
4	$\overline{C4i}$ Period	t_{CP}	190	244.1	300	ns	
5	$\overline{C4i}$ Pulse Width High	t_{CH}	85		150	ns	
6	$\overline{C4i}$ Pulse Width Low	t_{CL}	85		150	ns	
7	$\overline{C4i}$ Rise/Fall Time	t_r, t_f			10	ns	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD1}=3.3V and for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - Serial Streams for ST-BUS and GCI Backplanes

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Rin/Sin Set-up Time	t_{SIS}	10			ns	
2	Rin/Sin Hold Time	t_{SIH}	10			ns	
3	Rout/Sout Delay - Active to Active	t_{SOD}			60	ns	C_L=150pF
4	Output Data Enable (ODE) Delay	t_{ODE}			30	ns	C_L=150pF, R_L=1K See Note 1

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD1}=3.3 V and for design aid only: not guaranteed and not subject to production testing
* Note1: High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

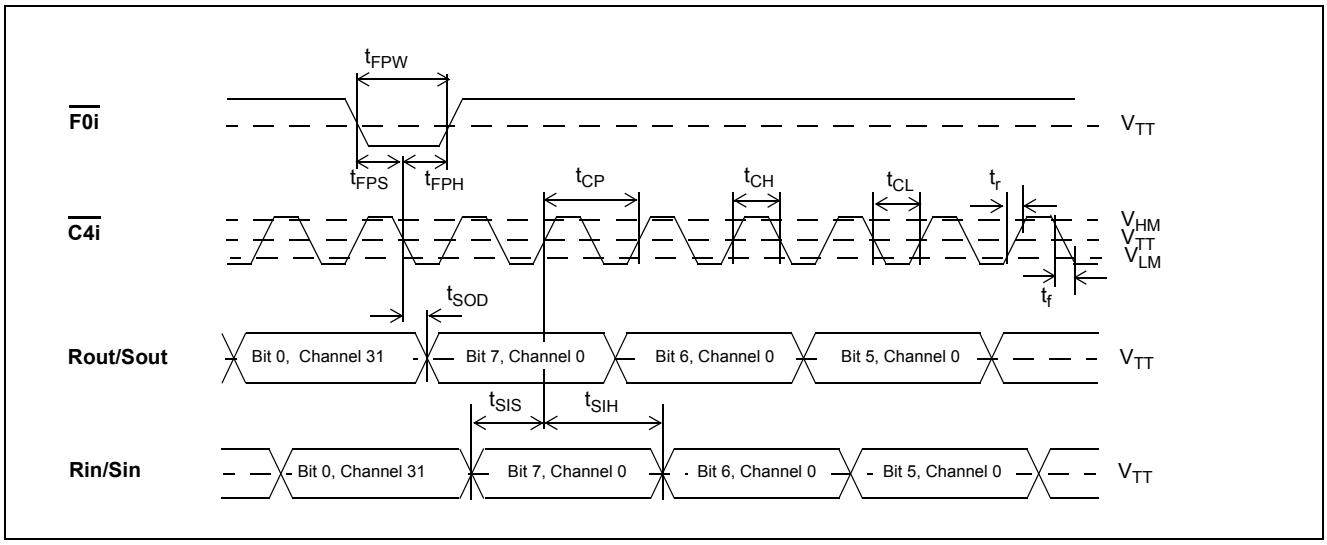


Figure 9 - ST-BUS Timing at 2.048 Mb/s

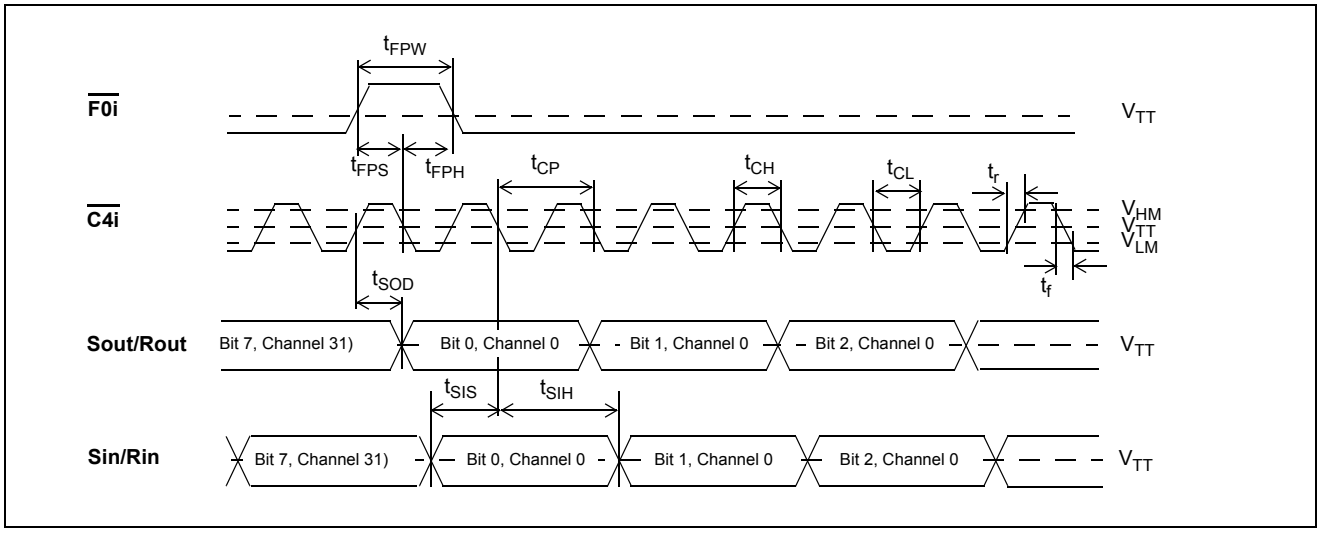


Figure 10 - GCI Interface Timing at 2.048 Mb/s

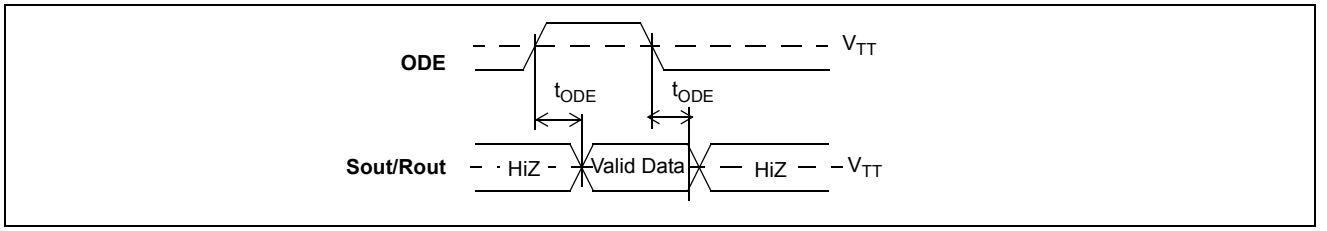


Figure 11 - Output Driver Enable (ODE)

AC Electrical Characteristics† - Master Clock - Voltages are with respect to ground (V_{SS}). unless otherwise stated.

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Master Clock Frequency, - Fsel = 0 - Fsel = 1	 f_{MCF0} f_{MCF1}	 19.0 9.5	 20.0 10.0	 21.0 10.5	 MHz MHz	
2	Master Clock Low	t_{MCL}	20			ns	
3	Master Clock High	t_{MCH}	20			ns	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD1}=3.3V and for design aid only: not guaranteed and not subject to production testing

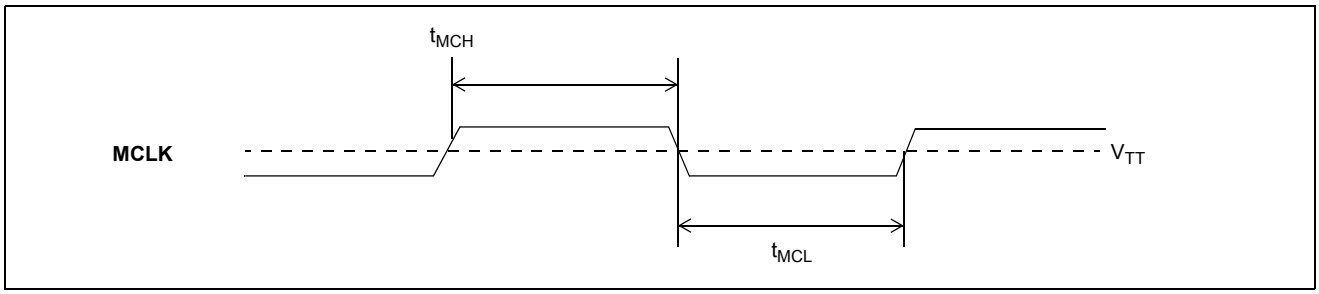


Figure 12 - Master Clock

AC Electrical Characteristics† - Motorola Non-Multiplexed Bus Mode

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	$\overline{CS}$ setup from DS falling	t_{CSS}	0			ns	
2	R/$\overline{W}$ setup from DS falling	t_{RWS}	0			ns	
3	Address setup from DS falling	t_{ADS}	0			ns	
4	$\overline{CS}$ hold after DS rising	t_{CSH}	0			ns	
5	R/$\overline{W}$ hold after DS rising	t_{RWH}	0			ns	
6	Address hold after DS rising	t_{ADH}	0			ns	
7	Data delay on read	t_{DDR}			79	ns	C_L=150pF, R_L=1K
8	Data hold on read	t_{DHR}	3		15	ns	C_L=150pF, R_L=1K See Note 1
9	Data setup on write	t_{DSW}	0			ns	
10	Data hold on write	t_{DHW}	0			ns	
11	Acknowledgment delay	t_{AKD}			80	ns	C_L=150pF, R_L=1K
12	Acknowledgment hold time	t_{AKH}	0		8	ns	C_L=150pF, R_L=1K, See Note 1
13	$\overline{IRQ}$ delay	t_{IRD}	20		65	ns	C_L=150pF, R_L=1K, See Note 1

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD1}=3.3 V and for design aid only: not guaranteed and not subject to production testing
*Note 1:High Impedance is measured by pulling to the appropriate rail with RL, with timing corrected to cancel time taken to discharge CL.

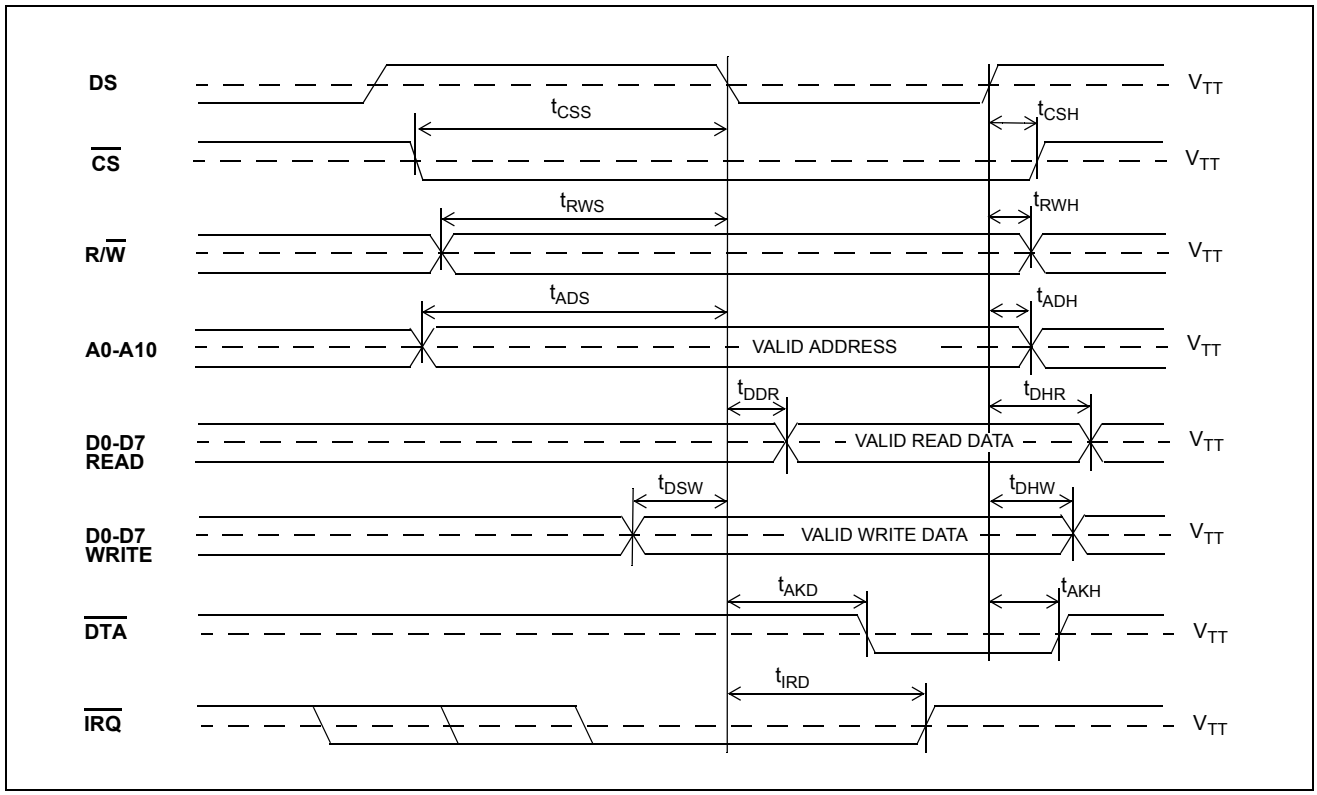
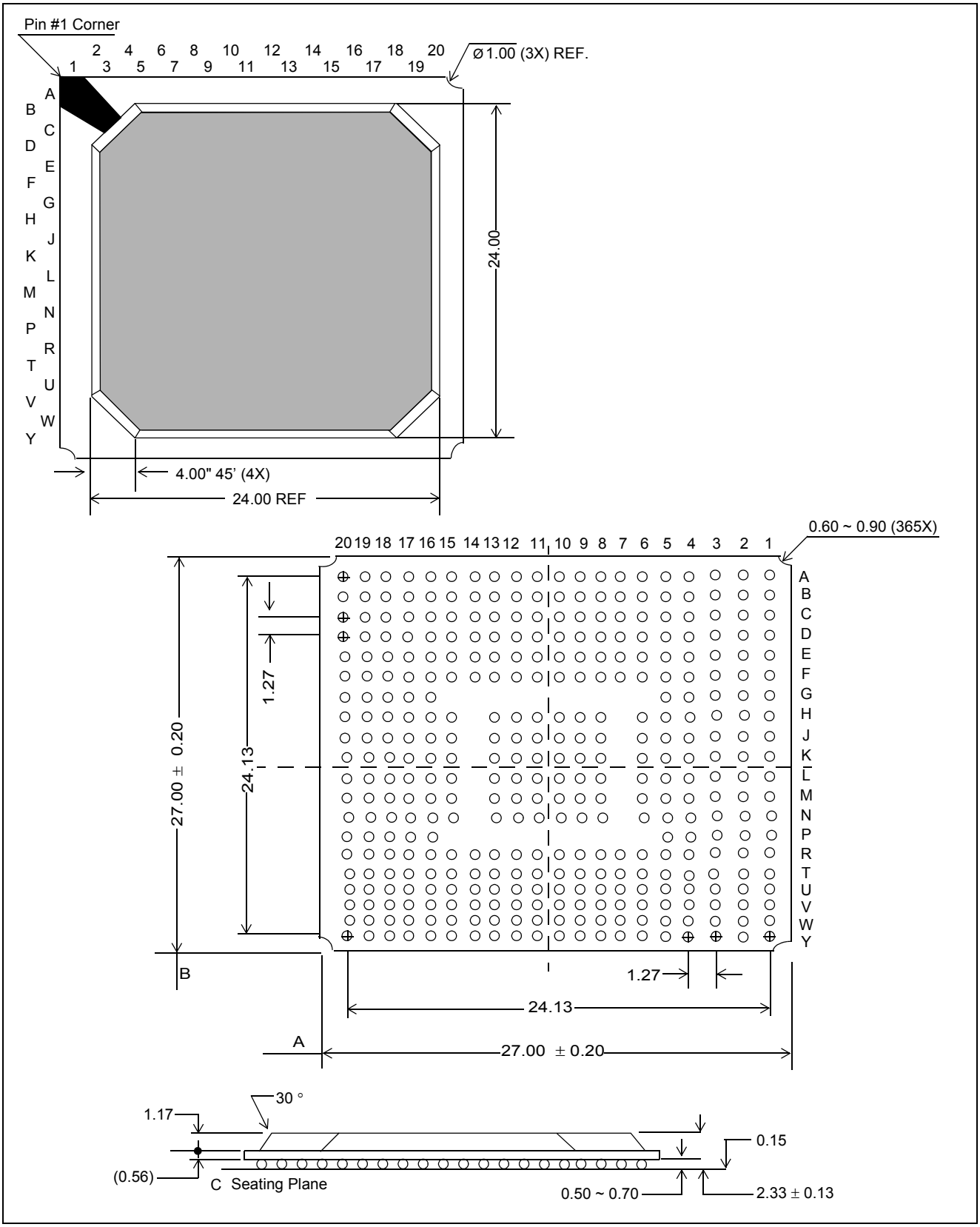
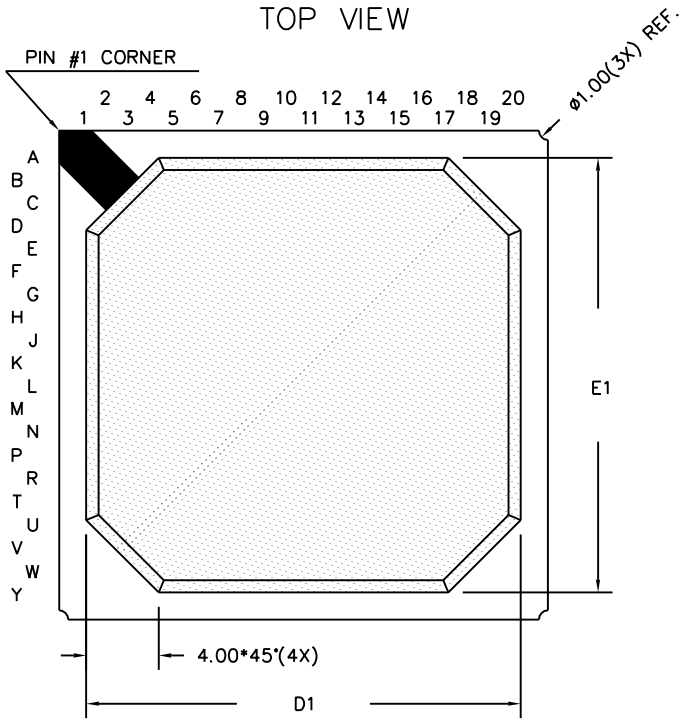


Figure 13 - Motorola Non-Multiplexed Bus Timing

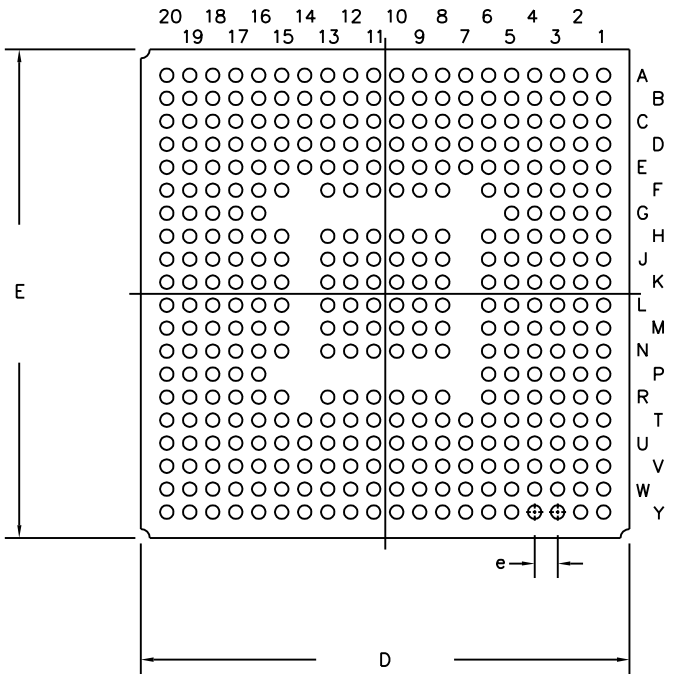


MT93L04AG 365 -Ball BGA

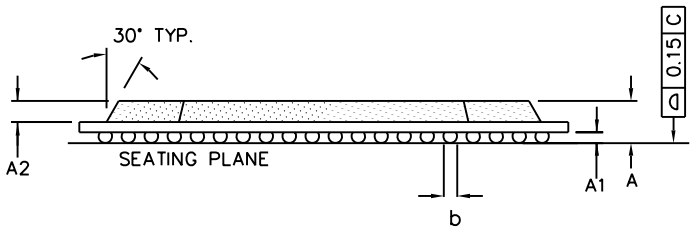
TOP VIEW



BOTTOM VIEW



DIMENSION	MIN	MAX
A	2.20	2.46
A1	0.50	0.70
A2	1.17 REF	
D	26.80	27.20
D1	24.00 REF	
E	26.80	27.20
E1	24.00 REF	
b	0.60	0.90
e	1.27	
N	365	
Conforms to JEDEC MS-034		



SIDE VIEW

NOTES: –
1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crow of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.56 MM.
6. Ball diameter and standoff different from Jedec Spec MS-034

ISSUE	1			
ACN	26Sep02			
DATE	213469			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

Package Code GB

Package Outline for 365 B MCM BGA (27x27x2.33mm)

GPD00800

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