

International IR Rectifier

PD - 94867

IRFI9Z34NPbF

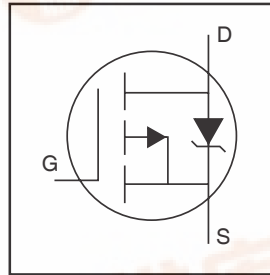
HEXFET® Power MOSFET

- Advanced Process Technology
- Isolated Package
- High Voltage Isolation = 2.5KVRMS ⑤
- Sink to Lead Creepage Dist. = 4.8mm
- P-Channel
- Fully Avalanche Rated
- Lead-Free

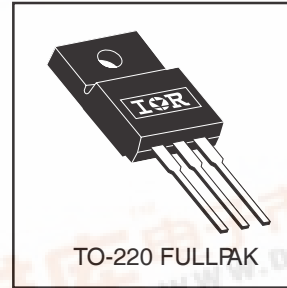
Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



$V_{DSS} = -55V$
$R_{DS(on)} = 0.10\Omega$
$I_D = -14A$



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-14	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-10	
I_{DM}	Pulsed Drain Current ①⑥	- 68	
$P_D @ T_C = 25^\circ C$	Power Dissipation	37	W
	Linear Derating Factor	0.24	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑥	180	mJ
I_{AR}	Avalanche Current①⑥	-10	A
E_{AR}	Repetitive Avalanche Energy①	3.7	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑥	-5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf·in (1.1N·m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	4.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	---	65	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-55	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	-0.05	—	V/°C	Reference to 25°C, I _D = -1mA⑥
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.10	Ω	V _{GS} = -10V, I _D = -7.8A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance	4.2	—	—	S	V _{DS} = 25V, I _D = -10A⑥
I _{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	V _{DS} = -55V, V _{GS} = 0V
		—	—	-250		V _{DS} = -44V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	35	nC	I _D = -10A
Q _{gs}	Gate-to-Source Charge	—	—	7.9		V _{DS} = -44V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	16		V _{GS} = -10V, See Fig. 6 and 13 ④⑥
t _{d(on)}	Turn-On Delay Time	—	13	—	ns	V _{DD} = -28V
t _r	Rise Time	—	55	—		I _D = -10A
t _{d(off)}	Turn-Off Delay Time	—	30	—		R _G = 13Ω
t _f	Fall Time	—	41	—		R _D = 2.6Ω, See Fig. 10 ④⑥
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	620	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	280	—		V _{DS} = -25V
C _{rss}	Reverse Transfer Capacitance	—	140	—		f = 1.0MHz, See Fig. 5⑥

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-14	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	-68		
V _{SD}	Diode Forward Voltage	—	—	-1.3	V	T _J = 25°C, I _S = -7.8A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	54	82	ns	T _J = 25°C, I _F = -10A
Q _{rr}	Reverse Recovery Charge	—	110	160	nC	di/dt = -100A/μs ④⑥
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 3.6mH
R_G = 25Ω, I_{AS} = -10A. (See Figure 12)
- ③ I_{SD} ≤ -10A, di/dt ≤ -290A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ t = 60s, f = 60Hz
- ⑥ Uses IRF9Z34N data and test conditions

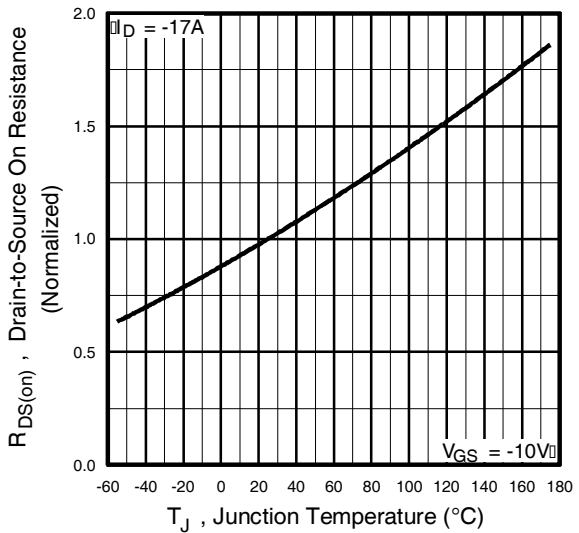
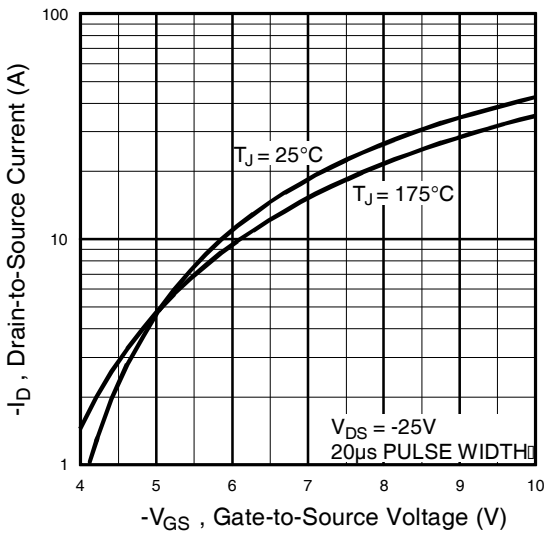
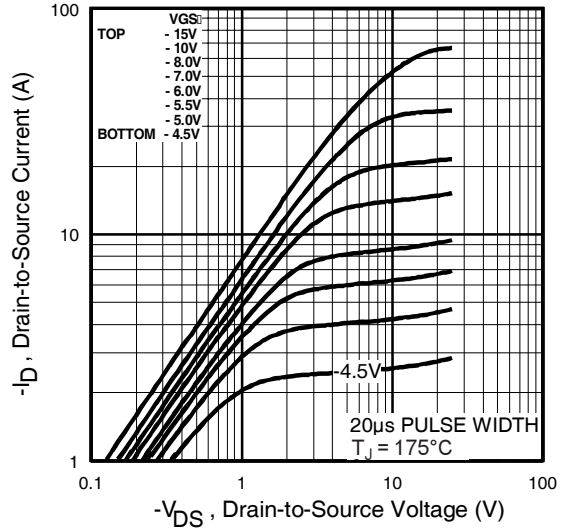
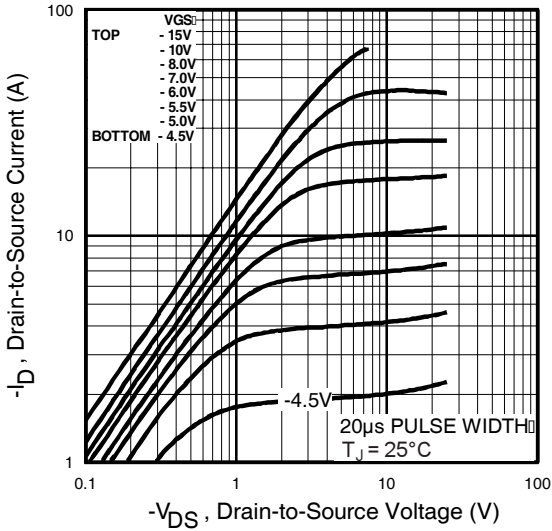


Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance Vs. Temperature

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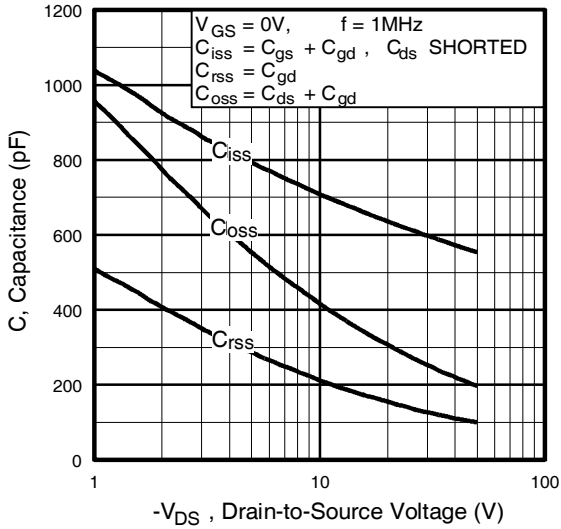


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

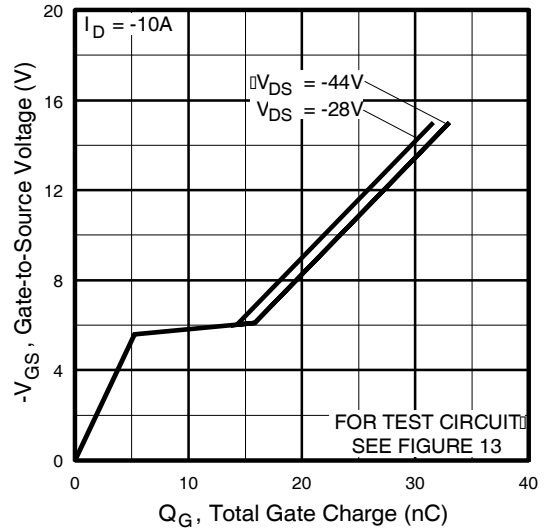


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

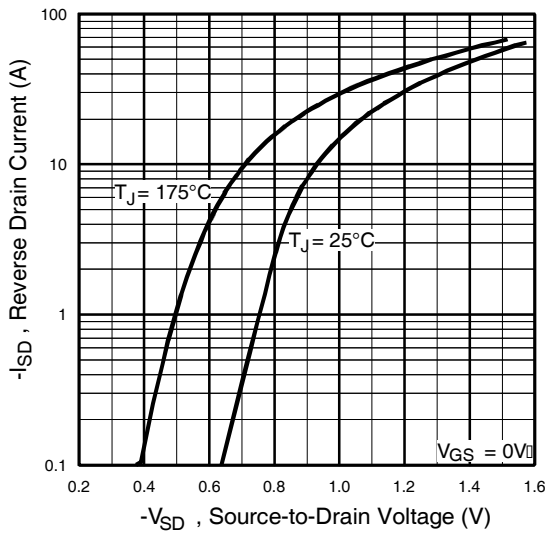


Fig 7. Typical Source-Drain Diode Forward Voltage

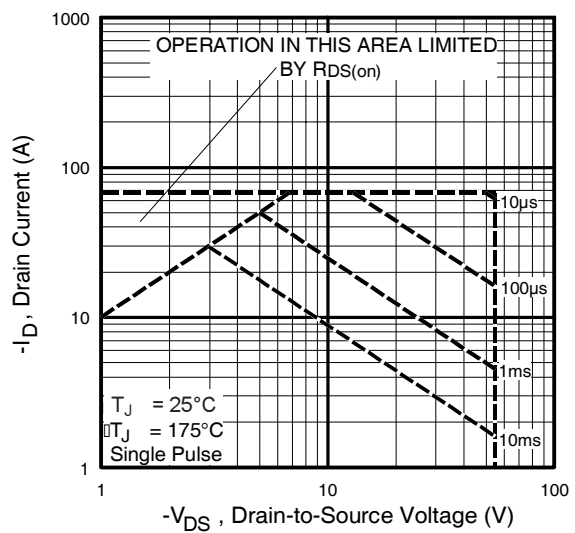


Fig 8. Maximum Safe Operating Area

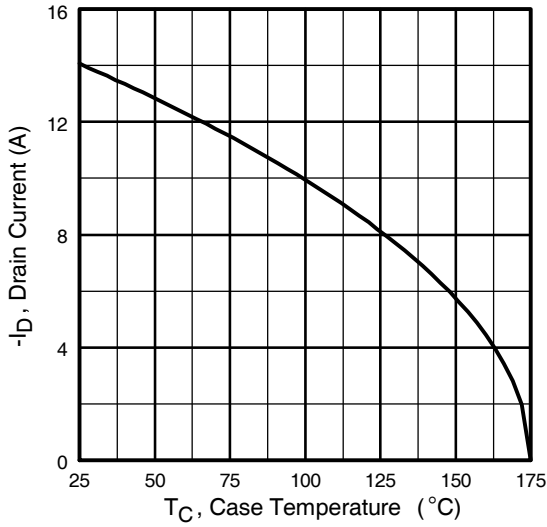


Fig 9. Maximum Drain Current Vs. Case Temperature

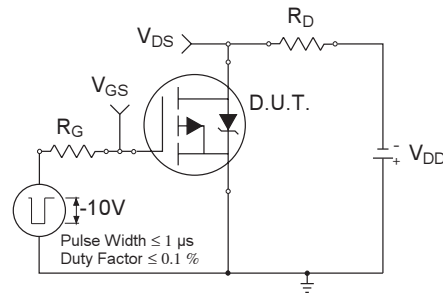


Fig 10a. Switching Time Test Circuit

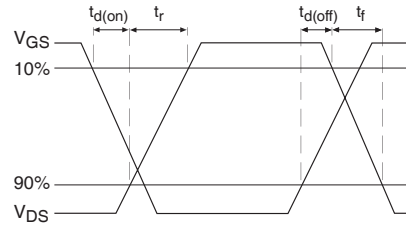


Fig 10b. Switching Time Waveforms

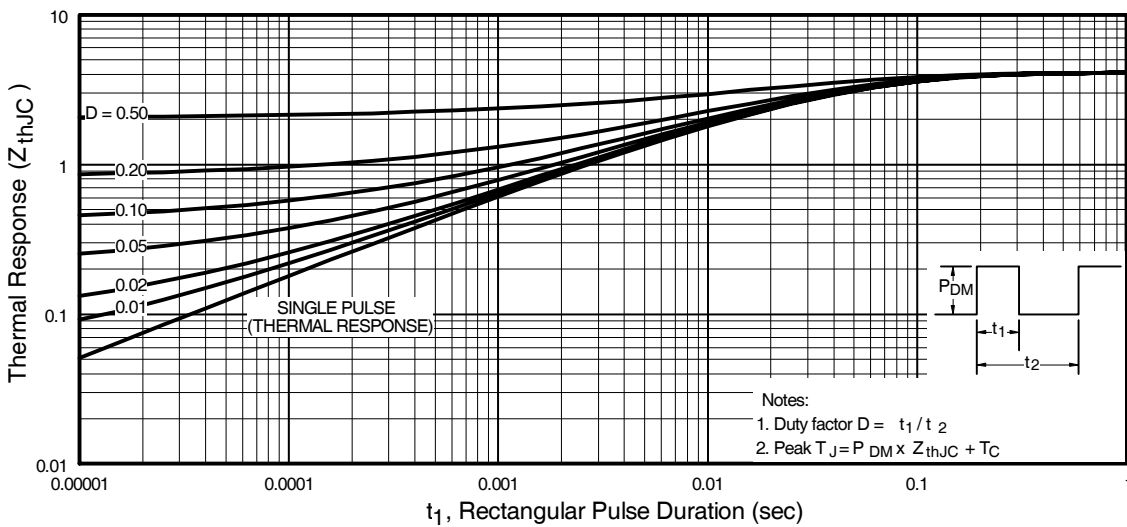


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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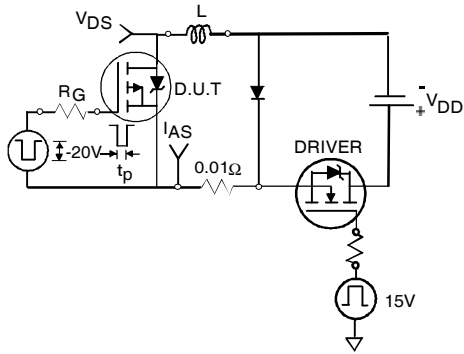


Fig 12a. Unclamped Inductive Test Circuit

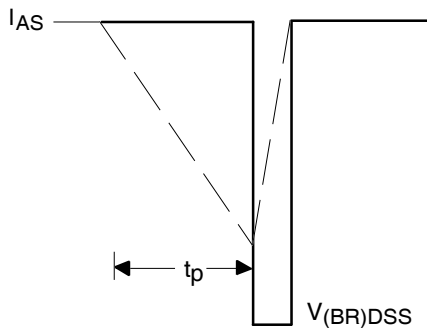


Fig 12b. Unclamped Inductive Waveforms

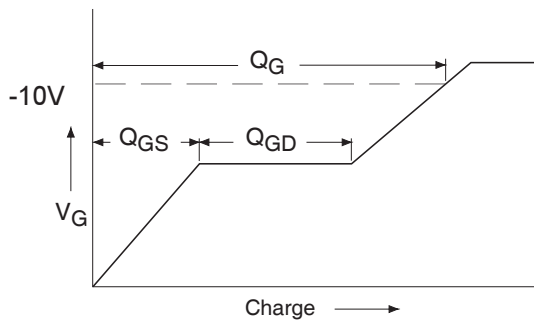


Fig 13a. Basic Gate Charge Waveform

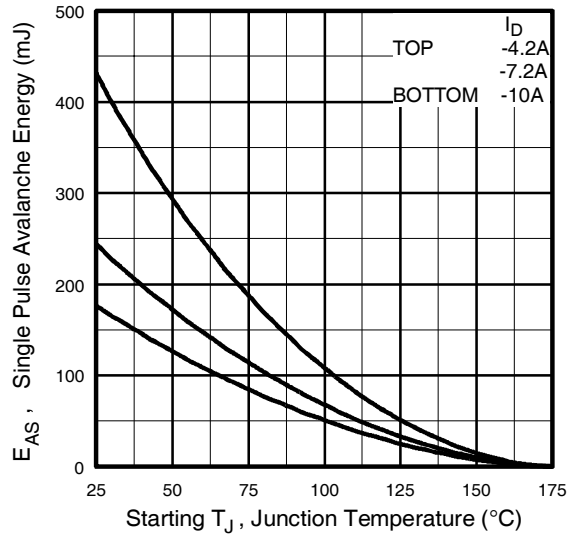


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

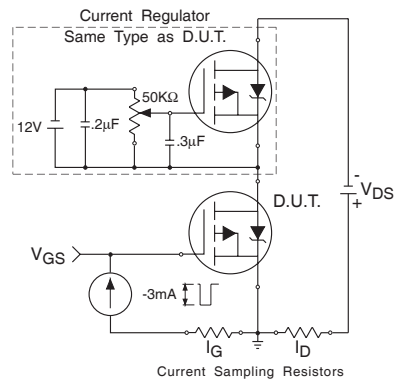
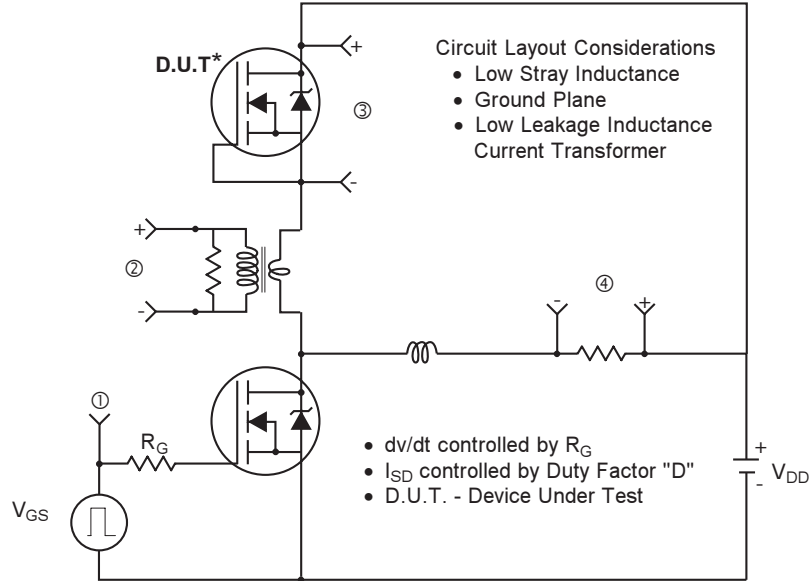
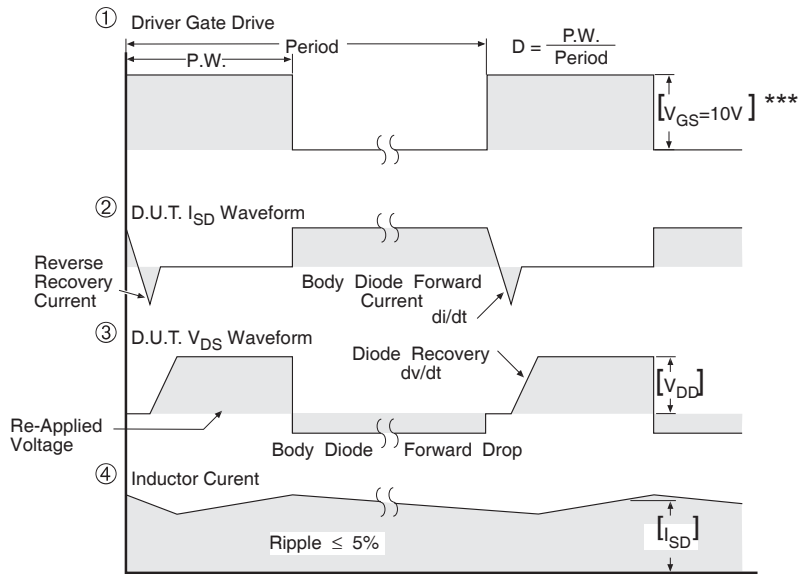


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

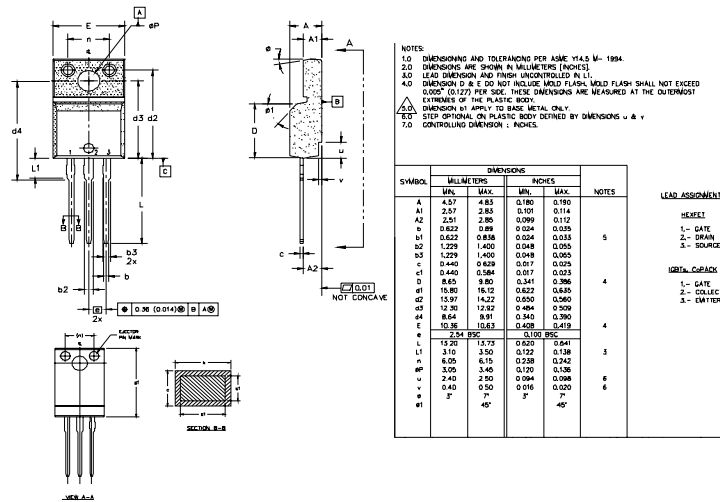
Fig 14. For P-Channel HEXFETS

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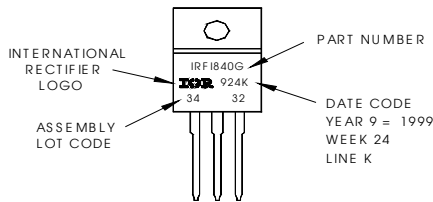
TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
 WITH ASSEMBLY
 LOT CODE 3432
 ASSEMBLED ON WW 24 1999
 IN THE ASSEMBLY LINE "K"
Note: "P" in assembly line
 position indicates "Lead-Free"



Data and specifications subject to change without notice.

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 Visit us at www.irf.com for sales contact information.12/03

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>