**Freescale Semiconductor**
Data Sheet

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# SCF5249 Integrated ColdFire® Microprocessor Data Sheet

## 1 Introduction

This document provides an overview of the SCF5249 ColdFire® processor and general descriptions of SCF5249 features and its various modules.

The SCF5249 was designed as a system controller/decoder for MP3 music players, especially portable MP3 CD players. The 32-bit ColdFire core with Enhanced Multiply Accumulate (EMAC) unit provides optimum performance and code density for the combination of control code and signal processing required for MP3 decode, file management, and system control.

Low power features include a hardwired CD ROM decoder, advanced 0.18um CMOS process technology, 1.8V core power supply, and on-chip 96KByte SRAM. MP3 decode requires less than 20MHz CPU bandwidth and runs in on-chip SRAM with external access only for data input and output.

The SCF5249 is also an excellent general purpose system controller with over 125 Dhrystone 2.1 MIPS @ 140MHz performance at a very competitive price. The

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integrated peripherals and EMAC allow the SCF5249 to replace both the microcontroller and the DSP in certain applications. Most peripheral pins can also be remapped as General Purpose I/O pins.

# 1.1 Orderable Parts Numbers

## 1.1.1 Orderable Part Table

**Table 1. Orderable Part Numbers**

| Orderable Part Number | Maximum Clock Frequency | Package Type | Operating Temperature Range | Part Status |
|---|---|---|---|---|
| SCF5249LPV120 | 120 MHz | 144 pin QFP | -20°C to 70°C | Leaded |
| SCF5249LAG120 | 120 MHz | 144 pin QFP | -20°C to 70°C | Lead Free |
| SCF5249VF140 | 140 MHz | 160 ball MAPBGA | -20°C to 70°C | Leaded |
| SCF5249VM140 | 140 MHz | 160 ball MAPBGA | -20°C to 70°C | Lead Free |

# 1.2 SCF5249 Features

The SCF5249 integrated microprocessor combines a Version 2 ColdFire® processor core operating at 140MHz with the following modules.

- DMA controller with 4 DMA channels
- Integrated Enhanced Multiply-accumulate Unit (EMAC)
- 8-KByte Direct Mapped Instruction Cache
- 96-KByte SRAM (A 64K and a 32K bank)
- Operates from external crystal oscillator
- Supports 16-bit wide SDRAM memories
- Serial Audio Interface which supports IIS and EIAJ audio protocols
- Digital audio transmitter and two receivers compliant with IEC958 audio protocol
- CD-ROM and CD-ROM XA block decoding and encoding function
- Two UARTS
- Queued Serial Peripheral Interface (QSPI) (Master Only)
- Two timers
- IDE and SmartMedia interfaces
- Analog/Digital Converter
- Flash Memory Card Interface
- Two $I^2C$ modules
- System debug support
- General Purpose I/O pins shared with other functions

- 1.8V core, 3.3V I/O
- 160 pin MAPBGA package (qualified at 140 MHz) and 144 pin QFP package (qualified at 120 MHz)
- $-20^0$ C to $70^0$ C ambient operating temperature range

# 2 SCF5249 Block Diagram

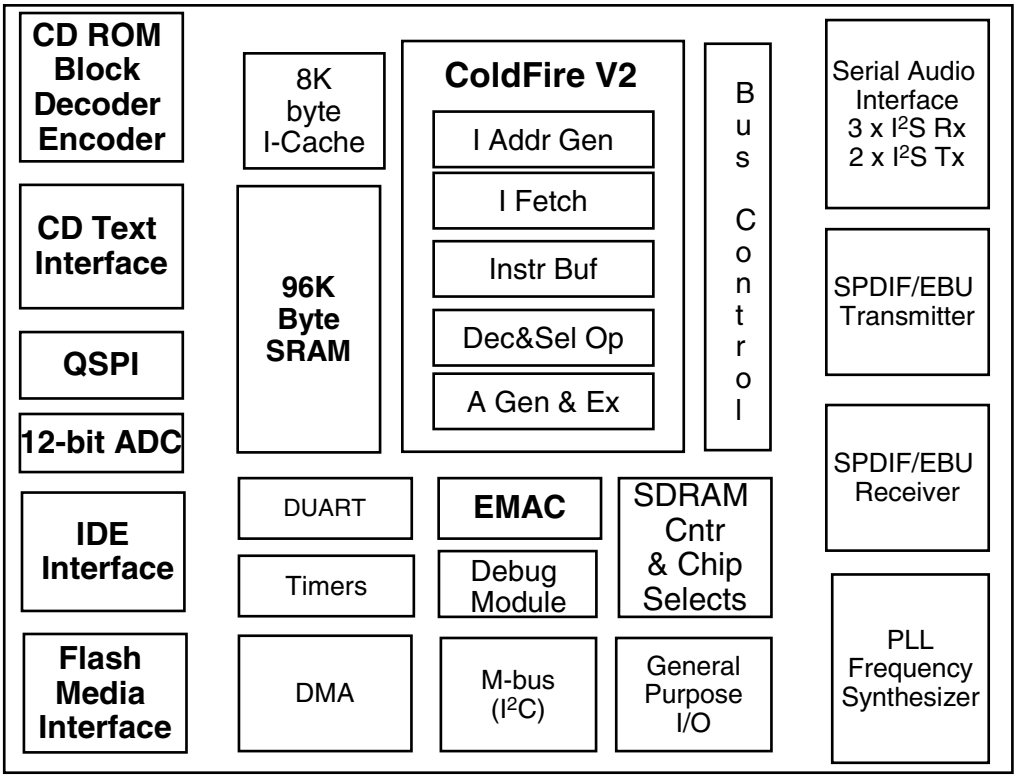


**Figure 1. SCF5249 Block Diagram**

# 3 SCF5249 Feature Details

The primary features of the SCF5249 integrated processor include the following:

- ColdFire V2 Processor Core operating at 140MHz
  - — Clock-doubled Version 2 microprocessor core
  - — 32-bit internal data bus, 16 bit external data bus
  - — 16 user-visible, 32-bit general-purpose registers
  - — Supervisor/user modes for system protection
  - — Vector base register to relocate exception-vector table
  - — Optimized for high-level language constructs

- DMA controller
  - Four fully programmable channels: Two dedicated to the audio interface module and two dedicated to the UART module (External requests are not supported.)
  - Supports dual- and single-address transfers with 32-bit data capability
  - Two address pointers that can increment or remain constant
  - 16-/24-bit transfer counter
  - Operand packing and unpacking support
  - Auto-alignment transfers supported for efficient block movement
  - Supports bursting and cycle stealing
  - All channels support memory to memory transfers
  - Interrupt capability
  - Provides two clock cycle internal access
- Enhanced Multiply-accumulator Unit
  - Single-cycle multiply-accumulate operations for 32 x 32 bit and 16 x 16 bit operands
  - Support for signed, unsigned, integer, and fixed-point fractional input operands
  - Four 48-bit accumulators to allow the use of a 40-bit product
  - The addition of 8 extension bits to increase the dynamic number range
  - Fast signed and unsigned integer multiplies
- 8-KByte Direct Mapped instruction cache
  - Clock-doubled to match microprocessor core speed
  - Flush capability
  - Non-blocking cache provides fast access to critical code and data
- 96-KByte SRAM
  - Provides one-cycle access to critical code and data
  - Split into two banks, SRAM0 (32K), and SRAM1 (64K)
  - DMA requests to/from internal SRAM1 supported
- Crystal Trim
  - The XTRIM output can be used to trim an external crystal oscillator circuit which would allow lock with an incoming IEC958 or serial audio signal
- Audio Interfaces
  - IEC958 input and output
  - Four serial Philips IIS/Sony EIAJ interfaces
    - One with input and output, one with output only, two with input only (Three inputs, two outputs)
    - Master and Slave operation

- CD Text Interface
  - Allows the interface of CD subcode (transmitter only)
- Dual Universal Synchronous/asynchronous Receiver/Transmitter (Dual UART)
  - Full duplex operation
  - Baud-rate generator
  - Modem control signals: clear-to-send (CTS) and request-to-send (RTS)
  - DMA interrupt capability
  - Processor-interrupt capability
- Queued Serial Peripheral Interface (QSPI)
  - Programmable queue to support up to 16 transfers without user intervention
  - Supports transfer sizes of 8 to 16 bits in 1-bit increments
  - Four peripheral chip-select lines for control of up to 15 devices
  - Baud rates from 273 Kbps to 17.5 Mbps at 140MHz
  - Programmable delays before and after transfers
  - Programmable clock phase and polarity
  - Supports wraparound mode for continuous transfers
  - Master mode only
- Dual 16-bit General-purpose Multimode Timers
  - Clock source selectable from external, CPU clock/2 and CPU clock/32.
  - 8-bit programmable prescaler
  - 2 timer inputs and 2 outputs
  - Processor-interrupt capability
  - 14.3 nS resolution with CPU clock at 140MHz
- IDE/ SmartMedia Interface
  - Allows direct connection to an IDE hard drive or other IDE peripheral
- Analog/Digital Converter
  - 12-Bit Resolution
  - 4 Muxed inputs
- Flash Memory Card Interface
  - Allows connection to Sony MemoryStick compatible devices
  - Support SD cards and other types of flash media
- Dual $I^2C$ Interfaces
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, keypads
  - Master and slave modes, support for multiple masters
  - Automatic interrupt generation with programmable level

- System debug support
  - — Real-time instruction trace for determining dynamic execution path
  - — Background debug mode (BDM) for debug features while halted
  - — Debug exception processing capability
  - — Real-time debug support
- System Interface
  - — Glueless bus interface with four chip selects and DRAMC support for interface to 16-bit for DRAM, SRAM, ROM, FLASH, and I/O devices
    - – Two programmable chip-select signals for static memories or peripherals, with programmable wait states and port sizes.
    - – Two dedicated chip selects for 16-bit wide DRAM /SDRAM.
    - – CS0 is active after reset to provide boot-up from external FLASH/ROM.
  - — Programmable interrupt controller
    - – Low interrupt latency
    - – Eight external interrupt requests
    - – Programmable autovector generator
  - — 44 programmable general-purpose inputs*
  - — 46 programmable general-purpose outputs*
    - – * For the 160 MAPBGA package
  - — IEEE 1149.1 Test (JTAG) Module
- Clocking
  - — Clock-multiplied PLL, programmable frequency
- 1.8V Core, 3.3V I/O
- 160 pin MAPBGA package (qualified at 140 MHz) and 144 pin QFP package (qualified at 120 MHz)

# 4 160 MAPBGA Ball Assignments

The following signals are not available on the 144 QFP package.

**NOTE**

The 144 QFP part is qualified for 120 MHz operation. The 160MAPBGA part is qualified for 140 MHz.

**Table 2. 160 MAPBGA Ball Assignments**

| 160 MAPBGA Ball Number | Function | GPIO |
|---|---|---|
| E3 | cmd_sdio2 | gpio34 |
| G4 | sdata0_sdio1 | gpio54 |
| H3 | RSTO/sdata2_bs2 | |
| K3 | A25 | gpo8 |
| L4 | QSPI_CS1 | gpio24 |
| L8 | QSPI_CS3 | gpio22 |
| N8 | SDRAM_CS2 | gpio7 |
| P9 | EbuOut2 | gpo 37 |
| K11 | BUFENb2 | gpio17 |
| G12 | subr | gpio 53 |
| F13 | sfsy | gpio 52 |
| F12 | rck | gpio 51 |
| E8 | SRE | gpio11 |
| B8 | lrck3 | gpio 45 |
| E7 | SWE | gpio12 |
| A7 | sclk3 | gpio 49 |

# 5 SCF5249 Functional Overview

## 5.1 ColdFire V2 Core

The ColdFire processor Version 2 core consists of two independent, decoupled pipeline structures to maximize performance while minimizing core size.The instruction fetch pipeline (IFP) is a two-stage pipeline for prefetching instructions. The prefetched instruction stream is then gated into the two-stage operand execution pipeline (OEP), which decodes the instruction, fetches the required operands, and then executes the required function. Because the IFP and OEP pipelines are decoupled by an instruction buffer that serves as a FIFO queue, the IFP can prefetch instructions in advance of their actual use by the OEP, which minimizes time stalled waiting for instructions. The OEP is implemented in a two-stage pipeline featuring a traditional RISC data path with a dual-read-ported register file feeding an arithmetic/logic unit (ALU).

## 5.2 DMA Controller

The SCF5249 provides four fully programmable DMA channels for quick data transfer. Single and dual address mode is supported with the ability to program bursting and cycle stealing. Data transfer is selectable as 8, 16, 32, or 128-bits. Packing and unpacking is supported.

Two internal audio channels and the dual UART can be used with the DMA channels. All channels can perform memory to memory transfers. The DMA controller has a user-selectable, 24- or 16-bit counter and a programmable DMA exception handler.

External requests are not supported.

## 5.3 Enhanced Multiply and Accumulate Module (EMAC)

The integrated EMAC unit provides a common set of DSP operations and enhances the integer multiply instructions in the ColdFire architecture. The EMAC provides functionality in three related areas:

1. Faster signed and unsigned integer multiplies
2. New multiply-accumulate operations supporting signed and unsigned operands
3. New miscellaneous register operations

Multiplies of 16x16 and 32x32 with 48-bit accumulates are supported in addition to a full set of extensions for signed and unsigned integers plus signed, fixed-point fractional input operands. The EMAC has a single-clock issue for 32x32-bit multiplication instructions and implements a four-stage execution pipeline.

## 5.4 Instruction Cache

The instruction cache improves system performance by providing cached instructions to the execution unit in a single clock. The SCF5249 processor uses a 8K-byte, direct-mapped instruction cache to achieve 125 MIPS at 140 Mhz. The cache is accessed by physical addresses, where each 16-byte line consists of an address tag and a valid bit. The instruction cache also includes a bursting interface for 16-bit and 8-bit port sizes to quickly fill cache lines.

## 5.5 Internal 96-KByte SRAM

The 96-KByte on-chip SRAM is split over two banks, SRAM0 (32k) and SRAM1 (64K). It provides one clock-cycle access for the ColdFire core. This SRAM can store processor stack and critical code or data segments to maximize performance. Memory in the second bank can be accessed under DMA.

## 5.6 DRAM Controller

The SCF5249 DRAM controller provides a glueless interface for up to two banks of DRAM, each of which can be up to 32 MBytes. The controller supports a 16-bit data bus. A unique addressing scheme allows for increases in system memory size without rerouting address lines and rewiring boards. The controller operates in page mode, non-page mode, and burst-page mode and supports SDRAMS.

## 5.7 System Interface

The SCF5249 provides a glueless interface to 16-bit port size SRAM, ROM, and peripheral devices with independent programmable control of the assertion and negation of chip-select and write-enable signals.

The SCF5249 also supports bursting ROMs.

## 5.8 External Bus Interface

The bus interface controller transfers information between the ColdFire core or DMA and memory, peripherals, or other devices on the external bus. The external bus interface provides 23 bits of address bus space, a 16-bit data bus, Output Enable, and Read/Write signals. This interface implements an extended synchronous protocol that supports bursting operations.

## 5.9 Serial Audio Interfaces

The SCF5249 digital audio interface provides four serial Philips IIS/Sony EIAJ interfaces. One interface is a 4-pin (1 bit clock, 1 word clock, 1 data in, 1 data out), the other three interfaces are 3-pin (1 bit clock, 1 word clock, 1 data in or out). The serial interfaces have no limit on minimum sampling frequency. Maximum sampling frequency is determined by maximum frequency on bit clock input. This is 1/3 the frequency of the internal system clock.

## 5.10 IEC958 Digital Audio Interfaces

The SCF5249 has two digital audio input interfaces, and one digital audio output interface. There are four digital audio input pins, two digital audio output pins. An internal multiplexer selects one of the four inputs to the digital audio input interface. There is one digital audio output interface but it has two IEC958 outputs. One output carries the professional “c” channel, and the other carries the consumer “c” channel. The rest carry identical data.

The IEC958 output can take the output from the internal IEC958 generator, or multiplex out one of the four IEC958 inputs.

## 5.11 Audio Bus

The audio interfaces connect to an internal bus that carries all audio data. Each receiver places its received data on the audio bus and each transmitter takes data from the audio bus for transmission. Each transmitter has a source select register.

In addition to the audio interfaces, there are six CPU accessible registers connected to the audio bus. Three of these registers allow data reads from the audio bus and allow selection of the audio source. The other three register provide a write path to the audio bus and can be selected by transmitters as the audio source. Through these registers, the CPU has access to the audio samples for processing.

Audio can be routed from a receiver to a transmitter without the data being processed by the core so the audio bus can be used as a digital audio data switch. The audio bus can also be used for audio format conversion.

## 5.12 CD-ROM Encoder/Decoder

The SCF5249 is capable of processing CD-ROM sectors in hardware. Processing is compliant with CD-ROM and CD-ROM XA standards.

The CD-ROM decoder performs following functions in hardware:

- Sector sync recognition
- Descrambling of sectors
- Verification of the CRC checksum for Mode 1, Mode 2 Form 1, and Mode 2 Form 2 sectors
- Third-layer error correction is not performed

The CD-ROM encoder performs following functions in hardware:

- Sector sync recognition
- Scrambling of sectors
- Insertion of the CRC checksum for Mode 1, Mode 2 Form 1, and Mode 2 Form 2 sectors.
- Third-layer error encoding needs to be done in software. This can use approximately 5-10 Mhz of performance for single-speed.

## 5.13 Dual UART Module

Two full-duplex UARTs with independent receive and transmit buffers are in this module. Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity, and up to 2 stop bits in 1/16 increments. Four-byte receive buffers and two-byte transmit buffers minimize CPU service calls. The Dual UART module also provides several error-detection and maskable-interrupt capabilities. Modem support includes request-to-send ($\overline{\text{RTS}}$) and clear-to-send ($\overline{\text{CTS}}$) lines.

The system clock provides the clocking function from a programmable prescaler. You can select full duplex, auto-echo loopback, local loopback, and remote loopback modes. The programmable Dual UARTs can interrupt the CPU on various normal or error-condition events.

## 5.14 Queued Serial Peripheral Interface QSPI

The QSPI module provides a serial peripheral interface with queued transfer capability. It supports up to 16 stacked transfers at a time, making CPU intervention between transfers unnecessary. Transfers of up to 37 Mbits/second are possible at a CPU clock of 140 MHz. The QSPI supports master mode operation only.

## 5.15 Timer Module

The timer module includes two general-purpose timers, each of which contains a free-running 16-bit timer for use in any of three modes:

1. Timer Capture. This mode captures the timer value with an external event.
2. Output Capture. This mode triggers an external signal or interrupts the CPU when the timer reaches a set value
3. Event Counter. This mode counts external events.

The timer unit has an 8-bit prescaler that allows programming of the clock input frequency, which is derived from the system clock. In addition to the ÷1 and ÷16 clock derived from the bus clock (CPU clock / 2), the programmable timer-output pins either generate an active-low pulse or toggle the outputs.

## 5.16 IDE and SmartMedia Interfaces

The SCF5249 system bus allows connection of an IDE hard disk drive and SmartMedia flash card with a minimum of external hardware. The external hardware consists of bus buffers for address and data and are intended to reduce the load on the bus and prevent SDRAM and Flash accesses to propagate to the IDE bus. The control signals for the buffers are generated in the SCF5249.

## 5.17 Analog/Digital Converter (ADC)

The four channel ADC is a based on the Sigma-Delta concept with 12-bit resolution. The digital portion of the ADC is provided internally. The analog voltage comparator must be provided externally as well as an external integrator circuit (resistor/capacitor) which is driven by the ADC output. A software interrupt is provided when the ADC measurement cycle is complete.

## 5.18 Flash Memory Card Interface

The interface is Sony MemoryStick and SecureDigital compatible. However, there is no hardware support for MagicGate.

## 5.19 $I^2C$ Module

The two-wire $I^2C$ bus interface, which is compliant with the Philips $I^2C$ bus standard, is a bidirectional serial bus that exchanges data between devices. The $I^2C$ bus minimizes the interconnection between devices in the end system and is best suited for applications that need occasional bursts of rapid communication over short distances among several devices. Bus capacitance and the number of unique addresses limit the maximum communication length and the number of devices that can be connected.

## 5.20 Chip-Selects

Two programmable chip-select outputs provide signals that enable glueless connection to external memory and peripheral circuits. The base address, access permissions and automatic wait-state insertion are programmable with configuration registers. These signals also interface to 16-bit ports.

CS0 is active after reset to provide boot-up from external FLASH/ROM.

## 5.21 GPIO Interface

A total of 44 General Purpose inputs and 46 General Purpose outputs are available. These are multiplexed with various other signals. Eight of the GPIO inputs have edge sensitive interrupt capability.

## 5.22 Interrupt Controller

The interrupt controller provides user-programmable control of a total of 57 interrupts. There are 49 internal interrupt sources. In addition, there are 8 GPIOs where interrupts can be generated on the rising or falling edge of the pin. All interrupts are autovectored and interrupt levels are programmable.

## 5.23 JTAG

To help with system diagnostics and manufacturing testing, the SCF5249 includes dedicated user-accessible test logic that complies with the IEEE 1149.1A standard for boundary scan testability, often referred to as Joint Test Action Group, or JTAG. For more information, refer to the IEEE 1149.1A standard. Freescale provides BSDL files for JTAG testing.

## 5.24 System Debug Interface

The ColdFire processor core debug interface supports real-time instruction trace and debug, plus background-debug mode. A background-debug mode (BDM) interface provides system debug.

In real-time instruction trace, four status lines provide information on processor activity in real time (PST pins). A four-bit wide debug data bus (DDATA) displays operand data and change-of-flow addresses, which helps track the machine's dynamic execution path.

## 5.25 Crystal and On-chip PLL

Typically, an external 16.92 Mhz or 33.86 Mhz clock input is used for CD R/W applications, while an 11.2896 MHz clock is more practical for Portable CD player applications. However, the on-chip programmable PLL, which generates the processor clock, allows the use of almost any low frequency external clock (5-35 Mhz).

Two clock outputs (MCLK1 and MCLK2) are provided for use as Audio Master Clock. The output frequencies of both outputs are programmable to Fxtal, Fxtal/2, Fxtal/3, and Fxtal/4. The Fxtal/3 option is only available when the 33.86 Mhz crystal is connected.

The SCF5249 supports VCO operation of the oscillator by means of a 16-bit pulse density modulation output. Using this mode, it is possible to lock the oscillator to the frequency of an incoming IEC958 or IIS signal. The maximum trim depends on the type and design of the oscillator. Typically a trim of +/- 100 ppm can be achieved with a crystal oscillator and over +/- 1000 ppm with an LC oscillator.

# 6 General Device Information

The SCF5249 is available in a 160-pin MAP BGA package, or a 144-pin QFP package.

# 7 Documentation

Table 3 lists the documents that provide a complete description of the SCF5249 and are required to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, a Freescale Literature Distribution Center, or through the Freescale DSP home page on the internet; http://www.freescale.com/
(the source for the latest information).

**Table 3. SCF5249 Documentation**

| Document Name | Description | Order Number |
|---|---|---|
| CFPRM/D | ColdFire Family Programmer's Reference Manual | CFPRM/D |
| ColdFire2UM | Version 2/2M ColdFire Core Processor User's Manual | ColdFire2UM/D |
| ColdFire2UMAD | Version 2/2M ColdFire Core Processor User's Manual Addendum | ColdFire2UMAD/D |
| SCF5249UM | SCF5249 User's Manual | SCF5249UM/D |

# 8 Signal Descriptions

## 8.1 Introduction

This section describes the SCF5249 input and output signals. The signal descriptions as shown in Table 4 are grouped according to relevant functionality.

**Table 4. SCF5249 Signal Index**

| Signal Name | Mnemonic | Function | Input/ Output | Reset State |
|---|---|---|---|---|
| Address | A[23:1]<br>A[25]/GPO8 | 23 address lines, address line 25 multiplexed with gpo8. | Out | X |
| Read-write control | RW_b | Bus write enable - indicates if read or write cycle in progress | Out | H |
| Output enable | OE | Output enable for asynchronous memories connected to chip selects | Out | negated |
| Data | D[31:16] | Data bus used to transfer word data | In/Out | Hi-Z |
| Synchronous row address strobe | SDRAS | Row address strobe for external SDRAM. | Out | negated |
| Synchronous column address strobe | SDCAS | Column address strobe for external SDRAM | Out | negated |
| SDRAM write enable | SDWE | Write enable for external SDRAM | Out | negated |
| SDRAM upper byte enable | SDUDQM | Indicates during write cycle if high byte is written | Out | |
| SDRAM lower byte enable | SDLDQM | Indicates during write cycle if low byte is written | Out | |
| SDRAM chip selects | SDRAMCS1 | SDRAM chip select | Outt | negated |
| SDRAM chip selects | SDRAMCS2/GPIO7 | SDRAM chip select | In/Out | negated |
| SDRAM clock enable | BCLKE | SDRAM clock enable | Out | |
| System clock | SCLK/GPIO10 | SDRAM clock output | In/Out | |

**Table 4. SCF5249 Signal Index (continued)**

| Signal Name | Mnemonic | Function | Input/ Output | Reset State |
|---|---|---|---|---|
| ISA bus read strobes | CS2/IDE-DIOR/GPIO13<br>CS3/SRE/GPIO11 | There are 2 ISA bus read strobes and 2 ISA bus write strobes. They allow connection of two independent ISA bus peripherals, e.g. an IDE slave device and a SmartMedia card. | In/Out | |
| ISA bus write strobes | IDE-DIOW/GPIO14<br>SWE/GPIO12 | | In/Out | |
| ISA bus wait signal | IDE-IORDY/GPIO16 | ISA bus wait line - available for both busses | In/Out | |
| Chip Selects[1:0] | $\overline{CS0}$<br>$\overline{CS1}$/GPIO58 | Enables peripherals at programmed addresses.<br>$\overline{CS}$[1:0]. $\overline{CS}$[0]provides boot ROM selection | Out<br>In/Out | negated |
| Buffer enable 1 | $\overline{BUFENB1}$/GPIO57 | Two programmable buffer enables allow seamless steering of external buffers to split data and address bus in sections. | In/Out | |
| Buffer enable 2 | $\overline{BUFENB2}$/GPIO7 | | In/Out | |
| Transfer acknowledge | TA/GPIO20 | Transfer Acknowledge signal | In/Out | |
| Serial Clock Line | SCL0/QSPI_CLK | Clock signal for first $I^2C$ module operation<br>Signal is also QSPI clock | In/Out | |
| Serial Data Line | SDA0/QSPI_DIN | Serial data port first $I^2C$ module operation<br>Signal is also QSPI data in | In/Out | |
| Serial Clock Line | SCL1_GPIO_3 | Clock signal for second $I_2C$ module operation | In/Out | |
| Serial Data Line | SDA1_GPIO55 | Serial data port for second $I_2C$ module operation | In/Out | |
| Receive Data | RXD1/GPI28/ADIN2<br>RXD0/GPI27 | Signal is receive serial data input for DUART | In | |
| Transmit Data | TXD1/GPO28<br>TXD0/GPO27 | Signal is transmit serial data output for DUART | Out | asserted |
| Request-To-Send | $\overline{RTS1}$/GPO31<br>$\overline{RTS2}$/GPO30 | DUART signals a ready to receive data query | Out | negated |
| Clear-To-Send | $\overline{CTS1}$/ADIN3/GPI31<br>$\overline{CTS0}$/GPI30 | Signals to DUART that data can be transmitted to peripheral<br>CTS2 is multiplexed with an A/D input | In | |
| Timer Input | TIN0/GPI33<br>TIN1/GPIO23 | Provides clock input to timer or provides trigger to timer value capture logic | In<br>In/Out | |
| Timer Output | TOUT0/GPO33<br>TOUT1/ADOUT/GPO35 | Capable of output waveform or pulse generation | Out | |

**Table 4. SCF5249 Signal Index (continued)**

| Signal Name | Mnemonic | Function | Input/ Output | Reset State |
|---|---|---|---|---|
| IEC958 inputs | EBUIN1/GPI36<br>EBUIN2/GPI37<br>EBUIN3/ADIN0/GPI38<br>EBUIN4/ADIN1/GPI39 | Audio interfaces IEC958 inputs multiplexed with some A/D inputs | In | |
| IEC958 outputs | EBUOUT1/GPO36<br>EBUOUT2/GPO37 | Audio interfaces IEC958 outputs | Out | |
| Serial data in | SDATAI1<br>SDATAI3/GPI41<br>SDATA14/GPI42 | Audio interfaces serial data inputs | In | |
| Serial data out | SDATAO1/GPIO25<br>SDATAO2/GPO41 | Audio interfaces serial data outputs | In/Out<br>Out | |
| Word clock | LRCK1<br>LRCK2/GPIO44<br>LRCK3/GPIO45<br>LRCK4/GPIO46 | Audio interfaces serial word clocks | In/Out | |
| Bit clock | SCLK1<br>SCLK2/GPIO48<br>SCLK3/GPIO49<br>SCLK4/GPIO50 | Audio interfaces serial bit clocks | In/Out | |
| Serial input | EF/GPIO19 | Error flag serial in | In/Out | |
| Serial input | CFLG/GPIO18 | C-flag serial in | In/Out | |
| Subcode clock | RCK/GPIO51 | Audio interfaces subcode clock | In/Out | |
| Subcode sync | SFSY/GPIO52 | Aaudio interfaces subcode sync | In/Out | |
| Subcode data | SUBR/GPIO53 | Audio interfaces subcode data | In/Out | |
| Clock frequency trim | XTRIM/GPO38 | Clock trim control | Out | |
| Audio clocks out | MCLK1/GPIO39<br>MCLK2/GPIO42 | DAC output clocks | Out | |
| MemoryStick/SecureDigital interface | CMDSDIO2/GPIO34 | Secure Digital command lane<br>MemoryStick interface 2 data i/o | In/Out | |
| | SCLKOUT/GPIO15 | Clock out for both MemoryStick interfaces and for Secure Digital | In/Out | |
| | SDATA0_SDIO1/GPIO54 | SecureDigital serial data bit 0<br>MemoryStick interface 1 data i/o | In/Out | |
| | SDATA1_BS1/GPIO9 | SecureDigital serial data bit 1<br>MemoryStick interface 1 strobe | In/Out | |
| | RSTO/SDATA2_BS2 | SecureDigital serial data bit 2<br>MemoryStick interface 2 strobe<br>Reset output signal | In/Out | |
| | SDATA3/GPIO56 | SecureDigital serial data bit 3 | In/Out | |

**Table 4. SCF5249 Signal Index (continued)**

| Signal Name | Mnemonic | Function | Input/ Output | Reset State |
|---|---|---|---|---|
| ADC | EBUIN3/ADIN0/GPI38<br>EBUIN4/ADIN1/GPI39<br>RXD2/ADIN2/GPI28<br>CTS2/ADIN3/GPI31 | Analog to Digital converter input signals | In/Out | |
| ADC | TOUT1/ADOUT/GPO35 | Analog to digital convertor output signal. | In/Out | |
| QSPI clock | SCL/QSPI_CLK | QSPI clock signal | In/Out | |
| QSPI data in | SDA/QSPI_DIN | QSPI data input | In/Out | |
| QSPI data out | QSPIDOUT/GPIO26 | QSPI data out | In/Out | |
| QSPI chip selects | QSPICS0/GPIO29<br>QSPICS1/GPIO24<br>QSPICS2/GPIO21<br>QSPICS3/GPIO22 | QSPI chip selects | In/Out | |
| Crystal in | CRIN | Crystal input | In | |
| Reset In | RSTI | Processor Reset Input | In | |
| Freescale Test Mode | TEST[3:0] | Should always be low. | In | |
| High Impedance | HIZ | Assertion three-states all output signal pins. | In | |
| Debug Data | DDATA3/GPIO4<br>DDATA2/GPIO2<br>DDATA1/GPIO1<br>DDATA0/GPIO0 | Displays captured processor data and break-point status. | In/Out | Hi-Z |
| Processor Status | PST3/GPIO62<br>PST2/GPIO61<br>PST1/GPIO60<br>PST0/GPIO59 | Indicates internal processor status. | In/Out | Hi-Z |
| Processor clock | PSTCLK/GPO63 | Processor clock output | Out | |
| Test Clock | TCK | Clock signal for IEEE 1149.1A JTAG. | In | |
| Test Reset/Development Serial Clock | $\overline{\text{TRST}}$/DSCLK | Multiplexed signal that is asynchronous reset for JTAG controller. Clock input for debug module. | In | |
| Test Mode Select/ Break Point | TMS/$\overline{\text{BKPT}}$ | Multiplexed signal that is test mode select in JTAG mode and a hardware break-point in debug mode. | In | |
| Test Data Input / Development Serial Input | TDI/DSI | Multiplexed serial input for the JTAG or background debug module. | In | |
| Test Data Output/Development Serial Output | TDO/DSO | Multiplexed serial output for the JTAG or background debug module. | Out | |
| **Note:** The CMD_SDIO2, SDATA0_SDIO1, RSTO/SDATA2_BS2, A25, QSPI_CS1, QSPI_CS3, SDRAM_CS2, EBUOUT2, BUFENB2, SUBR, SFSY, RCK, SRE, LRCK3, SWE, and the SCLK3 signals are only used in the 160 MAPBGA package. | | | | |

# 8.2 GPIO

Many pins have a GPIO as first or second function. If GPIO is second function, following rules apply:

- General purpose input is always active, regardless of state of pin.
- General purpose output or primary output is determined by value written to GPIO function select register.
- Power-on reset function is not GPIO.

# 8.3 SCF5249 Bus Signals

These signals provide the external bus interface to the SCF5249.

## 8.3.1 Address Bus

- The address bus provides the address of the byte or most significant byte of the word or longword being transferred.The address lines also serve as the DRAM address pins, providing multiplexed row and column address signals.
- Bits 23 down to 1 and 25 of the address are available. A25 is intended to be used with 256 Mbit DRAM's. Signals are named:
- A[23:1]
- A[25]/GPO8

## 8.3.2 Read-Write Control

This signal indicates during any bus cycle whether a read or write is in progress. A low is write cycle and a high is a read cycle.

## 8.3.3 Output Enable

The $\overline{OE}$ signal is intended to be connected to the output enable of asynchronous memories connected to chip selects. During bus read cycles, the ColdFire processor will drive $\overline{OE}$ low.

## 8.3.4 Data Bus

The data bus (D[31:16]) is bi-directional and non-multiplexed. Data is registered by the SCF5249 on the rising clock edge. The port width for each chip-select and DRAM bank are programmable. The data bus uses a default configuration if none of the chip-selects or DRAM bank match the address decode. All 16 bits of the data bus are driven during writes, regardless of port width or operand size.

## 8.3.5 Transfer Acknowledge

The $\overline{TA}$/GPIO20 pin is the transfer acknowledge signal.

# 8.4 SDRAM Controller Signals

The following SDRAM signals provide a seamless interface to external SDRAM. An SDRAM width of 16 bits is supported and can access as much as 64 Mybtes of memory. ADRAMs are not supported.

**Table 5. SDRAM Controller Signals**

| SDRAM Signal | Description |
|---|---|
| Synchronous DRAM row address strobe | The $\overline{\text{SDRAS}}$ active low pin provides a seamless interface to the RAS input on synchronous DRAM |
| Synchronous DRAM Column Address Strobe | The $\overline{\text{SDCAS}}$ active low pin provides a seamless interface to CAS input on synchronous DRAM. |
| Synchronous DRAM Write | The $\overline{\text{SDWE}}$ active-low pin is asserted to signify that a SDRAM write cycle is underway. This pin outputs logic '1' during read bus cycles. |
| Synchronous DRAM Chip Enable | The $\overline{\text{SD\_CS1}}$ and The $\overline{\text{SDRAM\_CS2}}$/GPIO7 active-low output signal is used during synchronous mode to route directly to the chip select of up to two SDRAM devices.<br>The $\overline{\text{SDRAM\_CS2}}$/gpio7 can be programmed to be gpio using the GPIO-FUNCTION register. |
| Synchronous DRAM UDQM and LQDM signals | The DRAM byte enables UDMQ and LDQM are driven by the SDUDQM and SDLDQM byte enable outputs. |
| Synchronous DRAM clock | The DRAM clock is driven by the SCLK signal |
| Synchronous DRAM Clock Enable | The BCLKE active high output signal is used during synchronous mode to route directly to the SCKE signal of external SDRAMs. This signal provides the clock enable to the SDRAM. |

**NOTE**

The SDRAM_CS2 signal is only used on the 160 MAPBGA package.

# 8.5 Chip Selects

There are two chip select outputs on the SCF5249 device. $\overline{\text{CS0}}$ and $\overline{\text{CS1}}$/GPIO58. The second signal is multiplexed with a GPIO signal. The active low chip selects can be used to access asynchronous memories. The interface is glueless.

# 8.6 ISA Bus

The SCF5249 supports an ISA bus. (No ISA DMA channel). Using the ISA bus protocol, reads and writes to up to two ISA bus peripherals are possible. For the first peripheral, CS2/IDE-$\overline{\text{DIOR}}$/GPIO13 and IDE-$\overline{\text{DIOW}}$/GPIO14 are the read and write strobe. For the second peripheral, CS3/$\overline{\text{SRE}}$/GPIO11 and $\overline{\text{SWE}}$/GPIO12 are the read and write strobe. Either peripheral can insert wait states by pulling IDE-IORDY/GPIO16

## 8.7 Bus Buffer Signals

As the SCF5249 has a quite complicated slave bus, with the possibility to put DRAM on the bus, put asynchronous memories on the bus, and to put ISA bus peripherals on the bus, it may become necessary to introduce a bus buffer on the bus. The SCF5249 has a glueless interface to steer these bus buffers with 2 bus buffer output signals $\overline{\text{BUFENB1}}$/GPIO57 and $\overline{\text{BUFENB2}}$/GPIO7.

**NOTE**

The BUFENB2 signal is only used in the 160 MAPBGA package.

## 8.8 $I^2C$ Module Signals

There are two $I^2C$ interfaces on this device.

The $I^2C$ module acts as a quick two-wire, bidirectional serial interface between the SCF5249 processor and peripherals with an $I^2C$ interface (e.g., LED controller, A-to-D converter, D-to-A converter). When devices connected to the $I^2C$ bus drive the bus, they will either drive logic-0 or high-impedance. This can be accomplished with an open-drain output.

**Table 6. $I^2C$ Module Signals**

| $I^2c$ Module Signal | Description |
|---|---|
| $I^2C$ Serial Clock | The SCL/QPSICLK and SCL2/GPIO3 bidirectional signals are the clock signal for first and second $I^2C$ module operation. The $I^2C$ module controls this signal when the bus is in master mode; all $I^2C$ devices drive this signal to synchronize $I^2C$ timing.<br>Signals are multiplexed<br>Function select is done via PLLCR register. |
| $I^2C$ Serial Data | The SDA/QSPI_DIN and SDA2/GPIO55 bidirectional signals are the data input/output for the first and second serial $I^2C$ interface.<br>Signals are multiplexed<br>Function select is done via PLLCR register. |

## 8.9 Serial Module Signals

The following signals transfer serial data between the two UART modules and external peripherals.

All serial module signals can be used as gpi or gpo. The GPIO-FUNCTION and GPIO1-FUNCTION registers must be programmed to determine pin functions of the inputs and outputs. If used as gpo or gpi, UART functionality is lost.

**Table 7. Serial Module Signals**

| Serial Module Signal | Description |
|---|---|
| Receive Data | The RXD1_GPI27 and RXD2/ADIN2/GPI28 are the inputs on which serial data is received by the DUART. Data is sampled on RxD[1:0] on the rising edge of the serial clock source, with the least significant bit received first. |
| Transmit Data | The DUART transmits serial data on the TXD1/GPO27 and TXD2/GPO28 output signals. Data is transmitted on the falling edge of the serial clock source, with the least significant bit transmitted (LSB) first. When no data is being transmitted or the transmitter is disabled, these two signals are held high. TxD[1:0] are also held high in local loopback mode. |
| Request To Send | The $\overline{\text{RTS1}}$/GPO30 and $\overline{\text{RTS2}}$/GPO31 request-to-send outputs indicate to the peripheral device that the DUART is ready to send data and requires a clear-to-send signal to initiate transfer. |
| Clear To Send | Peripherals drive the $\overline{\text{CTS1}}$/GPI30 and $\overline{\text{CTS2}}$/ADIN3/GPI31 inputs to indicate to the SCF5249 serial module that it can begin data transmission. |

# 8.10 Timer Module Signals

The following signals are external interface to the two general-purpose SCF5249 timers. These 16-bit timers can capture timer values, trigger external events, or internal interrupts, or count external events. These pins can be reused as GPO or GPI. Registers GPIO-FUNCTION and GPIO1-FUNCTION must be programmed for this.

**Table 8. Timer Module Signals**

| Serial Module Signal | Description |
|---|---|
| Timer Input | Users can program the TIN0/GPI33 and TIN1/GPIO23 inputs as clocks that cause events in the counter and prescalars. They can also cause capture on the rising edge, falling edge, or both edges. |
| Timer Output | The TOUT0/GPO33 and TOUT1/ADOUT/GPO35 programmable outputs pulse or toggle on various timer events. |

# 8.11 Serial Audio Interface Signals

All serial audio interface signals can be programmed to serve as general purpose I/Os or as serial audio interface signals. The function is programmed using GPIO-FUNCTION and GPIO1-FUNCTION registers.

**NOTE**

The LRCK3 and SCLK3 signals are only used in the 160 MAPBGA package..

**Table 9. Serial Audio Interface Signals**

| Serial Module Signal | Description |
|---|---|
| Serial Audio Bit Clock | The SCLK1, SCLK2/GPIO48 and SCLK3/GPIO49, and SCLK4/GPIO50 multiplexed pins can serve as general purpose I/Os or serial audio bit clocks. As bit clocks, these bidirectional pins can be programmed as outputs to drive their associated serial audio (IIS) bit clocks. Alternately, these pins can be programmed as inputs when the serial audio bit clocks are driven internally. The functionality is programmed within the Audio module. During reset, these pins are configured as input serial audio bit clocks. |
| Serial Audio Word Clock | The LRCK1, LRCK2/GPIO44, LRCK3/GPIO45, and LRCK/GPIO46 multiplexed pins can serve as general purpose I/Os or serial audio word clocks. As word clocks, the bidirectional pins can be programmed as inputs to drive their associated serial audio word clock. Alternately, these pins can be programmed as outputs when the serial audio word clocks are derived internally. The functionality is programmed within the Audio module. During reset, these pins are configured as input serial audio word clocks. |
| Serial Audio Data In | The SDATAI1, SDATAI3/GPIO41, and SDATAI4/GPI42 multiplexed pins can serve as general purpose I/Os or serial audio inputs. As serial audio inputs the data is sent to interfaces 1and 3 respectively. The functionality of these pins is programmed with the GPIO-FUNCTION and GPIO1-FUNCTION registers. During reset, the pins are configured as serial data inputs. |
| Serial Audio Data Out | The SDATAO1/GPIO25 AND SDATAO2/GPI41 multiplexed pins can serve as general purpose I/Os or serial audio outputs. The functionality of these pins is programmed with registers GPIO-FUNCTION and GPIO1-FUNCTION. During reset, the pins are configured as serial data outputs.. |
| Serial audio error flag | The EF/GPIO19 multiplexed pin can serve as general purpose I/Os or error flag input. As error flag input, this pin will input the error flag delivered by the CD-DSP. EF/GPIO19 is only relevant for serial interface interface 1. |
| Serial audio CFLG | The CFLG/GPIO18 multiplexed pin can serve as general purpose I/O or CFLG input. As CFLG input, the pin will input the CFLG flag delivered by the CD-DSP. CFLG/GPIO18 is only relevant for serial interface 1. |

# 8.12 Digital Audio Interface Signals

**Table 10. Digital Audio Interface Signals**

| Serial Module Signal | Description |
|---|---|
| Digital Audio In | The EBUIN1/GPI36, EBUIN2/GPI37, EBUIN3/ADIN0/GPI38, and EBUIN4/ADIN1/GPI39 multiplexed signals can serve as general purpose input or can be driven by various digital audio (IEC958) input sources. Both functionalities are always active. Input chosen for IEC958 receiver is programmed within the audio module. Input value on the 4 pins can always be read from the appropriate gpio register.. |
| Digital Audio Out | The EBUOUT1_GPO36 and EBUOUT2_GPO37 multiplexed pins can serve as general purpose I/O or as digital audio (IEC958) output. EBUOUT1 is digital audio out for consumer mode, EBUOUT2 is digital audio out for professional mode. The functionality of the pins is programmed with the GPIO-FUNCTION and GPIO1-FUNCTION register. During reset, the pin is configured as a digital audio output. |

**NOTE**

The EBUOUT2 signal is only used on the 160 MAPBGA package.

# 8.13 Subcode Interface

There is a 3-line subcode interface on the SCF5249. This 3-line subcode interface allows the device to format and transmit subcode in EIAJ format to a CD channel encoder device. The three signals are described in Table 11.

**Table 11. Subcode Interface Signal**

| Signal name | Description |
|---|---|
| RCK/GPIO51 | Subcode clock input. When pin is used as subcode clock, this pin is driven by the CD channel encoder. |
| SFSY/GPIO52 | Subcode sync output<br>This signal is driven high if a subcode sync needs to be inserted in the EFM stream. |
| SUBR/GPIO53 | Subcode data output<br>This signal is a subcode data out pin. |

**NOTE**

The SUBR, SFSY, and the RCK signals are only used in the 160 MAPBGA package.

## 8.14 Analog to Digital Converter (ADC)

The single output on the TOUT1/ADOUT/GPO35 pin provides the reference voltage in PDM format therefore this output requires an external integrator circuit (resistor/capacitor) to convert it to a DC level to be used by the external comparator circuit. Four external comparators compare the DC level obtained after filtering TOUT1/ADOUT/GPO35 with the relevant input signals. The outputs of the comparators are fed to the 4 ADIN inputs on the SCF5249: EBUIN3/ADIN0/GPI38, EBUIN4/ADIN1/GPI39, RXD2/ADIN2/GPI38 and CTS2/ADIN3/GPI31. Selection of function for pin TOUT1/ADOUT/GPO35 is done by writing GPIO function select register (determines if function is GPIO or not), and differentiation between timer and adout functions is done in the ADCONFIG Register.

## 8.15 Secure Digital/ MemoryStick Card Interface

The device has a versatile flash card interface that supports both SecureDigital and MemoryStick cards. The interface can either support one SecureDigital or two MemoryStick cards. No mixing of card types is possible. Table 12 gives the pin descriptions.

**Table 12. Flash Memory Card Signals**

| Flash Memory Signal | Description |
|---|---|
| SCLKOUT/GPIO15 | Clock out for both MemoryStick interfaces and for SecureDigital |
| CMD_SDIO2/GPIO34 | Secure Digital command line<br>MemoryStick interface 2 data i/o |
| SDATA0_SDIO1/GPIO54 | SecureDigital serial data bit 0<br>MemoryStick interface 1 data i/o |
| SDATA1_BS1/GPIO9 | SecureDigital serial data bit 1<br>MemoryStick interface 1 strobe |
| RSTO/SDATA2_BS2 | SecureDigital serial data bit 2<br>MemoryStick interface 2 strobe<br>Reset output signal<br>Selection between Reset function and SDATA2_BS2 is done by programming PLLCR register. |
| SDATA3/GPIO57 | SecureDigital serial data bit 3 |

**NOTE**

The SDATA0_SDIO1 and RSTO/SDATA2_BS2 signals are only used in the 160 MAPBGA package.

# 8.16 Queued Serial Peripheral Interface (QSPI)

**Table 13. Queued Serial Peripheral Interface (QSPI) Signals**

| Serial Module Signal | Description |
|---|---|
| SCL_QSPICLK | Multiplexed signal IIC interface clock or QSPI clock output<br>Function select is done via PLLCR register. |
| SDA_QSPIDIN | Multiplexed signal IIC interface data or QSPI data input.<br>Function select is done via PLLCR register. |
| QSPIDOUT_GPIO26 | QSPI data output |
| QSPICS0_GPIO29 | 4 different QSPI chip selects |
| QSPICS1_GPIO24 | |
| QSPICS2_GPIO21 | |
| QSPICS3_GPIO22 | |

**NOTE**

The QSPI interface is a high-speed serial interface allowing transmit and receive of serial data.

# 8.17 Crystal Trim

The XTRIM_GPIO38 output produces a pulse-density modulated phase/frequency difference signal to be used after low-pass filtering to control varicap-voltage to control crystal oscillation frequency. This will lock the crystal to the incoming digital audio signal.

# 8.18 Clock Out

The MCLK1/GPO39 and /MCLK2/GPO42 can serve as general purpose I/Os or as DAC clock outputs. When programmed as DAC clock outputs, these signals are directly derived from the crystal.

# 8.19 Debug and Test Signals

These signals interface with external I/O to provide processor status signals.

## 8.19.1 Test Mode

The TEST[3:0] inputs are used for various manufacturing and debug tests. For normal mode these inputs should be always be tied low. Use TEST0 to switch between background debug mode and JTAG mode. Drive TEST0 high for debug mode.

## 8.19.2 High Impedance

The assertion of $\overline{\text{HI\_Z}}$ will force all output drivers to a high-impedance state. The timing on $\overline{\text{HI\_Z}}$ is independent of the clock.

**NOTE**

JTAG operation will override the $\overline{\text{HI\_Z}}$ pin.

## 8.19.3 Processor Clock Output

The internal PLL generates this PSTCLK/GPO63 and output signal, and is the processor clock output that is used as the timing reference for the Debug bus timing (DDATA[3:0] and PST[3:0]). The PSTCLK/GPO63 is at the same frequency as the core processor and cache memory. The frequency will be twice the bus clock (SCLK) frequency.

## 8.19.4 Debug Data

The debug data pins, DDATA0_GPIO0, DDATA1_GPIO1, DDATA2_GPIO2, and DDATA3_GPIO4, are four bits wide. This nibble-wide bus displays captured processor data and break-point status.

## 8.19.5 Processor Status

The processor status pins, PST0_GPIO59, PST1_GPIO60, PST2_GPIO61, and PST3_GPIO62, indicate the SCF5249 processor status. During debug mode, the timing is synchronous with the processor clock (PSTCLK) and the status is not related to the current bus transfer. .

**Table 14. Processor Status Signal Encodings**

| PST[3:0] | | Definition |
|---|---|---|
| (HEX) | (BINARY) | |
| $0 | 0000 | Continue execution |
| $1 | 0001 | Begin execution of an instruction |
| $2 | 0010 | Reserved |
| $3 | 0011 | Entry into user-mode |
| $4 | 0100 | Begin execution of PULSE and WDDATA instructions |
| $5 | 0101 | Begin execution of taken branch or Synch_PC[1] |
| $6 | 0110 | Reserved |
| $7 | 0111 | Begin execution of RTE instruction |
| $8 | 1000 | Begin 1-byte data transfer on DDATA |
| $9 | 1001 | Begin 2-byte data transfer on DDATA |
| $A | 1010 | Begin 3-byte data transfer on DDATA |
| $B | 1011 | Begin 4-byte data transfer on DDATA |
| $C | 1100 | Exception processing[2] |
| $D | 1101 | Emulator mode entry exception processing[2] |
| $E | 1110 | Processor is stopped, waiting for interrupt[2] |
| $F | 1111 | Processor is halted[2] |

Notes:
4. Rev. B enhancement.
5. These encodings are asserted for multiple cycles.

# 8.20 BDM/JTAG Signals

The SCF5249 complies with the IEEE 1149.1A JTAG testing standard. The JTAG test pins are multiplexed with background debug pins.

## 8.20.1 Test Clock

TCK is the dedicated JTAG test logic clock that is independent of the SCF5249 processor clock. Various JTAG operations occur on the rising or falling edge of TCK. The internal JTAG controller logic is designed such that holding TCK high or low for an indefinite period of time will not cause the JTAG test logic to lose state information. If TCK will not be used, it should be tied to ground.

## 8.20.2 Test Reset/Development Serial Clock

The TEST[3:0] signals determine the function of the TRST/DSCLK dual-purpose pin. If TEST[3:0]=0001, the DSCLK function is selected. If TEST[3:0]= 0000, the TRST function is selected. TEST[3:0] should not be changed while RSTI = 1. When used as TRST, this pin will asynchronously reset the internal JTAG controller to the test logic reset state, causing the JTAG instruction register to choose the ìbypassî command. When this occurs, all the JTAG logic is benign and will not interfere with the normal functionality of the SCF5249 processor. Although this signal is asynchronous, Freescale recommends that TRST make only a 0 to 1 (asserted to negated) transition while TMS is held at a logic 1 value. TRST has an internal pullup so that if it is not driven low its value will default to a logic level of 1. However, if TRST will not be used, it can either be tied to ground or, if TCK is clocked, it can be tied to VDD. If it is tied to ground, it will place the JTAG controller in the test logic reset state immediately. If it is tied to VDD, it will cause the JTAG controller (if TMS is a logic 1) to eventually end up in the test logic reset state after 5 clocks of TCK. This pin is also used as the development serial clock (DSCLK) for the serial interface to the Debug Module.The maximum frequency for the DSCLK signal is 1/5 the BCLKO frequency.

## 8.20.3 Test Mode Select/Break Point

The TEST[3:0] signals determine the TMS/BKPT pin function. If TEST[3:0] =0001, the BKPT function is selected. If TEST[3:0] = 0000, then the TMS function is selected. TEST[3:0] should not change while $_{RSTI}$ = 1. When used as TMS, this input signal provides the JTAG controller with information to determine which test operation mode should be performed. The value of TMS and current state of the internal 16-state JTAG controller state machine at the rising edge of TCK determine whether the JTAG controller holds its current state or advances to the next state. This directly controls whether JTAG data or instruction operations occur. TMS has an internal pullup so that if it is not driven low, its value will default to a logic level of 1. However, if TMS will not be used, it should be tied to VDD. This pin also signals a hardware breakpoint to the processor when in the debug mode.

## 8.20.4 Test Data Input/Development Serial Input

The TDI/DS is a dual-function pin. If TEST[3:0] = 0001, then DSI is selected. If TEST[3:0] = 0000, then TDI is selected. When used as TDI, this input signal provides the serial data port for loading the various JTAG shift registers composed of the boundary scan register, the bypass register, and the instruction register. Shifting in of data depends on the state of the JTAG controller state machine and the instruction currently in the instruction register. This data shift occurs on the rising edge of TCK. TDI also has an internal pullup so that if it is not driven low its value will default to a logic level of 1. However, if TDI will not be used, it should be tied to VDD. This pin also provides the single-bit communication for the debug module commands.

## 8.20.5 Test Data Output/Development Serial Output

The TDO/DSO is a dual-function pin. When TEST[3:0] = 0001, then DSO is selected. When TEST[3:0] = 0000, TDO is selected. When used as TDO, this output signal provides the serial data port for outputting

data from the JTAG logic. Shifting out of data depends on the state of the JTAG controller state machine and the instruction currently in the instruction register. This data shift occurs on the falling edge of TCK. When TDO is not outputting test data, it is three-stated. TDO can also be placed in three-state mode to allow bussed or parallel connections to other devices having JTAG. This signal also provides single-bit communication for the debug module responses.

## 8.21 Clock and Reset Signals

These signals configure the SCF5249 and provide interface signals to the external system.

### 8.21.1 Reset In

Asserting $\overline{\text{RSTI}}$ causes the SCF5249 to enter reset exception processing. When $\overline{\text{RSTI}}$ is recognized, the data bus is tri-stated.

### 8.21.2 System Bus Input

The CRIN signal is the system clock input. The device has no on-chip clock oscillator, and needs an external oscillator.

# 9 Electrical Characteristics

**Table 15. Maximum Ratings**

| Rating | Symbol | Value | Units |
|---|---|---|---|
| Supply Core Voltage | $V_{cc}$ | -0.5 to +2.5 | V |
| Maximum Core Operating Voltage | $V_{cc}$ | +1.98 | V |
| Minimum Core Operating Voltage | $V_{cc}$ | +1.62 | V |
| Supply I/O Voltage | $V_{cc}$ | -0.5 to +4.6 | V |
| Maximum I/O Operating Voltage | $V_{cc}$ | +3.6 | V |
| Minimum I/O Operating Voltage | $V_{cc}$ | +3.0 | V |
| Input Voltage | $V_{in}$ | -0.5 to +6.0 | V |
| Storage Temperature Range | $T_{stg}$ | -65 to150 | $^{o}$C |

**Table 16. Operating Temperature**

| Characteristic | Symbol | Value | Units |
|---|---|---|---|
| Maximum Operating Ambient Temperature | $T_{Amax}$ | 85[1] | $^{o}$C |
| Minimum Operating Ambient Temperature | $T_{Amin}$ | 0 | $^{o}$C |
| Note: This published maximum operating ambient temperature should be used only as a system design guideline. All device operating parameters are guaranteed only when the junction temperature does not exceed 105°C. | | | |

**Table 17. DC Electrical Specifications (Vcc = 3.3 Vdc ± 0.3 Vdc)**

| Characteristic | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Operation Voltage Range for I/O | $V_{cc}$ | 3.0 | 3.6 | V |
| Input High Voltage | $V_{IH}$ | 2 | 5.5 | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | 0.8 | V |
| Input Leakage Current @ 0.0 V /3.3 V During Normal Operation | $I_{in}$ | - | ±1 | μμA |
| Hi-Impedance (Three-State) Leakage Current @ 0.0 V/3.3 V During Normal Operation | $I_{TSI}$ | - | ±1 | μμA |
| Output High Voltage $I_{OH}$ = 8mA[1], 4mA[2], 2mA[3] | $V_{OH}$ | 2.4 | - | V |
| Output Low Voltage $I_{OL}$ = 8mA[1], 4mA[2], 2mA[3] | $V_{OL}$ | - | 0.4 | V |
| Schmitt Trigger Low to High Threshold Point[6] | $V_{T+}$ | 1.47 | - | V |
| Schmitt Trigger High to Low Threshold Point[6] | $V_{T-}$ | - | .95 | V |
| Load Capacitance (DATA[31:16], DCL0, DCL1, SCLK[4:1], SCLKOUT, EBUOUT[2:1], LRCK[4:1], SDATAO[2:1], CFLG, EF, DBCDDATA[3:0], DBCPST[3:0], CNPSTCLK, IDEDIOR, IDEDIOW, IORDY, SRE, SWE) | $C_L$ | - | 50 | pF |
| Load Capacitance (ADDR[25, 23:9], SCLK) | $C_L$ | - | 40 | pF |
| Load Capacitance (BCLKE, SDCAS, SDRAS, SDLDQM, SDRAMCS[2:1],, SDUDQM, SDWE, BUFENB[2:1]) | $C_L$ | - | 30 | pF |
| Load Capacitance (SDA, SDA2, SCL, SCL2, CMDSDIO2, SDATA2BS2, SDATA1BS1, SDATA0SDIO1, CS[1:0], OE, R/$\overline{W}$, TA, TXD[2:0], XTRIM, TDO/DSO, RCK, SFSY, SUBR, SDATA3, TOUT[1:0], QSPIDOUT, QSPICS[3:0], GP[6:5]) | $C_L$ | - | 20 | pF |
| Capacitance[5], $V_{in}$ = 0 V, f = 1 MHz | $C_{IN}$ | - | 6 | pF |

1. DATA[31:16], ADDR[25, 23:9], PSTCLK, SCLK
2. SCL, SDA, PST[3:0], DDATA[3:0], TDSO, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, $\overline{SDRAMCS}$[2:1], $\overline{SDLDQM}$, $\overline{SDUDQM}$, R/$\overline{W}$
3. TOUT[1:0], RTS[2:0], TXD[2:1], SCLK[4:1]
4. $\overline{BKPT}$/TMS, DSI/TDI, DSCLK/$\overline{TRST}$
5. Capacitance $C_{IN}$ is periodically sampled rather than 100% tested.
6. SCLK[4:1], SCL, SCL2, SDA, SDA2, CRIN, RSTI

# 9.1 Supply Voltage Sequencing and Separation Cautions

Figure 2 shows two situations to avoid in sequencing the CoreVdd and PADVdd (I/O) and PLLL supplies.

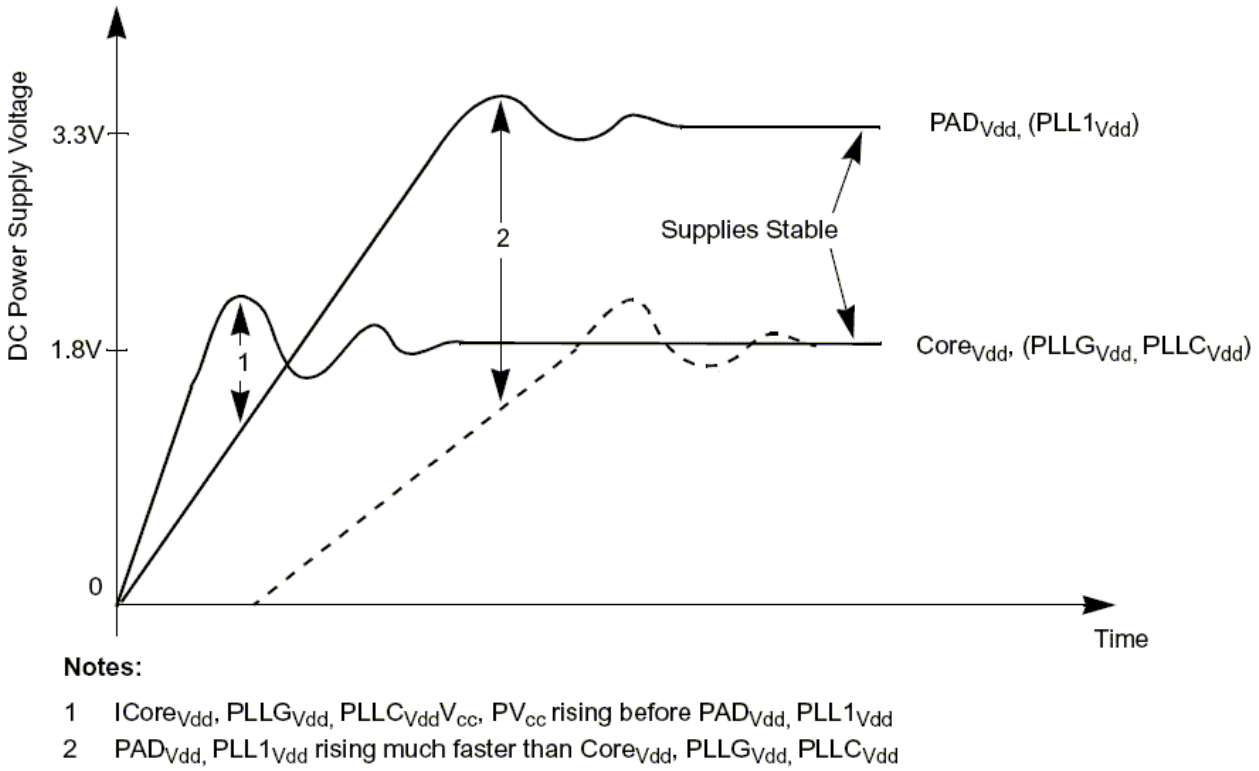


**Figure 2. Supply Voltage Sequencing and Separation Cautions**

CoreVdd supply should not be allowed to rise early (1). This is usually avoided by running the regulator for the CoreVdd supply (1.8 V) from the voltage generated by the 3.3V supply (PADVdd). This keeps the CoreVdd supply from rising faster than PADVdd supply.

Also CoreVdd, PLLGVdd, PLLCVdd supply should not rise so late that a large voltage difference is allowed between the two supplies (2). Typically this situation is avoided by using external discrete diodes in series between supplies. The series diodes forward bias when the difference between PADVdd and CoreVdd reaches approximately 2.1V, causing CoreVdd to rise as PADVdd ramps up. When the CoreVdd regulator begins proper operation, the difference between supplies should not exceed 1.5 V and conduction through the diode chain reduces to essentially leakage current.

During supply sequencing, the following general relationship should be adhered to: PADVdd, >= CoreVdd, PLLGVdd, >= (PADVdd - 2.1 V).

The PLL core supplies (PLLGVdd and PLLCVdd) should comply with these constraints just as the CoreVdd does. In practice, PLLGVdd and PLLCVdd are typically connected directly to the CoreVdd with some filtering. Further, the PLL PAD supply (PLL1VDD) would be connected directly to the PAD supply via some filtering.

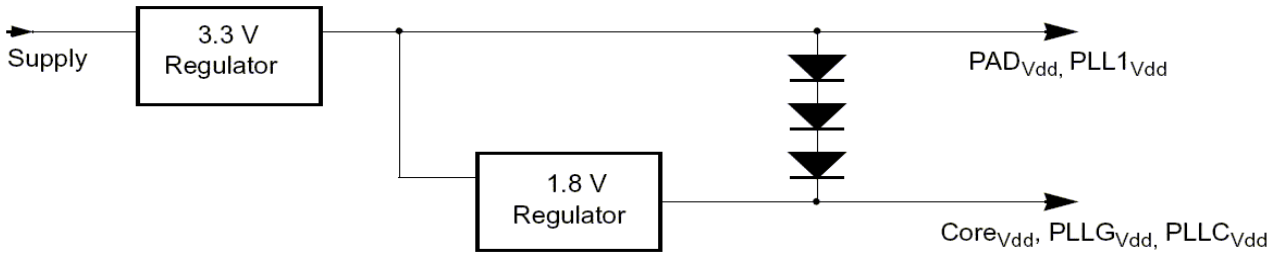


**Figure 3. Example Circuit to Control Supply Sequencing**

When a DC-DC convertor is used in the system to generate the 1.8V supply, additional care is required. If possible, the 1.8V DC-DC convertor should be supplied by the 3.3V supply. If this is impossible or considered inefficient, the designer needs to ensure that the rise time of the 1.8V supply still complies with the recommendations stated above. Adding the 3 diodes will help resolve issues associated with a slow rise time of the 1.8V supply. Further, a Schotty diode could be added between the supplies, which would have the effect of holding the 1.8V supply to match the 3.3V supply should the 1.8V supply come-up first. This diode also has the function of ensuring that there is not a large voltage differential between the Core supply and the PAD supply during power-down.

Refer to the *M5249C3 Reference Board Userís Manual* for the recommended diode types.

A further note is the recommendation for hard resetting of the device. Freescale recommends using a dynamic reset circuit. This allows for control of the voltage at which the reset will be released and ensure that the correct voltage level at the RESET pin is achieved in all cases. Passive (RC) reset networks do not always achieve the desired results.

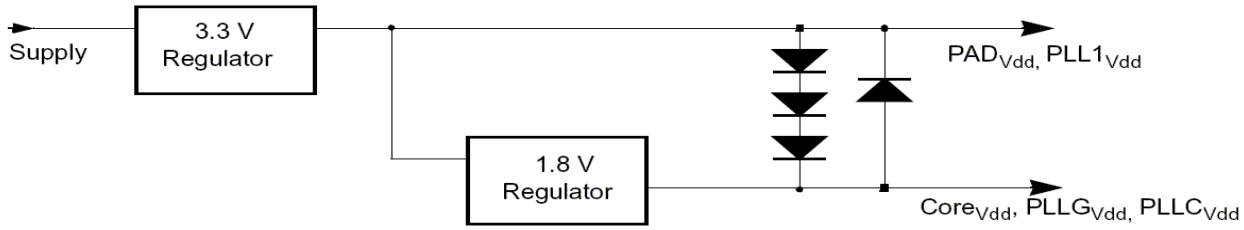


**Figure 4. SCF5249 Power Supply**

## NOTE

The following signals are not available on the 144 QFP package.

**Table 18. 160 MAPBGA Ball Assignments**

| 160MAPBGA Ball Number | Function | GPIO |
|---|---|---|
| E3 | CMD_SDIO2 | GPIO34 |
| G4 | SDATA0-SDIO1 | GPIO54 |
| H3 | RSTO/SDATA2_BS2 | |
| K3 | A25 | GPO8 |

**Table 18. 160 MAPBGA Ball Assignments (continued)**

| 160MAPBGA Ball Number | Function | GPIO |
|---|---|---|
| L4 | QSPI_CS1 | GPIO24 |
| L8 | QSPI_CS3 | GPIO22 |
| N8 | SDRAM_CS2 | GPIO7 |
| P9 | EBUOUT2 | GPO37 |
| K11 | BUFENB2 | GPIO17 |
| G12 | SUBR | GPIO53 |
| F13 | SFSY | GPIO52 |
| F12 | RCK | GPIO51 |
| E8 | SRE | GPIO11 |
| B8 | LRCK3 | GPIO45 |
| E7 | SWE | GPIO12 |
| A7 | SCLK3 | GPIO49 |

**Table 19. Clock Timing Specification**

| NUM | Characteristic | | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| | CRIN Frequency[1] | 11.29 | 33.86 | MHz |
| C5 | PSTCLK cycle time | 7.1 | — | nSec |
| C6 | PSTCLK duty cycle | 40 | 60 | % |
| C7 | BCLK cycle time | 14.2 | — | nSec |
| C8 | BCLK duty cycle | 45 | 55 | % |

Note: There are only three choices for the valid Audio frequencies 11.29 MHz, 16.93 MHz, or 33.86 MHz; no other values are allowed. The System Clock is derived from one of these crystals via an internal PLL.

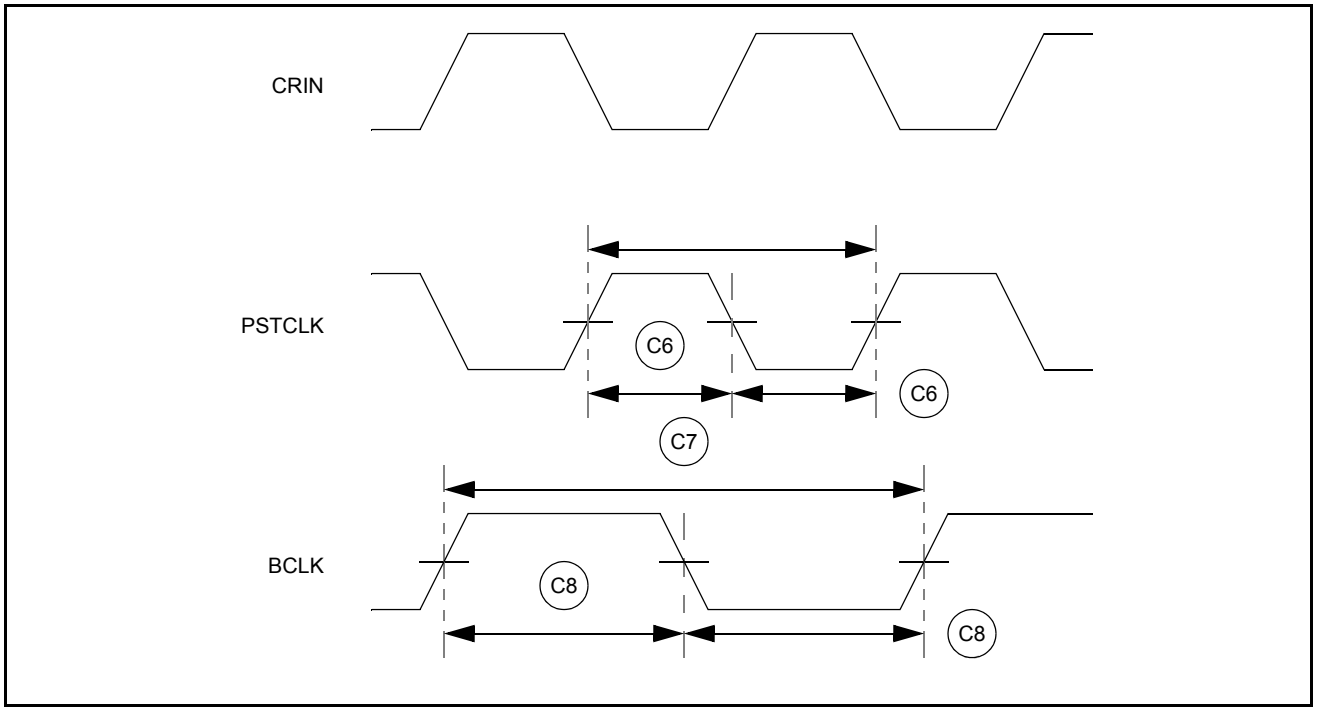


**Figure 5. Clock Timing Definition**

**NOTE**

Signals above are shown in relation to the clock. No relationship between signals is implied or intended.

## 9.1.1 Processor Bus Input Timing Specification

Table 20 lists processor bus input timings.

**NOTE**

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the SCLK output. All other timing relationships can be derived from these values.

**Table 20. External Bus Input Timing Specifications**

| Num | Characteristic[a] | | | | Units |
|---|---|---|---|---|---|
| | | Symbol | Min | Max | |
| B0 | SCLK | tCYC | 14.26 | — | ns |
| B1 | Control input valid to SCLK high[b] | tCVCH | 10 | — | ns |
| B2 | SCLK high to control inputs valid[b] | tCHCII | 2 | — | ns |
| B4 | Data input (D[31:0]) valid to SCLK high | tDIVCH | 6 | — | ns |

**Table 20. External Bus Input Timing Specifications (continued)**

| Num | Characteristic[a] | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| B5 | SCLK high to data input (D[31:0]) invalid | tCHDII | 2 | — | ns |

a. Timing specifications have been indicated taking into account the full drive strength for the pads.
b. TA pin is being referred to as control input.

## 9.1.2 Processor Bus Output Timing Specifications

Table 21 lists processor bus output timings.

**Table 21. External Bus Output Timing Specifications**

| NAME | CHARACTERISTIC | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Control Outputs | | | | | |
| B6a | SCLK high to chip selects valid [a] | $t_{CHCV}$ | — | $0.5t_{CYC}$ +10 | ns |
| B6b | SCLK high to output enable ($\overline{OE}$) valid[b] | $t_{CHOV}$ | — | $0.5t_{CYC}$ +10 | ns |
| B7a | SCLK high to control output ($\overline{OE}$) invalid | $t_{CHCOI}$ | $0.5t_{CYC}$ + 2 | — | ns |
| B7b | SCLK high to chip selects invalid | $t_{CHCI}$ | $0.5t_{CYC}$ + 2 | — | ns |
| Address and Attribute Outputs | | | | | |
| B8 | SCLK high to address (A[23:1]) and control (R/$\overline{W}$) valid | $t_{CHAV}$ | — | 10 | ns |
| B9 | SCLK high to address (A[23:1]) and control (R/$\overline{W}$) invalid | $t_{CHAI}$ | 2 | — | ns |
| Data Outputs | | | | | |
| B11 | SCLK high to data output (D[31:16]) valid | $t_{CHDOV}$ | — | 10 | ns |
| B12 | SCLK high to data output (D[31:16]) invalid | $t_{CHDOI}$ | 2 | — | ns |
| B13 | SCLK high to data output (D[31:16]) high impedance | $t_{CHDOZ}$ | — | 14 | ns |

a. $\overline{CSn}$ transitions after the falling edge of SCLK.
b. $\overline{OE}$ transitions after the falling edge of SCLK.

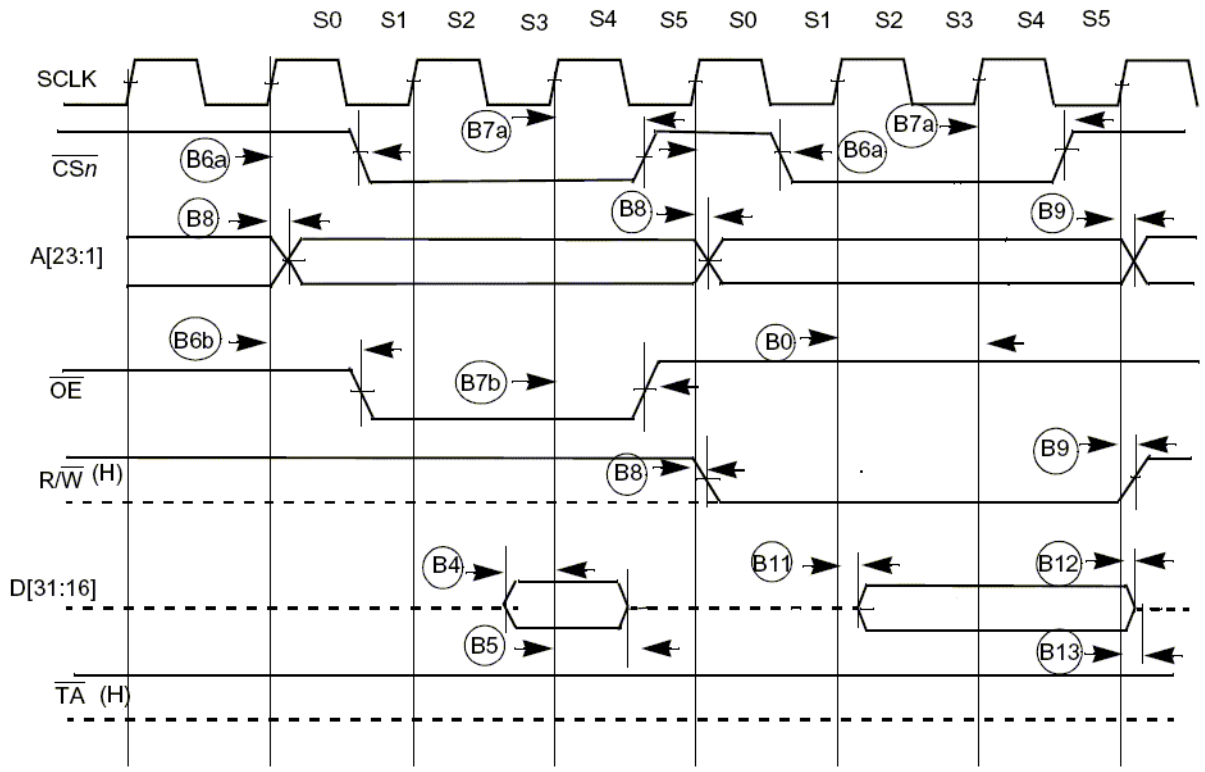


**Figure 6. Read/Write (Internally Terminated) Timing**

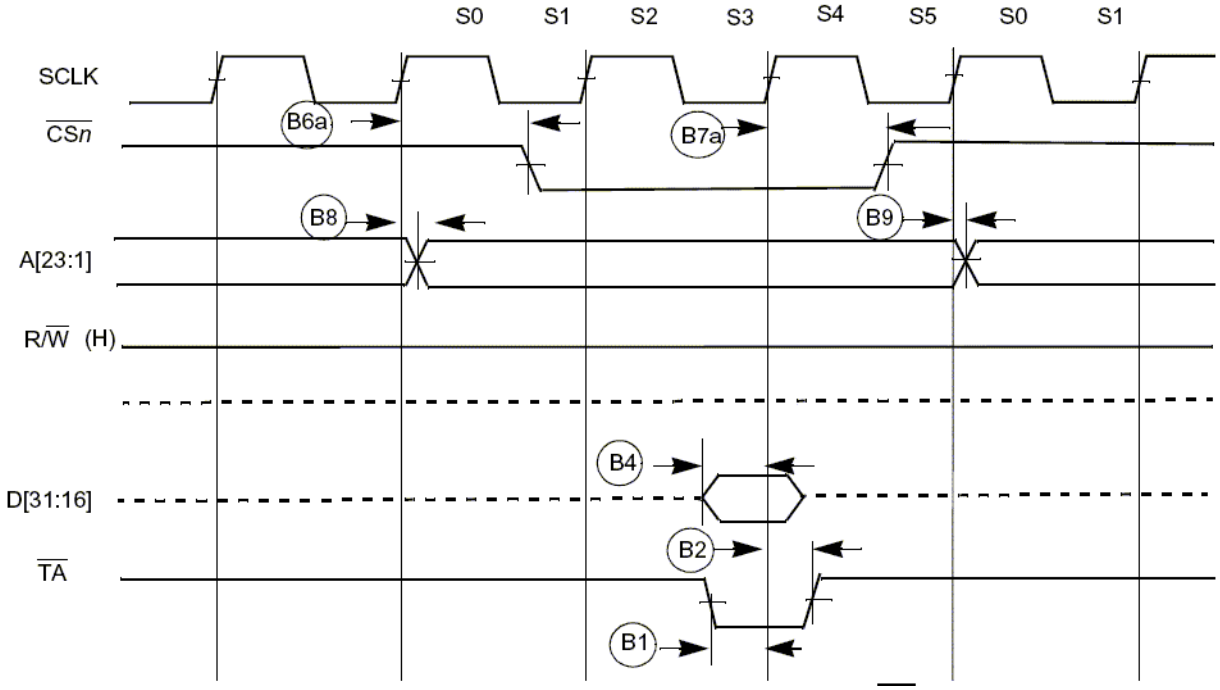


**Figure 7. Read Bus Cycle Terminated by TA**

**Table 22. SDRAM Timing**

| NUM | CHARACTERISTIC[A] | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| SD1 | SCLK high to SDRAM address valid | $t_{CHDAV}$ | — | 10 | ns |
| SD2 | SCLK high to SDRAM control valid | $t_{CHDCV}$ | — | 11 | ns |
| SD3 | SCLK high to SDRAM address invalid | $t_{CHDAI}$ | 2 | — | ns |
| SD4 | SCLK high to SDRAM control invalid | $t_{CHDCI}$ | 2 | — | ns |
| SD5 | SDRAM data valid to SCLK high | $t_{DDVCH}$ | 6 | — | ns |
| SD6 | SCLK high to SDRAM data invalid | $t_{CHDDI}$ | 2 | — | ns |
| SD7[b] | SCLK high to SDRAM data valid | $t_{CHDDVW}$ | — | 10 | ns |
| SD8[2] | SCLK high to SDRAM data invalid | $t_{CHDDIW}$ | 2 | — | ns |

a. All timing specifications are based on taking into account, a 25pF load on the SDRAM output pins.
b. D7 and D8 are for write cycles only.

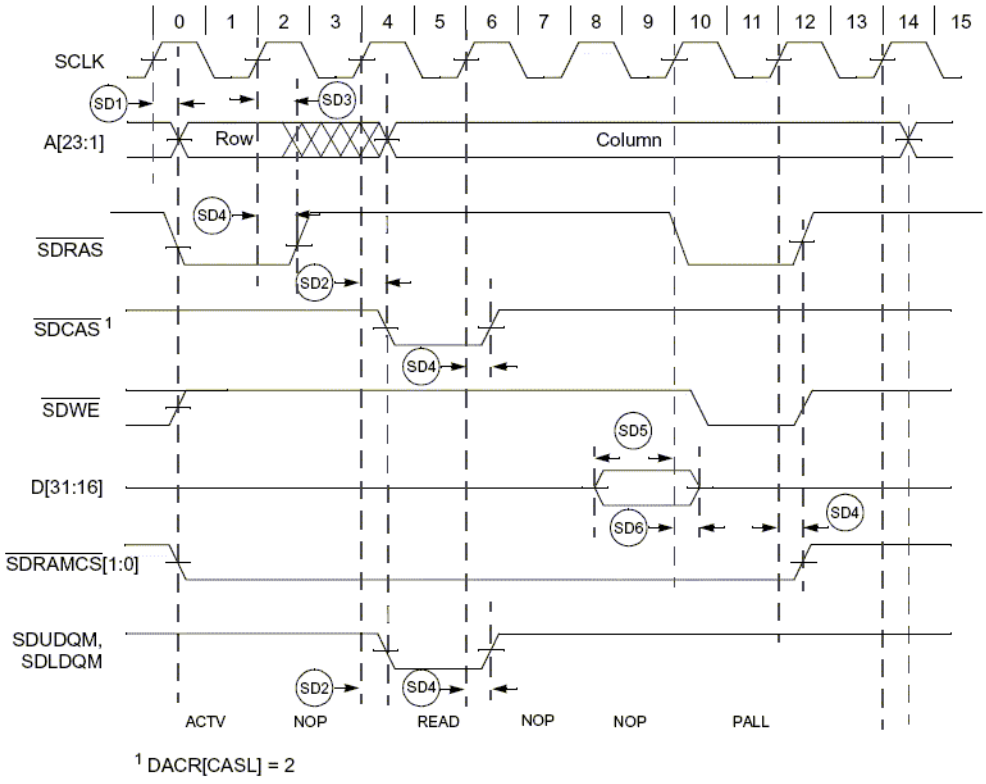


**Figure 8. SDRAM Read Cycle**

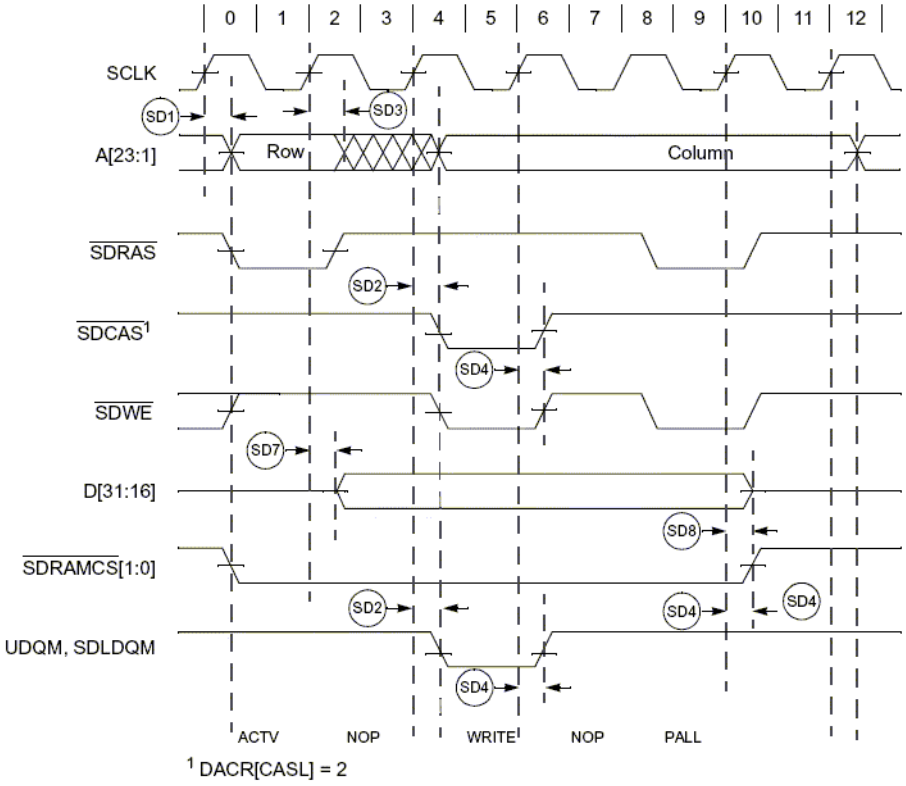


**Figure 9. SDRAM Write Cycle**

**Table 23. Debug AC Timing Specification**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| D1 | PSTCLK to signal Valid (Output valid) | --- | 6 | nSec |
| D2 | PSTCLK to signal Invalid (Output hold) | 1.8 | — | nSec |
| D3[1] | Signal Valid to PSTCLK (Input setup) | 3 | — | nSec |
| D4 | PSTCLK to signal Invalid (Input hold) | 5 | — | nSec |

1. DSCLK and DSI are internally synchronized. This setup time must be met only if recognition on a particular clock is required.
2. AC timing specs assume 50pF load capacitance on PSTCLK and output pins. If this value is different, the input and output timing specifications would need to be adjusted to match the clock load.

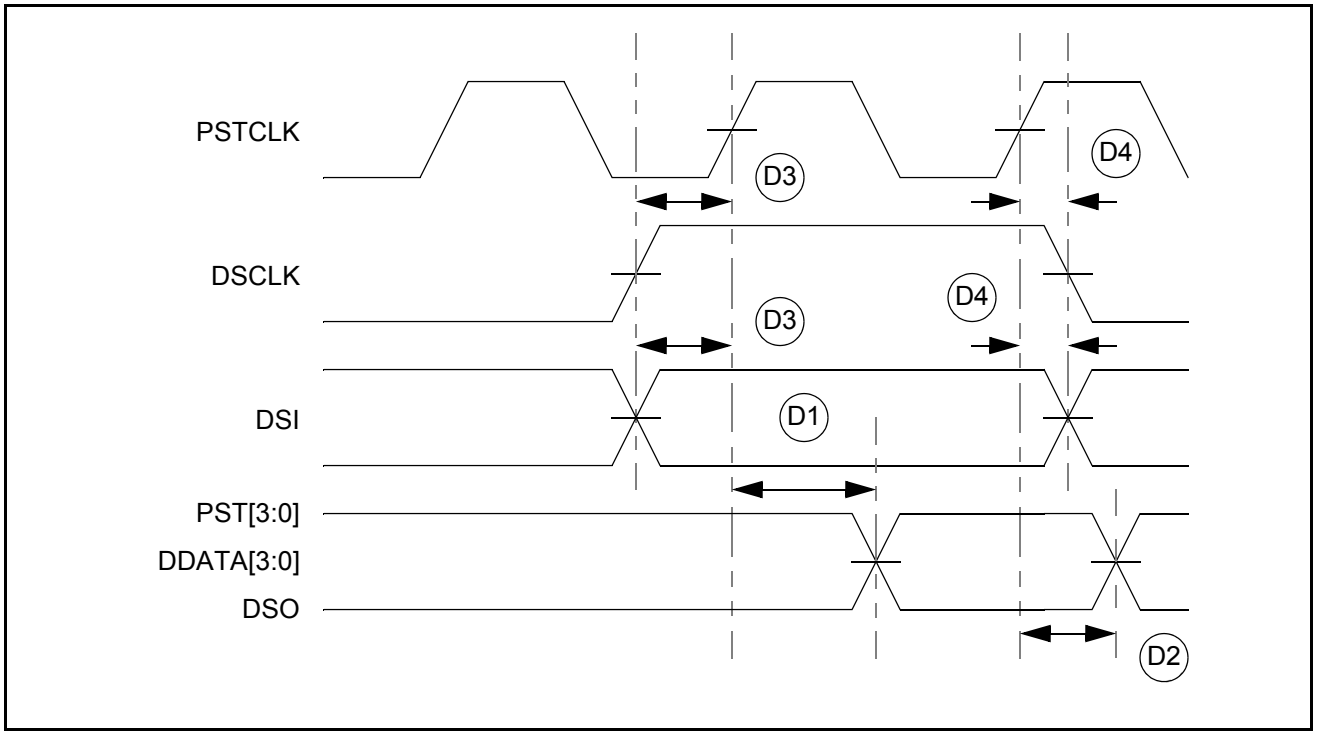


**Figure 10. Debug Timing Definition**

**Table 24. Timer Module AC Timing Specification**

| Num | Characteristic | | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| T1 | TIN Cycle time | tbd | — | bus clocks |
| T2 | TIN Valid to BCLK (input setup) | tbd | — | nSec |
| T3 | SCLK to TIN Invalid (input hold) | tbd | — | nSec |
| T4 | SCLK to TOUT Valid (output valid) | — | tbd | nSec |
| T5 | SCLK to TOUT Invalid (output hold) | tbd | — | nSec |
| T6 | TIN Pulse Width | tbd | — | bus clocks |
| T7 | TOUT Pulse Width | tbd | — | bus clocks |

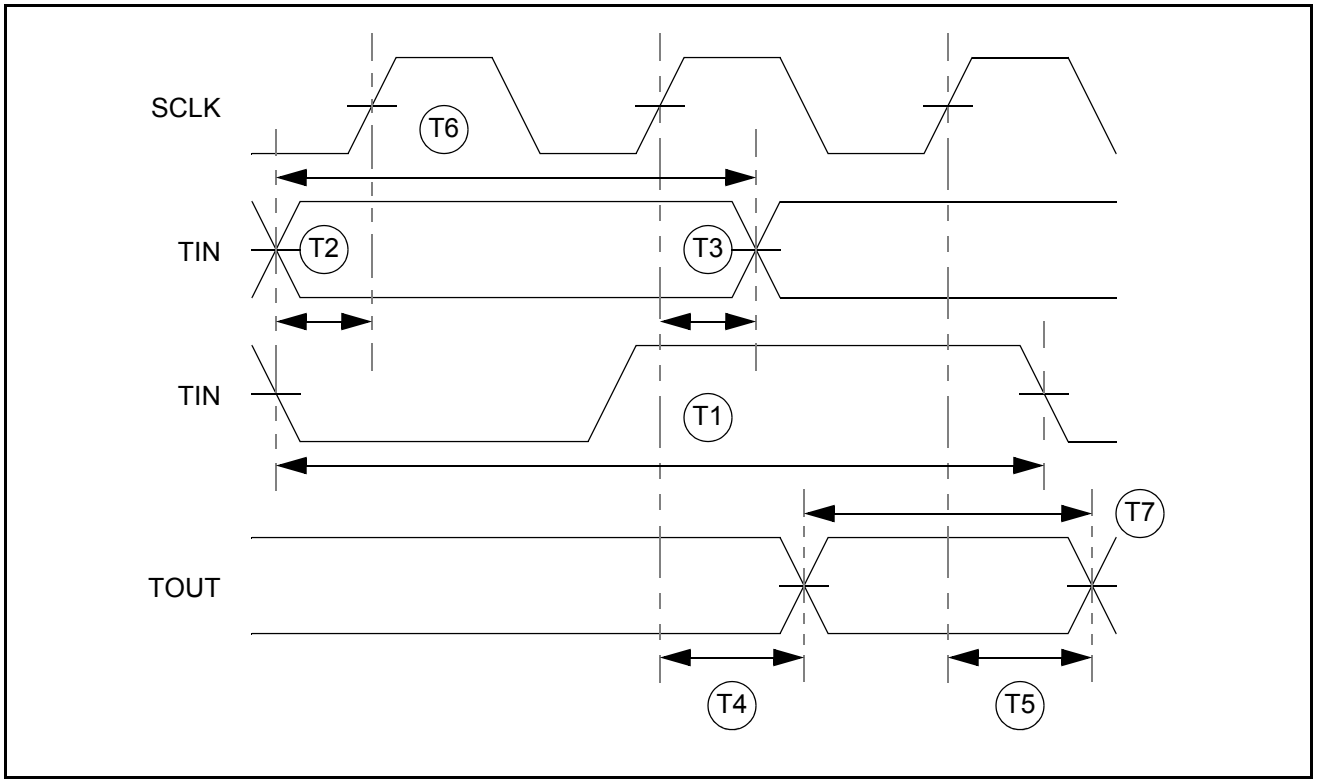


**Figure 11. Timer Module Timing Definition**

**Table 25. UART Module AC Timing Specifications**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| U1 | RXD Valid to BCLK (input setup) | tbd | — | nSec |
| U2 | SCLK to RXD Invalid (input hold) | tbd | — | nSec |
| U3 | $\overline{\text{CTS}}$ Valid to SCLK (input setup) | tbd | — | nSec |
| U4 | SCLK to $\overline{\text{CTS}}$ Invalid (input hold) | tbd | — | nSec |
| U5 | SCLK to TXD Valid (output valid) | --- | tbd | nSec |
| U6 | SCLK to TXD Invalid (output hold) | tbd | — | nSec |
| U7 | SCLK to $\overline{\text{RTS}}$ Valid (output valid) | --- | tbd | nSec |
| U8 | SCLK to $\overline{\text{RTS}}$ Invalid (output hold) | tbd | — | nSec |

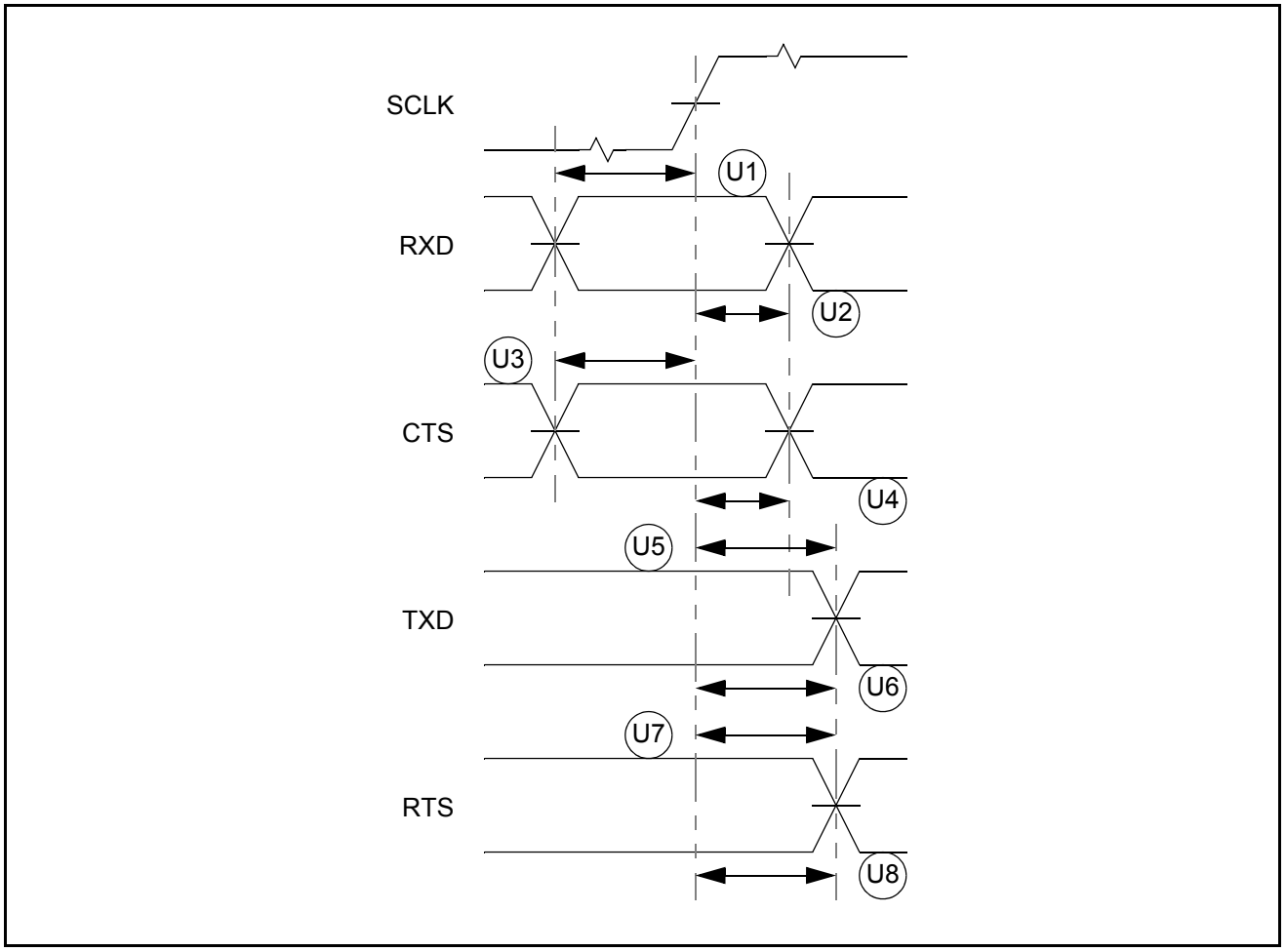


**Figure 12. UART Timing Definition**

**Table 26. I2C-Bus Input Timing Specifications Between SCL and SDA**

| Num | Characteristic | | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| M1 | Start Condition Hold Time | tbd | — | bus clocks |
| M2 | Clock Low Period | tbd | — | bus clocks |
| M3 | SCL/SDA Rise Time (VIL= 0.5 V to VIH = 2.4 V) | — | tbd | mSec |
| M4 | Data Hold Time | tbd | — | nSec |
| M5 | SCL/SDA Fall Time (VIH= 2.4 V to VIL = 0.5 V) | — | tbd | mSec |
| M6 | Clock High time | tbd | — | bus clocks |
| M7 | Data Setup Time | tbd | — | nSec |
| M8 | Start Condition Setup Time (for repeated start condition only) | tbd | — | bus clocks |

**Table 26. I2C-Bus Input Timing Specifications Between SCL and SDA**

| Num | Characteristic | | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| M9 | Stop Condition Setup Time | tbd | — | bus clocks |

**Table 27. I2C-Bus Output Timing Specifications Between SCL and SDA**

| Num | Characteristic | | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| M1[1] | Start Condition Hold Time | tbd | — | bus clocks |
| M2[1] | Clock Low Period | tbd | — | bus clocks |
| M3[2] | SCL/SDA Rise Time ($V_{IL}$= 0.5 V to $V_{IH}$ = 2.4 V) | — | tbd | mSec |
| M4[1] | Data Hold Time | tbd | — | bus clocks |
| M5[3] | SCL/SDA Fall Time ($V_{IH}$= 2.4 V to $V_{IL}$ = 0.5 V) | — | tbd | nSec |
| M6[1] | Clock High time | tbd | — | bus clocks |
| M7[1] | Data Setup Time | tbd | — | bus clocks |
| M8[1] | Start Condition Setup Time (for repeated start condition only) | tbd | — | bus clocks |
| M9[1] | Stop Condition Setup Time | tbd | — | bus clocks |

1. Note: Output numbers are dependent on the value programmed into the MFDR; an MFDR programmed with the maximum frequency (MFDR = 0x20) will result in minimum output timings as shown in the above table. The MBUS interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the MFDR; however, numbers given in the above table are the minimum values.
2. Since SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values.
3. Specified at a nominal 20 pF load.

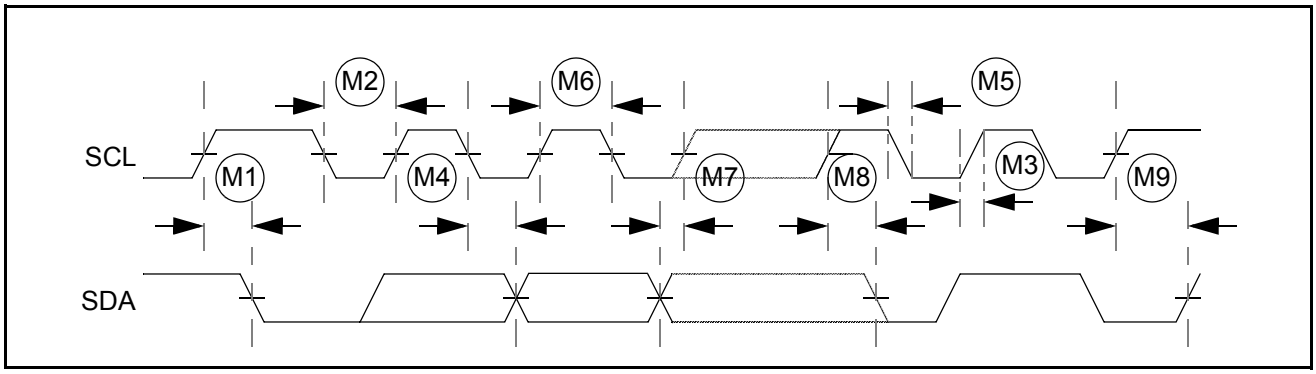


**Figure 13. I2C Timing Definition**

**Table 28. I2C Output Bus Timings**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| M10[3] | SCL, SDA Valid to SCLK (input setup) | tbd | — | nSec |
| M11 | SCLK to SCL, SDA Invalid (input hold) | tbd | — | nSec |
| M12[1] | SCLK to SCL, SDA Low (output valid) | — | tbd | nSec |
| M13[2] | SCLK to SCL, SDA Invalid (output hold) | tbd | — | nSec |

1. Since SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, this specification applies only when SCL or SDA are driven low by the processor. The time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values.
2. Since SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, this specification applies only when SCL or SDA are actively being driven or held low by the processor.
3. SCL and SDA are internally synchronized.This setup time must be met only if recognition on a particular clock is required.

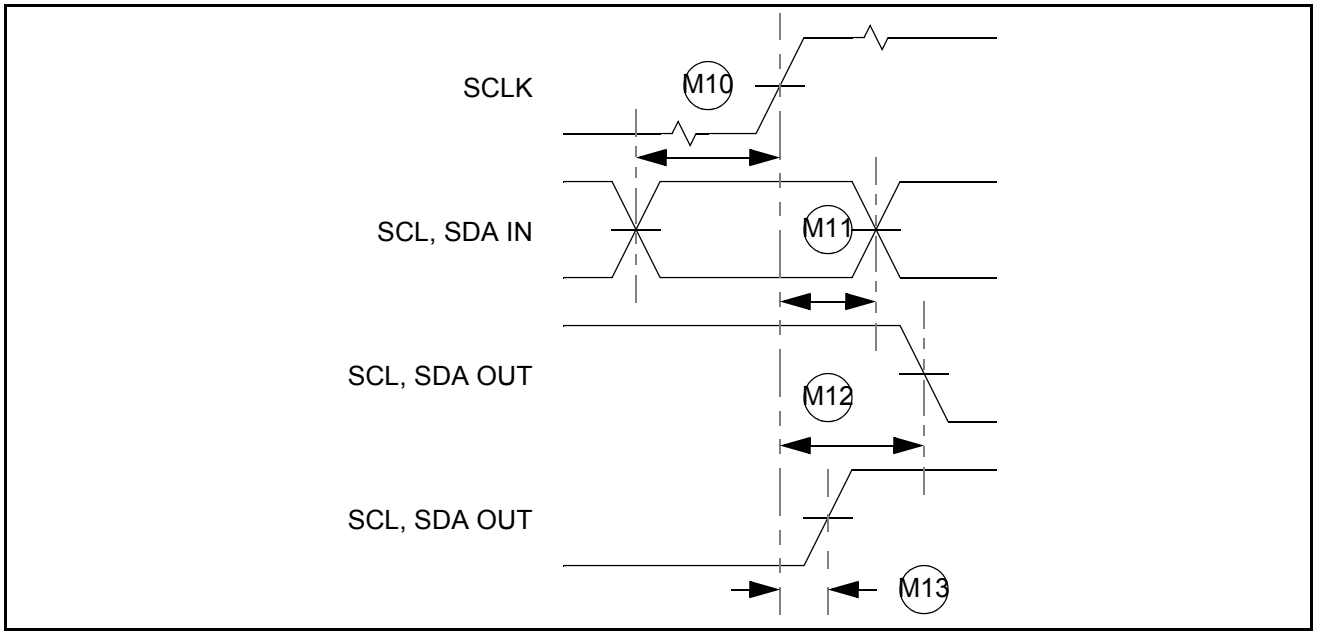


**Figure 14. I²C and System Clock Timing Relationship**

**Table 29. General-Purpose I/O Port AC Timing Specifications**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| P1 | GPIO Valid to SCLK (input setup) | tbd | — | nSec |
| P2 | SCLK to GPIO Invalid (input hold) | tbd | — | nSec |

**Table 29. General-Purpose I/O Port AC Timing Specifications**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| P3 | SCLK to GPIO Valid (output valid) | — | tbd | nSec |
| P4 | SCLK to GPIO Invalid (output hold) | tbd | — | nSec |

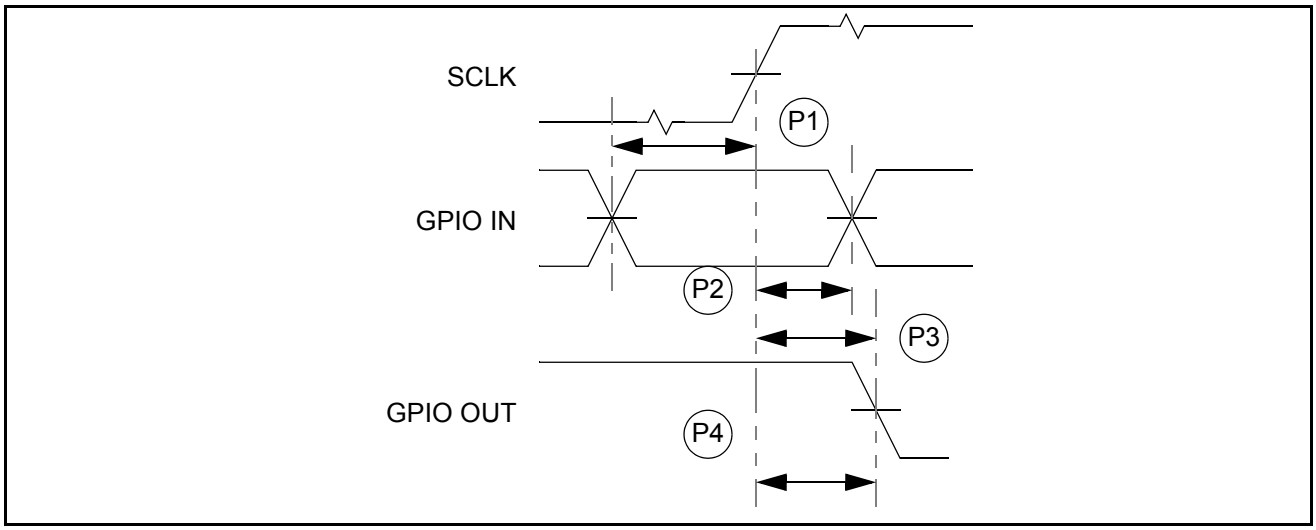


**Figure 15. General-Purpose Parallel Port Timing Definition**

**Table 30. IEEE 1149.1 (JTAG) AC Timing Specifications**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| - | TCK Frequency of Operation | 0 | 10 | MHz |
| J1 | TCK Cycle Time | 100 | - | nSec |
| J2a | TCK Clock Pulse High Width | 25 | - | nSec |
| J2b | TCK Clock Pulse Low Width | 25 | - | nSec |
| J3a | TCK Fall Time ($V_{IH}$=2.4 V to $V_{IL}$=0.5 V) | — | 5 | nSec |
| J3b | TCK Rise Time ($V_{IL}$=0.5 v to $V_{IH}$=2.4 V) | — | 5 | nSec |
| J4 | TDI, TMS to TCK rising (Input Setup) | 8 | — | nSec |
| J5 | TCK rising to TDI, TMS Invalid (Hold) | 10 | — | nSec |
| J6 | Boundary Scan Data Valid to TCK (Setup) | tbd | — | nSec |
| J7 | TCK to Boundary Scan Data Invalid to rising edge (Hold) | tbd | — | nSec |

**Table 30. IEEE 1149.1 (JTAG) AC Timing Specifications**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| J8 | $\overline{\text{TRST}}$ Pulse Width (asynchronous to clock edges) | 12 | — | nSec |
| J9 | TCK falling to TDO Valid (signal from driven or three-state) | — | 15 | nSec |
| J10 | TCK falling to TDO High Impedance | — | 15 | nSec |
| J11 | TCK falling to Boundary Scan Data Valid (signal from driven or three-state) | — | tbd | nSec |
| J12 | TCK falling to Boundary Scan Data High Impedance | — | tbd | nSec |

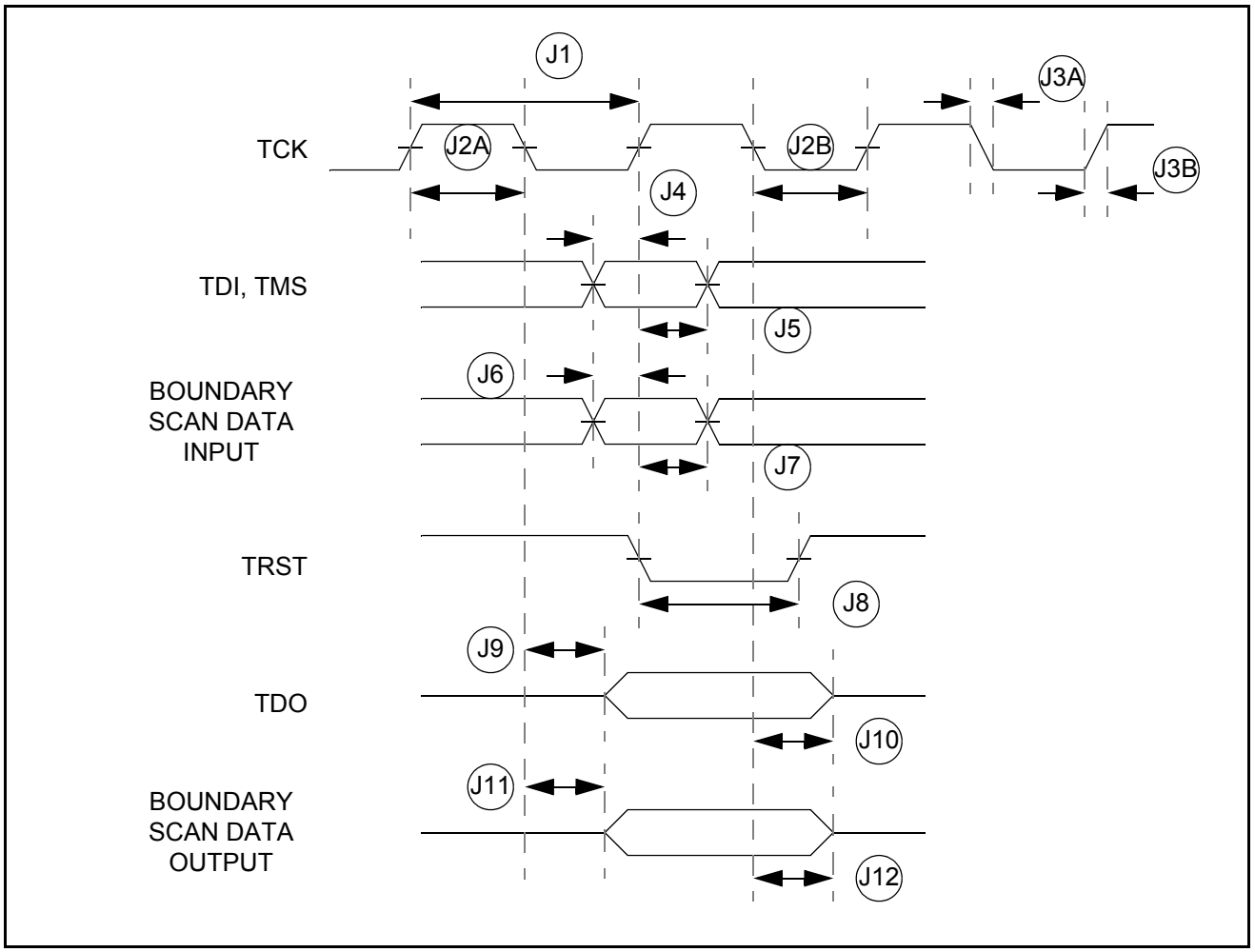


**Figure 16. JTAG Timing**

# 9.2 JTAG Timing Definition IIS Module AC Timing Specifications

**Table 31. SCLK INPUT, SDATAO OUTPUT Timing Specifications**

| Name | Characteristic | | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| TU | SCLK fall to SDATAO rise | --- | 25 | ns |
| TD | SCLK fall to SDATAO fall | --- | 25 | ns |

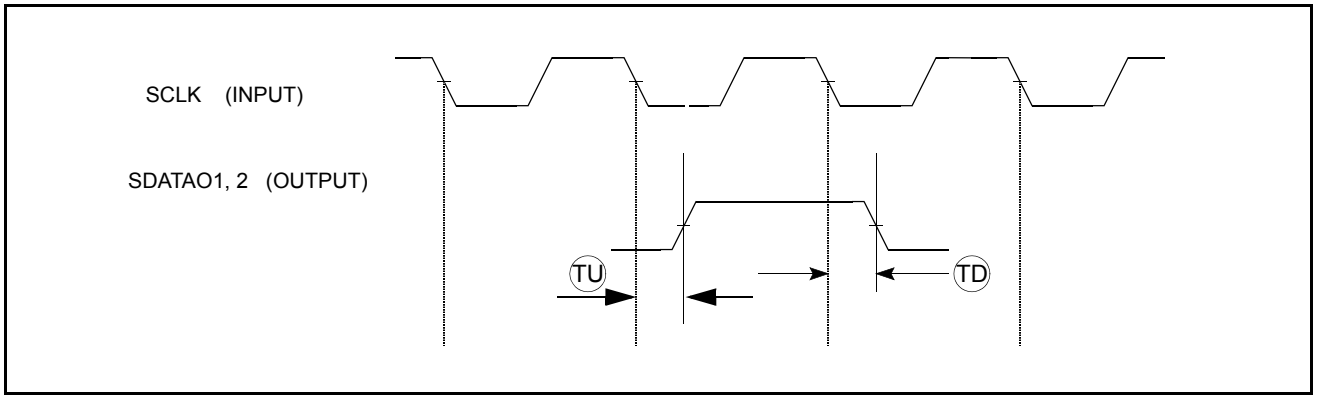


**Figure 17. SCLK Input, SDATA Output Timing**

**Table 32. SCLK OUTPUT, SDATA0 OUTPUT Timing Specifications**

| Name | Characteristic | | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| TU | SCLK fall to SDATAO rise | --- | 3 | ns |
| TD | SCLK fall to SDATAO fall | --- | 3 | ns |

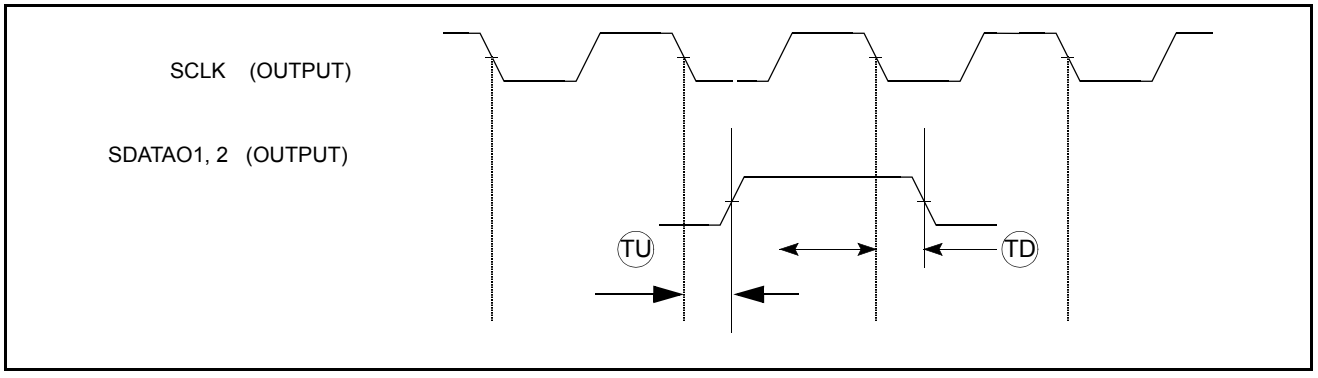


**Figure 18. SCLK Output, SDATAO Output Timing Diagram**

**Table 33. SCLK INPUT, SDATAI INPUT Timing Specifications**

| Name | Characteristic | | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| TSU | SDATAI IN to SCLKn | -5 | — | ns |
| TH | SCLK rise to SDATAI | 3 | — | ns |

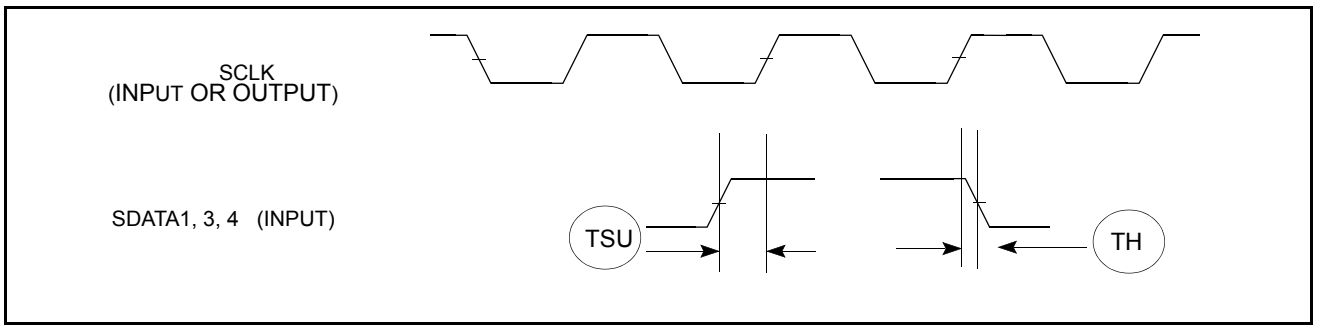


**Figure 19. SCLK Input/Output, SDATAI Input Timing Diagram**

# 10 Pin-Out and Package Information

## 10.1 Pinning Chart

**Table 34. 144 QFP Pin Assignments**

| 144 QFP Pin Number | Name | Type | Description |
|---|---|---|---|
| 01 | SCL/QSPI_CLK | I/O | IIC clock/QSPI clock pin function select is PLLCR(11) |
| 02 | CS0 | O | static chip select 0 |
| 03 | A21 | O | SDRAM address / static adr |
| 04 | A11 | O | SDRAM address / static adr |
| 05 | A10 | O | SDRAM address / static adr |
| 06 | A9 | O | SDRAM address / static adr |
| 07 | A18 | O | SDRAM address / static adr |
| 08 | A17 | O | SDRAM address / static adr |
| 09 | BCLK/GPIO10 | I/O | sdram clock output |

**Table 34. 144 QFP Pin Assignments (continued)**

| 144 QFP Pin Number | Name | Type | Description |
|---|---|---|---|
| 10 | SCLK_OUT/GPIO15 | I/O | MemoryStick/SD |
| 11 | BCLKE | O | sdram clock enable output |
| 12 | SDA/QSPI_DIN | I/O | IIC data/QSPI data in function select is PLLCR(11) |
| 13 | DATA24 | I/O | data |
| 14 | A22 | O | SDRAM address / static adr |
| 15 | SDUDQM | O | SDRAM UDQM |
| 16 | EF/GPIO19 | I/O | error flag input |
| 17 | DATA25 | I/O | data |
| 18 | DATA26 | I/O | data |
| 19 | DATA27 | I/O | data |
| 20 | PAD-GND | | PAD-GND |
| 21 | DATA28 | I/O | data |
| 22 | DATA29 | I/O | data |
| 23 | SDATA3/GPIO56 | I/O | SD interface data line |
| 24 | DATA30 | I/O | data |
| 25 | BUFENB1/GPIO57 | I/O | external buffer 1 enable |
| 26 | DATA31 | I/O | data |
| 27 | CORE-VDD | | CORE-VDD |
| 28 | A13 | O | SDRAM address / static adr |
| 29 | CORE-GND | | CORE-GND |
| 30 | A23 | O | SDRAM address / static adr |
| 31 | A14 | O | SDRAM address / static adr |
| 32 | A15 | O | SDRAM address / static adr |
| 33 | A16 | O | SDRAM address / static adr |
| 34 | PAD-VDD | | PAD-VDD |
| 35 | A19 | O | SDRAM address / static adr |

**Table 34. 144 QFP Pin Assignments (continued)**

| 144 QFP Pin Number | Name | Type | Description |
|---|---|---|---|
| 36 | A20 | O | SDRAM address / static adr |
| 37 | TEST2 | I | test |
| 38 | SDRAM-CS1 | O | SDRAM chip select out 1 |
| 39 | SDATA1_BS1/GPIO9 | I/O | Memory Stick / SD |
| 40 | SDRAS | O | SDRAM RAS |
| 41 | SDCAS | O | SDRAM CAS |
| 42 | SDWE | O | SDRAM write enable |
| 43 | SDLDQM | O | SDRAM LDQM |
| 44 | GPIO5 | I/O | GPIO5 |
| 45 | QSPI_CS0/GPIO29 | I/O | QSPI chip select 0 |
| 46 | QSPI_DOUT/GPIO26 | I/O | QSPI data out |
| 47 | GPIO6 | I/O | GPIO6 |
| 48 | DATA21 | I/O | data |
| 49 | DATA19 | I/O | data |
| 50 | QSPI_CS2/GPIO21 | I/O | QSPI chip select 2 |
| 51 | DATA20 | I/O | data |
| 52 | DATA22 | I/O | data |
| 53 | DATA18 | I/O | data |
| 54 | DATA23 | I/O | data |
| 55 | DATA17 | I/O | data |
| 56 | PADD-VDD | | PAD-VDD |
| 57 | DATA16 | I/O | data |
| 58 | CFLG/GPIO18 | I/O | CFLG input |
| 59 | EBUOUT1/GPO36 | O | audio interfaces EBU out 1 |
| 60 | CORE-GND | | CORE-GND |
| 61 | EBUIN3/ADIN0/GPI38 | I | audio interfaces EBU in 3 / AD convertor input0 |

**Table 34. 144 QFP Pin Assignments (continued)**

| 144 QFP Pin Number | Name | Type | Description |
|---|---|---|---|
| 62 | EBUIN2/GPI37 | I | audio interfaces EBU in 2 |
| 63 | CORE-VDD | | CORE-VDD |
| 64 | SCL2/GPIO3 | I/O | IIS2 clock line |
| 65 | RSTI | I | Reset |
| 66 | TOUT1/ADOUT/GPO35 | O | timer output 1 / AD output |
| 67 | LRCK2/GPIO44 | O | audio interfaces EBU out 1 |
| 68 | OE | O | Output Enable |
| 69 | SDA2/GPIO55 | I/O | IIS2 data |
| 70 | SDATAO2/GPO41 | O | audio interfaces serial data output 2 |
| 71 | SCLK2/GPIO48 | I/O | audio interfaces serial clock 2 |
| 72 | PAD-GND | | PAD-GND |
| 73 | TEST3 | I | test |
| 74 | SDATAO1/GPIO25 | I/O | audio interfaces serial data output 1 |
| 75 | LRCK1 | I/O | audio interfaces word clock 1 |
| 76 | LRCK4/GPIO46 | I/O | audio interfaces word clock 4 |
| 77 | SDATAI4/GPI42 | I | audio interfaces serial data in 4 |
| 78 | SCLK1 | I/O | audio interfaces serial clock 1 |
| 79 | SCLK4/GPIO50 | I/O | audio interfaces serial clock 4 |
| 80 | TA/GPIO20 | I/O | Transfer acknowledge |
| 81 | SDATAI1 | I | audio interfaces serial data in 1 |
| 82 | EBUIN1/GPI36 | I | audio interfaces EBU in 1 |
| 83 | PLLGRDVDD | | PLLGRDVDD |
| 84 | PLLGRDGND | | PLLGRDGND |
| 85 | PLLPADGND | | PLLPADGND |
| 86 | PLLPADVDD | | PLLPADVDD |
| 87 | PLLCOREGND | | PLLCOREGND |
| 88 | PLLCOREVDD | | PLLCOREVDD |

**Table 34. 144 QFP Pin Assignments (continued)**

| 144 QFP Pin Number | Name | Type | Description |
|---|---|---|---|
| 89 | IDE-DIOW/GPIO14 | I/O | ide diow |
| 90 | CRIN | I | crystal |
| 91 | IDE-DIOR/GPIO13 | I/O | ide dior |
| 92 | IDE-IORDY/GPIO16 | I/O | ide iordy |
| 93 | MCLK1/GPO39 | O | Audio master clock output 1 |
| 94 | MCLK2/GPO42 | O | Audio master clock output 2 |
| 95 | XTRIM/GPO38 | O | audio interfaces X-tal trim |
| 96 | TRST/DSCLK | I | Debug / interrupt monitor output 2 |
| 97 | CORE-VDD | | CORE-VDD |
| 98 | RW_B | O | Bus write enable |
| 99 | TMS/BKPT | I | JTAG/debug |
| 100 | CORE-GND | | CORE-GND |
| 101 | TCK | I | JTAG |
| 102 | PAD-GND | | PAD-GND |
| 103 | PST3/GPIO62 | I/O | debug |
| 104 | CNPSTCLK/GPO63 | O | debug |
| 105 | PST1/GPIO60 | I/O | debug |
| 106 | PAD-VDD | | PAD-VDD |
| 107 | PST2/GPIO61 | I/O | debug |
| 108 | PST0/GPIO59 | I/O | debug |
| 109 | TDI/DSI | I | jtag/debug |
| 110 | TEST0 | I | test |
| 111 | TIN0/GPI33 | I | timer input 0 |
| 112 | HI-Z | I | jtag |
| 113 | DDATA3/GPIO4 | I/O | debug |
| 114 | TOUT0/GPO33 | O | timer output 0 |
| 115 | DDATA1/GPIO1 | I/O | debug |

**Table 34. 144 QFP Pin Assignments (continued)**

| 144 QFP Pin Number | Name | Type | Description |
|---|---|---|---|
| 116 | DDATA2/GPIO2 | I/O | debug |
| 117 | CTS2_B/ADIN3/GPI31 | I | second UART clear / AD input 3 |
| 118 | DDATA0/GPIO0 | I/O | debug |
| 119 | RXD2/GPI28/ADIN2 | I | second UART receive data input / AD input 2 |
| 120 | TDSO | O | JTAG/debug |
| 121 | RTS2_B/GPO31 | O | second UART request to send |
| 122 | SDATAI3/GPI41 | I | audio interfaces serial data input 3 |
| 123 | CTS1_B/GPI30 | I | first UART clear to send |
| 124 | TXD2/GPO28 | O | second UART transmit data output |
| 125 | RTS1_B/GPO30 | O | first UART request to send |
| 126 | EBUIN4/ADIN1/GPI39 | I | audio interfaces EBU input 4 / AD input 1 |
| 127 | TXD1/GPO27 | O | first UART transmit data output |
| 128 | 128 RXD1/GPI27 | I | first UART receive data input |
| 129 | CS1/GPIO58 | I/O | chip select 1 |
| 130 | CORE-GND | | CORE-GND |
| 131 | A1 | O | SDRAM address / static adr |
| 132 | TIN1/GPIO23 | I/O | Timer input 1 |
| 133 | A2 | O | address |
| 134 | A3 | O | address |
| 135 | PAD-GND | | PAD-GND |
| 136 | A4 | O | address |
| 137 | A6 | O | address |
| 138 | A5 | O | address |
| 139 | A8 | O | address |
| 140 | A7 | O | address |

**Table 34. 144 QFP Pin Assignments (continued)**

| 144 QFP Pin Number | Name | Type | Description |
|---|---|---|---|
| 141 | CORE-VDD | | CORE-VDD |
| 142 | A12 | O | address |
| 143 | TEST1 | I | test |
| 144 | PAD-VDD | | PAD-VDD |

## 10.2 Package

The SCF5249 is assembled in 144-pin QFP package. Thermal characteristics are not available at this time.

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