



**3.3V/5V 800MHz  
LVTT/LVCMOS-to-DIFFERENTIAL  
LVPECL TRANSLATOR**

**Precision Edge®  
SY89329V**

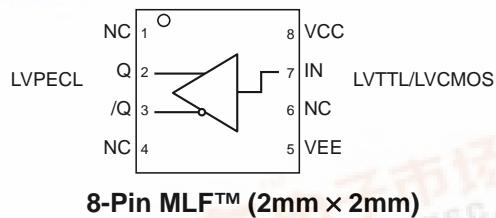
## FEATURES

- Guaranteed AC performance over temp and voltage:
  - DC-to-800MHz  $f_{MAX}$
  - <100ps IN-to-OUT  $t_{pd}$
- Ultra-low jitter design:
  - <1ps<sub>RMS</sub> random jitter
  - <10ps<sub>PP</sub> deterministic jitter
  - <1ps<sub>RMS</sub> cycle-to-cycle jitter
  - <1ps<sub>PP</sub> total jitter (clock)
- Differential LVPECL output
- $I_{CC}$  max. 20mA
- Q output will default HIGH with inputs open
- Power supply 3.3V  $\pm 10\%$  or 5.0V  $\pm 10\%$
- -40°C to +85°C temperature range
- Available in ultra-small 8-pin (2mm x 2mm) MLF™ package

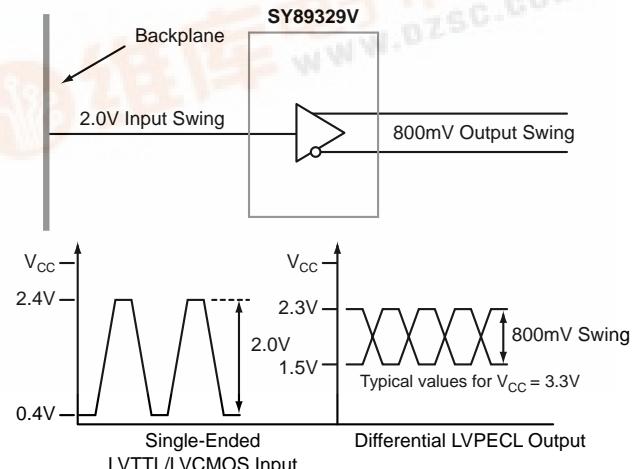
## APPLICATIONS

- High-speed logic
- Data communications systems
- Wireless communications systems
- Telecom systems

## FUNCTIONAL BLOCK DIAGRAM

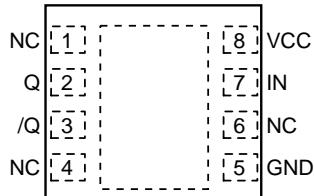


## TYPICAL APPLICATIONS CIRCUIT



## PACKAGE/ORDERING INFORMATION

## Ordering Information



Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89329VMITR	MLF-8	Industrial	329	Sn-Pb
SY89329VMGTR	MLF-8	Industrial	329 with Pb-Free bar-line indicator	Pb-Free NiPdAu

## PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
7	IN	Single-ended input: This is the LVTT/LVCMOS input to the device. Input switching threshold is $V_{CC}/2$ . If left floating, Q output will default HIGH.
8	VCC	Positive power supply. Bypass with $0.1\mu F \parallel 0.01\mu F$ low ESR capacitors.
2, 3	Q, /Q	Differential LVPECL output: This output is the output of the device. Terminate with $50\Omega$ to $V_{CC}-2V$ . See "Output Interface Applications" section. Defaults HIGH if IN is floating.
5	GND, Exposed Pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.
1, 4, 6	NC	No connect.

**Absolute Maximum Ratings<sup>(1)</sup>**

Supply Voltage ( $V_{CC}$ ) .....	-0.5V to + 4.0V
Input Voltage ( $V_{IN}$ ) .....	-0.5V to $V_{CC}$
LVPECL Output Voltage ( $V_{OUT}$ ) ....	$V_{CC}$ -1.0V to $V_{CC}$ +0.5V
LVPECL Output Current ( $I_{OUT}$ )	
Continuous .....	50mA
Surge .....	100mA
Input Current	
Source or sink current on IN .....	$\pm$ 50mA
Lead Temperature (soldering, 20 sec.) .....	+260°C
Storage Temperature ( $T_S$ ) .....	-65°C to +150°C

**Operating Ratings<sup>(2)</sup>**

Supply Voltage ( $V_{CC}$ ) .....	3.0V to 3.3V
	..... 4.5V to 5.5V
Ambient Temperature ( $T_A$ ) .....	-40°C to +85°C
Package Thermal Resistance <sup>(3)</sup>	
MLF™ ( $\theta_{JA}$ )	
Still-Air .....	93°C/W
500lfpm .....	87°C/W
MLF™ ( $\Psi_{JB}$ )	
Junction-to-board .....	32°C/W

**DC ELECTRICAL CHARACTERISTICS<sup>(4)</sup>**

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply		3.0	3.3	3.6	V
			4.5	5.0	5.5	V
$I_{CC}$	Power Supply Current	No load, max. $V_{CC}$ .			20	mA

**LVTT/LVCMOS ELECTRICAL CHARACTERISTICS<sup>(4)</sup>**

$T_A$  = -40°C to +85°C; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input HIGH Voltage (IN, /IN)		2.0			V
$V_{IL}$	Input LOW Voltage (IN, /IN)				0.8	V
$I_{IH}$	Input HIGH Current	$V_{IN}$ = 2.7V			20	$\mu$ A
		$V_{IN}$ = $V_{CC}$			100	$\mu$ A
$I_{IL}$	Input LOW Current	$V_{IN}$ = 0.5V			-0.2	mA
$V_{IK}$	Input Clamp Voltage	$I_{IN}$ = -18mA			-1.2	V

**LVPECL OUTPUTS DC ELECTRICAL CHARACTERISTICS<sup>(4)</sup>**

$V_{CC}$  = 3.3V  $\pm$ 10% or 5V  $\pm$ 10%;  $T_A$  = -40°C to +85°C;  $R_L$  = 50 $\Omega$  to  $V_{CC}$ -2V, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage Q, /Q	Note 2	$V_{CC}$ -1.080		$V_{CC}$ -0.880	V
$V_{OL}$	Output LOW Voltage Q, /Q		$V_{CC}$ -1.830		$V_{CC}$ -1.550	V
$V_{OUT}$	Output Voltage Swing Q, /Q	See Figure 1a.	600	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q, /Q	See Figure 1b.	1200	1600		mV

**Notes:**

1. Permanent device damage may occur if the "Absolute Maximum Ratings" are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.  $\Psi_{JB}$  uses 4-layer  $\theta_{JA}$  in still-air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## AC ELECTRICAL CHARACTERISTICS (5)

$V_{CC} = 3.3V \pm 10\%$  or  $5.0V \pm 10\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Operating Frequency	$V_{OUT} \geq 350mV$			800	MHz
$t_{pd}$	Propagation Delay IN-to-Q, /IN-to-/Q		100		600	ps
$t_{JITTER}$	Random Jitter (RJ)	<b>Note 6</b>			1	ps <sub>RMS</sub>
	Deterministic Jitter (DJ)	<b>Note 7</b>			10	ps <sub>PP</sub>
	Cycle-to-Cycle Jitter	<b>Note 8</b>			1	ps <sub>RMS</sub>
	Total Jitter (TJ)	<b>Note 9</b>			25	ps <sub>PP</sub>
$t_r, t_f$	Rise / Fall Time (20% to 80%) Q, /Q	At full output swing.	200		500	ps

## Notes:

- Measured with outputs loaded with  $50\Omega$  to  $V_{CC} - 2V$  unless otherwise stated. See "Timing Diagrams" section for definition of parameters. High-frequency AC-parameters are guaranteed by design and characterization.
- RJ is measured with a K28.7 comma detect character pattern, measured at  $f_{MAX}$ .
- DJ is measured at  $f_{MAX}$ , with both K28.5 and 2<sup>23</sup>-1 PRBS pattern
- Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles,  $T_n - T_{n-1}$  where T is the time between rising edges of the output signal.
- Total jitter definition: with an ideal clock input of frequency  $\leq f_{MAX}$ , no more than one output edge in  $10^{12}$  output edges will deviate by more than the specified peak-to-peak jitter value.

## SINGLE-ENDED AND DIFFERENTIAL SWING

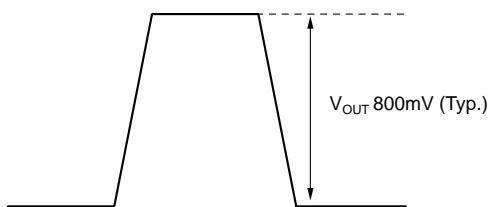


Figure 1a. Single-Ended Voltage Swing

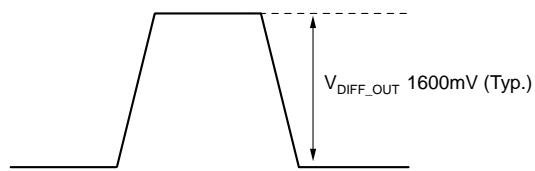


Figure 1b. Differential Voltage Swing

## TIMING DIAGRAM

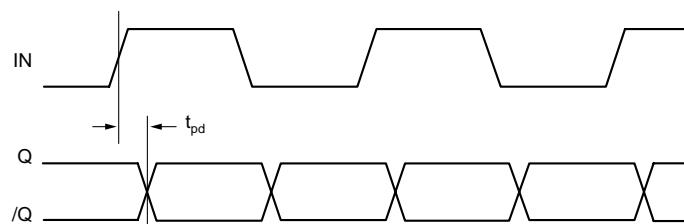


Figure 2. Timing Diagram

## OUTPUT INTERFACE APPLICATIONS

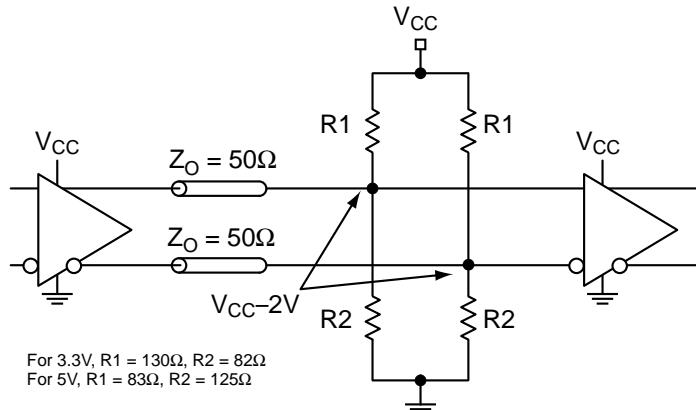


Figure 3a. Parallel Thevenin-Equivalent Termination

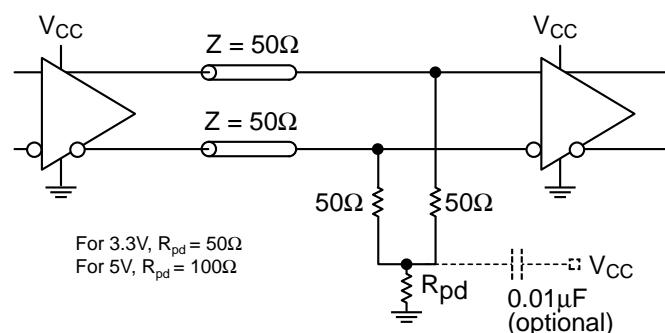


Figure 3b. Three-Resistor Termination

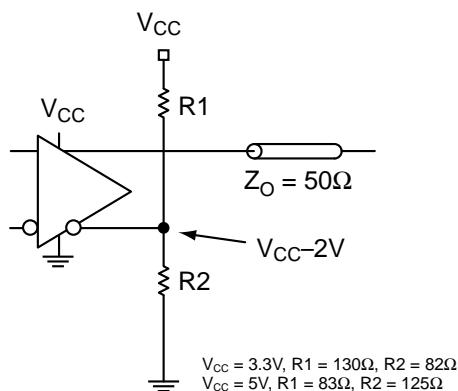
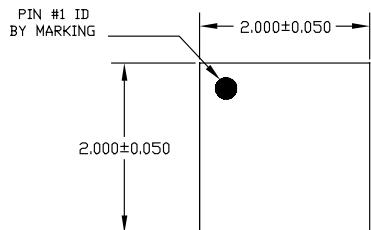


Figure 3c. Terminating Unused I/O

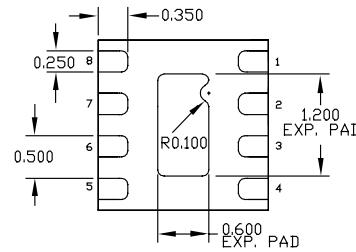
## RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY89322V	3.3V/5V Dual LV TTL/LV CMOS-to-Differential LVPECL Translator	<a href="http://www.micrel.com/product-info/products/sy89322v.shtml">www.micrel.com/product-info/products/sy89322v.shtml</a>
	MLF™ Application Note	<a href="http://www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf">www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf</a>
HBW Solutions	New Products and Applications	<a href="http://www.micrel.com/product-info/products/solutions.shtml">www.micrel.com/product-info/products/solutions.shtml</a>

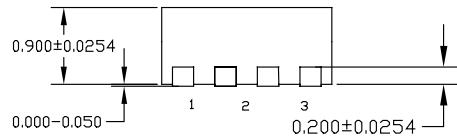
## 8 LEAD MicroLeadFrame (MLF-8)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

## NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

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**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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