MC1489, MC1489A表 8N55 189 C 5N 185 189 A 2 SN 7 5 189 A QUADRUPLE LINE RECEIVERS

SLLS095D - SEPTEMBER 1973 - REVISED OCTOBER 1998

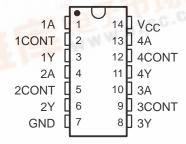
- Input Resistance . . . 3 k Ω to 7 k Ω
- Input Signal Range . . . ±30 V
- Operate From Single 5-V Supply
- **Built-In Input Hysteresis (Double** Thresholds)
- **Response Control that Provides:** Input Threshold Shifting **Input Noise Filtering**
- Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V.28
- Fully Interchangeable With Motorola™ MC1489 and MC1489A

description

These devices are monolithic low-power Schottky quadruple line receivers designed to satisfy the requirements of the standard interface between data-terminal equipment and data-communication equipment as defined by TIA/EIA-232-F. A separate response-control (CONT) terminal is provided for each receiver. A resistor or a resistor and bias-voltage source can be connected between this terminal and ground to shift the input threshold levels. An external capacitor can be connected between this terminal and ground to provide input noise filtering.

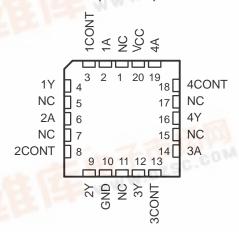
The SN55189 and SN55189A are characterized for operation over the full military temperature range of -55°C to 125°C. The MC1489, MC1489A, SN75189, and SN75189A are characterized for operation from 0°C to 70°C.

SN55189, SN55189A...JOR W PACKAGE MC1489, MC1489A, SN75189, SN75189A D, N, OR NST PACKAGE (TOP VIEW)



† The NS package is only available left-end taped and reeled. For SN75189, order SN75189NSR.

SN55189, SN55189A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection



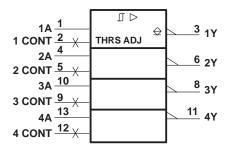
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





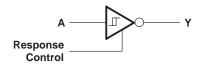
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logic symbol†

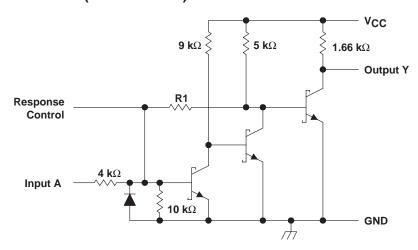


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, N, NS, and W packages.

logic diagram (positive logic)



schematic (each receiver)



	MC1489 SN55189 SN75189	MC1489A SN55189A SN75189A
R1	8.4 kΩ	1.84 kΩ

Resistor values shown are nominal.



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†
Supply voltage, V _{CC} (see Note 1)
Input voltage, V _I ±30 V
Output voltage, IO 20 mA
Continuous total power dissipation See Dissipation Rating Table
Operating free-air temperature range, T _A : SN55189, SN55189A
MC1489, MC1489A, SN75189, SN75189A 0°C to 70°C
Storage temperature range, T _{stg} –65°C to 150°C
Case temperature for 60 seconds, FK package
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or NS package

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	N/A
NS	625 mW	4.0 mW/°C	445 mW	N/A
W	1000 mW	8.0 mW/°C	640 mW	200 mW

[‡] In the J package, SN55189 and SN55189A chips are either silver glass or alloy mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	4.5	5	5.5	V
Input voltage, V _I	-25		25	V
High-level output current, IOH			-0.5	mA
Low-level output current, IOL			10	mA
Operating free-air temperature, TA	0		70	°C



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electrical characteristics over operating free-air temperature range, V_{CC} = 5 V \pm 1% (unless otherwise noted)

	PARAMETER		TEST CONDITIONS†			SN55189 SN55189A			MC1489, MC1489A SN75189 SN75189A			
				MIN	TYP‡	MAX	MIN	TYP‡	MAX			
				T _A = 25°C	1	1.3	1.5	1	1.3	1.5		
			'89	$T_A = 0$ °C to 70 °C				0.9		1.6		
V _{IT+}	Positive-going input	1		$T_A = -55^{\circ}C \text{ to } 125^{\circ}C$	0.6		1.9				V	
threshold voltage	'		T _A = 25°C	1.75	1.9	2.25	1.75	1.9	2.25	V		
			'89A	$T_A = 0$ °C to 70 °C				1.55		2.25		
				$T_A = -55^{\circ}C \text{ to } 125^{\circ}C$	1.30		2.65					
	Negative-going input threshold voltage			T _A = 25°C	0.75	1.0	1.25	0.75	1.0	1.25		
V_{IT-}		1	'89, '89A	$T_A = 0$ °C to 70 °C				0.65		1.25	V	
				$T_A = -55^{\circ}C$ to $125^{\circ}C$	0.35		1.6					
Vон	High-level	1	$V_I = 0.75 V$,	$I_{OH} = -0.5 \text{ mA}$	2.6	4	5	2.6	4	5	V	
VОН	output voltage	'	Input open,	$I_{OH} = -0.5 \text{ mA}$	2.6	4	5	2.6	4	5	V	
VOL	Low-level output voltage	1	V _I = 3 V,	$I_{OL} = 10 \text{ mA}$		0.2	0.45		0.2	0.45	٧	
1	High-level	2	V _I = 25 V		3.6		8.3	3.6		8.3	mA	
ΙΗ	input current		V _I = 3 V		0.43			0.43			IIIA	
1	Low-level	2	V _I = −25 V		-3.6		-8.3	-3.6		-8.3	mA	
¹IL	input current		V _I = −3 V		-0.43			-0.43			IIIA	
los	Short-circuit output current	3				-3			-3		mA	
ICC	Supply current	2	V _I = 5 V,	Outputs open		20	26		20	26	mA	

[†] All characteristics are measured with the response-control terminal open.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low- to high-level output		$R_L = 3.9 \text{ k}\Omega$		25	85	20
tPHL	Propagation delay time, high- to low-level output		R _L = 390 Ω		25	50	ns
tTLH	Transition time, low- to high-level output	4	$R_L = 3.9 \text{ k}\Omega$		120	175	no
tTHL	Transition time, high- to low-level output		R _L = 390 Ω		10	20	ns

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

PARAMETER MEASUREMENT INFORMATION[†]

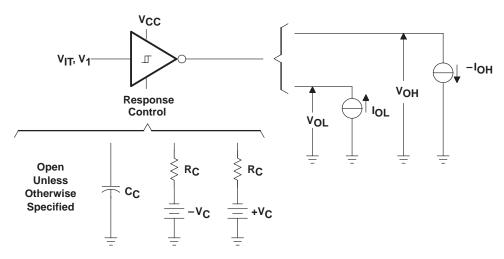
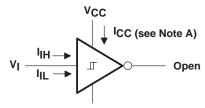


Figure 1. V_{IT+} , V_{IT-} , V_{OH} , V_{OL}



Response Control Open

NOTE A: ICC is tested for all four receivers simultaneously.

Figure 2. I_{IH} , I_{IL} , I_{CC}

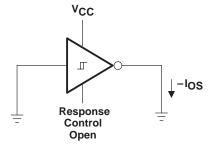


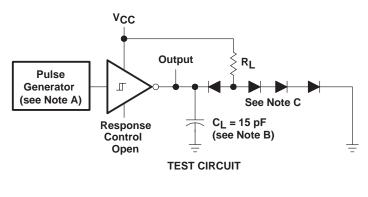
Figure 3. I_{OS}

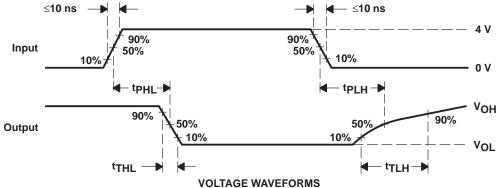


[†] Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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PARAMETER MEASUREMENT INFORMATION





NOTES: A. The pulse generator has the following characteristics: Z_{O} = 50 Ω , t_{W} = 500 ns.

- B. C_L includes probe and jig capacitances.
- C. All diodes are 1N3064 or equivalent.

Figure 4. Test Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

SN65189, SN75189 **OUTPUT VOLTAGE INPUT VOLTAGE**

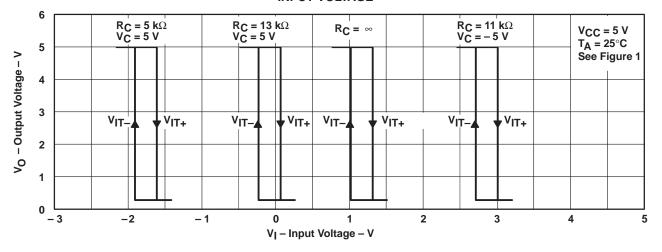


Figure 5

SN65189A, SN75189A **OUTPUT VOLTAGE** vs

INPUT VOLTAGE

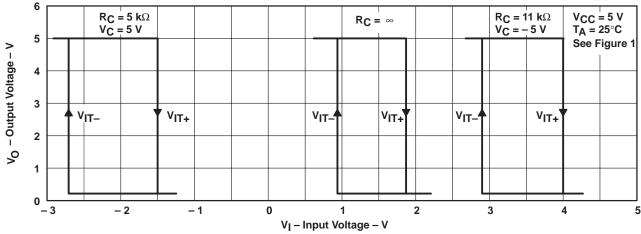


Figure 6

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TYPICAL CHARACTERISTICS[†]

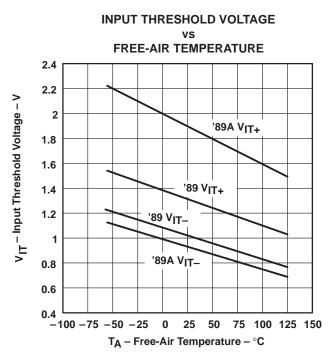
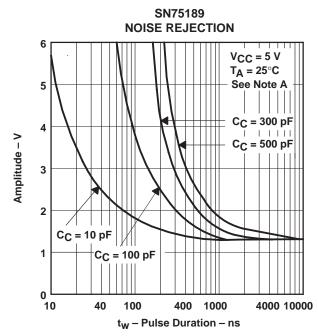


Figure 7



NOTE A: Maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

Figure 9

INPUT THRESHOLD VOLTAGE vs

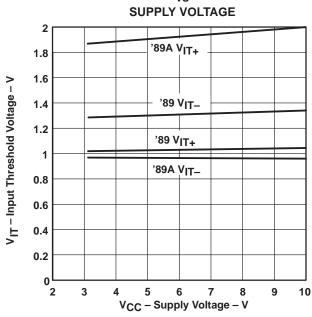
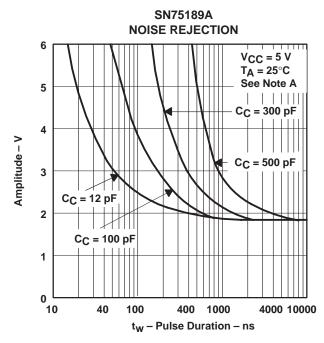


Figure 8



NOTE A: Maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

Figure 10

[†] Data for free-air temperatures below 0°C and above 70°C are applicable to SN55189 and SN55189A circuits only.



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TYPICAL CHARACTERISTICS

INPUT CURRENT vs

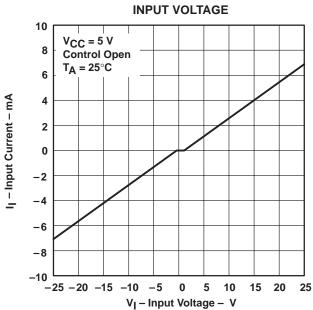


Figure 11

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9-Oct-2007

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp (3)
5962-86888022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8688802CA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8688802DA	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	N / A for Pkg Type
MC1489AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MC1489ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MC1489N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MC1489NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN55189AJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN55189J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN75189AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75189ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75189ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75189ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75189ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75189ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75189AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75189ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75189ANSLE	OBSOLETE	SO	NS	14		TBD	Call TI	Call TI
SN75189ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75189ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75189D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75189DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75189DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN75189DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN75189DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIN
SN75189DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75189N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type



PACKAGE OPTION ADDENDUM

9-Oct-2007

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75189NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75189NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75189NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75189NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ55189AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ55189AJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ55189AW	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ55189FK	OBSOLETE	LCCC	FK	20	•	TBD	Call TI	Call TI
SNJ55189J	OBSOLETE	CDIP	J	14	•	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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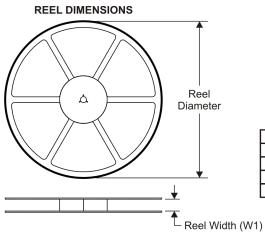
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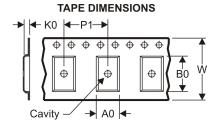


PACKAGE MATERIALS INFORMATION

11-Mar-2008

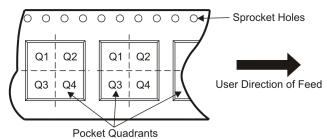
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



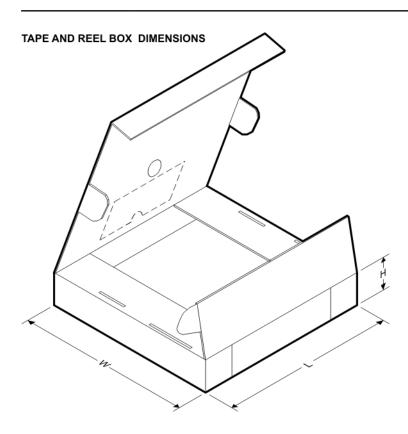
*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75189ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75189ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75189DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75189NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1





11-Mar-2008



*All dimensions are nominal

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	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
S	N75189ADR	SOIC	D	14	2500	346.0	346.0	33.0
SI	N75189ANSR	SO	NS	14	2000	346.0	346.0	33.0
9	SN75189DR	SOIC	D	14	2500	346.0	346.0	33.0
S	N75189NSR	SO	NS	14	2000	346.0	346.0	33.0

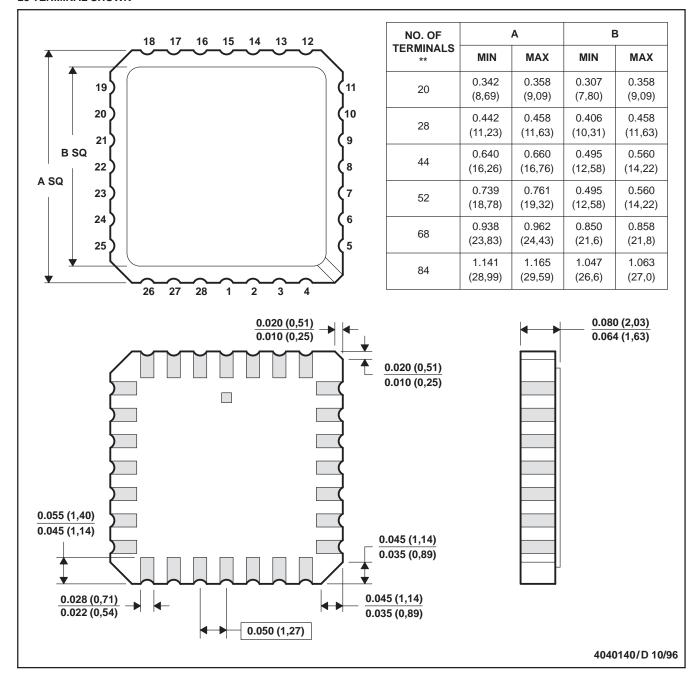


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

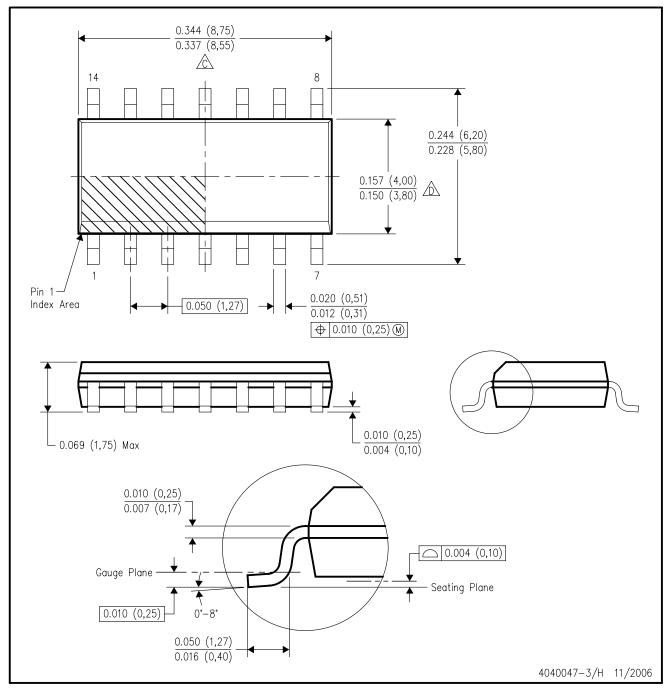


- . All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE

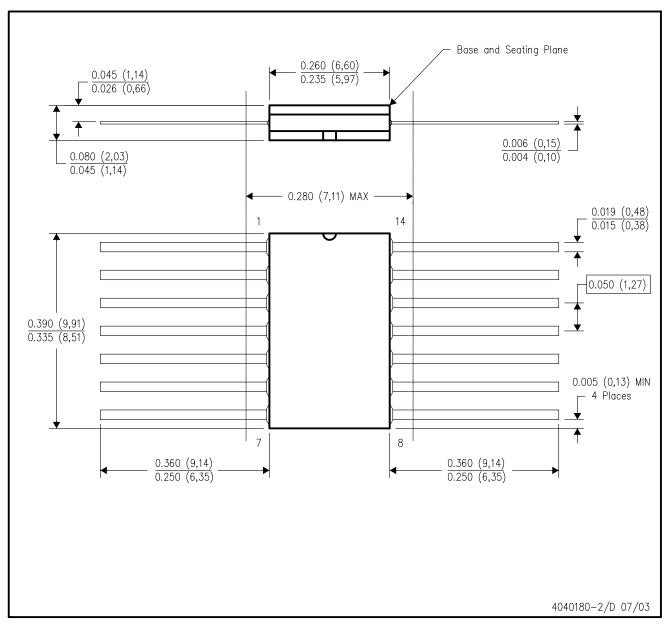


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AB.



W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



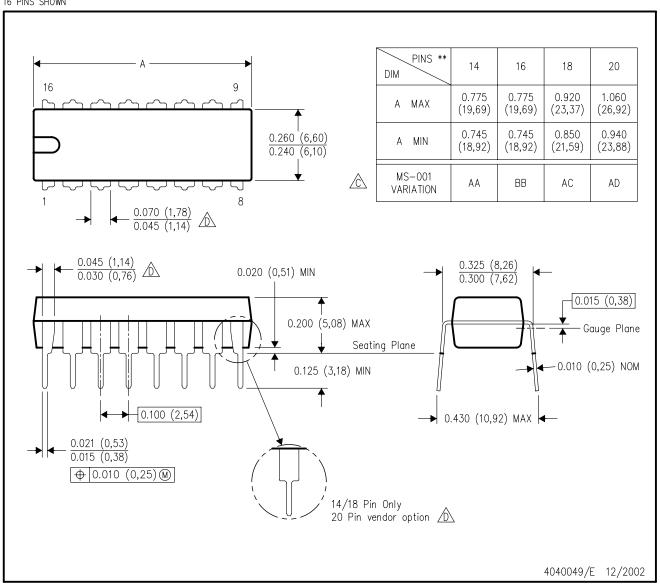
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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