NLAS44599

Low Voltage Single Supply Dual DPDT Analog Switch

The NLAS44599 is an advanced dual−independent CMOS double pole−double throw (DPDT) analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining CMOS low power dissipation. This DPDT controls analog and digital voltages that may vary across the full power−supply range (from V_{CC} to GND).

The device has been designed so the ON resistance (R_{ON}) is much lower and more linear over input voltage than R_{ON} of typical CMOS analog switches.

The channel select input is compatible with standard CMOS outputs.

The channel select input structure provides protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. This input structure helps prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

The NLAS44599 can also be used as a quad 2−to−1 multiplexer−demultiplexer analog switch with two Select pins that each controls two multiplexer−demultiplexers.
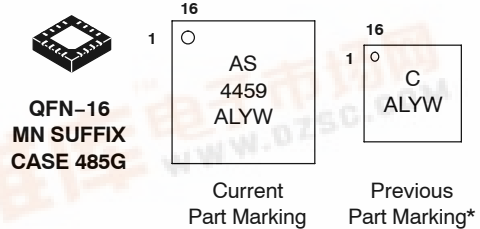
- Channel Select Input Over−Voltage Tolerant to 5.5 V
- Fast Switching and Propagation Speeds
- Break−Before−Make Circuitry
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- Diode Protection Provided on Channel Select Input
- Improved Linearity and Lower ON Resistance over Input Voltage
- Latch−up Performance Exceeds 300 mA
- ESD Performance: Human Body Model; > 2000 V, Machine Model; > 200 V
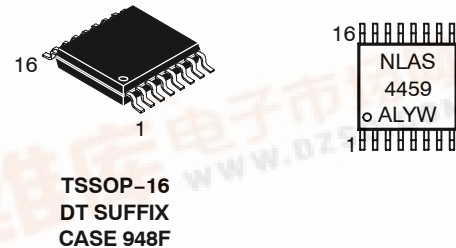- Chip Complexity: 158 FETs
- Pb−Free Packages are Available

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS

QFN−16
MN SUFFIX
CASE 485G

16
1
AS
4459
ALYW

Current
Part Marking

16
1
C
ALYW

Previous
Part Marking*

*Previous releases of this device may be marked as shown in this diagram.

TSSOP−16
DT SUFFIX
CASE 948F

16
NLAS
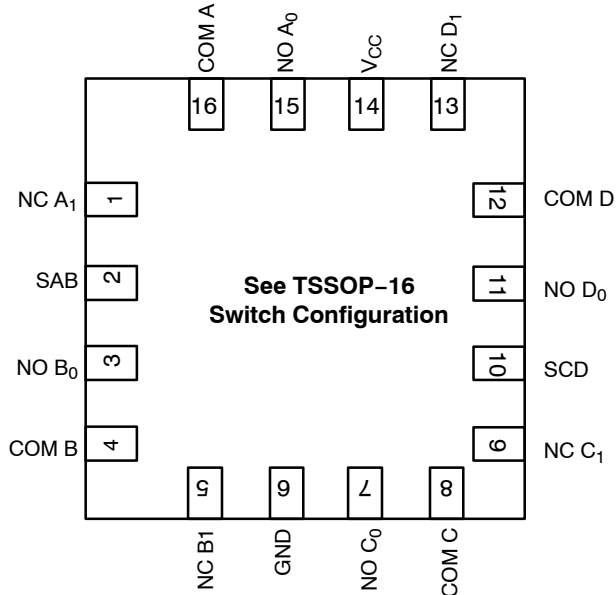4459
ALYW

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

1

Publication Order Number:

NLAS44599

QFN−16 PACKAGE

COM A   NO A_0 V_{CC} NC D_1

16   15   14   13

NC A_1 — 1

SAB — 2

NO B_0 — 3

COM B — 4

See TSSOP−16 Switch Configuration

12 — COM D

11 — NO D_0

10 — SCD

9 — NC C_1

5   6   7   8

NC B1   GND   NO C_0 COM C

FUNCTION TABLE

Select AB or CD	On Channel
L	NC to COM
H	NO to COM

TSSOP−16 PACKAGE

NO A_0	1	16	V_{CC}
COM A	2	15	NC D1
NC A_1	3	14	COM D
SELECT AB	4	13	NO D0
NO B_0	5	12	SELECT CD
COM B	6	11	NC C_1
NC B_1	7	10	COM C
GND	8	9	NO C_0

Figure 1. Logic Diagram

SELECT AB — X1   0 — NO A_0

COM A — 0/1   1 — NC A_1

   2 — NO B_0

COM B — 2/3   3 — NC B_1

SELECT CD — X1   0 — NO C_0

COM C — 0/1   1 — NC C_1

   2 — NO D_0

COM D — 2/3   3 — NC D_1
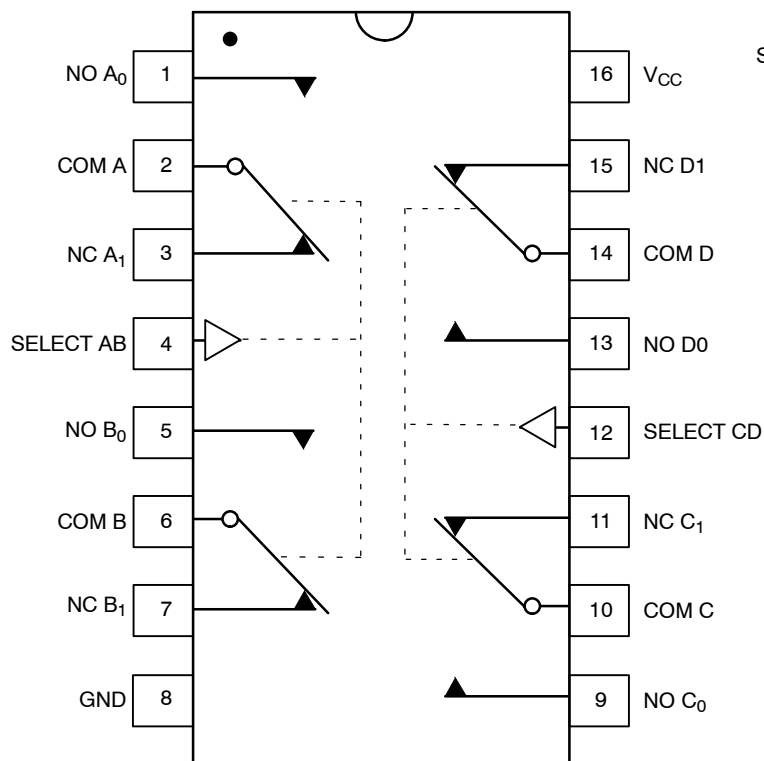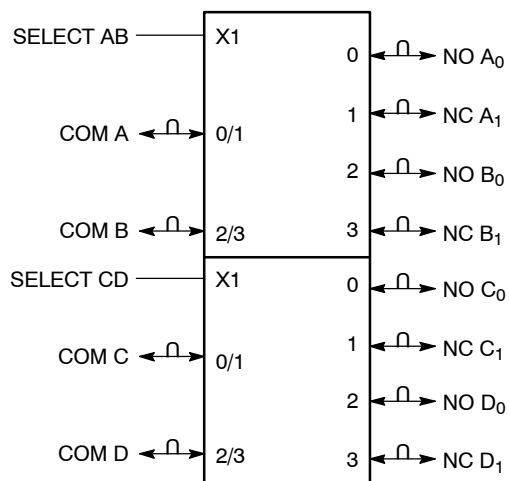
Figure 2. IEC Logic Symbol

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		-0.5 to $+7.0$	V
V_{IS}	Analog Input Voltage (V_{NO} or V_{COM})		$-0.5 \leq V_{IS} \leq V_{CC} +0.5$	
V_{IN}	Digital Select Input Voltage		$-0.5 \leq V_I \leq +7.0$	V
I_{IK}	DC Current, Into or Out of Any Pin		± 50	mA
P_D	Power Dissipation in Still Air	QFN–16	800	mW
		TSSOP–16	450	
T_{STG}	Storage Temperature Range		-65 to $+150$	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		$+150$	°C
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% – 35%	UL 94–V0 (0.125 in)	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1)	2000	V
		Machine Model (Note 2)	200	
		Charged Device Model (Note 3)	1000	
$I_{Latch-Up}$	Latch–Up Performance	Above V_{CC} and Below GND at 125°C (Note 4)	± 300	mA
θ_{JA}	Thermal Resistance	QFN–16	80	°C/W
		TSSOP–16	164	

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
1. Tested to EIA/JESD22–A114–A.
2. Tested to EIA/JESD22–A115–A.
3. Tested to JESD22–C101–A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	Digital Select Input Voltage		GND	5.5	V
V_{IS}	Analog Input Voltage (NC, NO, COM)		GND	V_{CC}	V
T_A	Operating Temperature Range		-55	$+125$	°C
t_r, t_f	Input Rise or Fall Time, SELECT	$V_{CC} = 3.3$ V $\pm$ 0.3 V	0	100	ns/V
		$V_{CC} = 5.0$ V $\pm$ 0.5 V	0	20	

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

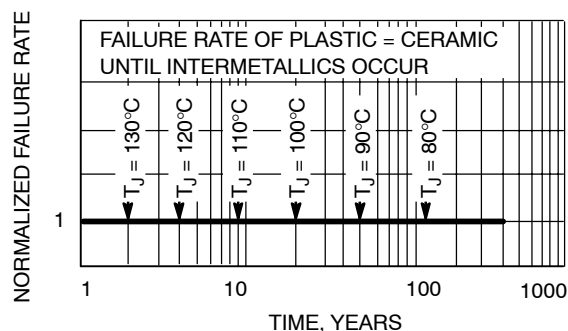| Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Figure 3. Failure Rate vs. Time Junction Temperature

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DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V$_{CC}$	Guaranteed Limit			Unit
				−55°C to 25°C	<85°C	<125°C	
V$_{IH}$	Minimum High–Level Input Voltage, Select Inputs		2.0	1.5	1.5	1.5	V
			2.5	1.9	1.9	1.9	
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			5.5	3.85	3.85	3.85	
V$_{IL}$	Maximum Low–Level Input Voltage, Select Inputs		2.0	0.5	0.5	0.5	V
			2.5	0.6	0.6	0.6	
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			5.5	1.65	1.65	1.65	
I$_{IN}$	Maximum Input Leakage Current	V$_{IN}$ = 5.5 V or GND	5.5	±0.2	±2.0	±2.0	µA
I$_{OFF}$	Power Off Leakage Current, Select Inputs	V$_{IN}$ = 5.5 V or GND	0	±10	±10	±10	µA
I$_{CC}$	Maximum Quiescent Supply Current	Select and V$_{IS}$ = V$_{CC}$ or GND	5.5	4.0	4.0	8.0	µA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Condition	V$_{CC}$	Guaranteed Limit			Unit
				−55°C to 25°C	<85°C	<125°C	
R$_{ON}$	Maximum "ON" Resistance (Figures 17 – 23)	V$_{IN}$ = V$_{IL}$ or V$_{IH}$ V$_{IS}$ = GND to V$_{CC}$ I$_{IN}$I ≤ 10.0 mA	2.5	85	95	105	Ω
			3.0	45	50	55	
			4.5	30	35	40	
			5.5	25	30	35	
R$_{FLAT\,(ON)}$	ON Resistance Flatness (Figures 17 – 23)	V$_{IN}$ = V$_{IL}$ or V$_{IH}$ I$_{IN}$I ≤ 10.0 mA V$_{IS}$ = 1 V, 2 V, 3.5 V	4.5	4	4	5	Ω
I$_{NC(OFF)}$ I$_{NO(OFF)}$	NO or NC Off Leakage Current (Figure 9)	V$_{IN}$ = V$_{IL}$ or V$_{IH}$ V$_{NO}$ or V$_{NC}$ = 1.0 V$_{COM}$ 4.5 V	5.5	1	10	100	nA
I$_{COM(ON)}$	COM ON Leakage Current (Figure 9)	V$_{IN}$ = V$_{IL}$ or V$_{IH}$ V$_{NO}$ 1.0 V or 4.5 V with V$_{NC}$ floating or V$_{NO}$ 1.0 V or 4.5 V with V$_{NO}$ floating V$_{COM}$ = 1.0 V or 4.5 V	5.5	1	10	100	nA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	V_{CC} (V)	V_{IS} (V)	Guaranteed Maximum Limit							Unit
					$-55°C$ to $25°C$			$<85°C$		$<125°C$		
					Min	Typ*	Max	Min	Max	Min	Max	
t_{ON}	Turn–On Time (Figures 12 and 13)	$R_L = 300\,\Omega$, $C_L = 35$ pF (Figures 5 and 6)	2.5	2.0	5	23	35	5	38	5	41	ns
			3.0	2.0	5	16	24	5	27	5	30	
			4.5	3.0	2	11	16	2	19	2	22	
			5.5	3.0	2	9	14	2	17	2	20	
t_{OFF}	Turn–Off Time (Figures 12 and 13)	$R_L = 300\,\Omega$, $C_L = 35$ pF (Figures 5 and 6)	2.5	2.0	1	7	12	1	15	1	18	ns
			3.0	2.0	1	5	10	1	13	1	16	
			4.5	3.0	1	4	6	1	9	1	12	
			5.5	3.0	1	3	5	1	8	1	11	
t_{BBM}	Minimum Break–Before–Make Time	$V_{IS} = 3.0$ V (Figure 4) $R_L = 300\,\Omega$, $C_L = 35$ pF	2.5	2.0	1	12		1		1		ns
			3.0	2.0	1	11		1		1		
			4.5	3.0	1	6		1		1		
			5.5	3.0	1	5		1		1		

Symbol		Parameter	Typical @ 25, $V_{CC} = 5.0$ V	Unit
C_{IN}		Maximum Input Capacitance, Select Input	8	pF
C_{NO} or C_{NC}		Analog I/O (switch off)	10	
C_{COM}		Common I/O (switch off)	10	
$C_{(ON)}$		Feedthrough (switch on)	20	

*Typical Characteristics are at 25°C.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

| Symbol	Parameter	Condition	V_{CC} V	Typical 25°C	Unit
BW	Maximum On–Channel –3dB Bandwidth or Minimum Frequency Response (Figure 11)	$V_{IN} = 0$ dBm V_{IN} centered between V_{CC} and GND (Figure 7)	3.0 4.5 5.5	145 170 175	MHz
V_{ONL}	Maximum Feedthrough On Loss	$V_{IN} = 0$ dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 7)	3.0 4.5 5.5	–3 –3 –3	dB
V_{ISO}	Off–Channel Isolation (Figure 10)	f = 100 kHz; $V_{IS} = 1$ V RMS V_{IN} centered between V_{CC} and GND (Figure 7)	3.0 4.5 5.5	–93 –93 –93	dB
Q	Charge Injection Select Input to Common I/O (Figure 15)	$V_{IN} = V_{CC}$ to GND, $F_{IS} = 20$ kHz $t_r = t_f = 3$ ns $R_{IS} = 0\,\Omega$, $C_L = 1000$ pF $Q = C_L * \Delta V_{OUT}$ (Figure 8)	3.0 5.5	1.5 3.0	pC
THD	Total Harmonic Distortion THD + Noise (Figure 14)	$F_{IS} = 20$ Hz to 100 kHz, $R_L = R_{gen} = 600\,\Omega$, $C_L = 50$ pF $V_{IS} = 5.0$ V_{PP} sine wave	5.5	0.1	%
VCT	Channel–to–Channel Crosstalk	f = 100 kHz; $V_{IS} = 1$ V RMS V_{IN} centered between V_{CC} and GND (Figure 7)	5.5 3.0	–90 –90	dB
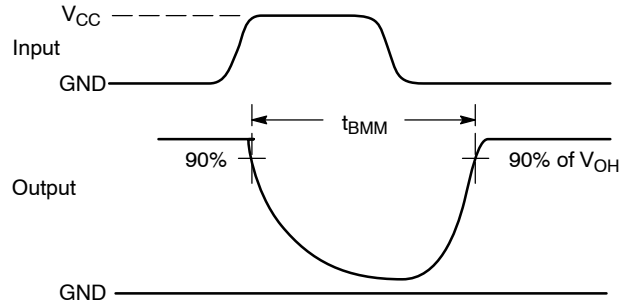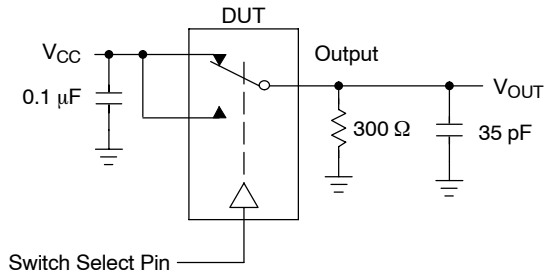
NLAS44599
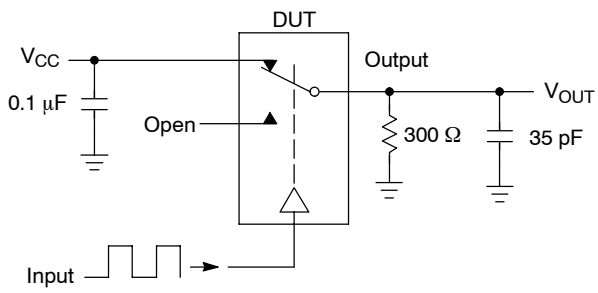

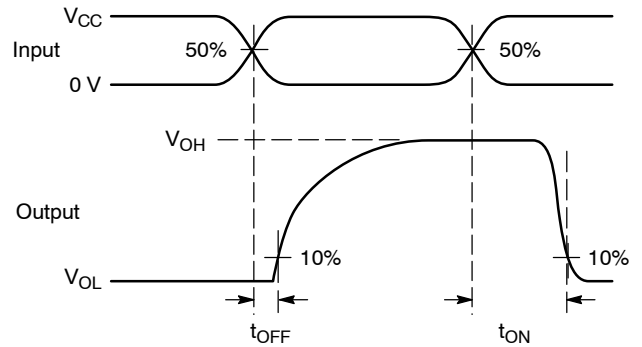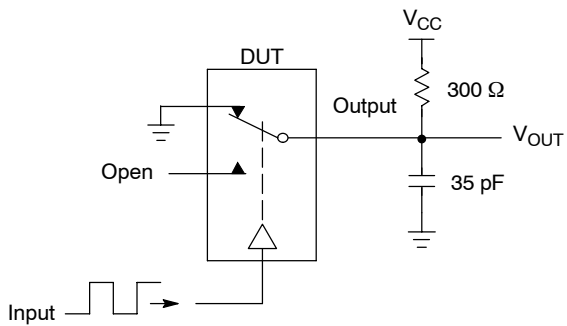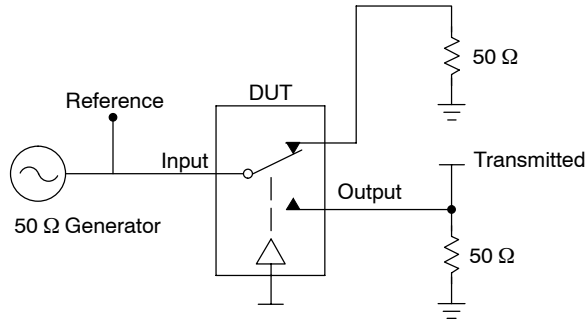**Figure 4. t_{BBM} (Time Break−Before−Make)**
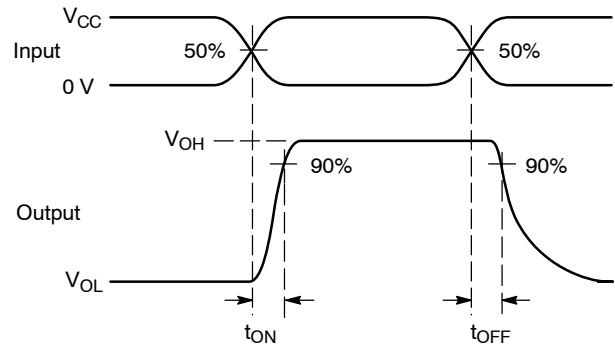
Figure 5. t_{ON}/t_{OFF}

Figure 6. t_{ON}/t_{OFF}

Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO}, Bandwidth and V_{ONL} are independent of the input signal direction.
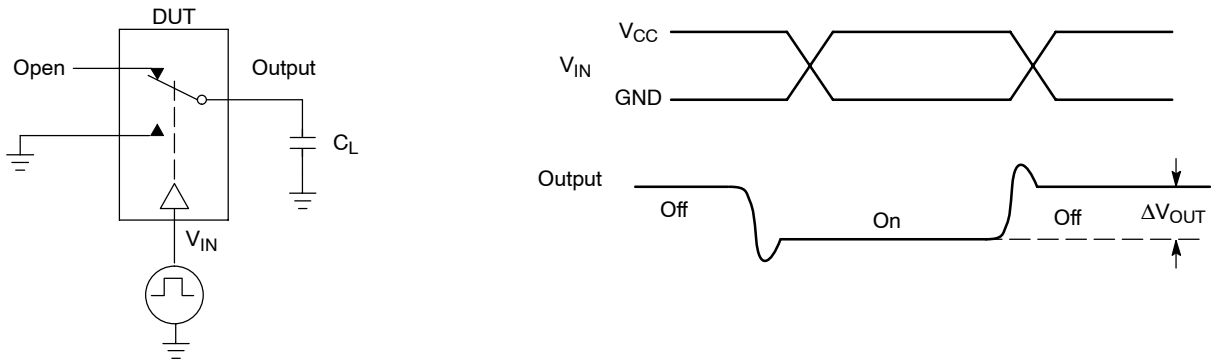
$$V_{ISO} = \text{Off Channel Isolation} = 20 \, \text{Log} \left(\frac{V_{OUT}}{V_{IN}}\right) \text{for } V_{IN} \text{ at 100 kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \, \text{Log} \left(\frac{V_{OUT}}{V_{IN}}\right) \text{for } V_{IN} \text{ at 100 kHz to 50 MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}
V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk
(On Channel to Off Channel)/V$_{ONL}$

Figure 8. Charge Injection: (Q)
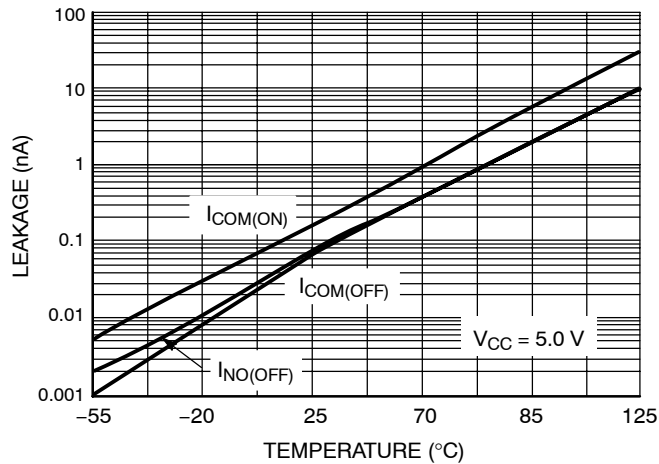
Figure 9. Switch Leakage vs. Temperature

NLAS44599
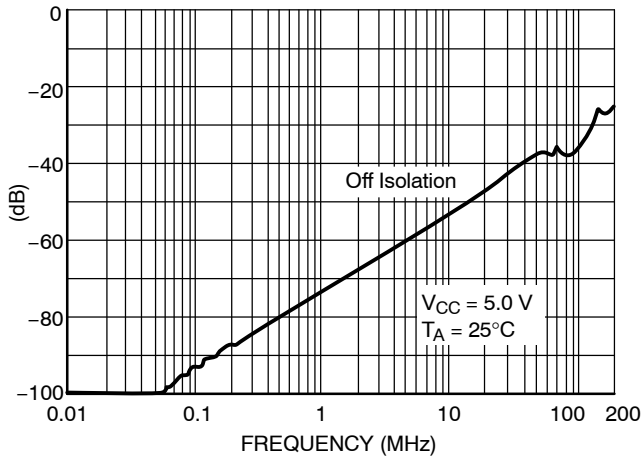
Figure 10. Off−Channel Isolation
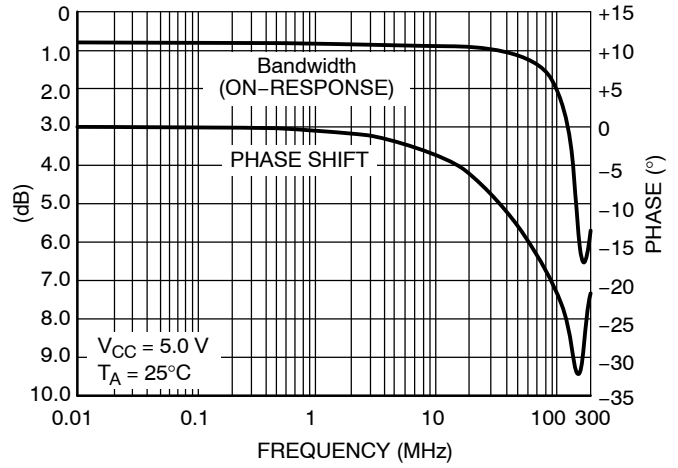
Figure 11. Typical Bandwidth and Phase Shift
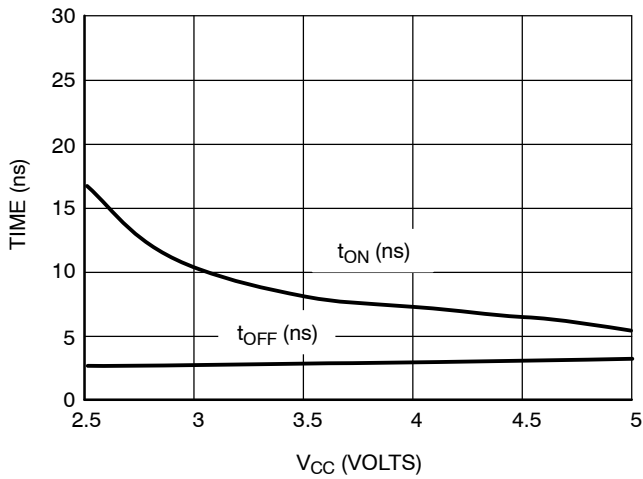
Figure 12. t_{ON} and t_{OFF} vs. V_{CC} at 25°C
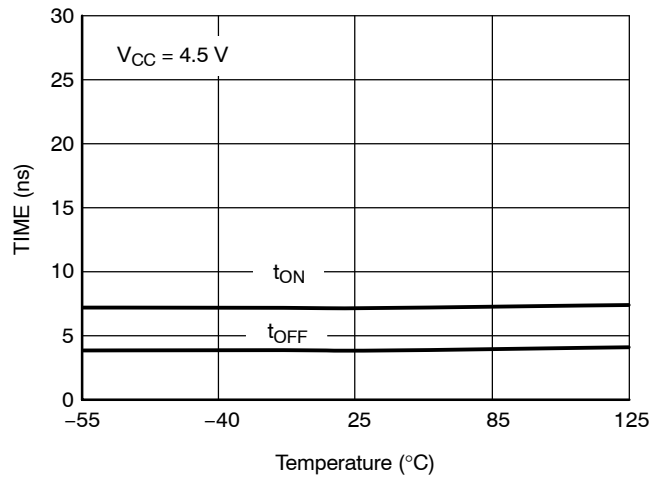
Figure 13. t_{ON} and t_{OFF} vs. Temp
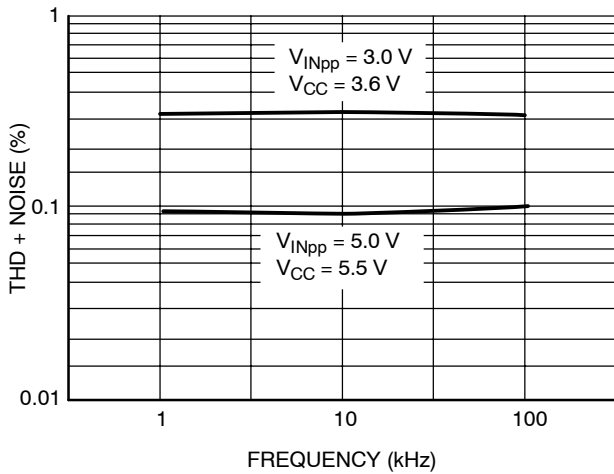
Figure 14. Total Harmonic Distortion
Plus Noise vs. Frequency
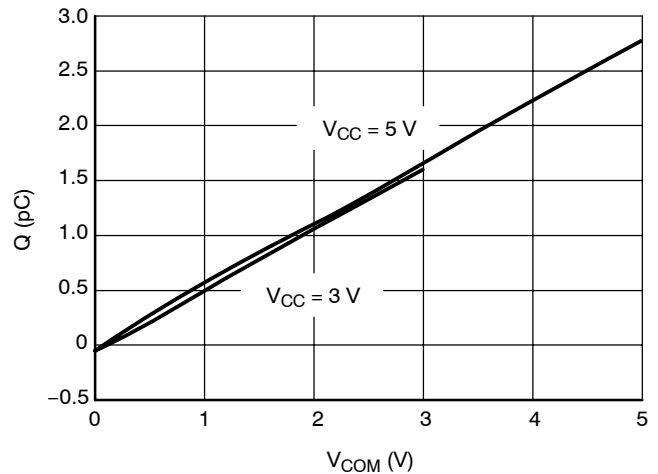
Figure 15. Charge Injection vs. COM Voltage

NLAS44599
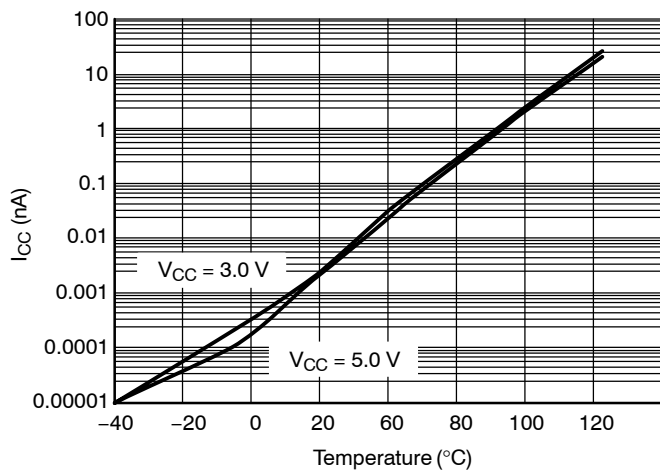
Figure 16. I_CC vs. Temp, V_CC = 3 V & 5 V
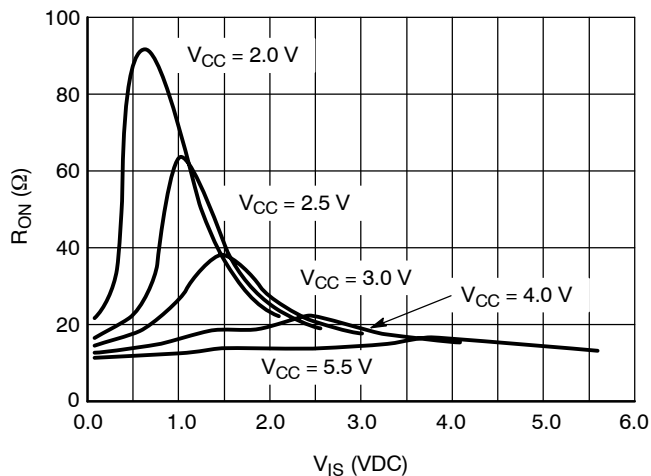
Figure 17. R_ON vs. V_CC, Temp = 25°C
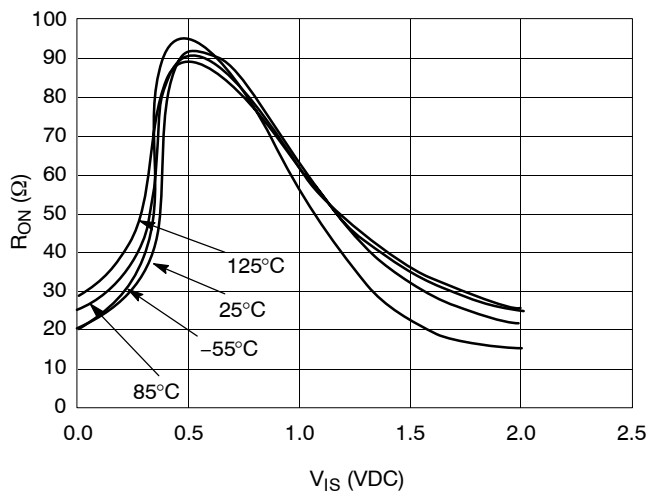
Figure 18. R_ON vs Temp, V_CC = 2.0 V
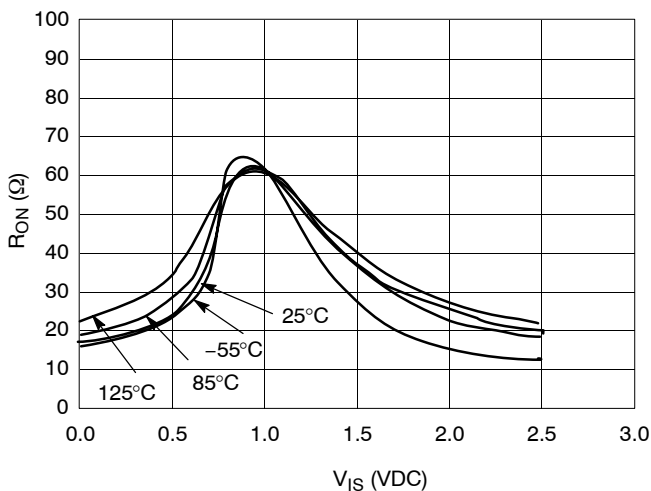
Figure 19. R_ON vs. Temp, V_CC = 2.5 V
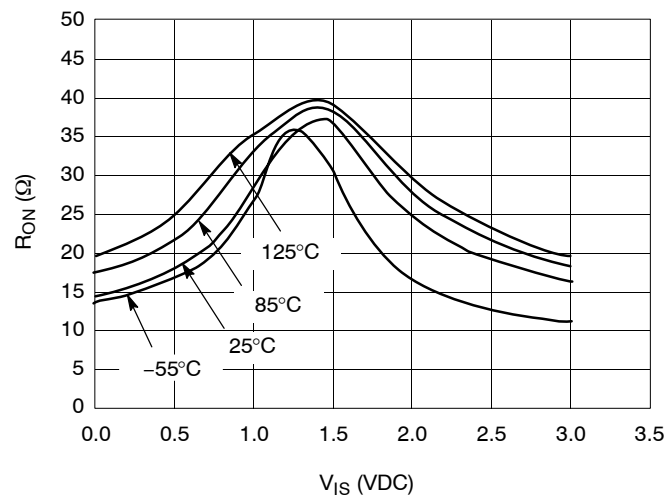
Figure 20. R_ON vs. Temp, V_CC = 3.0 V
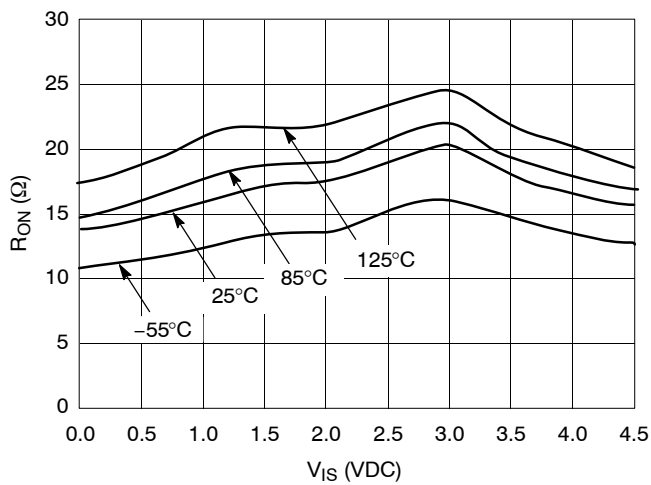
Figure 21. R_ON vs. Temp, V_CC = 4.5 V

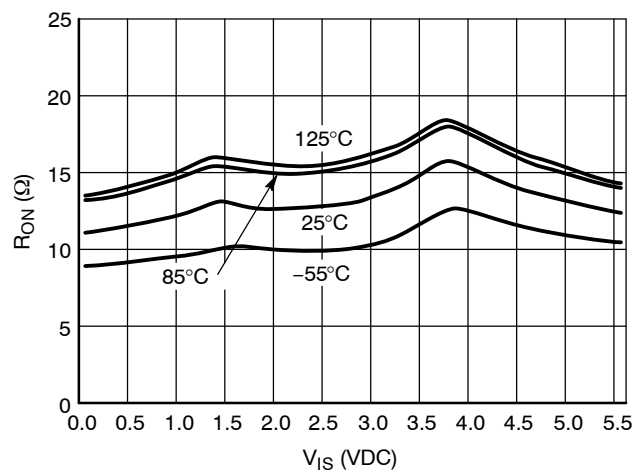# NLAS44599
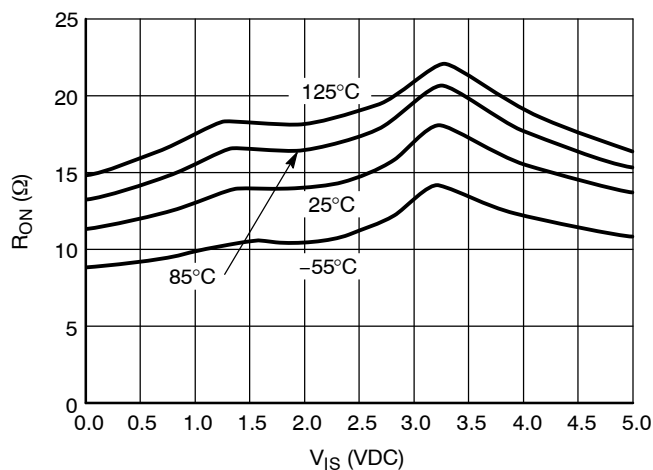
Figure 22. R_{ON} vs. Temp, V_{CC} = 5.0 V

Figure 23. R_{ON} vs. Temp, V_{CC} = 5.5 V

DEVICE ORDERING INFORMATION

| Device | Device Nomenclature | | | | | Package Type | Shipping[†] |
	Circuit Indicator	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
NLAS44599DT	NL	AS	44599	DT		TSSOP−16*	96 / Unit Rail
NLAS44599DTR2	NL	AS	44599	DT	R2	TSSOP−16*	2500 / Tape & Reel
NLAS44599MN	NL	AS	44599	MN		QFN−16	124 Unit / Rail
NLAS44599MNG	NL	AS	44599	MN		QFN−16 (Pb−Free)	124 Unit / Rail
NLAS44599MNR2	NL	AS	44599	MN	R2	QFN−16	2500 / Tape & Reel
NLAS44599MNR2G	NL	AS	44599	MN	R2	QFN−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

NLAS44599

PACKAGE DIMENSIONS
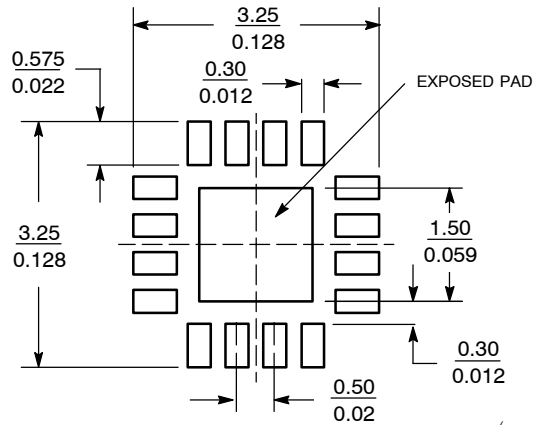
QFN−16
MN SUFFIX
CASE 485G−01
ISSUE B
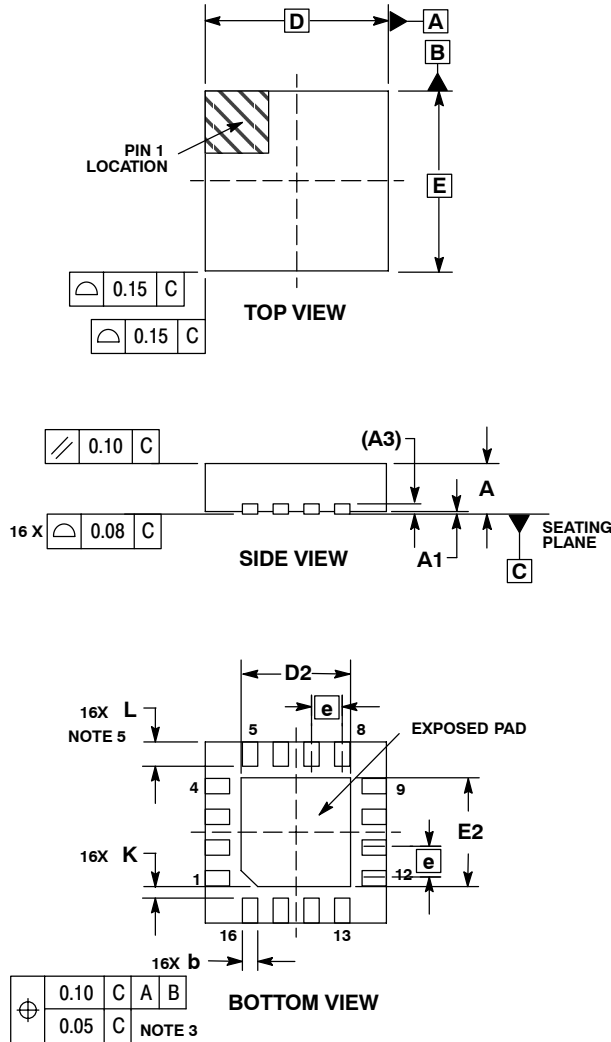
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

TOP VIEW

PIN 1 LOCATION

| △ | 0.15 | C |
| △ | 0.15 | C |

SIDE VIEW

(A3)
A
A1
SEATING PLANE
C

| // | 0.10 | C |
| 16 X △ | 0.08 | C |

BOTTOM VIEW

D2
16X L NOTE 5
16X K
e
E2
16X b
5 8
4 9
1 12
16 13
EXPOSED PAD

| ⊕ | 0.10 | C | A | B |
| | 0.05 | C | NOTE 3 |

SOLDERING FOOTPRINT

$\dfrac{3.25}{0.128}$

$\dfrac{0.575}{0.022}$

$\dfrac{0.30}{0.012}$

EXPOSED PAD

$\dfrac{3.25}{0.128}$

$\dfrac{1.50}{0.059}$

$\dfrac{0.50}{0.02}$

$\dfrac{0.30}{0.012}$

SCALE 10:1 $\left(\dfrac{mm}{inches}\right)$

NLAS44599

PACKAGE DIMENSIONS

TSSOP–16
CASE 948F–01
ISSUE A

16X **K** REF

⊕ | 0.10 (0.004) Ⓜ | T | U Ⓢ | V Ⓢ

△ | 0.15 (0.006) | T | U Ⓢ

2X **L/2**

16   9
B
–U–

PIN 1
IDENT.

1   8

△ | 0.15 (0.006) | T | U Ⓢ

A
–V–

L

K
K1

J1

J

SECTION N–N

N

0.25 (0.010)

M

N

F

DETAIL E

C

△ | 0.10 (0.004)

–T– SEATING
PLANE

D   **G**   **H**

DETAIL E

–W–
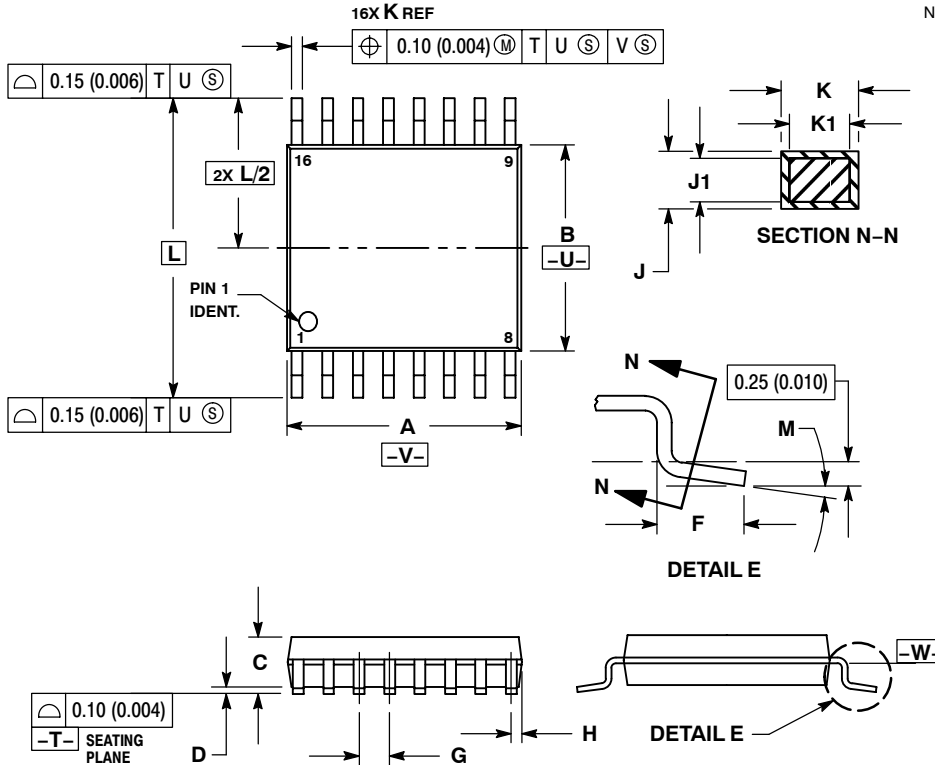
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °