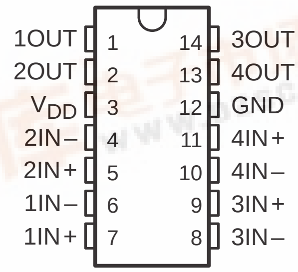
LinCMOS™ MICROPOWER QUAD COMPARATORS

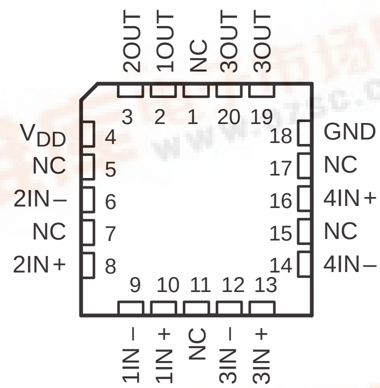
SLCS119 – DECEMBER 1986 – REVISED JANUARY 1991

- **Very Low Power . . . 200 µW Typ at 5 V**
- **Fast Response Time . . . 2.5 µs Typ With 5-mV Overdrive**
- **Single Supply Operation:**
  - **TLC139M . . . 4 V to 16 V**
  - **TLC339M . . . 4 V to 16 V**
  - **TLC339C . . . 3 V to 16 V**
  - **TLC339I . . . 3 V to 16 V**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Input Offset Voltage Change at Worst Case Input at Condition Typically 0.23 µV/Month Including the First 30 Days**
- **On-Chip ESD Protection**

D, J OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



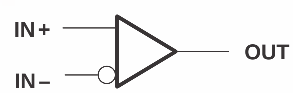
NC – No internal connection

description

The TLC139/TLC339 consists of four independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM139/LM339 family but uses 1/20th the power for similar response times. The open-drain MOS output stage interfaces to a variety of leads and supplies, as well as wired logic functions. For a similar device with a push-pull output configuration, see the TLC3704 data sheet.

The Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

symbol (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC339CD	—	—	TLC339CN
–40°C to 85°C	5 mV	TLC339ID	—	—	TLC339IN
–40°C to 125°C	5 mV	TLC339QD	—	—	TLC339QN
–55°C to 125°C	5 mV	TLC339MD	TLC139MFK	TLC139MJ	TLC339MN

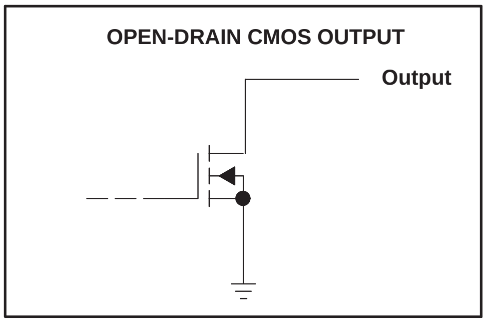
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC339CDR).

LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

The TLC139M and TLC339M are characterized for operation over the full military temperature range of –55°C to 125°C. The TLC339C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC339I is characterized for operation over the industrial temperature range of –40°C to 85°C. The TLC339Q is characterized for operation over the extended industrial temperature range of –40°C to 125°C.

output schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . –0.3 V to 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . ±18 V
Input voltage range, V_I . . . . –0.3 V to V_{DD}
Output voltage range, V_O . . . . –0.3 V to V_{DD}
Input current, I_I . . . . ±5 mA
Output current, I_O (each output) . . . . 20 mA
Total supply current into V_{DD} . . . . 40 mA
Total current out of GND . . . . 60 mA
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: TLC139M . . . . –55°C to 125°C
TLC339C . . . . 0°C to 70°C
TLC339I . . . . –40°C to 85°C
TLC339M . . . . –55°C to 125°C
TLC339Q . . . . –40°C to 125°C
Storage temperature range . . . . –65°C to 150°C
Case temperature for 60 seconds: FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN –.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

	TLC139M, TLC339M			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD}-1.5$	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	–55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC139M, TLC339M			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 3	V_{DD} = 5 V to 10 V,	25°C		1.4	5	mV
				–55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				125°C			30	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			V
				–55°C to 125°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				125°C		84		
				–55°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				125°C		84		
				–55°C		84		
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 6 mA	25°C		300	400	mV
				125°C			800	
I_{OH}	High-level output current	V_{ID} = –1 V,	V_O = 5 V	25°C		0.8	40	nA
				125°C			1	µA
I_{DD}	Supply current (four comparators)	Outputs low,	No load	25°C		44	80	µA
				–55°C to 125°C			175	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

	TLC339C MIN	TLC339C NOM	TLC339C MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	–0.2		$V_{DD}-1.5$	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC339C MIN	TLC339C TYP	TLC339C MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 3	V_{DD} = 5 V to 10 V,	25°C		1.4	5	mV
				0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				70°C			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			V
				0°C to 70°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				70°C		84		
				0°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				70°C		85		
				0°C		85		
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 6 mA	25°C		300	400	mV
				70°C			650	
I_{OH}	High-level output current	V_{ID} = –1 V,	V_O = 5 V	25°C		0.8	40	nA
				70°C			1	µA
I_{DD}	Supply current (four comparators)	Outputs low,	No load	25°C		44	80	µA
				0°C to 70°C			100	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

	TLC339I			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	–0.2		V_{DD}–1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC339I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 3	V_{DD} = 5 V to 10 V,	25°C		1.4	5	mV
				–40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				85°C			2	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD}–1			V
				–40°C to 85°C	0 to V_{DD}–1.5			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C		84		dB
				85°C		84		
				–40°C		84		
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C		85		dB
				85°C		85		
				–40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 6 mA	25°C		300	400	mV
				85°C			700	
I_{OH}	High-level output current	V_{ID} = –1 V,	V_O = 5 V	25°C		0.8	40	nA
				85°C			1	µA
I_{DD}	Supply current (four comparators)	Outputs low,	No load	25°C		44	80	µA
				–40°C to 85°C			125	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

	TLC339Q MIN	TLC339Q NOM	TLC339Q MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD}-1.5$	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	– 40		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	TLC339Q MIN	TLC339Q TYP	TLC339Q MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 3	V_{DD} = 5 V to 10 V,	25°C		1.4	5	mV
				–40°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V		25°C		1		pA
				125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V		25°C		5		pA
				125°C			30	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			V
				–40°C to 125°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min		25°C	84			dB
				125°C	84			
				–40°C	84			
k_{SVR}	Supply-voltage rejection ratio	V_{DD} = 5 V to 10 V		25°C	85			dB
				125°C	84			
				–40°C	84			
V_{OL}	Low-level output voltage	V_{ID} = –1 V,	I_{OL} = 6 mA	25°C		300	400	mV
				125°C			800	
I_{OH}	High-level output current	V_{ID} = –1 V,	V_O = 5 V	25°C		0.8	40	nA
				125°C			1	µA
I_{DD}	Supply current (four comparators)	Outputs low,	No load	25°C		44	80	µA
				–40°C to 125°C			125	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

switching characteristics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

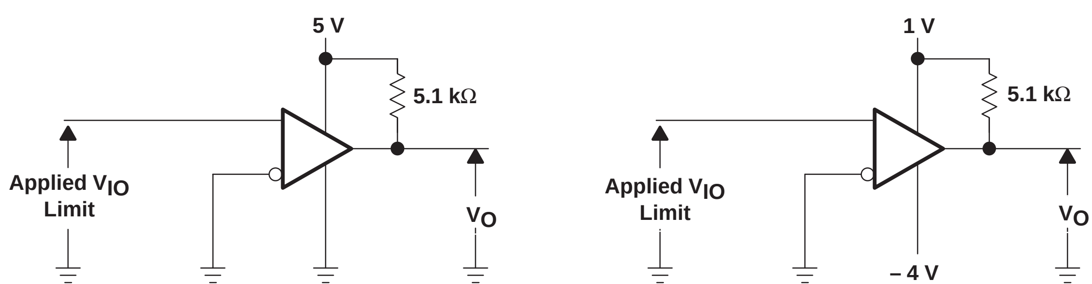
PARAMETER		TEST CONDITIONS		TLC139M, TLC339C TLC339I, TLC339M TLC339Q MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.5		
			Overdrive = 10 mV		1.7		
			Overdrive = 20 mV		1.2		
			Overdrive = 40 mV		1.0		
		V_I = 1.4 V step at IN+			1.1		
t_{PHL}	Propagation delay time, high-to-low level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		3.6		µs
			Overdrive = 5 mV		2.1		
			Overdrive = 10 mV		1.3		
			Overdrive = 20 mV		0.85		
			Overdrive = 40 mV		0.55		
		V_I = 1.4 V step at IN+			0.10		
t_{THL}	Transition time, high-to-low level output	f = 10 kHz, C_L = 15pF	Overdrive = 50 mV		20		ns

PARAMETER MEASUREMENT INFORMATION

The TLC139 and TLC339 contain a digital output stage that, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 V (b) V_{IO} WITH V_{IC} = 4 V

Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits

PARAMETER MEASUREMENT INFORMATION

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes state.

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

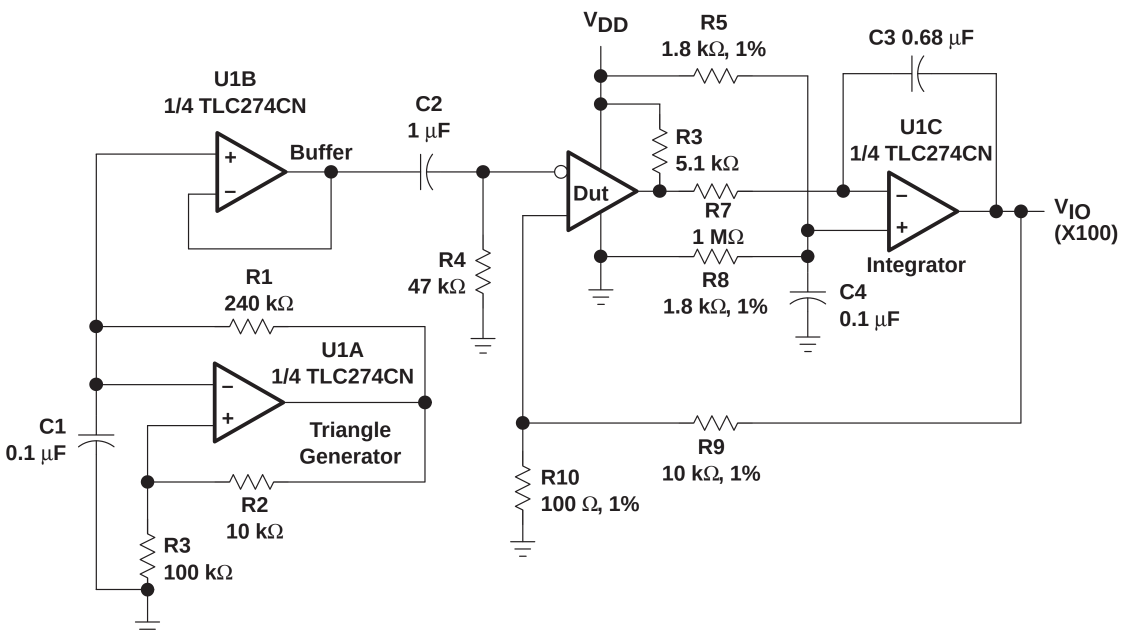
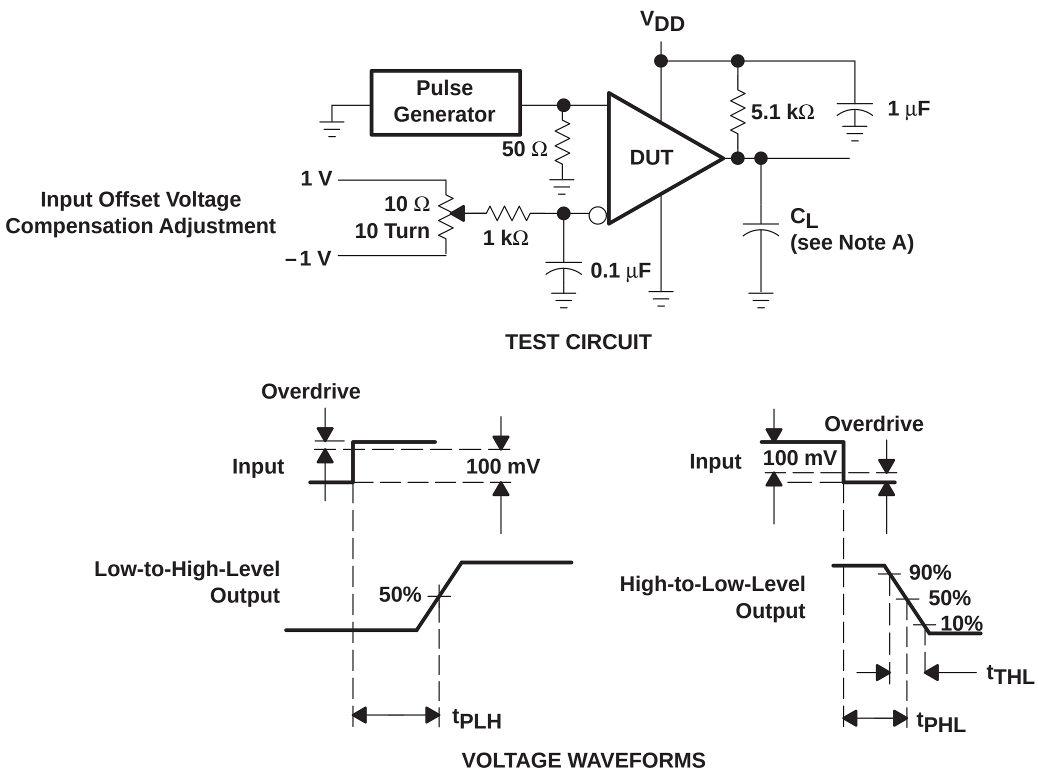


Figure 2. Circuit for Input Offset Voltage Measurement

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained, with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 3, so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.



NOTE A: C_L includes probe and jig capacitance.

Figure 3. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Free-air temperature	5
CMRR	Common-mode rejection ratio	vs Free-air temperature	6
k_{SVR}	Supply-voltage rejection ratio	vs Free-air temperature	7
I_{OH}	High-level output current	vs High-level output voltage vs Free-air temperature	8 9
V_{OL}	Low-level output voltage	vs Low-level output current vs Free-air temperature	10 11
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	12 13
t_{PLH}	Low-to-high level output propagation delay time	vs Supply voltage	14
t_{PHL}	Low-to-high level output propagation delay time	vs Supply voltage	15
	Overdrive voltage	vs Low-to-high-level output propagation delay time	16
t_f	Output fall time	vs Supply voltage	17
	Overdrive voltage	vs High-to-low-level output propagation delay time	18

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF INPUT OFFSET VOLTAGE

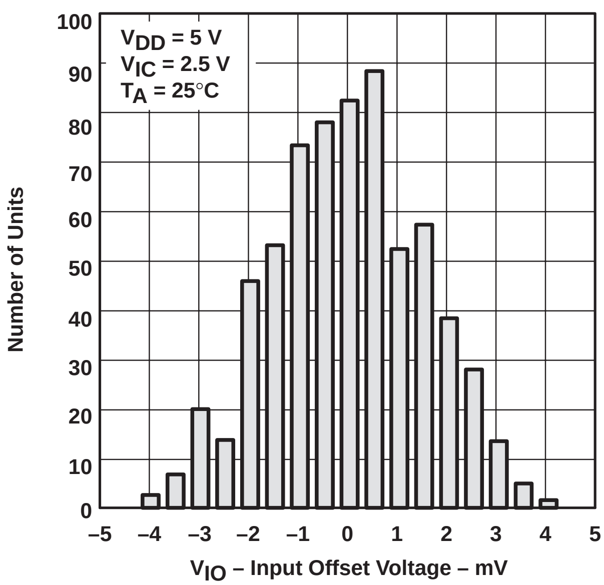


Figure 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

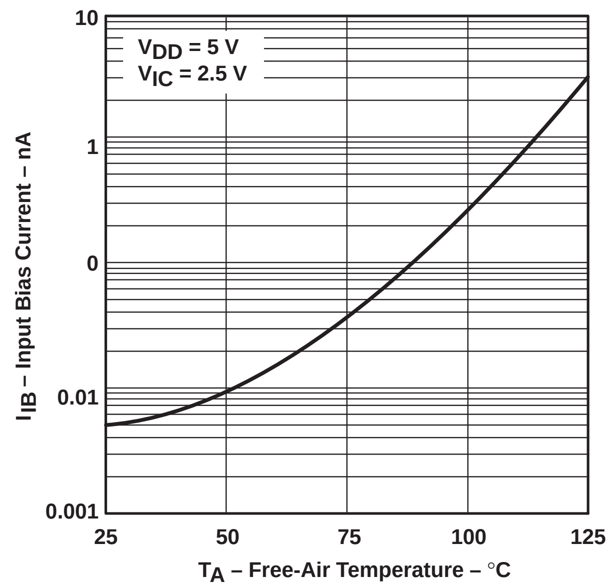


Figure 5

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

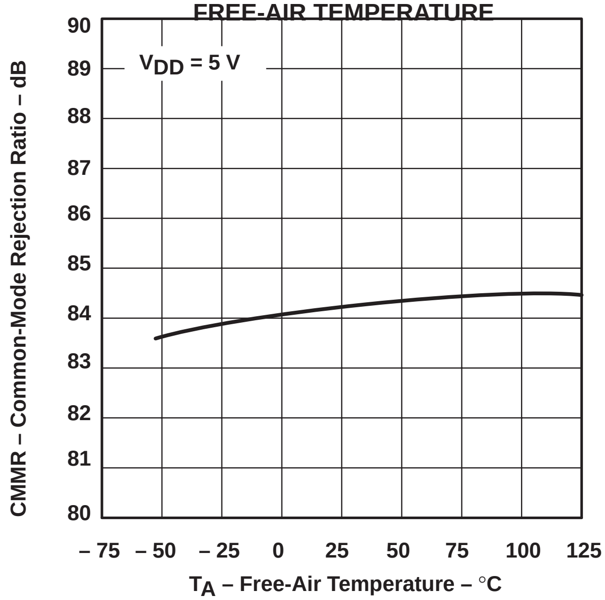


Figure 6

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

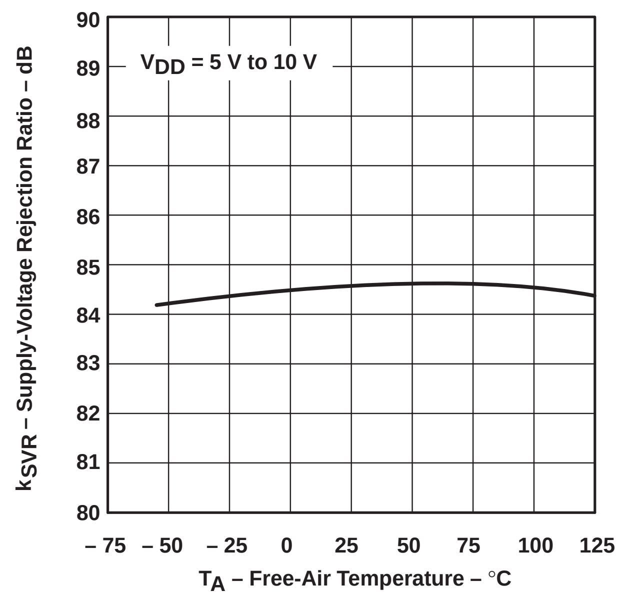


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

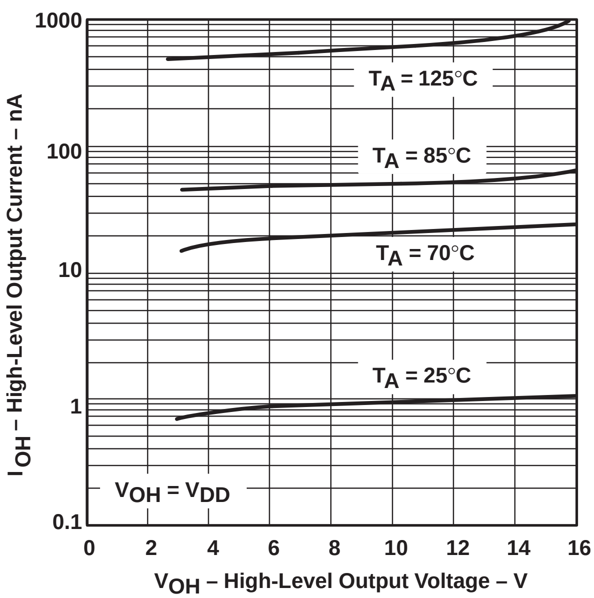


Figure 8

HIGH-LEVEL OUTPUT CURRENT vs FREE-AIR TEMPERATURE

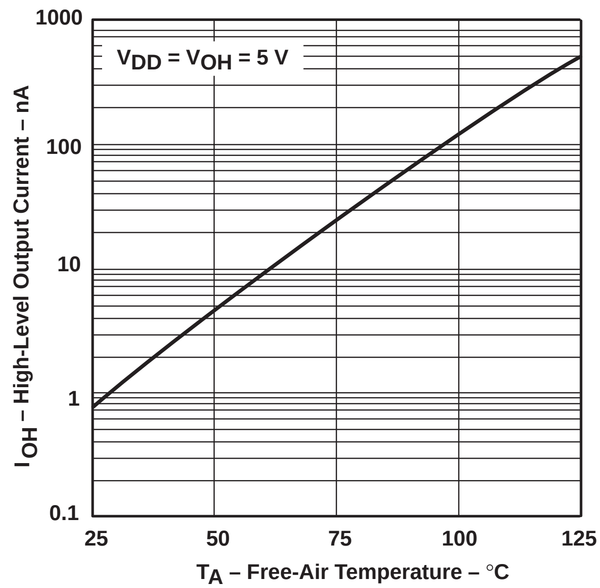


Figure 9

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

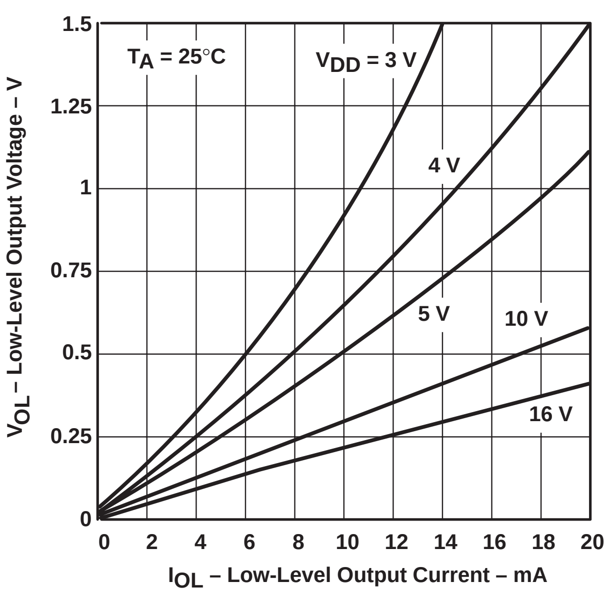


Figure 10

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

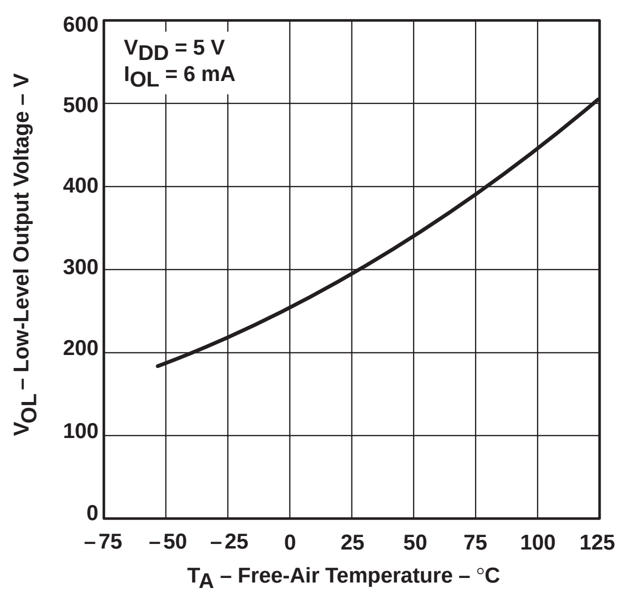


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

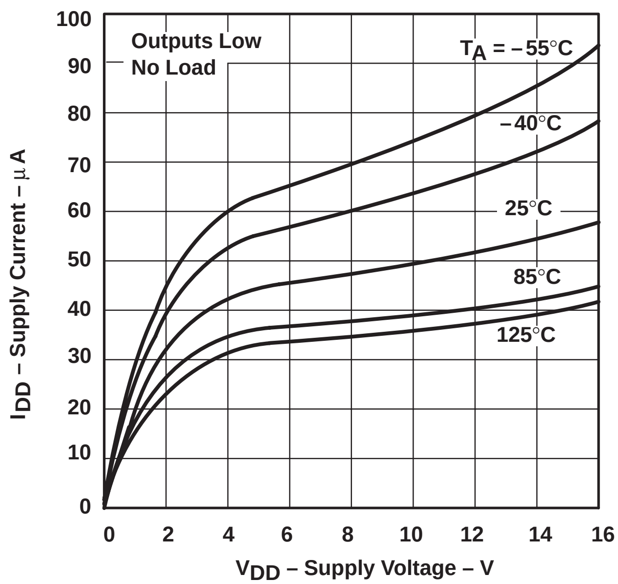


Figure 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

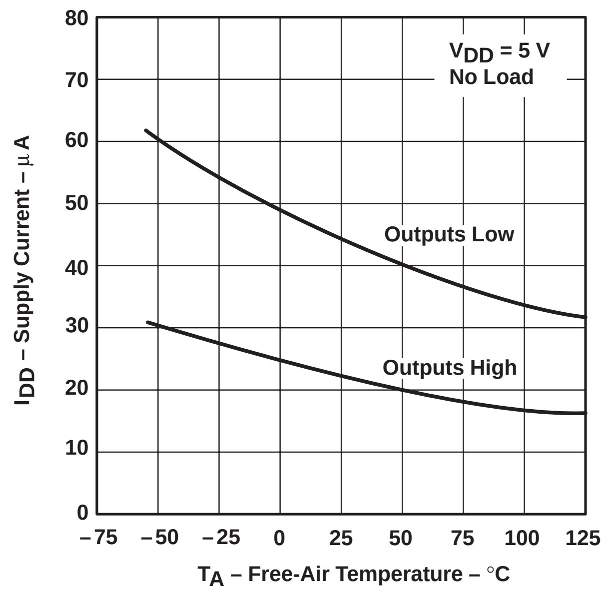


Figure 13

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

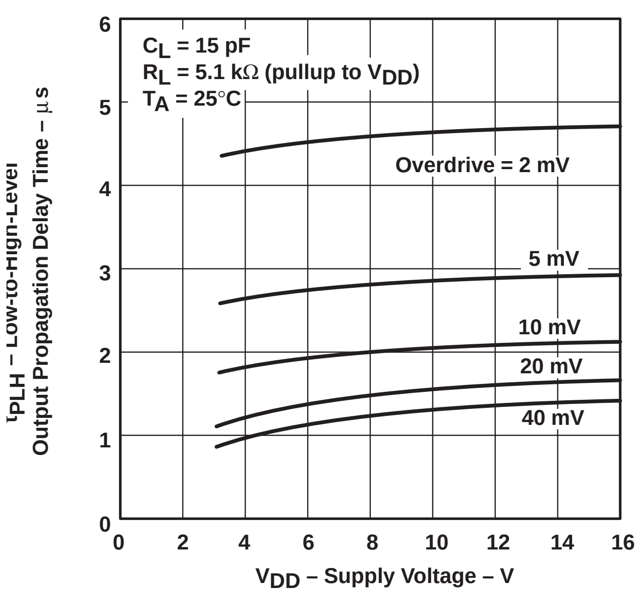


Figure 14

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

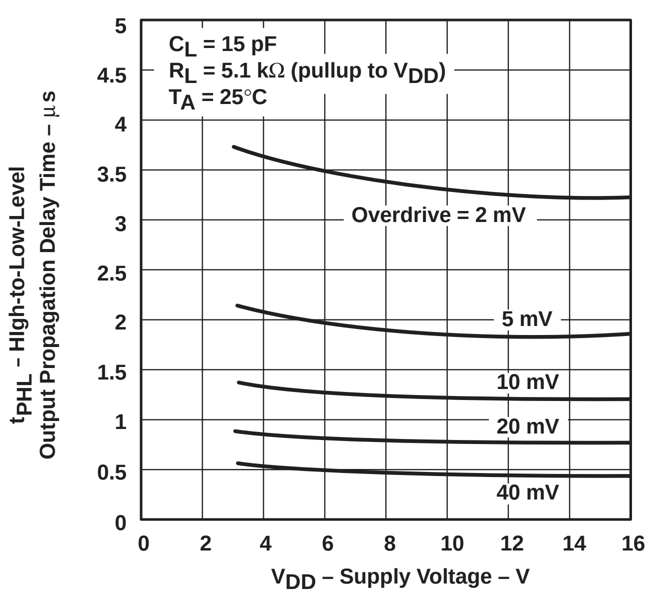


Figure 15

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS OVERDRIVE VOLTAGES

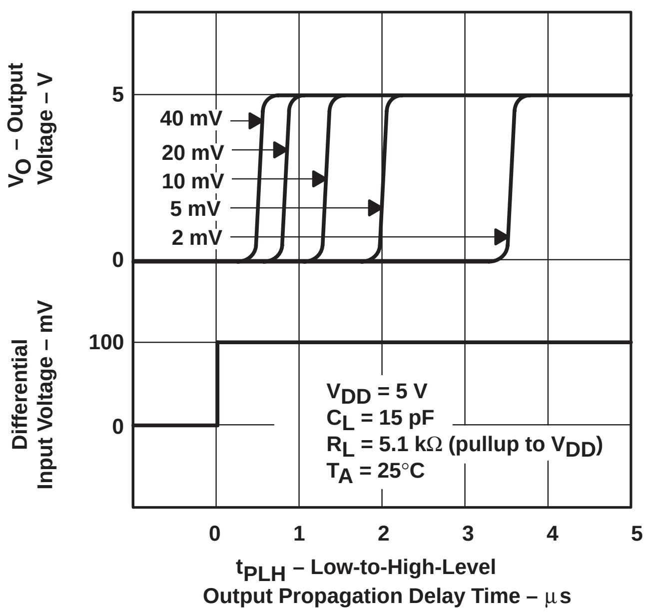


Figure 16

OUTPUT FALL TIME vs SUPPLY VOLTAGE

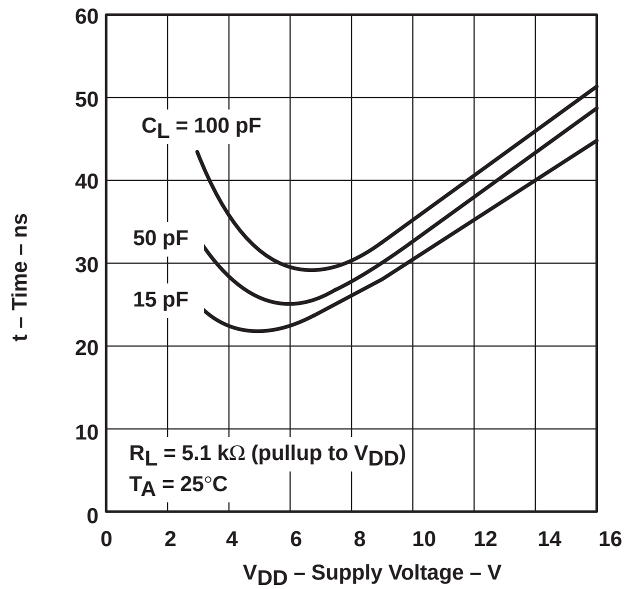


Figure 17

HIGH-TO-LOW-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS OVERDRIVE VOLTAGES

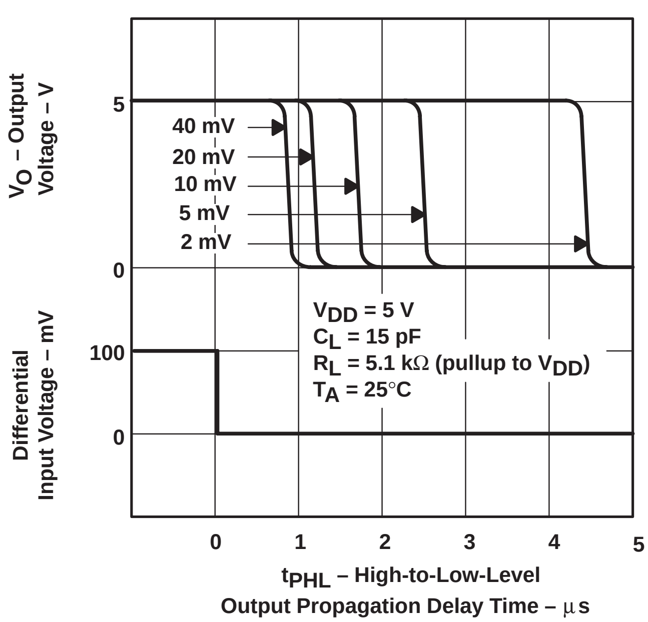


Figure 18

APPLICATION INFORMATION

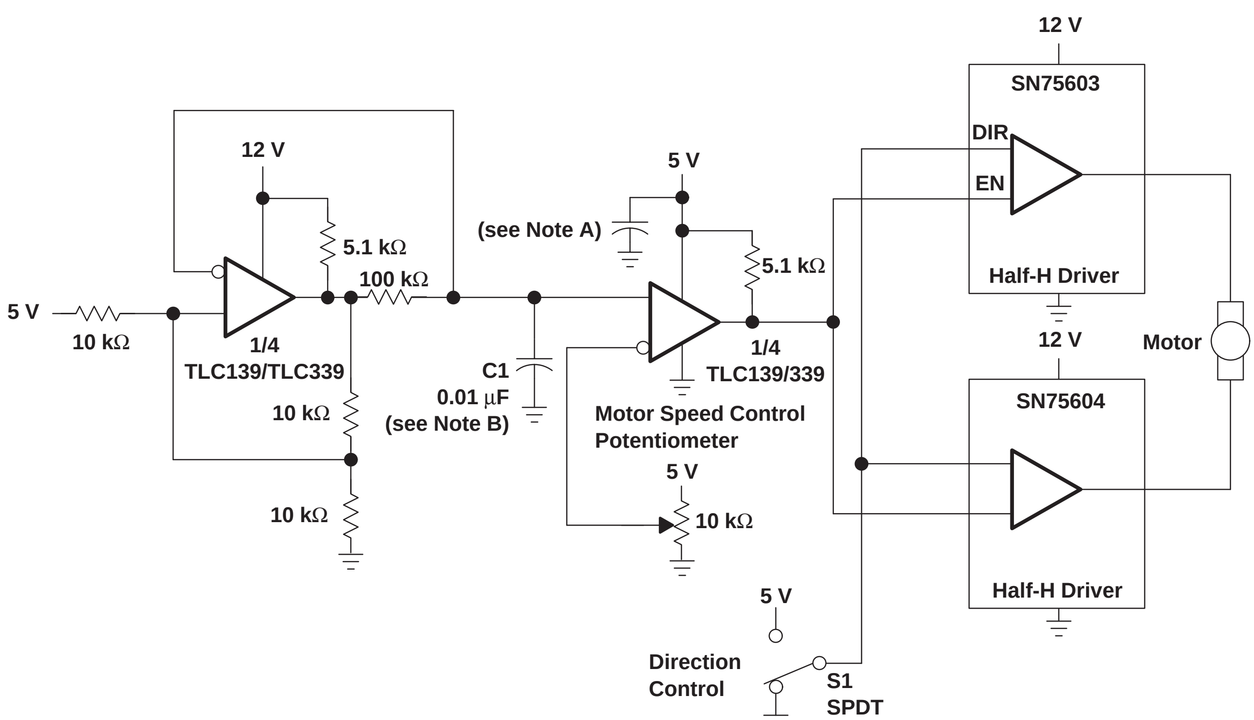
The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not damaged as long as the input current is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between –0.2 V and 4 V to assure proper device operation. To assure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) positioned as close to the device as possible.

The output and supply currents require close observation since the TLC139/TLC339 does not provide current protection. For example, each output can source or sink a maximum of 20 mA; however, the total current to ground has an absolute maximum of 60 mA. This prohibits sinking 20 mA from each of the four outputs simultaneously since the total current to ground would be 80 mA.

The TLC139 and TLC339 have internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, exercise care when handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

Table of Applications

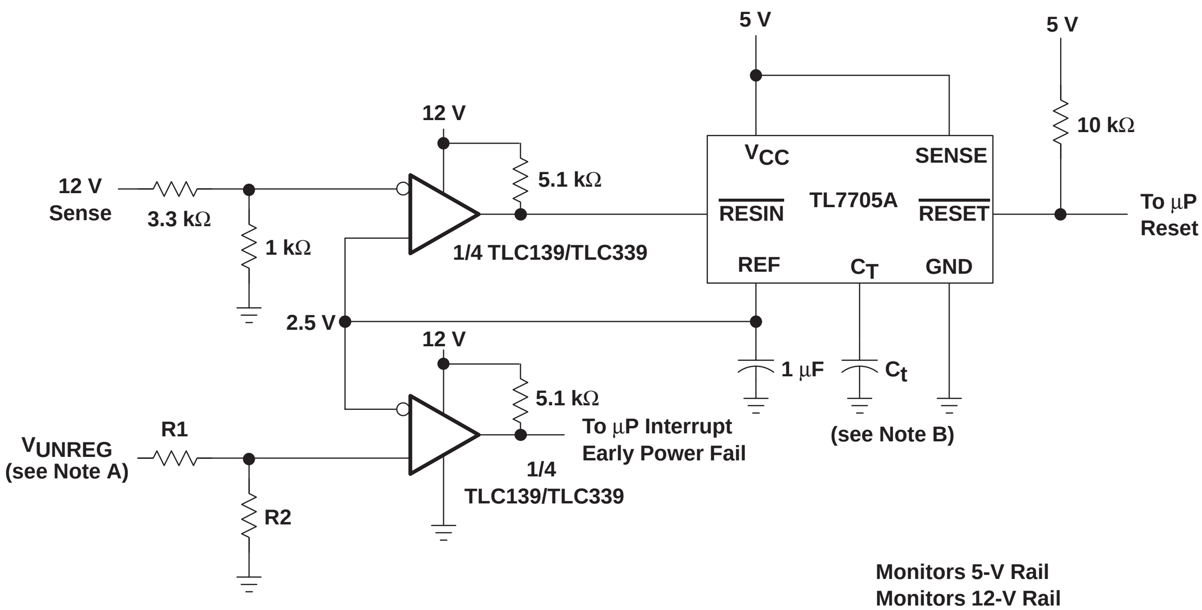
	FIGURE
Pulse-width-modulated motor speed controller	19
Enhanced supply supervisor	20
Two-phase nonoverlapping clock generator	21



NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Select C1 for change in oscillator frequency.

Figure 19. Pulse-Width-Modulated Motor Speed Controller

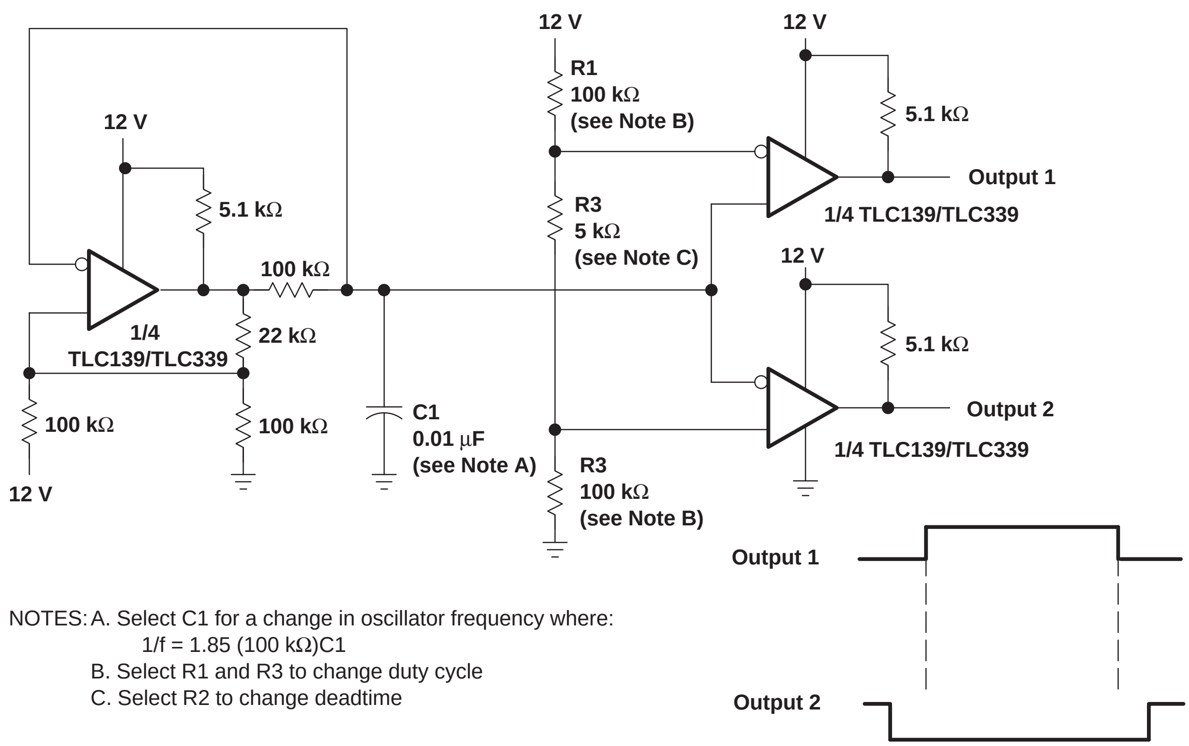
TYPICAL APPLICATION DATA



NOTES: A. $V_{UNREG} = 2.5 \left(\frac{R1 + R2}{R2}\right)$

B. The value of C_t determines the time delay of reset.

Figure 20. Enhanced Supply Supervisor



NOTES: A. Select C1 for a change in oscillator frequency where:
$1/f = 1.85\ (100\ k\Omega)C1$
B. Select R1 and R3 to change duty cycle
C. Select R2 to change deadtime

Figure 21. Two-Phase Nonoverlapping Clock Generator

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