



## Programmable FTG for Differential CPU, PCI Express\* & SATA Clocks

### Recommended Application:

Frequency Timing Generator for Differential CPU, PCI Express & SATA clocks

### Features:

- Generates common CPU/PCI Express frequencies from 14.318 MHz or 25 MHz
- Crystal or reference input
- 7 - 0.7V current-mode differential output pairs
- 3 - 33MHz PCI outputs
- 1 - REFOUT
- Supports Serial-ATA at 100 MHz
- Two spread spectrum modes: 0 to -0.5 downspread and +/-0.25% centerspread
- Unused inputs may be disabled in either driven or Hi-Z state for power management.

### Key Specifications:

- Output cycle-to-cycle jitter for DIF outputs < 50 ps (<85ps @ 266 MHz)
- Output to output skew for DIF outputs < 85 ps
- +/-300 ppm frequency accuracy on output clocks

### Frequency Select Table

| SEL14M_25M#<br>(FS3) | FS2 | FS1 | FS0 | OUTPUT(MHz) |
|----------------------|-----|-----|-----|-------------|
| 0                    | 0   | 0   | 0   | 100.00      |
| 0                    | 0   | 0   | 1   | 125.00      |
| 0                    | 0   | 1   | 0   | 133.33      |
| 0                    | 0   | 1   | 1   | 166.67      |
| 0                    | 1   | 0   | 0   | 200.00      |
| 0                    | 1   | 0   | 1   | 266.66      |
| 0                    | 1   | 1   | 0   | 333.33      |
| 0                    | 1   | 1   | 1   | 400.00      |
| 1                    | 0   | 0   | 0   | 100.00      |
| 1                    | 0   | 0   | 1   | 125.00      |
| 1                    | 0   | 1   | 0   | 133.33      |
| 1                    | 0   | 1   | 1   | 166.67      |
| 1                    | 1   | 0   | 0   | 200.00      |
| 1                    | 1   | 0   | 1   | 266.66      |
| 1                    | 1   | 1   | 0   | 333.33      |
| 1                    | 1   | 1   | 1   | 400.00      |

### Pin Configuration

| Pin | Signal        | Pin | Signal        |
|-----|---------------|-----|---------------|
| 1   | XIN/CLKIN     | 48  | VDDA          |
| 2   | X2            | 47  | GNDA          |
| 3   | VDD           | 46  | IREF          |
| 4   | GND           | 45  | *DWNSPRD#     |
| 5   | *FS2/REFOUT   | 44  | **FS1         |
| 6   | GND           | 43  | *OE_0         |
| 7   | *FS0/PCICLK_F | 42  | DIF_0         |
| 8   | PCICLK0       | 41  | DIF_0#        |
| 9   | PCICLK1       | 40  | VDD           |
| 10  | VDD           | 39  | DIF_1         |
| 11  | **OE_6        | 38  | DIF_1#        |
| 12  | DIF_6         | 37  | **OE_1        |
| 13  | DIF_6#        | 36  | VDD           |
| 14  | VDD           | 35  | GND           |
| 15  | GND           | 34  | **OE_2        |
| 16  | **OE_5        | 33  | DIF_2         |
| 17  | DIF_5         | 32  | DIF_2#        |
| 18  | DIF_5#        | 31  | VDD           |
| 19  | VDD           | 30  | DIF_3         |
| 20  | DIF_4         | 29  | DIF_3#        |
| 21  | DIF_4#        | 28  | *OE_3         |
| 22  | *OE_4         | 27  | **SEL14M_25M# |
| 23  | SDATA         | 26  | *SPREAD       |
| 24  | SCLK          | 25  | DIF_STOP#     |

ICS9FG107

### 48-pin SSOP & TSSOP

#### Notes:

- Pins preceded by \* have 120 Kohm pull DOWN resistors
- Pins preceded by \*\* have 120 Kohm pull UP resistors



### Pin Description

| PIN # | PIN NAME      | PIN TYPE | DESCRIPTION   |
|-------|---------------|----------|---|
| 1     | XIN/CLKIN     | IN       | Crystal input or Reference Clock input  |
| 2     | X2            | OUT      | Crystal output, Nominally 14.318MHz   |
| 3     | VDD           | PWR      | Power supply, nominal 3.3V  |
| 4     | GND           | PWR      | Ground pin.   |
| 5     | *FS2/REFOUT   | I/O      | Frequency select latch input pin / Reference clock output                           |
| 6     | GND           | PWR      | Ground pin.   |
| 7     | *FS0/PCICLK_F | I/O      | Frequency select latch input pin / 3.3V PCI free running clock output.              |
| 8     | PCICLK0       | OUT      | PCI clock output.   |
| 9     | PCICLK1       | OUT      | PCI clock output.   |
| 10    | VDD           | PWR      | Power supply, nominal 3.3V  |
| 11    | **OE_6        | IN       | Active high input for enabling outputs.<br>0 = tri-state outputs, 1= enable outputs |
| 12    | DIF_6         | OUT      | 0.7V differential true clock outputs  |
| 13    | DIF_6#        | OUT      | 0.7V differential complement clock outputs  |
| 14    | VDD           | PWR      | Power supply, nominal 3.3V  |
| 15    | GND           | PWR      | Ground pin.   |
| 16    | **OE_5        | IN       | Active high input for enabling outputs.<br>0 = tri-state outputs, 1= enable outputs |
| 17    | DIF_5         | OUT      | 0.7V differential true clock outputs  |
| 18    | DIF_5#        | OUT      | 0.7V differential complement clock outputs  |
| 19    | VDD           | PWR      | Power supply, nominal 3.3V  |
| 20    | DIF_4         | OUT      | 0.7V differential true clock outputs  |
| 21    | DIF_4#        | OUT      | 0.7V differential complement clock outputs  |
| 22    | *OE_4         | IN       | Active high input for enabling outputs.<br>0 = tri-state outputs, 1= enable outputs |
| 23    | SDATA         | I/O      | Data pin for SMBus circuitry, 5V tolerant.  |
| 24    | SCLK          | IN       | Clock pin of SMBus circuitry, 5V tolerant.  |

Pin Description (Continued)

| PIN # | PIN NAME      | PIN TYPE | DESCRIPTION   |
|-------|---------------|----------|---|
| 25    | DIF_STOP#     | IN       | Active low input to stop differential output clocks.  |
| 26    | *SPREAD       | IN       | Asynchronous, active high input, with internal 120Kohm pull-up resistor, to enable spread spectrum functionality.   |
| 27    | **SEL14M_25M# | IN       | Select 14.31818 MHz or 25 Mhz input frequency. 1 = 14.31818 MHz, 0 = 25 MHz   |
| 28    | *OE_3         | IN       | Active high input for enabling outputs.<br>0 = tri-state outputs, 1= enable outputs   |
| 29    | DIF_3#        | OUT      | 0.7V differential complement clock outputs  |
| 30    | DIF_3         | OUT      | 0.7V differential true clock outputs  |
| 31    | VDD           | PWR      | Power supply, nominal 3.3V  |
| 32    | DIF_2#        | OUT      | 0.7V differential complement clock outputs  |
| 33    | DIF_2         | OUT      | 0.7V differential true clock outputs  |
| 34    | **OE_2        | IN       | Active high input for enabling outputs.<br>0 = tri-state outputs, 1= enable outputs   |
| 35    | GND           | PWR      | Ground pin.   |
| 36    | VDD           | PWR      | Power supply, nominal 3.3V  |
| 37    | **OE_1        | IN       | Active high input for enabling outputs.<br>0 = tri-state outputs, 1= enable outputs   |
| 38    | DIF_1#        | OUT      | 0.7V differential complement clock outputs  |
| 39    | DIF_1         | OUT      | 0.7V differential true clock outputs  |
| 40    | VDD           | PWR      | Power supply, nominal 3.3V  |
| 41    | DIF_0#        | OUT      | 0.7V differential complement clock outputs  |
| 42    | DIF_0         | OUT      | 0.7V differential true clock outputs  |
| 43    | *OE_0         | IN       | Active high input for enabling outputs.<br>0 = tri-state outputs, 1= enable outputs   |
| 44    | **FS1         | I/O      | Frequency select latch input pin / 3.3V 66.66MHz clock output.  |
| 45    | *DWNSPRD#     | IN       | 3.3V input that selects spread mode. This input is not latched at power up.<br>0 = Down Spread, 1 = Center Spread   |
| 46    | IREF          | OUT      | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 47    | GND_A         | PWR      | Ground pin for the PLL core.  |
| 48    | VDD_A         | PWR      | 3.3V power for the PLL core.  |

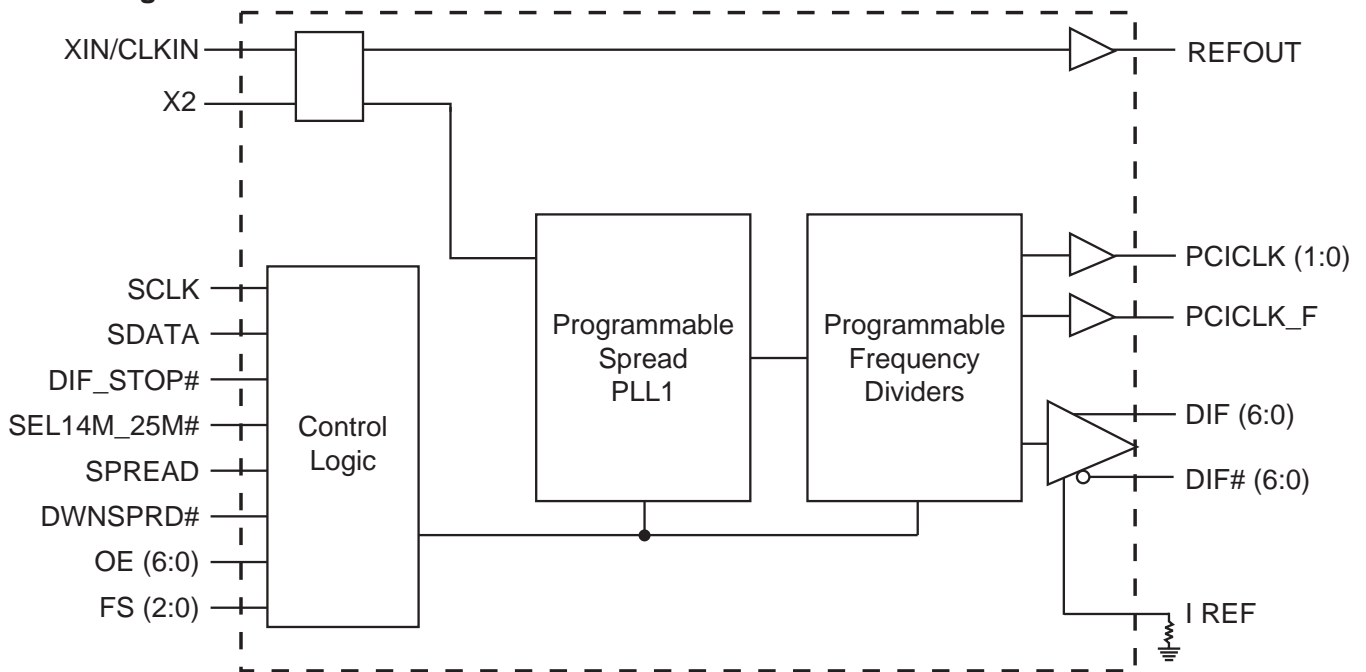
Pins preceded by \* have 120 Kohm pull DOWN resistors

Pins preceded by \*\* have 120 Kohm pull UP resistors

## General Description

ICS9FG107 is a Frequency Timing Generator that provides 7 differential output pairs that are compliant to the Intel CK409/CK410 specification. It provides support for PCI-Express, next generation I/O, and SATA. The part synthesizes several output frequencies from either a 14.31818 Mhz crystal or a 25 MHz crystal. The device can also be driven by a reference input clock instead of a crystal. It provides outputs with cycle-to-cycle jitter of less than 85 ps and output-to-output skew of less than 85 ps. ICS9FG107 also provides a copy of the reference clock and 3 33 MHz PCI output clocks. Frequency selection can be accomplished via strap pins or SMBus control.

## Block Diagram



## Power Groups

| Pin Number     |       | Description                   |
|----------------|-------|-------------------------------|
| VDD            | GND   |                               |
| 3              | 4     | REFOUT, Digital Inputs, SMBus |
| 10             | 6     | PCI Outputs                   |
| 14,19,31,36,40 | 15,35 | DIF Outputs                   |
| N/A            | 47    | IREF                          |
| 48             | 47    | Analog VDD & GND for PLL Core |

### Absolute Max

| Symbol   | Parameter                                | Min       | Max             | Units |
|----------|--|-----------|-----------------|-------|
| VDD_A    | 3.3V Core Supply Voltage                 |           | $V_{DD} + 0.5V$ | V     |
| VDD_In   | 3.3V Logic Input Supply Voltage          | GND - 0.5 | $V_{DD} + 0.5V$ | V     |
| Ts       | Storage Temperature                      | -65       | 150             | °C    |
| Tambient | Ambient Operating Temp                   | 0         | 70              | °C    |
| Tcase    | Case Temperature                         |           | 115             | °C    |
| ESD_prot | Input ESD protection<br>human body model | 2000      |                 | V     |

### Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^{\circ}C$ ; Supply Voltage  $V_{DD} = 3.3 V \pm 5\%$

| PARAMETER                             | SYMBOL        | CONDITIONS  | MIN            | TYP | MAX            | UNITS | NOTES |
|---------------------------------------|---------------|---|----------------|-----|----------------|-------|-------|
| Input High Voltage                    | $V_{IH}$      | 3.3 V +/-5%   | 2              |     | $V_{DD} + 0.3$ | V     |       |
| Input Low Voltage                     | $V_{IL}$      | 3.3 V +/-5%   | $V_{SS} - 0.3$ |     | 0.8            | V     |       |
| Input High Current                    | $I_{IH}$      | $V_{IN} = V_{DD}$   | -5             |     | 5              | uA    |       |
| Input Low Current                     | $I_{IL1}$     | $V_{IN} = 0 V$ ; Inputs with no pull-up resistors                       | -5             |     |                | uA    |       |
|                                       | $I_{IL2}$     | $V_{IN} = 0 V$ ; Inputs with pull-up resistors                          | -200           |     |                | uA    |       |
| Operating Supply Current              | $I_{DD3.30P}$ | Full Active, $C_L = \text{Full load}$ ;<br>$f = 400 \text{ MHz}$        |                |     | 250            | mA    |       |
|                                       |               | Full Active, $C_L = \text{Full load}$ ;<br>$f = 100 \text{ MHz}$        |                |     | 200            | mA    |       |
| Input Frequency <sup>3</sup>          | $F_i$         | $V_{DD} = 3.3 V$  | 14             |     | 25             | MHz   | 3     |
| Pin Inductance <sup>1</sup>           | $L_{pin}$     |   |                |     | 7              | nH    | 1     |
| Input/Output Capacitance <sup>1</sup> | $C_{IN}$      | Logic Inputs  | 1.5            |     | 5              | pF    | 1     |
|                                       | $C_{OUT}$     | Output pin capacitance  |                |     | 6              | pF    | 1     |
| Clk Stabilization <sup>1,2</sup>      | $T_{STAB}$    | From $V_{DD}$ Power-Up and after input clock stabilization to 1st clock |                |     | 1.8            | ms    | 1,2   |
| Modulation Frequency                  | $f_{MOD}$     | Triangular Modulation   | 30             |     | 40             | kHz   | 1     |
| DIF output enable                     | $t_{DIFOE}$   | DIF output enable after DIF_Stop# de-assertion                          |                |     | 10             | ns    | 1     |
| Input Rise and Fall times             | $t_R/t_F$     | 20% to 80% of VDD   |                |     | 5              | ns    | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>See timing diagrams for timing requirements.

<sup>3</sup>Input frequency should be measured at the REFOUT pin and tuned to ideal 14.31818MHz or 25 MHz to meet ppm frequency accuracy on PLL outputs.

**Electrical Characteristics - DIF 0.7V Current Mode Differential Pair**

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 2\text{pF}$ ,  $R_S = 33.2\Omega$ ,  $R_P = 49.9\Omega$   $\square_{REF} \square_{9}$ ,

| PARAMETER                       | SYMBOL              | CONDITIONS   | MIN    | TYP | MAX     | UNITS    | NOTES |
|---------------------------------|---------------------|--|--------|-----|---------|----------|-------|
| Current Source Output Impedance | $Z_o^1$             | $V_O = V_x$  | 3000   |     |         | $\Omega$ | 1     |
| Voltage High                    | VHigh               | Statistical measurement on single ended signal using oscilloscope math function. | 660    |     | 850     | mV       | 1     |
| Voltage Low                     | VLow                |  | -150   |     | 150     |          | 1     |
| Max Voltage                     | Vovs                | Measurement on single ended signal using absolute value.                         |        |     | 1150    | mV       | 1     |
| Min Voltage                     | Vuds                |  | -300   |     |         |          | 1     |
| Crossing Voltage (abs)          | Vcross(abs)         |  | 250    |     | 550     | mV       | 1     |
| Crossing Voltage (var)          | d-Vcross            | Variation of crossing over all edges   |        |     | 140     | mV       | 1     |
| Long Accuracy                   | ppm                 | see Tperiod min-max values   | -300   |     | 300     | ppm      | 1,2   |
| Average period                  | Tperiod             | 400MHz nominal   | 2.4993 |     | 2.5008  | ns       | 2     |
|                                 |                     | 400MHz spread  | 2.4993 |     | 2.5133  | ns       | 2,3   |
|                                 |                     | 333.33MHz nominal  | 2.9991 |     | 3.0009  | ns       | 2     |
|                                 |                     | 333.33MHz spread   | 2.9991 |     | 3.016   | ns       | 2,3   |
|                                 |                     | 266.66MHz nominal  | 3.7489 |     | 3.7511  | ns       | 2     |
|                                 |                     | 266.66MHz spread   | 3.7489 |     | 3.77    | ns       | 2,3   |
|                                 |                     | 200MHz nominal   | 4.9985 |     | 5.0015  | ns       | 2     |
|                                 |                     | 200MHz spread  | 4.9985 |     | 5.0266  | ns       | 2,3   |
|                                 |                     | 166.66MHz nominal  | 5.9982 |     | 6.0018  | ns       | 2     |
|                                 |                     | 166.66MHz spread   | 5.9982 |     | 6.0320  | ns       | 2,3   |
|                                 |                     | 133.33MHz nominal  | 7.4978 |     | 7.5023  | ns       | 2     |
|                                 |                     | 133.33MHz spread   | 7.4978 |     | 5.4000  | ns       | 2,3   |
|                                 |                     | 100.00MHz nominal  | 9.9970 |     | 10.0030 | ns       | 2     |
|                                 |                     | 100.00MHz spread   | 9.9970 |     | 10.0533 | ns       | 2,3   |
| Absolute min period             | T <sub>absmin</sub> | 400MHz nominal/spread  | 2.4143 |     |         | ns       | 1,2   |
|                                 |                     | 333.33MHz nominal/spread   | 2.9141 |     |         | ns       | 1,2   |
|                                 |                     | 266.66MHz nominal/spread   | 3.6639 |     |         | ns       | 1,2   |
|                                 |                     | 200MHz nominal/spread  | 4.8735 |     |         | ns       | 1,2   |
|                                 |                     | 166.66MHz nominal/spread   | 5.8732 |     |         | ns       | 1,2   |
|                                 |                     | 133.33MHz nominal/spread   | 7.3728 |     |         | ns       | 1,2   |
|                                 |                     | 100.00MHz nominal/spread   | 9.8720 |     |         | ns       | 1,2   |
| Rise Time                       | $t_r$               | $V_{OL} = 0.175\text{V}$ , $V_{OH} = 0.525\text{V}$                              | 175    |     | 700     | ps       | 1     |
| Fall Time                       | $t_f$               | $V_{OH} = 0.525\text{V}$ $V_{OL} = 0.175\text{V}$                                | 175    |     | 700     | ps       | 1     |
| Rise Time Variation             | d- $t_r$            |  |        |     | 125     | ps       | 1     |
| Fall Time Variation             | d- $t_f$            |  |        |     | 125     | ps       | 1     |
| Duty Cycle                      | $d_{t3}$            | Measurement from differential waveform   | 45     |     | 55      | %        | 1     |
| Skew                            | $t_{sk3}$           | $V_T = 50\%$   |        |     | 85      | ps       | 1     |
| Jitter, Cycle to cycle          | $t_{jyc-cyc}$       | Measurement from differential waveform f not equal 266 MHz                       |        |     | 50      | ps       | 1     |
|                                 |                     | Measurement from differential waveform f = 266 MHz                               |        |     | 85      | ps       | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz or 25 MHz

<sup>3</sup>Figures are for down spread.

### Electrical Characteristics - PCICLK/PCICLK\_F

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 30\text{ pF}$  (unless otherwise specified)

| PARAMETER                     | SYMBOL              | CONDITIONS  | MIN      | TYP | MAX      | UNITS | Notes |
|-------------------------------|---------------------|---|----------|-----|----------|-------|-------|
| Long Accuracy                 | ppm                 | see Tperiod min-max values                        | -300     |     | 300      | ppm   | 1,2   |
| Clock period                  | $T_{\text{period}}$ | 33.33MHz output nominal                           | 29.99100 |     | 30.00900 | ns    | 2     |
|                               |                     | 33.33MHz output spread                            | 29.99100 |     | 30.15980 | ns    | 2     |
| Absolute Min/Max Clock period | $T_{\text{abs}}$    | 33.33MHz output nominal                           | 29.49100 |     | 30.50900 | ns    | 2     |
|                               |                     | 33.33MHz output spread                            | 29.49100 |     | 30.65980 | ns    | 2     |
| Clk High Time                 | $t_{h1}$            |   | 12       |     | N/A      | ns    | 1     |
| Clock Low Time                | $t_{l1}$            |   | 12       |     | N/A      | ns    | 1     |
| Output High Voltage           | $V_{OH}$            | $I_{OH} = -1\text{ mA}$                           | 2.4      |     |          | V     |       |
| Output Low Voltage            | $V_{OL}$            | $I_{OL} = 1\text{ mA}$                            |          |     | 0.55     | V     |       |
| Output High Current           | $I_{OH}$            | $V_{OH} @ \text{MIN} = 1.0\text{ V}$              | -33      |     |          | mA    |       |
|                               |                     | $V_{OH} @ \text{MAX} = 3.135\text{ V}$            |          |     | -33      | mA    |       |
| Output Low Current            | $I_{OL}$            | $V_{OL} @ \text{MIN} = 1.95\text{ V}$             | 30       |     |          | mA    |       |
|                               |                     | $V_{OL} @ \text{MAX} = 0.4\text{ V}$              |          |     | 38       | mA    |       |
| Edge Rate                     |                     | Rising edge rate                                  | 1        |     | 4        | V/ns  | 1     |
| Edge Rate                     |                     | Falling edge rate                                 | 1        |     | 4        | V/ns  | 1     |
| Rise Time                     | $t_{r1}$            | $V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.4\text{ V}$ | 0.5      | 1.4 | 2        | ns    | 1     |
| Fall Time                     | $t_{f1}$            | $V_{OH} = 2.4\text{ V}$ , $V_{OL} = 0.4\text{ V}$ | 0.5      | 1.4 | 2        | ns    | 1     |
| Duty Cycle                    | $d_{t1}$            | $V_T = 1.5\text{ V}$                              | 45       |     | 55       | %     | 1     |
| Skew                          | $t_{sk1}$           | $V_T = 1.5\text{ V}$                              |          |     | 500      | ps    | 1     |
| Jitter                        | $t_{jvc-cvc}$       | $V_T = 1.5\text{ V}$                              |          |     | 250      | ps    | 1     |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz or 25 MHz

### Electrical Characteristics - REF-14.318/25 MHz

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 10-20\text{ pF}$  (unless otherwise specified)

| PARAMETER           | SYMBOL              | CONDITIONS   | MIN     | TYP     | MAX     | UNITS | Notes |
|---------------------|---------------------|--|---------|---------|---------|-------|-------|
| Long Accuracy       | ppm                 | see Tperiod min-max values   | -300    | 0       | 300     | ppm   | 1     |
| Clock period        | $T_{\text{period}}$ | 14.318MHz output nominal   | 69.8270 | 69.8413 | 69.8550 | ns    | 1,2   |
|                     |                     | 25.000MHz output nominal   | 39.9880 | 40.0000 | 40.0120 | ns    | 1,2   |
| Output High Voltage | $V_{OH}$            | $I_{OH} = -1\text{ mA}$  | 2.4     |         |         | V     | 1     |
| Output Low Voltage  | $V_{OL}$            | $I_{OL} = 1\text{ mA}$   |         |         | 0.4     | V     | 1     |
| Output High Current | $I_{OH}$            | $V_{OH} @ \text{MIN} = 1.0\text{ V}$ ,<br>$V_{OH} @ \text{MAX} = 3.135\text{ V}$ | -29     |         | -23     | mA    | 1     |
| Output Low Current  | $I_{OL}$            | $V_{OL} @ \text{MIN} = 1.95\text{ V}$ ,<br>$V_{OL} @ \text{MAX} = 0.4\text{ V}$  | 29      |         | 27      | mA    | 1     |
| Rise Time           | $t_{r1}$            | $V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.4\text{ V}$                                | 1       | 1.6     | 2       | ns    | 1     |
| Fall Time           | $t_{f1}$            | $V_{OH} = 2.4\text{ V}$ , $V_{OL} = 0.4\text{ V}$                                | 1       | 1.6     | 2       | ns    | 1     |
| Duty Cycle          | $d_{t1}$            | $V_T = 1.5\text{ V}$   | 45      |         | 55      | %     | 1     |
| Jitter              | $t_{jvc-cvc}$       | $V_T = 1.5\text{ V}$   |         | 160     | 250     | ps    | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818 or 25.00 MHz

## General SMBus serial interface information for the ICS9FG107

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address  $DC_{(H)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**  
(see Note 2)
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation |           |                      |
|-----------------------------|-----------|----------------------|
| Controller (Host)           |           | ICS (Slave/Receiver) |
| T                           | starT bit |                      |
| Slave Address $DC_{(H)}$    |           |                      |
| WR                          | WRite     |                      |
|                             |           | ACK                  |
| Beginning Byte = N          |           |                      |
|                             |           | ACK                  |
| Data Byte Count = X         |           |                      |
|                             |           | ACK                  |
| Beginning Byte N            |           |                      |
|                             | X Byte    | ACK                  |
| ○                           |           |                      |
| ○                           |           | ○                    |
| ○                           |           | ○                    |
| Byte N + X - 1              |           | ○                    |
|                             |           | ACK                  |
| P                           | stoP bit  |                      |

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address  $DC_{(H)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address  $DD_{(H)}$
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if  $X_{(H)}$  was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation |                 |                      |
|----------------------------|-----------------|----------------------|
| Controller (Host)          |                 | ICS (Slave/Receiver) |
| T                          | starT bit       |                      |
| Slave Address $DC_{(H)}$   |                 |                      |
| WR                         | WRite           |                      |
|                            |                 | ACK                  |
| Beginning Byte = N         |                 |                      |
|                            |                 | ACK                  |
| RT                         | Repeat starT    |                      |
| Slave Address $DD_{(H)}$   |                 |                      |
| RD                         | ReaD            |                      |
|                            |                 | ACK                  |
|                            |                 | Data Byte Count = X  |
| ACK                        |                 |                      |
| ACK                        |                 | Beginning Byte N     |
|                            | X Byte          | ○                    |
| ○                          |                 | ○                    |
| ○                          |                 | ○                    |
| ○                          |                 |                      |
|                            |                 | Byte N + X - 1       |
| N                          | Not acknowledge |                      |
| P                          | stoP bit        |                      |

I<sup>2</sup>C Table: Device Control Register, READ/WRITE ADDRESS (DC/DD)

| Byte 0 |    | Pin # | Name  | Control Function | Type | 0                                     | 1               | PWD    |
|--------|----|-------|---|------------------|------|---------------------------------------|-----------------|--------|
| Bit 7  | 27 |       | FS3 <sup>1</sup>  |                  | RW   | See Frequency Selection Table, Page 1 |                 | Pin 27 |
| Bit 6  | 5  |       | FS2 <sup>1</sup>  |                  | RW   |                                       |                 | Pin 5  |
| Bit 5  | 44 |       | FS1 <sup>1</sup>  |                  | RW   |                                       |                 | Pin 44 |
| Bit 4  | 7  |       | FS0 <sup>1</sup>  |                  | RW   |                                       |                 | Pin 7  |
| Bit 3  | 26 |       | Spread Enable <sup>1</sup>  |                  | RW   | Off                                   | On              | Pin 26 |
| Bit 2  | -  |       | Enable Software Control of Frequency, Spread Enable and Spread Type |                  | RW   | Hardware Select                       | Software Select | 0      |
| Bit 1  |    |       | DIF_STOP# drive mode  |                  | RW   | Driven                                | Hi-Z            | 0      |
| Bit 0  | 45 |       | DWNSPRD# <sup>1</sup>   |                  | RW   | Down                                  | Center          | Pin 45 |

Notes:

1. These bits reflect the latched state of the corresponding pins at power up, but may be written to if Byte 0, bit 2 is set to '1'. FS3 is the SEL14M\_25M# pin.

I<sup>2</sup>C Table: Output Enable Register

| Byte 1 |       | Pin # | Name    | Control Function | Type | 0        | 1      | PWD |
|--------|-------|-------|---------|------------------|------|----------|--------|-----|
| Bit 7  | 8     |       | PCICLK0 | Output Enable    | RW   | Stop Low | Enable | 1   |
| Bit 6  | 12,13 |       | DIF_6   | Output Enable    | RW   | Disable  | Enable | 1   |
| Bit 5  | 17,18 |       | DIF_5   | Output Enable    | RW   | Disable  | Enable | 1   |
| Bit 4  | 20,21 |       | DIF_4   | Output Enable    | RW   | Disable  | Enable | 1   |
| Bit 3  | 30,29 |       | DIF_3   | Output Enable    | RW   | Disable  | Enable | 1   |
| Bit 2  | 33,32 |       | DIF_2   | Output Enable    | RW   | Disable  | Enable | 1   |
| Bit 1  | 39,38 |       | DIF_1   | Output Enable    | RW   | Disable  | Enable | 1   |
| Bit 0  | 42,41 |       | DIF_0   | Output Enable    | RW   | Disable  | Enable | 1   |

I<sup>2</sup>C Table: Output Stop Mode Register

| Byte 2 |       | Pin # | Name    | Control Function | Type | 0        | 1         | PWD |
|--------|-------|-------|---------|------------------|------|----------|-----------|-----|
| Bit 7  | 9     |       | PCICLK1 | Output Enable    | RW   | Stop Low | Enable    | 1   |
| Bit 6  | 12,13 |       | DIF_6   | Stop Mode        | RW   | Free-run | Stop-able | 0   |
| Bit 5  | 17,18 |       | DIF_5   | Stop Mode        | RW   | Free-run | Stop-able | 0   |
| Bit 4  | 20,21 |       | DIF_4   | Stop Mode        | RW   | Free-run | Stop-able | 0   |
| Bit 3  | 30,29 |       | DIF_3   | Stop Mode        | RW   | Free-run | Stop-able | 0   |
| Bit 2  | 33,32 |       | DIF_2   | Stop Mode        | RW   | Free-run | Stop-able | 0   |
| Bit 1  | 39,38 |       | DIF_1   | Stop Mode        | RW   | Free-run | Stop-able | 0   |
| Bit 0  | 42,41 |       | DIF_0   | Stop Mode        | RW   | Free-run | Stop-able | 0   |

I<sup>2</sup>C Table: Frequency Select Readback Register

| Byte 3 |    | Pin # | Name                              | Control Function | Type | 0  | 1      | PWD    |
|--------|----|-------|-----------------------------------|------------------|------|--|--------|--------|
| Bit 7  | 27 |       | SEL14M_25M# <sup>1</sup><br>(FS3) | State of pin 27  | R    | See Frequency<br>Selection Table, Page 1 |        | Pin 27 |
| Bit 6  | 5  |       | FS2 <sup>1</sup>                  | State of pin 6   | R    |  |        | Pin 5  |
| Bit 5  | 44 |       | FS1 <sup>1</sup>                  | State of pin 44  | R    |  |        | Pin 44 |
| Bit 4  | 7  |       | FS0 <sup>1</sup>                  | State of pin 7   | R    |  |        | Pin 7  |
| Bit 3  | 26 |       | SPREAD <sup>1</sup>               | State of pin 26  | R    | Off                                      | On     | Pin 26 |
| Bit 2  |    |       | RESERVED                          |                  | R    | RESERVED                                 |        | X      |
| Bit 1  |    |       | RESERVED                          |                  | R    | RESERVED                                 |        | X      |
| Bit 0  | 45 |       | DWNSPRD <sup>1</sup>              | State of pin 45  | R    | Down                                     | Center | Pin 45 |

**Notes:**

1. These read-only bits always reflect the latched state of the corresponding pins at power up.

I<sup>2</sup>C Table: Vendor & Revision ID Register

| Byte 4 |   | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|---|-------|------|------------------|------|---|---|-----|
| Bit 7  | - |       | RID3 | REVISION ID      | R    | - | - | 0   |
| Bit 6  | - |       | RID2 |                  | R    | - | - | 0   |
| Bit 5  | - |       | RID1 |                  | R    | - | - | 0   |
| Bit 4  | - |       | RID0 |                  | R    | - | - | 0   |
| Bit 3  | - |       | VID3 | VENDOR ID        | R    | - | - | 0   |
| Bit 2  | - |       | VID2 |                  | R    | - | - | 0   |
| Bit 1  | - |       | VID1 |                  | R    | - | - | 0   |
| Bit 0  | - |       | VID0 |                  | R    | - | - | 1   |

I<sup>2</sup>C Table: DEVICE ID

| Byte 5 |   | Pin # | Name                               | Control Function | Type | 0        | 1 | PWD |
|--------|---|-------|------------------------------------|------------------|------|----------|---|-----|
| Bit 7  | - |       | Device ID = 07 Hex<br>Bit 7 is MSB |                  | R    | RESERVED |   | 0   |
| Bit 6  | - |       |                                    |                  | R    | RESERVED |   | 0   |
| Bit 5  | - |       |                                    |                  | R    | RESERVED |   | 0   |
| Bit 4  | - |       |                                    |                  | R    | RESERVED |   | 0   |
| Bit 3  | - |       |                                    |                  | R    | RESERVED |   | 0   |
| Bit 2  | - |       |                                    |                  | R    | RESERVED |   | 1   |
| Bit 1  | - |       |                                    |                  | R    | RESERVED |   | 1   |
| Bit 0  | - |       |                                    |                  | R    | RESERVED |   | 1   |

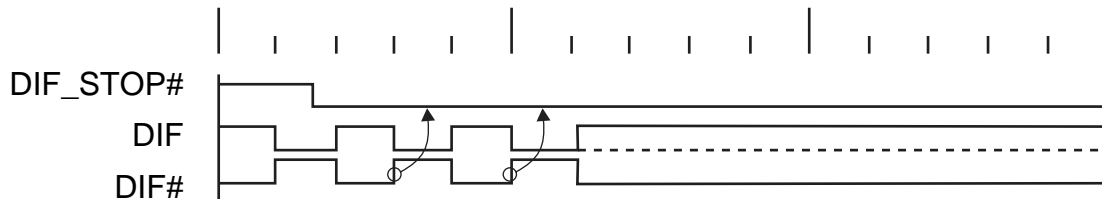


I<sup>2</sup>C Table: Byte Count Register

| Byte 6 |   | Pin # | Name | Control Function   | Type | 0 | 1 | PWD |
|--------|---|-------|------|--|------|---|---|-----|
| Bit 7  | - |       | BC7  | Writing to this register will configure how many bytes will be read back, default is 07 = 7 bytes. | RW   | - | - | 0   |
| Bit 6  | - |       | BC6  |  | RW   | - | - | 0   |
| Bit 5  | - |       | BC5  |  | RW   | - | - | 0   |
| Bit 4  | - |       | BC4  |  | RW   | - | - | 0   |
| Bit 3  | - |       | BC3  |  | RW   | - | - | 0   |
| Bit 2  | - |       | BC2  |  | RW   | - | - | 1   |
| Bit 1  | - |       | BC1  |  | RW   | - | - | 1   |
| Bit 0  | - |       | BC0  |  | RW   | - | - | 1   |

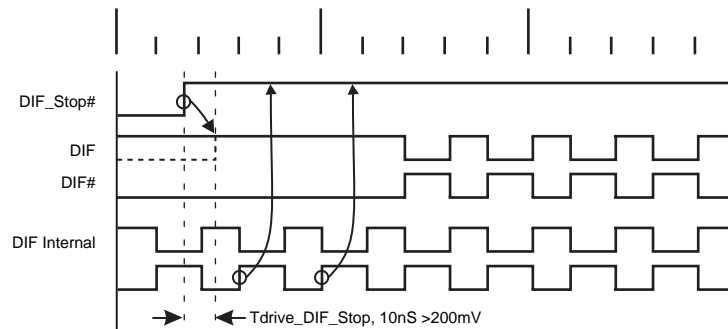
**DIF\_STOP# - Assertion (transition from '1' to '0')**

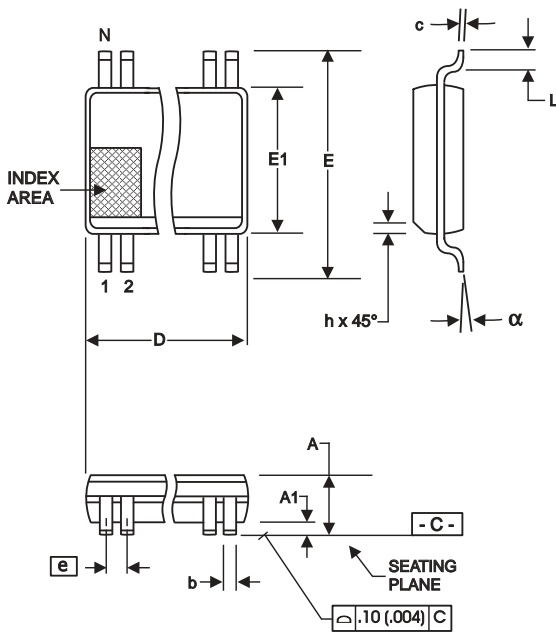
Asserting DIF\_STOP# pin stops all DIF outputs that are set to be stoppable after their next transition. When the I2C DIF\_STOP tri-state bit corresponding to the DIF output of interest is programmed to a '0', DIF output will stop DIF\_True = HIGH and DIF\_Complement = LOW. When the I2C DIF\_STOP tri-state bit corresponding to the DIF output of interest is programmed to a '1', DIF outputs will be tri-stated.



**DIF\_STOP# - De-assertion (transition from '0' to '1')**

With the de-assertion of DIF\_STOP# all stopped DIF outputs will resume without a glitch. The maximum latency from the de-assertion to active outputs is 2 - 6 DIF clock periods. If the control register tristate bit corresponding to the output of interest is programmed to '1', then the stopped DIF outputs will be driven High within 10nS of DIF\_Stop# de-assertion to a voltage greater than 200mV.





| SYMBOL | In Millimeters    |       | In Inches         |       |
|--------|-------------------|-------|-------------------|-------|
|        | COMMON DIMENSIONS |       | COMMON DIMENSIONS |       |
|        | MIN               | MAX   | MIN               | MAX   |
| A      | 2.41              | 2.80  | .095              | .110  |
| A1     | 0.20              | 0.40  | .008              | .016  |
| b      | 0.20              | 0.34  | .008              | .0135 |
| c      | 0.13              | 0.25  | .005              | .010  |
| D      | SEE VARIATIONS    |       | SEE VARIATIONS    |       |
| E      | 10.03             | 10.68 | .395              | .420  |
| E1     | 7.40              | 7.60  | .291              | .299  |
| e      | 0.635 BASIC       |       | 0.025 BASIC       |       |
| h      | 0.38              | 0.64  | .015              | .025  |
| L      | 0.50              | 1.02  | .020              | .040  |
| N      | SEE VARIATIONS    |       | SEE VARIATIONS    |       |
| alpha  | 0°                | 8°    | 0°                | 8°    |

VARIATIONS

| N  | D mm. |       | D (inch) |      |
|----|-------|-------|----------|------|
|    | MIN   | MAX   | MIN      | MAX  |
| 48 | 15.75 | 16.00 | .620     | .630 |

Reference Doc.: JEDEC Publication 95, MO-118

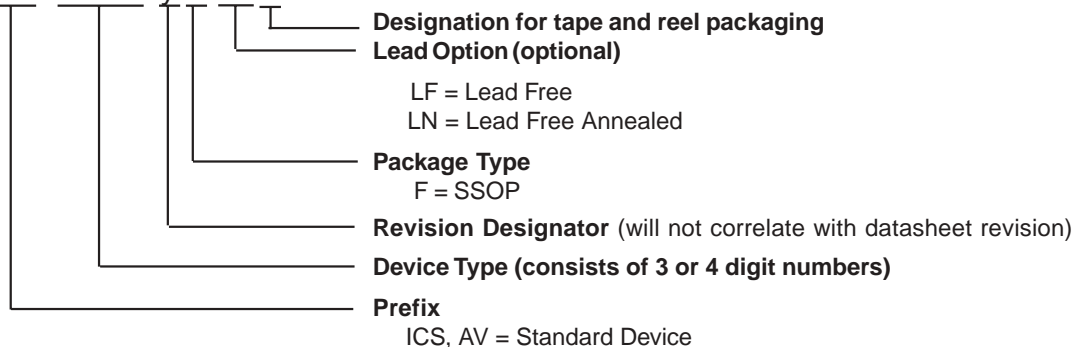
10-0034

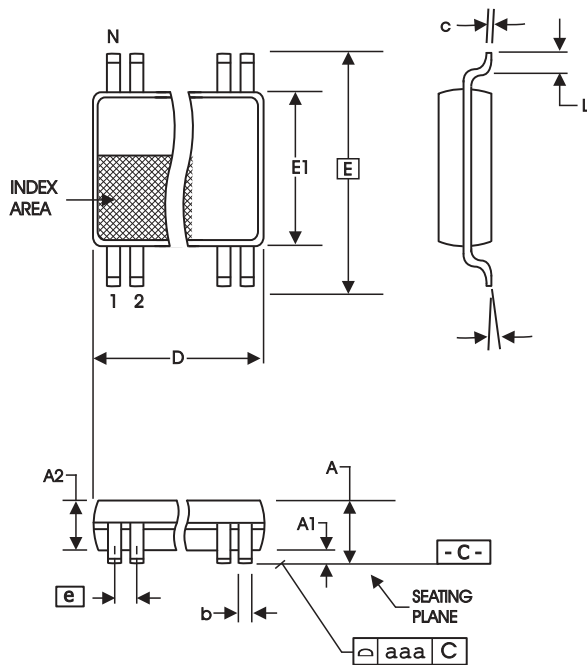
**Ordering Information**

**ICS9FG107yFLFT**

Example:

**ICS XXXX y F Lx T**





**48-Lead, 6.10 mm. Body, 0.50 mm. Pitch TSSOP**  
(240 mil) (20 mil)

| SYMBOL | In Millimeters<br>COMMON DIMENSIONS |      | In Inches<br>COMMON DIMENSIONS |      |
|--------|-------------------------------------|------|--------------------------------|------|
|        | MIN                                 | MAX  | MIN                            | MAX  |
| A      | --                                  | 1.20 | --                             | .047 |
| A1     | 0.05                                | 0.15 | .002                           | .006 |
| A2     | 0.80                                | 1.05 | .032                           | .041 |
| b      | 0.17                                | 0.27 | .007                           | .011 |
| c      | 0.09                                | 0.20 | .0035                          | .008 |
| D      | SEE VARIATIONS                      |      | SEE VARIATIONS                 |      |
| E      | 8.10 BASIC                          |      | 0.319 BASIC                    |      |
| E1     | 6.00                                | 6.20 | .236                           | .244 |
| e      | 0.50 BASIC                          |      | 0.020 BASIC                    |      |
| L      | 0.45                                | 0.75 | .018                           | .030 |
| N      | SEE VARIATIONS                      |      | SEE VARIATIONS                 |      |
| a      | 0°                                  | 8°   | 0°                             | 8°   |
| aaa    | --                                  | 0.10 | --                             | .004 |

**VARIATIONS**

| N  | D mm. |       | D (inch) |      |
|----|-------|-------|----------|------|
|    | MIN   | MAX   | MIN      | MAX  |
| 48 | 12.40 | 12.60 | .488     | .496 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

## Ordering Information

**ICS9FG107yGLFT**

Example:

**ICS XXXX y G Lx T**

Designation for tape and reel packaging  
Lead Option (optional)

LF = Lead Free  
LN = Lead Free Annealed

Package Type  
G = TSSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV = Standard Device