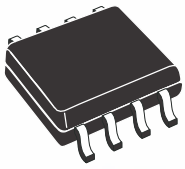
STS9D8NH3LL

Dual N-channel 30 V - 0.012 Ω - 9 A - SO-8 low on-resistance STripFET™ Power MOSFET

Features

Type		V_{DSS}	$R_{DS(on)}$	Qg	I_D
STS9D8NH3LL	Q_1	30V	< 0.022Ω	7nC	8A
	Q_2	30V	< 0.015Ω	8nC	9A

- Optimal R_{DS}(on) x Qg trade-off @ 4.5V
- Conduction losses reduced
- Switching losses reduced



S0-8

Application

- Switching applications

Description

This device uses the latest advanced design rules of ST's STrip based technology. The Q1 and Q2 transistors, show respectively, the best gate charge and on-resistance for minimizing the switching and conduction losses. This application specific Power MOSFET has been designed to replace two SO-8 packages in DC-DC converters.

Figure 1. Internal schematic diagram

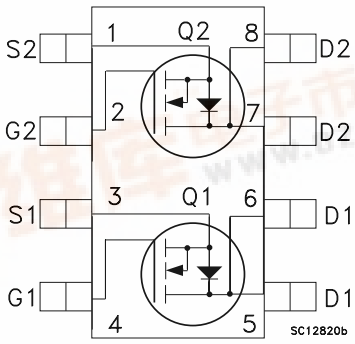


Table 1. Device summary

Order code	Marking	Package	Packaging
STS9D8NH3LL	9D8H3LL-	SO-8	Tape & reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Type	Value	Unit
V_{DS}	Drain-source voltage (v_{GS} = 0)	Q_1 Q_2	30 30	V V
V_{GS}	Gate- source voltage	Q_1 Q_2	±16 ±16	V V
I_D	Drain current (continuous) at T_C = 25°C	Q_1 Q_2	8 9	A A
I_D	Drain current (continuous) at T_C = 100°C	Q_1 Q_2	5 6.3	A A
I_{DM} (1)	Drain current (pulsed)	Q_1 Q_2	32 36	A A
P_{TOT}	Total dissipation at T_C = 25°C	Q_1 Q_2	2 2	W W
E_{AS}(2)	Single pulse avalanche energy		150	mJ

1. Pulse width limited by safe operating area
2. Starting T_J = 25 °C, I_D = 7.5 A

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}a}$ (1)	Thermal resistance junction-ambient max	62.5	°C/W
T_J	Thermal operating junction-ambient	150	°C
T_{stg}	Storage temperature	-55 to 150	°C

1. When mounted on 1 inch² FR-4 board, 2 oz. Cu., t ≤ 10s

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	Q_1 Q_2	30 30			V V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = Max rating	Q_1 Q_2			1 1	µA µA
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} =Max rating @125°C	Q_1 Q_2			10 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 16 V	Q_1 Q_2			±100 ±100	nA nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	Q_1 Q_2	1 1			V V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 4 A V_{GS} = 10 V, I_D = 4.5 A	Q_1 Q_2		0.018 0.012	0.022 0.015	Ω Ω
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 4.5 V, I_D = 4 A V_{GS} = 4.5 V, I_D = 4.5 A	Q_1 Q_2		0.020 0.014	0.025 0.0175	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	Q_1 Q_2		857 1070		pF pF
C_{oss}	Output capacitance		Q_1 Q_2		147 290		pF pF
C_{rss}	Reverse transfer capacitance		Q_1 Q_2		20 34		pF pF
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 8 A, V_{GS} = 4.5 V *(see Figure 25)*	Q_1 Q_2		7 8	10 11	nC nC
Q_{gs}	Gate-source charge		Q_1 Q_2		2.5 2		nC nC
Q_{gd}	Gate-drain charge		Q_1 Q_2		2.3 2.8		nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Type	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=15 V, I_D=4 A, R_G=4.7 Ω, V_{GS}= 4.5 V *(see Figure 27)*	Q_1		12		ns
			Q_2		8.2		ns
t_r	Rise time		Q_1		14.5		ns
			Q_2		6		ns
$t_{d(off)}$	Turn-off delay time	V_{DD}=15 V, I_D=4 A, R_G=4.7 Ω, V_{GS}= 4.5V *(see Figure 27)*	Q_1		23		ns
			Q_2		27.8		ns
t_f	Fall time		Q_1		8		ns
			Q_2		3.6		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Type	Min	Typ.	Max	Unit
I_{SD}	Source-drain current	V_{DD}=15 V, I_D=4 A, R_G=4.7 Ω, V_{GS}=4.5 V	Q_1			8	A
			Q_2			9	A
I_{SDM} (1)	Source-drain current (pulsed)	V_{DD}=15 V, I_D= 4A, R_G=4.7 Ω, V_{GS}=4.5 V	Q_1			32	A
			Q_2			36	A
V_{SD} (2)	Forward on voltage	I_{SD} = 8 A, V_{GS} = 0	Q_1			1.5	V
			Q_2			1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 8 A, V_{DD} = 15 V, di/dt = 100 A/µs, T_j = 150°C *(see Figure 26)*	Q_1		15		ns
			Q_2		22.8		ns
Q_{rr}	Reverse recovery charge		Q_1		5.7		nC
			Q_2		14.9		nC
I_{RRM}	Reverse recovery current		Q_1		0.76		A
			Q_2		1.3		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for Q1

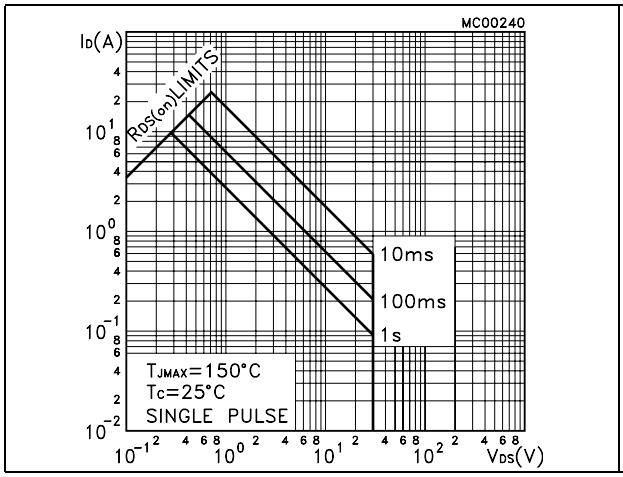


Figure 3. Safe operating area for Q2

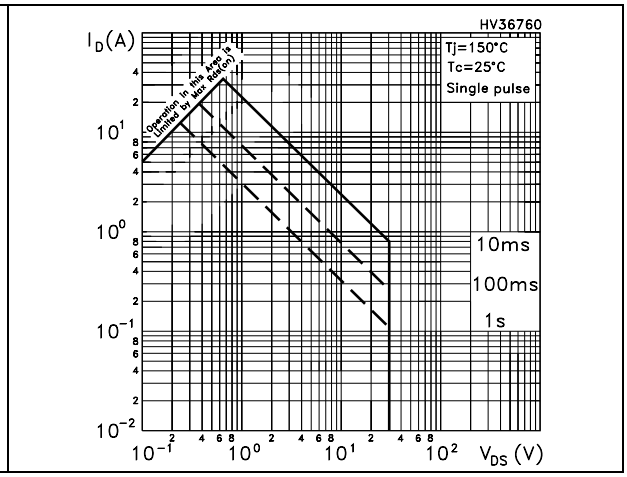


Figure 4. Thermal impedance for Q1

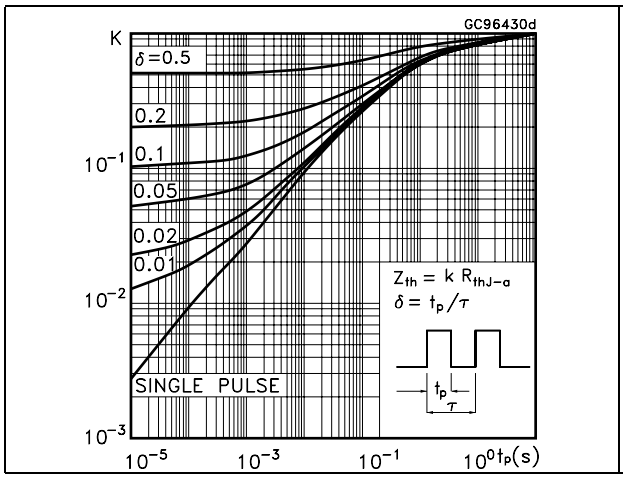


Figure 5. Thermal impedance for Q2

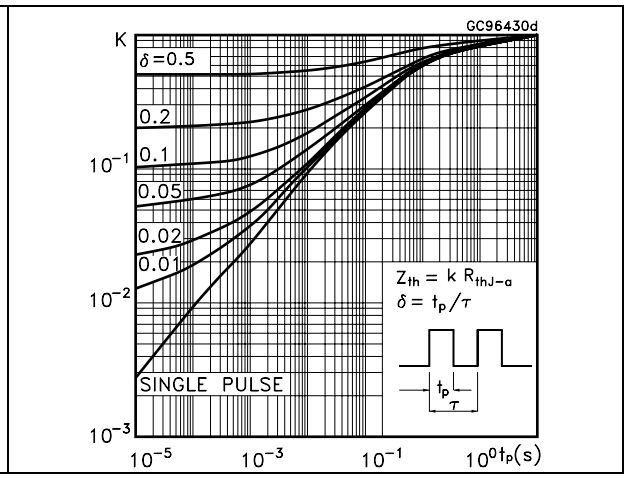


Figure 6. Output characteristics for Q1

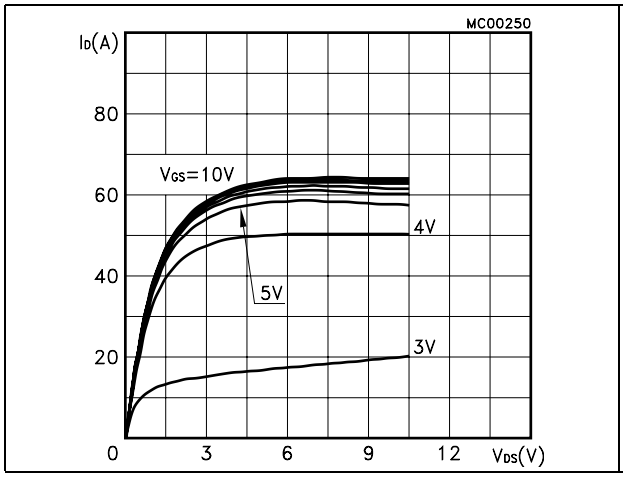


Figure 7. Output characteristics for Q2

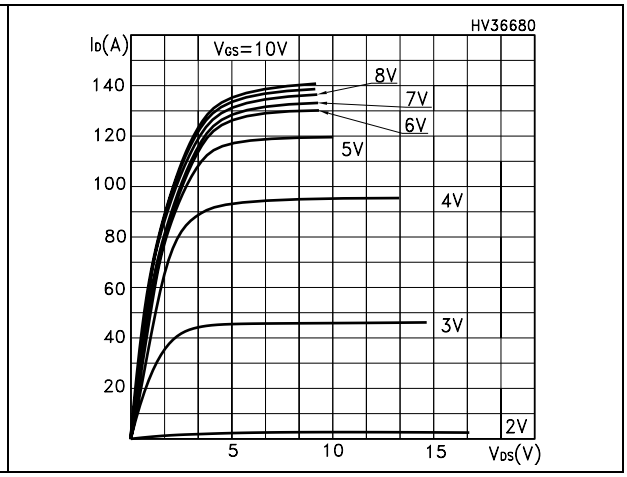


Figure 8. Transfer characteristics for Q1

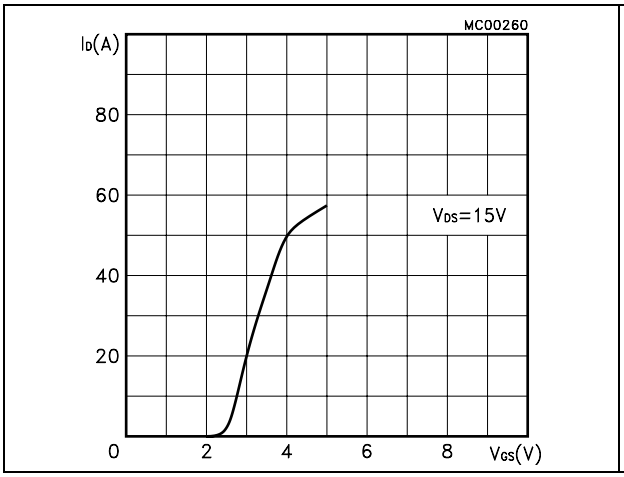


Figure 9. Transfer characteristics for Q2

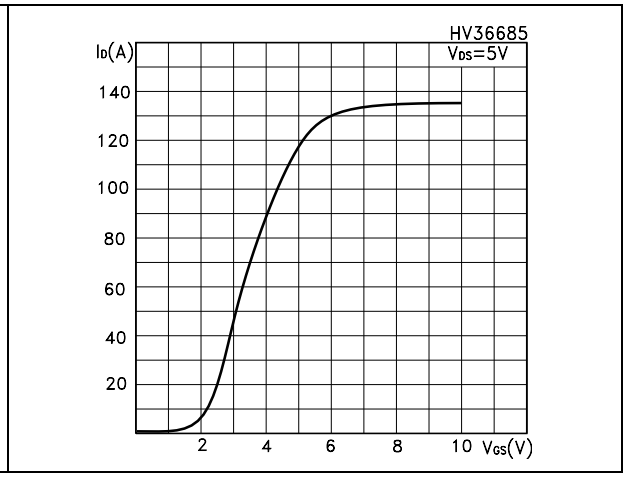


Figure 10. Static drain-source on resistance for Q1

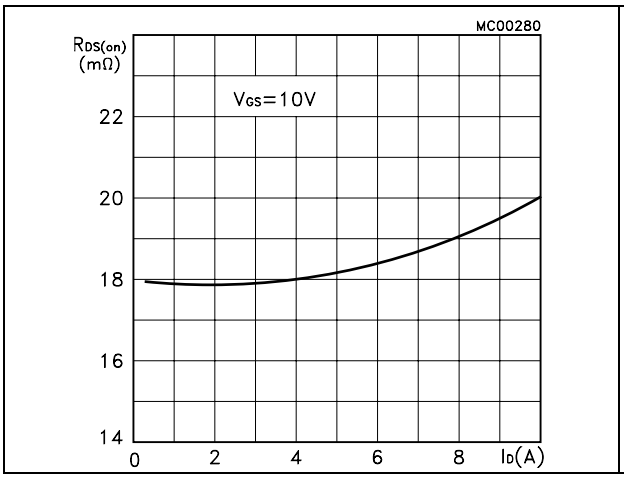


Figure 11. Static drain-source on resistance for Q2

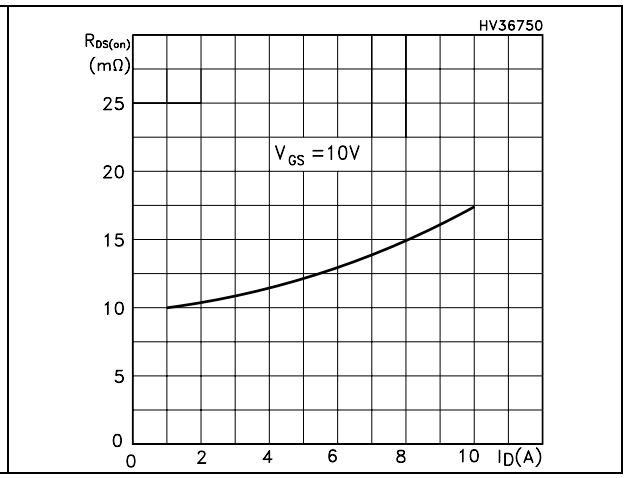


Figure 12. Normalized BV_{DSS} vs temperature for Q1

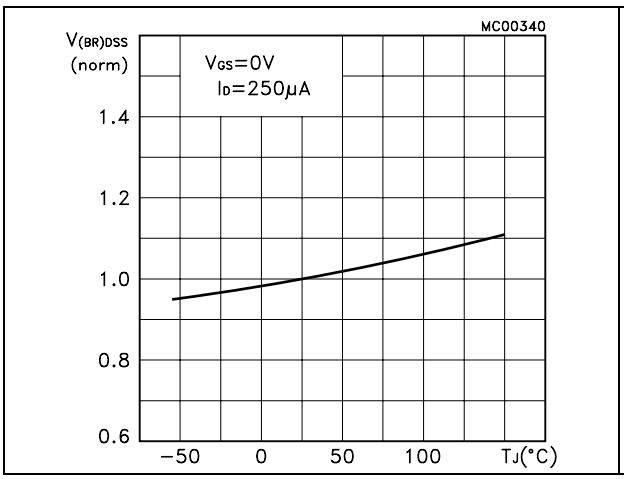


Figure 13. Normalized BV_{DSS} vs temperature for Q2

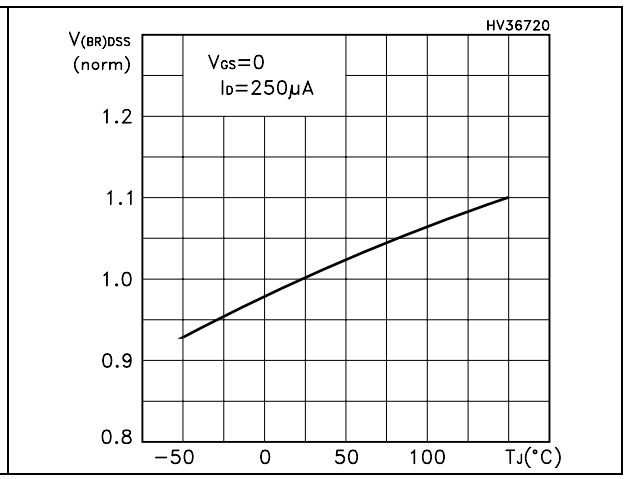


Figure 14. Gate charge vs gate-source voltage for Q1

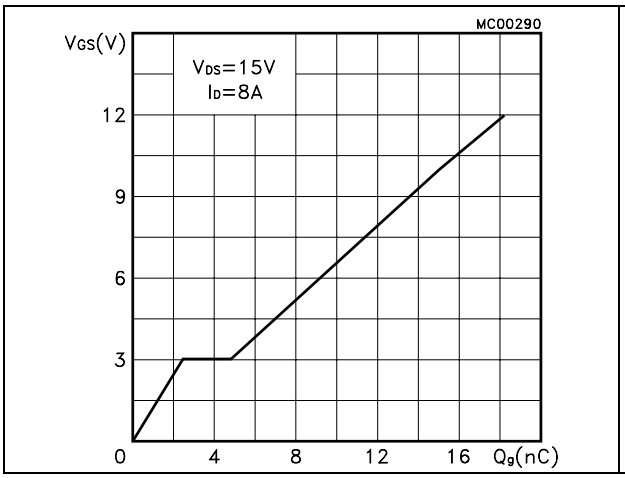


Figure 15. Gate charge vs gate-source voltage for Q2

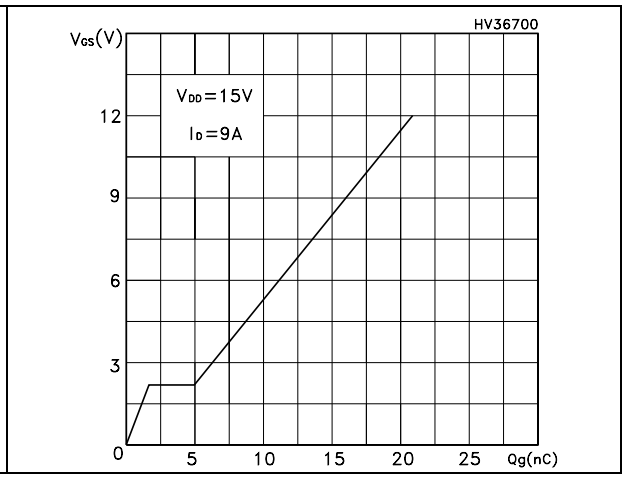


Figure 16. Capacitance variations for Q1

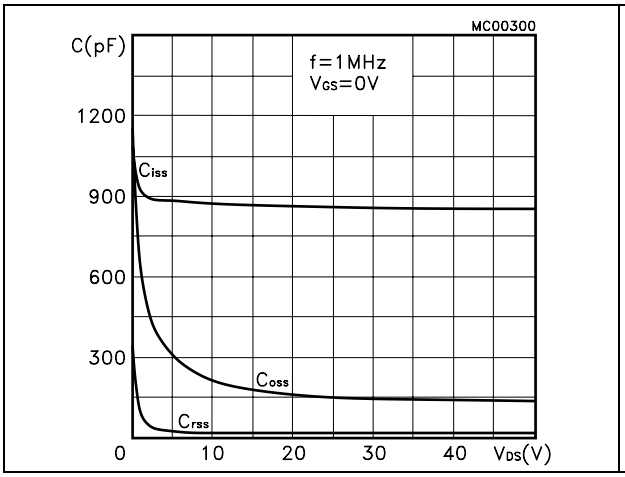


Figure 17. Capacitance variations for Q2

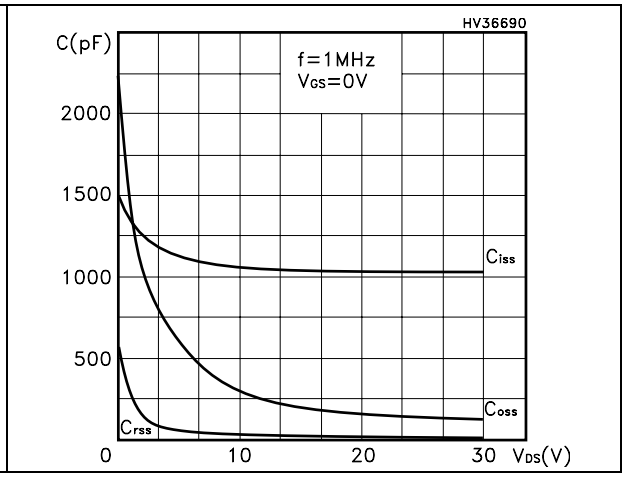


Figure 18. Normalized gate threshold voltage vs temperature for Q1

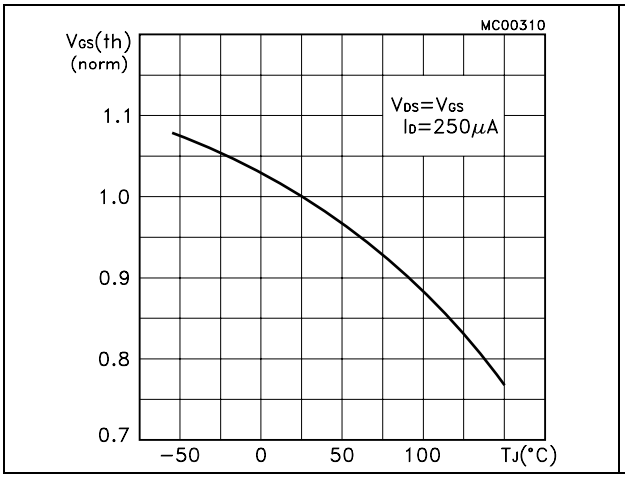


Figure 19. Normalized gate threshold voltage vs temperature for Q2

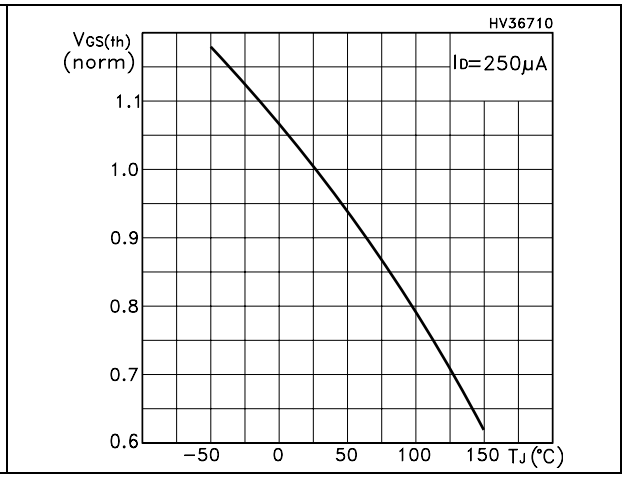


Figure 20. Normalized on resistance vs temperature for Q1

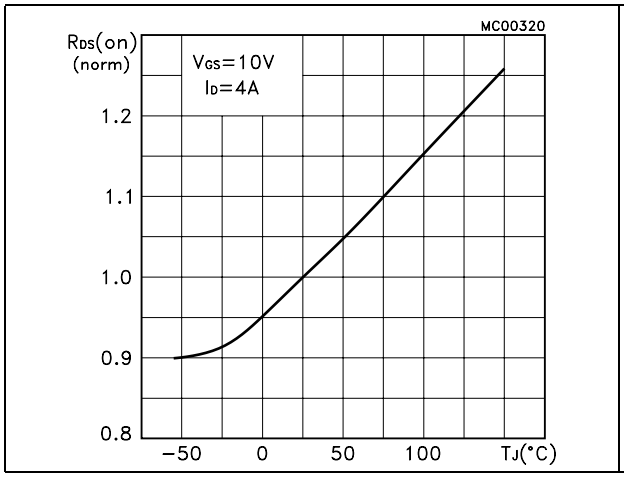


Figure 21. Normalized on resistance vs temperature for Q2

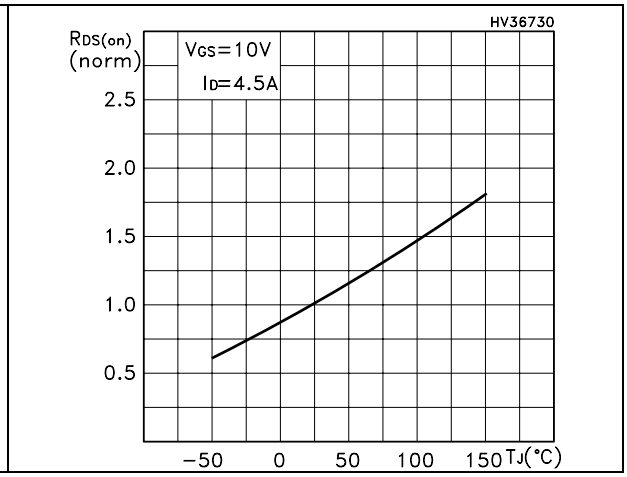


Figure 22. Source-drain diode forward characteristics for Q1

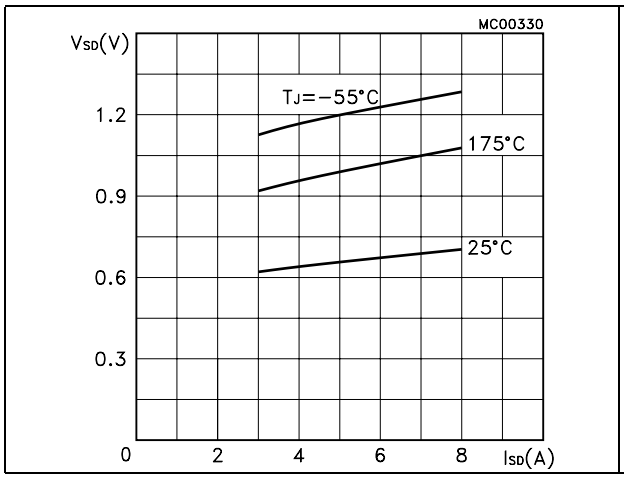
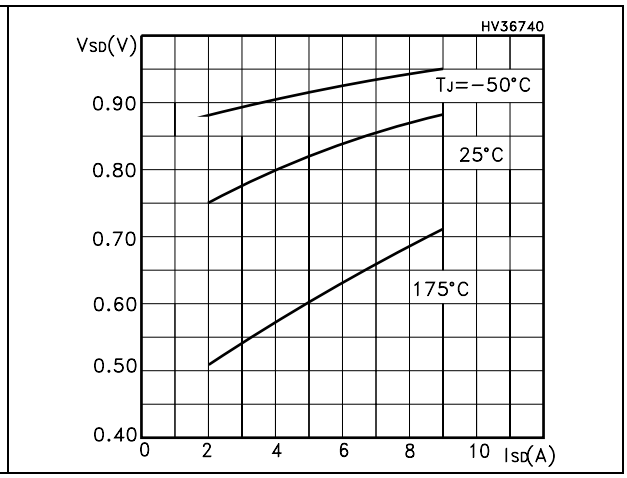


Figure 23. Source-drain diode forward characteristics for Q2



3 Test circuit

Figure 24. Switching times test circuit for resistive load

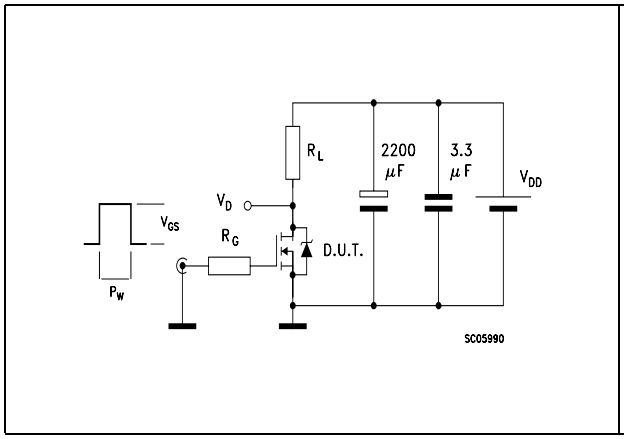


Figure 25. Gate charge test circuit

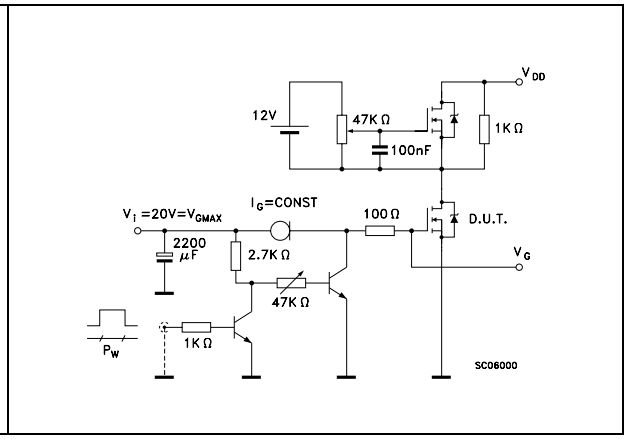


Figure 26. Test circuit for inductive load switching and diode recovery times

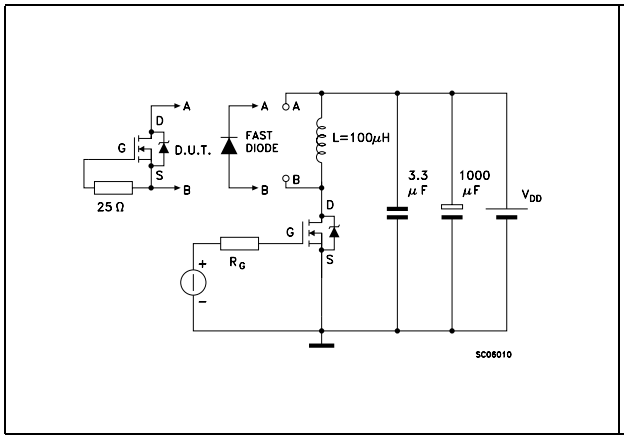


Figure 27. Unclamped Inductive load test circuit

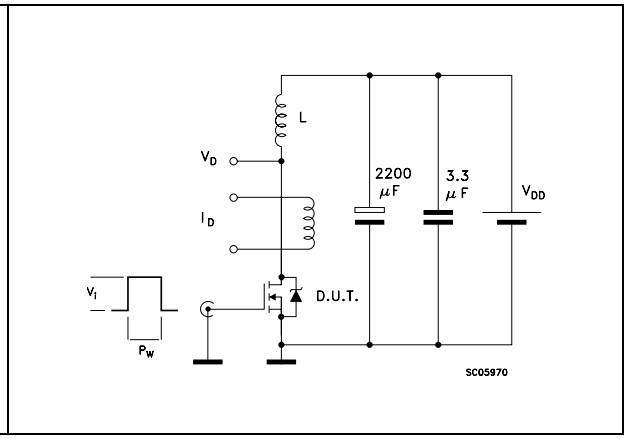


Figure 28. Unclamped inductive waveform

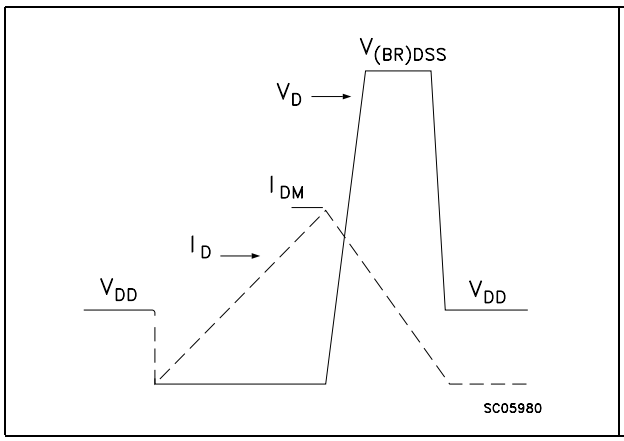
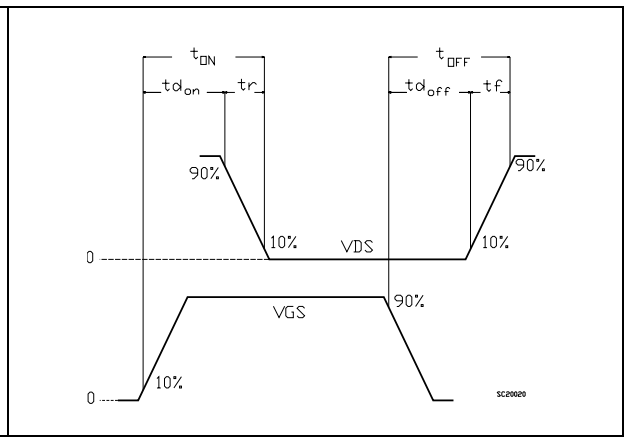


Figure 29. Switching time waveform

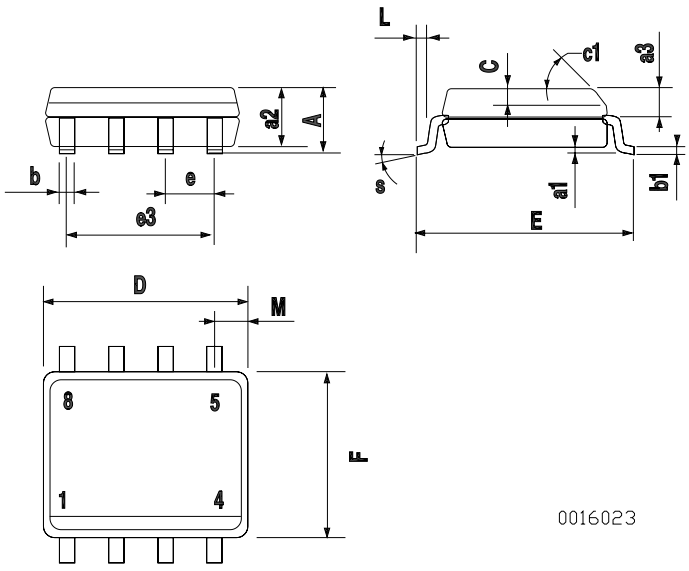


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
05-Jan-2007	1	First release
06-Mar-2007	2	Some value changed on *Table 4* ($R_{DS(on)}$ for Q2)
10-Dec-2007	3	Added E_{AS} value on *Table 2: Absolute maximum ratings*

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