MU9C8248
FDDI SRT Interface

PRELIMINARY DATA SHEET

DISTINCTIVE CHARACTERISTICS

- High-speed FDDI Source Routing and Transparent Bridging address filter supports up to sixteen ports
- Glue-free operation with the MUSIC MU9C1480 LANCAM and AMD, National Semiconductor, and Motorola FDDI chip sets
- Configurable for both Motorola and Intel processor addressing modes
- Complies with the ISO 9314 standard for FDDI
- 64-entry Instruction Buffer holds up to six down-loadable filtering and purging routines
- 64-entry Data Buffer or internal FIFO
- Automatic selection of Source Routing or Transparent filtering routines based on Transceiver output data
- Supplies proper XDAMAT, XSAMAT, SRMAT, ABORT, and CIP signals to the FDDI chip sets
- Selectable filtering options for each frame type
- Checks validity of Routing Information Field
- TTL-compatible interfaces
- Manufactured in CMOS technology
- Available in 100-pin PQFP package

GENERAL DESCRIPTION

The MU9C8248 is a Source Routing Transparent (SRT) Interface to the MUSIC Semiconductors LANCAM for use in FDDI LAN Bridges and Brouters. This interface operates in accordance with ISO standards while supporting address filtering rates up to 500,000 frames/sec for minimum-length frames.

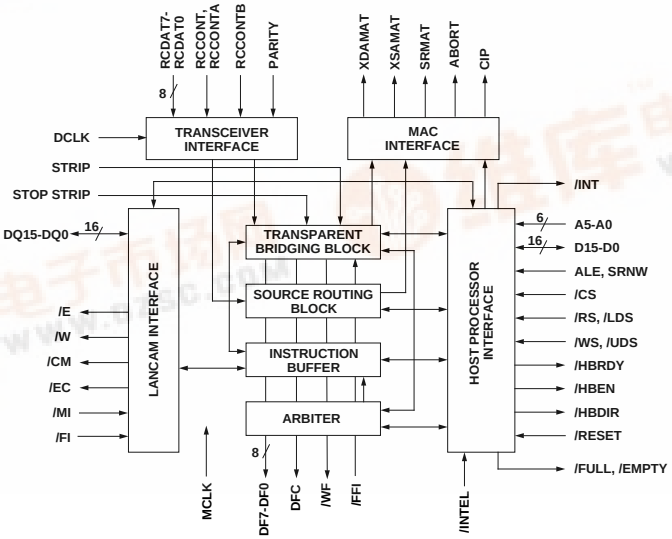
The MU9C8248 has five interfaces to provide “glue-free” address filtering. The Transceiver interface monitors receive data between the Physical Layer device and the MAC and determines whether to filter according to Source Routing or Transparent Bridging standards. The MAC interface supplies signals to instruct the FDDI chip set to reject or copy a frame. The LANCAM interface controls the companion LANCAM(s) for Transparent filtering. The Host Processor interface allows direct initialization of the MU9C8248, and downloading of the filtering and purging routines. The FIFO interface outputs new addresses received from the FDDI network.

The MU9C8248 can choose to copy or reject a frame depending on the frame's DA, RIF, and/or the frame type (MAC, LLC, or Reserved), and can perform multiple validity checks within the Routing Information Field (RIF), including general checks on every Routing Control Field (RCF) as well as multiple frame related checks.

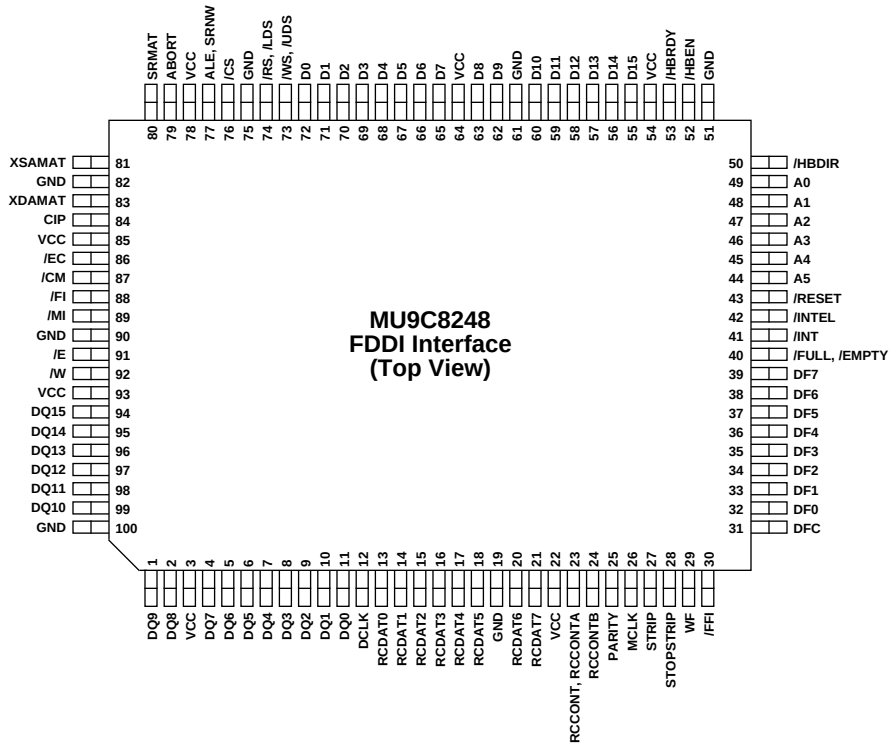
The internal RAM can store up to 64 instructions at initialization for the LANCAM to execute matching, learning, aging, and purging operations. Up to six routines can be stored here and started by the network or the Node Processor. Internal arbitration prioritizes execution of instructions by the LANCAM. A second internal RAM, which contains 64 16-bit words, is used for data buffering operations or as an internal FIFO.

With sixteen Ring-Bridge-Ring number combinations stored internally, the MU9C8248 is very well suited to operate as an address filter in multi-port Source Routing Bridge/Brouter environments.

BLOCK DIAGRAM



PINOUT DIAGRAM



PIN DESCRIPTIONS

(**/X** indicates an active LOW function)

LANCAM Interface:

DQ15–DQ0 (Data Bus, Common I/O, TTL)

The DQ15–DQ0 lines transfer data, commands and status between the MU9C8248 and the LANCAM. The direction and nature of the information that flows between the devices are determined by the states of /CM and /W.

/E (Chip Enable, Output, TTL)

The /E output enables the LANCAM while LOW and registers /W, /CM, /EC and DQ15–DQ0 (if /W is LOW) on the falling edge of /E. If /W is HIGH, data on DQ15–DQ0 from the LANCAM is valid on the rising edge of /E.

/W (Write Enable, Output, TTL)

The /W output selects the direction of data flow during a LANCAM cycle. DQ15–DQ0 write to the LANCAM if /W is LOW at the falling edge of /E. Read data is output from the LANCAM to DQ15–DQ0 on the rising edge of /E if /W is HIGH at the falling edge of /E.

/CM (Data/Command Select, Output, TTL)

The /CM signal determines whether DQ15–DQ0 contain LANCAM data or commands. /CM is LOW at the falling edge of /E for Command cycles and HIGH for Data cycles.

/EC (Enable Comparison, Output, TTL)

The /EC signal enables the LANCAM /MF pin to output the results of a comparison. If /EC is LOW at the falling edge of /E for a given cycle, the LANCAM /MF output is enabled on the rising edge of /E. If /EC is HIGH, the LANCAM /MF output is held HIGH.

/MI (Match Flag, Input, TTL)

The LANCAM /MF pin takes the MU9C8248's /MI input LOW if a valid match occurs during a Comparison cycle, and /EC was also LOW at the start of that cycle. The state of the /MI pin controls branching in the MU9C8248's routines and signalling to the FDDI chipset.

PIN DESCRIPTIONS (CONT'D)

/FI (Full Flag, Input, TTL)

The /FI input will be driven LOW by the LANCAM /FF output pin if all the LANCAM memory locations have valid contents. The status of the /FI pin can be read by the Host processor from the MU9C8248's Control register and is also used to prevent learning of new network addresses.

Transceiver Interface:

RCDAT7-RCDAT0 (Receive Data, Input, TTL)

The RCDAT pins monitor the data received by the Physical layer device from the FDDI network. RCDAT7-RCDAT0 are clocked on the rising edge of DCLK. The first symbol received from the fiber is placed on RCDAT7-RCDAT4 whereby the first bit received from the fiber is placed on RCDAT7. For chipsets using two associated Receive Data Control bits, each four-bit symbol has an associated RCCONT bit to indicate whether the four-bit symbol is to be considered a Data symbol or a Control symbol. RCCONT B is associated with RCDAT7-RCDAT4 and RCCONT A is associated with RCDAT3-RCDAT0. For chipsets using one associated Receive Data Control bit, RCCONT A becomes RCCONT and is the indicator for both symbols.

RCCONT A or RCCONT (Receive Data Control Bit, Input, TTL)

For chipsets providing two Receive Data Control bits, RCCONT A is associated with RCDAT3-RCDAT0 to indicate that the four-bit symbol being presented on RCDAT3-RCDAT0 is a Control symbol (RCCONT A is HIGH) or a Data symbol (RCCONT A is LOW).

For chipsets using only one Control bit for each symbol pair, RCCONT A becomes RCCONT and is the only Receive Data Control bit used. If RCCONT is HIGH, both RCDAT7-RCDAT4 and RCDAT3-RCDAT0 are Control symbols. If RCCONT is LOW, both RCDAT7-RCDAT4 and RCDAT3-RCDAT0 are Data symbols. RCCONT A or RCCONT is valid on the rising edge of DCLK.

RCCONT B (Receive Data Control Bit, Input, TTL)

RCCONT B is provided by the Physical layer devices, is valid on the rising edge of DCLK, and is used to indicate that the four-bit symbol being presented on RCDAT7-RCDAT4 is a Control symbol (RCCONT B is HIGH) or a Data symbol (RCCONT B is LOW). For FDDI chipsets which use only one control bit RCCONT B should be tied to GND.

PARITY (Parity, Input, TTL)

This input signal is the ODD parity of the RCDAT bus and RCCONT when the MU9C8248 is used in National Semiconductors (NS) mode. It is the ODD parity of the RCDAT bus and RCCONT A and -B when the MU9C8248 is programmed in not NS mode.

DCLK (Data Clock, Input, TTL)

The rising edge of DCLK clocks the RCDAT7-RCDAT0 data, RCCONT, RCCONTA , RCCONTB and PARITY received from the Physical layer device, which composed this data out of the data received from the FDDI network.

MAC Interface:

XDAMAT (External Destination Address Match, Output, Three-state TTL)

XDAMAT indicates, when made active, the FDDI chipset to copy a FDDI frame (this decision is made on basis of the Destination Address of the frame currently being received). The duration and polarity of XDAMAT are set in the Transparent Bridging/MAC register.

XSAMAT (External Source Address Match, Output, Three-state TTL)

XSAMAT, when active, indicates that the Source Address of the frame currently being received is found in the LANCAM database. The duration and polarity of XSAMAT are set in the Transparent Bridging/MAC register.

SRMAT (Source Routing Match, Output, Three-state TTL)

SRMAT, when active, indicates that the frame currently being received should be copied and forwarded based on information in the Routing Information Field of that frame. The duration and polarity of SRMAT are set in the Transparent Bridging/MAC register.

ABORT (Abort, Output, Three-state TTL)

ABORT is used to notify the FDDI chipset that the frame currently being received should not be copied and forwarded. The duration and polarity of ABORT are set in the Transparent Bridging/MAC register.

CIP (Compare in Progress, Output, TTL)

CIP is an output signal that National Semiconductors needs to notify their system interface that a Compare is in Progress. CIP goes HIGH on the third rising edge of DCLK after the edge that loaded a valid FC field into the MU9C8248. CIP returns LOW on the seventh rising edge of DCLK after the last byte of the Source Address field for frames not containing a Routing Information Field (RIF), or on the seventh rising edge of DCLK after the last byte of the RIF, if the frame contains such a field.

PIN DESCRIPTIONS (CONT'D)

Host Processor Interface:

ALE, SRNW (Address Latch Enable/System Read Not Write, Input, TTL)

This pin is ALE when the MU9C8248 is used in the Intel mode. A positive pulse on ALE latches the address from the multiplexed data/address lines. If the MU9C8248 is in the Motorola mode, this pin becomes SRNW, and is HIGH for a Host Processor Read cycle and LOW for a Write cycle.

/CS (Chip Select, Input, TTL)

/CS going LOW enables the Host Processor interface of the MU9C8248 for a Host Processor read or write. When /CS is HIGH, the Host Processor interface is not active.

A5–A0 (Address, Input, TTL)

The Address pins select the internal register for Host processor reads and writes. Depending on the Processor interface, the Address pins are latched by a positive pulse on ALE, or must remain stable until the rising edge of /RS, /WS, or /LDS and /UDS, as shown in the Timing diagrams.

D15–D0 (Data, Common I/O, TTL)

The Data pins transfer data between the Host Processor and the internal registers of the MU9C8248. Depending on the Processor Interface, the data pins are registered on the rising edge of /WS, or /LDS and /UDS; or must remain stable until the rising edge of /RS, or /LDS and /UDS, as shown in the Timing diagrams.

/RS, /LDS (Read Strobe/Lower Data Strobe, Input, TTL)

If the MU9C8248 is used in the Intel mode, this pin is /RS and goes LOW to begin a read cycle to the Host Processor interface. If the MU9C8248 is used in the Motorola mode, this pin is /LDS for Host processor read and write cycles and should be asserted in combination with /UDS. Data is read by the Host processor on the rising edge of /RS or /LDS, or is written into the MU9C8248 on the rising edge of /LDS.

/WS, /UDS (Write Strobe/Upper Data Strobe, Input, TTL)

If the MU9C8248 is used in the Intel mode, this pin is /WS, and goes LOW to begin a write cycle from the Host Processor interface. If the MU9C8248 is used in the Motorola mode, this pin is /UDS for Host processor read and write actions and should be asserted in combination with /LDS. Data is written into the MU9C8248 on the rising edge of /WS or /UDS, or is read from the MU9C8248 on the rising edge of /UDS.

/HBRDY (Ready, Output, Three-state TTL)

/HBRDY goes LOW to indicate to the Host processor that a data transfer is completed. After the Host processor has made /RS, /WS, or /LDS and /UDS HIGH, the MU9C8248 takes /HBRDY HIGH. /HBRDY becomes three-state one MCLK period later.

/HBEN (Data Buffer Enable, Output, TTL)

If external bi-directional buffers are needed on the D15–D0 lines, /HBEN goes LOW to enable the external buffers. /HBEN goes HIGH to disable the external buffers.

/HBDIR (Data Buffer Direction, Output, TTL)

/HBDIR controls the direction of external bi-directional buffers. /HBDIR goes LOW to read from the registers of the MU9C8248 and HIGH to write to the MU9C8248 registers.

External FIFO Interface:

DF7-DF0 (FIFO data, Output, TTL)

On the rising edge of /WF, DF7-DF0 contain a part of a new Source Address (SA), which is just learned by the LANCAM. This new SA is written into an external FIFO connected to these DF7-DF0 in six cycles.

DFC (FIFO Control data, Output, TTL)

On the rising edge of /WF, DFC indicates whether the part of the new SA present on DF7-DF0 is the first part of this SA. If this is the first of the six write cycles DFC is HIGH. For the other five cycles, DFC is LOW.

/WF (FIFO Write, Output, TTL)

On the rising edge of /WF, data on DF7-DF0 and DFC is present and can be written to e.g. an external FIFO.

/FFI (FIFO Full, Input, TTL)

When /FFI is LOW, the MU9C8248 is indicated that the external FIFO is full and can't accept new SAs. Learning of new SAs in the LANCAM is then also disabled. When /FFI is HIGH learning of new SAs both in the external FIFO and LANCAM is enabled.

Miscellaneous:

/RESET (Hardware Reset, Input, TTL)

Taking /RESET LOW for at least 1 MCLK cycle sets the MU9C8248 to a predefined state. The contents of all registers are 0000H after a Hardware reset.

/INT (Interrupt, Output, Open Drain)

This pin goes LOW to notify the Host processor that the MU9C8248 is accessing the LANCAM. /INT is synchronized on /HBRDY and becomes active directly if no Host Processor LANCAM access cycle is active or after a possible pending Host Processor LANCAM access cycle has been completed (/HBRDY is HIGH) succesfully.

PIN DESCRIPTIONS (CONT'D)

/FULL, /EMPTY (Full/Empty, Output, Open Drain)

If part of the Instruction buffer in the MU9C8248 is configured as a FIFO, this active-LOW pin can be configured to signal whether the FIFO is full (all entries contain valid data) or empty (no entry contains data). The definition of this signal is programmed in the FIFO Control/Delay register.

/INTEL (HPI Selection, Input, TTL)

The /INTEL pin identifies which type of microcontroller is connected to the Host Processor interface. This pin is set LOW for Intel-type addressing modes and HIGH for Motorola-type addressing modes.

STRIP (Strip, Input, TTL)

When STRIP has been asserted HIGH for only one MCLK period and STOP STRIP is kept LOW, the MU9C8248 stops the execution of the Routines 0 and 1 for the next FDDI frame. The result is that no signalling on the MAC interface and SA learning takes place. After STOP STRIP has been asserted for one MCLK period or any token or void frame has been received, signalling and learning is enabled again for the next FDDI frame.

STRIP is the overrulling signal which means that if STRIP is continuously kept HIGH, the assertion of STOP STRIP or the reception of a void frame or token doesn't enable the signalling and learning features of the MU9C8248.

STOP STRIP (Stop Strip, Input, TTL)

When STOP STRIP has been asserted for one MCLK period after STRIP has been HIGH for at least one MCLK period (and STRIP is LOW now), the MU9C8248 stops stripping and enables signalling and learning for the next FDDI frame.

MCLK (Master Clock, Input, TTL)

MCLK is the 25 MHz master clock. MCLK is used to clock all system parts of the MU9C8248.

VCC, GND (Positive Power Supply and Ground)

These pins are the main power supply connections to the MU9C8148. VCC must be held at +5V ± 10% relative to the GND pin, which is at 0V (system reference potential), for correct operation of the device.

FUNCTIONAL DESCRIPTION

Referring to the Block diagram shown on Page 1, the MU9C8248 consists of four functional blocks: the Transparent Bridging Block (TBB) , the Source Routing Block (SRB), the Instruction/Data Buffer (IB), and the Arbiter. Five interfaces connect the MU9C8248 to the FDDI Physical Layer device, the MAC controller or System interface, the Host processor, an external FIFO and the LANCAM. For a detailed description of FDDI frames, refer to the ISO9314-2 Standard.

Transparent Bridging Block

For all frames which do not contain a Routing Information Field (RIF), the TBB makes decisions whether to copy or discard a frame based on the Destination address (DA) and the Frame Control field (FC). If the MU9C8248 is not used in a Transparent Bridging Only mode and a frame containing an RIF is received the Source Routing Block performs the filtering actions and no DA comparison takes place. If the bridge is set for Transparent Bridging Only (the TBO bit in the Control register is HIGH), the TBB also makes copy or discard decisions (based on DA and/or FC) for frames which do contain an RIF.

The TBB parses the data as received from the Physical Layer device off the FDDI network, and indicates to the MAC interface whether to assert the XDAMAT, XSAMAT, ABORT and CIP signals. For each frame, the TBB examines the Frame Control field (FC), the Destination address (DA), and the Source address (SA), which contains the Routing Information indicator (RII). If this RII is HIGH that frame contains a RIF.

The FC field indicates whether the current frame is a Token or a regular frame. If a Token (Restricted or Non Restricted) is being received the TBB discards it, thereby having the 8248 not asserting any signals on the MAC interface. For a regular frame, the bits in the Frame Control field signify the type of frame (VOID, SMT, LLC, MAC, or Reserved) being received. The TBB decides either to copy or discard the frame directly, based on the settings in the Frame Type Selection register or to filter on the DA.

Positive or negative filtering on the DA is selected by the PONNE bit in the Transparent Bridging/MAC register. Filtering on the DA is done on all frames except for VOID-, SMT- and other types of frames with 16-bit addresses. No filtering and signalling takes place for these frames.

Positive filtering implies that a frame should be forwarded if its DA is found in the LANCAM address database. Routine 0 in the instruction buffer examines the DA to determine whether a frame should be copied or not. The results of this comparison are used to notify the FDDI chip set to copy or discard the frame. Negative filtering implies that a frame should be forwarded if its DA is not found in the address database. In this case, the MU9C8248 checks the DA and destinguishes between MAC, Broadcast, Functional and Group addresses. Based upon the settings of the Transparent Bridging/MAC register, the TBB discards a frame whose DA is either a Broadcast, Functional and/or Group address.

FUNCTIONAL DESCRIPTION (CONT'D)

Type	Condition	Action
Specifically Routed Frame	A prestored LIN-BN-LOUT combination is found in the RIF & that LOUT has occurred only once in the RIF.	Copy frame Signal MAC Interface
	A prestored LIN-BN-LOUT combination is found in the RIF & that LOUT has occurred more than one time in the RIF.	Discard frame Signal MAC Interface Increment DUPLOUT counter
	No prestored LIN-BN-LOUT combination is found in the RIF.	Discard frame Signal MAC Interface
	#RDs > SRFRD	Discard frame Signal MAC Interface
	Prestored LIN is found more than once in the RIF.	Discard frame Signal MAC interface
All Routes Explorer Frame	Last LOUT in RIF ≠ LIN	Discard frame Signal MAC Interface Increment LANIDMISMATCH counter
	#RDS > ARERD	Discard frame Signal MAC Interface Increment ARERDLIMIT-EXCEEDED counter
	Not all prestored LOUTs in RIF #RDs < ARERD	Copy frame Signal MAC Interface
	All prestored LOUTs in RIF	Discard frame Signal MAC Interface
Spanning Tree Explorer Frames	Last LOUT in RIF ≠ LIN	Discard frame Signal MAC Interface Increment LANIDMISMATCH counter
	#RDs > STERD	Discard frame Signal MAC Interface Increment STERDLIMIT-EXCEEDED counter
	Not all prestored LOUTs in RIF #RDs < STERD	Copy frame Signal MAC Interface
	All prestored LOUTs in RIF	Discard frame Signal MAC Interface Increment DUPLANIDOR-TREEERROR counter
	Bit DISSTE = ONE	Discard frame Signal MAC Interface

Note: Signalling takes place at the end of the RIF. Discard actions overrule copy actions.

Table 1: Source Routing Forwarding Conditions

FUNCTIONAL DESCRIPTION (CONT'D)

The Source Address (SA) of a frame can be used to update the database of addresses stored in the LANCAM. Routine 0 not only checks the DA but also the SA of a frame against all the entries in the database. If the SA is not found (the address is new) and if the frame received is error free, the address can be learned by adding it to the LANCAM database (by starting Routine 1) and at the same time writing it into the internal or external FIFO. The learning Routine 1 can be activated for specific frame types by setting the bits MLRN-FSLRN HIGH in the Transparent Briding/MAC register. Even SA's of erroneous frames can be learned when bit NOER of the Control register is programmed HIGH. If the SA is found in the database, XSAMAT is asserted.

Note that learning can only take place when the RII of the frame is ZERO, or for every frame when the TBO bit is HIGH. Thus, Routine 0 (performing a DA and SA comparison) is always started after the SD is received and stopped when the results of the DA and SA comparison are not needed. Routine 1 is started by the TBB block after the Error Indicator of the Frame Status field is received and all programmed conditions are met.

Source Routing Block

The Source Routing Block (SRB) only decides to copy or discard a frame if it contains an RIF.

When a frame is received, the SRB checks whether the Frame Control field indicates if a Token (Restricted or Non Restricted) is being received and no further processing is necessary. If a regular frame is being received and its RII bit is HIGH, the SRB signals the MAC interface, based on the frame type and the settings in the Frame Type Selection register, either to discard the frame; to continue to check the RIF of the frame, or to accept the frame immediately thereby having the MAC interface asserting XDAMAT.

If the RII is LOW, the SRB is not allowed to process the frame any further and waits for the next frame to arrive.

If a copy/discard decision is made based on the information in the RIF the FDDI chip set is signalled by SRMAT. The SRB examines the information contained in the Routing Control Field (RCF) which is part of the RIF. If the length (LTH) bits of the RCF indicate a length equal to zero, or contain an odd length, or if the length of the RIF is longer than the allowed length stored in the RIF Length register, reception of the frame is stopped, and the SRB indicates that the frame is to be discarded (SRMAT is not asserted). The D-bit of the RCF is used by the SRB to correctly interpret the Routing Descriptors (RDs) of the RIF.

The SRB provides for sixteen Ring(in)–Bridge–Ring(out) combinations (LIN-BN-LOUT) stored in the Source Ring Number register and Bridge/Destination Ring Number registers. LIN is the LAN ID of the ring connected to that specific port, while the BN(s) and LOUT(s) depend on the topology of the network and the bridge design. The SRB provides for checks between the LAN ring numbers and bridge numbers contained in every RD with every LIN-BN-LOUT stored, allowing the user to develop an SR(T) bridge with an internal virtual ring, or a bridge with a Full Mesh architecture.

If the Routing Type (RT) bits are equal to 0XXB, a Specifically-Routed Frame (SRF) is being received, and should be forwarded on the conditions shown in Table 1. If the RT bits are equal to 10XB, the frame is an All Routes Explorer (ARE) frame, and should be handled as shown in Table 1. If the RT bits are equal to 11XB, the frame is a Spanning Tree Explorer (STE) frame, and should be dealt with as shown in Table 1. Also described in Table 1 are the conditions on which the Error counters (Register 1DH) are incremented.

Instruction Buffer

The Instruction buffer (IB) shown in Figure 1 consists of the following: the 64-entry Instruction Storage (IS), the 64-entry Data Storage (DS), the Instruction pointer (IP), the Address pointer, the Start address registers, the FIFO, and FIFO control registers.

The IS can store up to six down-loaded routines which contain instructions for the LANCAM to execute. The IS location accessed by the Host Processor port is controlled by an auto-incrementing Address pointer, which is part of the Control register. Each instruction is a 16-bit LANCAM op-code or data word along with 3 bits that indicate the level of /W, /CM, /EC during the instruction. An S-bit is used to indicate whether this entry is a LANCAM instruction or a MU9C8248 instruction. The ST-bit indicates whether this instruction is the last instruction in a routine while bits L2-L0 indicate the length of the instruction.

The Instruction pointer (IP) points to the instruction currently being fetched. At the start of a routine (only for Routine 2-5) the IP is loaded with the appropriate Start address after which the IP is used for instruction prefetches during execution. At the start of Routine 0 and 1 the IP points at the second instruction address because of the standard instruction prefetch of the Start address used for a fast start of Routine 0 and 1. The IP can also be loaded from addresses contained in an instruction itself. For example, when a "Wait for a match" instruction is executed and no match has occurred, the IP is loaded with the address of the next instruction to execute.

The Start Address registers contain the start addresses of all six routines. When a routine is started (Routine 2-5), this address is copied into the IP and execution is started while for Routine 0 and 1 the IP is loaded with the second instruction of that routine.

Part of the ID may be used as a FIFO for data storage. Data from the routines can be moved either to or from the Host Processor interface through the FIFO or new network addresses can be moved into the FIFO by the learning process. The functionallity of the /FULL or /EMPTY flag is programmed in the FIFO Control register to prevent FIFO overflow or underflow situations.

Programming of Routines

The IS is loaded and read through the IB register in two 16-bit cycles. The first 16-bit cycle moves the data on the D15–D0 lines of the Host Processor interface into the data field of the location in the IB indicated by the Address pointer in the Control register, or vice-versa in case of a read from the IB

FUNCTIONAL DESCRIPTION (CONT'D)

register. The second 16-bit word is written to or read from the /W, /CM, /EC, /SP, S, L2-L0 bits of that same location.

The Control register contains an Address pointer that selects the accessed location in the IS (location 00H-3FH) and DS (location 40H-7FH). The Address pointer can be read out or overwritten. It is incremented when the Host processor has completed the two write or read cycles to/from one location of the IB.

Execution of Routines

Routines in the instruction buffer can be started either by the Host processor (Routines 2-5 only) or the Transparent Bridging Block (Routines 0-1 only). If a routine is started by the Host processor, it is started immediatly if the arbiter allows it. Otherwise the start is delayed as long as necessary.

The TBB starts Routine 0 and/or 1 when the enable bit of that routine is set HIGH. Routines 0, used for DA and SA comparison is started directly after the SD has been received or is started with a delay if this is programmed in the delay bits of the FIFO Control/Delay register, while Routine 1, used for the learning of network addresses, is started after the Error indicator of the FS field has been received.

Arbiter

The Arbiter block has two tasks: 1) Arbitration between the execution of different routines stored in the Instruction Buffer, 2) Arbitration between the execution of routines in the Instruction buffer and Host Processor access to the LANCAM.

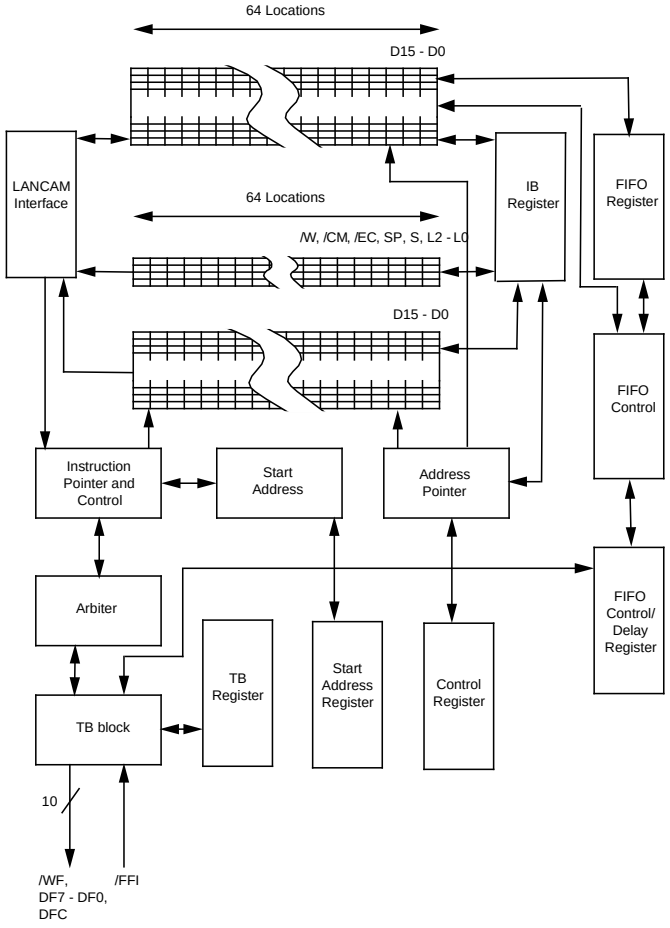


Figure 1: The Instruction Buffer

FUNCTIONAL DESCRIPTION (CONT'D)

Routine Priorities

Of the six routines stored in the Instruction buffer, execution of Routines 0–1 is time critical because there is a direct relation to the incoming data stream of the FDDI network; therefore, they have the highest priority and cannot be interrupted by other routines. The time length of Routines 0 plus Routine 1 must fit in the time interval of a minimum length frame. Routines 2-5 have a lower priority and a routine can be interrupted by all routines having a lower number.

During execution of Routine 0–1, no lower priority routine can be started. When during the execution of a routine, a second routine is programmed to be started and execution of the first routine has ended, this second routine is started immediately afterward. A currently running routine can be interrupted by a higher priority routine, and the lower priority routine will re-start from the beginning immediately after the interrupting routine has finished.

Host Processor Access

The Host processor is able to control the LANCAM directly via the MU9C8248, but is given access only when no pre-stored routine is being executed. The /INT pin will indicate when a pre-stored routine is exercizing the LANCAM. If execution of a pre-stored routine takes place during Host processor interaction, the current processor cycle is completed before the Host processor is interrupted, so that while the results of the Host processor interactions can not be guaranteed, it is notified that it has been interrupted. The MU9C8248 releases /INT after it has finished its LANCAM access. If /INT remains deasserted during Host processor activity, the Host processor has been able to complete its instruction sequence.

MAC Interface

The TBB and/or the SRB notify the MAC interface to copy or reject a frame through the XDAMAT, XSAMAT, SRMAT, ABORT and CIP pins. Polarity and assertion length of the signals can be programmed in the Transparent Bridging/MAC register.

Transceiver Interface

The MU9C8248 connects to the received data bus between the Physical Layer and MAC device. The encoded data received from the FDDI Physical Layer Device is input to the RCDAT pin clocked by the DCLK clock.

The Transceiver interface notifies the TBB and the SRB that it has detected a Starting Delimiter in the incoming data stream and to begin parsing the other fields of the frame. The Transceiver interface performs a number of error checks: whether the data contained any control characters before an ED was received; that no second SD is received before an ED is received. In any of these cases, both the TBB and SRB are notified and reception of data is cancelled. Also checked are: the correctness of the FCS, the value of the Error indicator symbol in the ED.

Host Processor Interface

The Host Processor interface is configured for Intel or Motorola addressing modes using the /INTEL pin. In both modes the MU9C8248 is a slave on the processor bus and can be programmed using the registers described in this document. The MU9C8248 provides /HBEN and /HBDIR to enable the user to add external bi-directional buffers in the D15-D0 datalines. In Intel mode the Host Processor interface can be used in a system with multiplexed or non-multiplexed data and address lines. The Host Processor interface can only be used for 16-bit transfers.

The Register Set

The internal Register set is detailed following the description of the Instruction set. The registers are selected by the A5–A0 Address bus, and written to or read from as shown in the Timing diagrams.

INSTRUCTION SET DESCRIPTION

Instruction: LANCAM Instruction
Binary Op Code: iiii iiii iiii iiii wce0 slll
- **i Instruction Code (see The LANCAM Handbook)**
- **w The state of /W**
- **c The state of /CM**
- **e The state of /EC**
- **s Stop routine**
- **l Instruction length**

This instruction transfers data or commands to or from the LANCAM. Instructions from the LANCAM instruction set are described in the LANCAM Handbook. The state of the control outputs /W, /CM and /EC at the falling edge of /E for this cycle are defined by w, c, and e. If s is set HIGH, the instruction is the last instruction of the routine and execution of the routine is stopped after this instruction has been executed. The length of the instruction is determined by l. For the coding of the l bits refer to Table 2.

Instruction: Wait for match for yyyyB + 5 cycles, if no match then execute at address aaaaaaB.
Binary Op Code: 0010 yyyy rraa aaaa xxx1
- **y Wait period**
- **r Reserved (set LOW)**
- **a Address**
- **x Don't Care**

This instruction waits for a maximum period of yyyyB + 5 clock cycles for the /MI input to become active. If no match condition occurs during that period, a branch is executed to the address which is stored in the “a” bits of the instruction. If a match condition is detected, execution proceeds to the instruction in the next address. This instruction is not needed for the basic DA and/or SA comparison.

Instruction: Move DA part 0 to DQ15–DQ0.
Binary Op Code: 0011 0000 0000 0000 0ce1 slll
- **c The state of /CM**
- **e The state of /EC**
- **s Stop routine**
- **l Instruction length**

The “Move DA part 0 to DQ15–DQ0” instruction places the least significant part of the DA address (bits 15–0) on the DQ15–DQ0 lines. The control outputs /CM and /EC at the falling edge of /E for this cycle are defined by c and e. If s is set HIGH, the instruction is the last instruction of the routine and execution of the routine is stopped after this instruction has been executed. The length of the instruction is determined by l. For the coding of the l bits refer to Table 2.

Instruction: Move DA part 1 to DQ15–DQ0.
Binary Op Code: 0011 0000 0000 0001 0ce1 slll
- **c The state of /CM**
- **e The state of /EC**
- **s Stop routine**
- **l Instruction length**

The “Move DA part 1 to DQ15–DQ0” instruction places DA address bits 31–16 on the DQ15–DQ0 lines. The control outputs /CM and /EC at the falling edge of /E for this cycle are defined by c and e. If s is set HIGH, the instruction is the last instruction of the routine and execution of the routine is stopped after this instruction has been executed. The length of the instruction is determined by l. For the coding of the l bits refer to Table 2.

Instruction: Move DA part 2 to DQ15–DQ0.
Binary Op Code: 0011 0000 0000 0010 0ce1 slll
- **c The state of /CM**
- **e The state of /EC**
- **s Stop routine**
- **l Instruction length**

This instruction places the most significant part of the DA address (bits 47–32) on the DQ15–DQ0 lines. The control outputs /CM and /EC at the falling edge of /E for this cycle are defined by c and e. If s is set HIGH, the instruction is the last instruction of the routine and execution of the routine is stopped after this instruction has been executed. The length of the instruction is determined by l. For the coding of the l bits refer to Table 2.

Instruction: Move SA part 0 to DQ15–DQ0.
Binary Op Code: 0011 0000 0000 0011 0ce1 slll
- **c The state of /CM**
- **e The state of /EC**
- **s Stop routine**
- **l Instruction length**

The “Move SA part 0 to DQ15–DQ0” instruction places the least significant part of the SA address (bits 15–0) on the DQ15–DQ0 lines. The control outputs /CM and /EC at the falling edge of /E for this cycle are defined by c and e. If s is set HIGH, the instruction is the last instruction of the routine and execution of the routine is stopped after this instruction has been executed. The length of the instruction is determined by l. For the coding of the l bits refer to Table 2.

Instruction: Move SA part 1 to DQ15–DQ0.
Binary Op Code: 0011 0000 0000 0100 0ce1 slll
- **c The state of /CM**
- **e The state of /EC**
- **s Stop routine**
- **l Instruction length**

The “Move SA part 1 to DQ15–DQ0” instruction places SA address bits 31–16 on the DQ15–DQ0 lines. The control outputs /CM and /EC at the falling edge of /E for this cycle are defined by c and e. If s is set HIGH, the instruction is the last instruction of the routine and execution of the routine is stopped after this instruction has been executed. The length of the instruction is determined by l. For the coding of the l bits refer to Table 2.

Instruction: Move SA part 2 to DQ15–DQ0.
Binary Op Code: 0011 0000 0000 0101 0ce1 slll
- **c The state of /CM**
- **e The state of /EC**
- **s Stop routine**
- **l Instruction length**

This instruction places the most significant part of the SA address (bits 47–32) on the DQ15–DQ0 lines. The control outputs /CM and /EC at the falling edge of /E for this cycle are defined by c and e. If s is set HIGH, the instruction is the last

INSTRUCTION SET DESCRIPTION (CONT'D)

instruction of the routine and execution of the routine is stopped after this instruction has been executed. The length of the instruction is determined by l. For the coding of the l bits refer to Table 2.

Instruction: Move data from address 1aaaaaaB to DQ15–DQ0.
Binary Op Code: 0100 rrrr r1aa aaaa 0ce1 slll

- **r Reserved**
- **a Address**
- **c The state of /CM**
- **e The state of /EC**
- **s Stop routine**
- **l Instruction length**

The "Move data from address 1aaaaaaB to DQ15–DQ0" instruction places the contents of the address specified by the "a" bits on the DQ15–DQ0 lines. The control outputs /CM and /EC at the falling edge of /E for this cycle are defined by c and e. If s is set HIGH, the instruction is the last instruction of the routine and execution of the routine is stopped after this instruction has been executed. The length of the instruction is determined by l. For the coding of the l bits refer to Table 2.

Instruction: Move data from DQ15–DQ0 to address 1aaaaaaB.
Binary Op Code: 0101 rrrr r1aa aaaa 1ce1 slll

- **r Reserved**
- **a Address**
- **c The state of /CM**
- **e The state of /EC**
- **s Stop routine**
- **l Instruction length**

This instruction places the values on the DQ15–DQ0 lines in the address specified by the "a" bits. The control outputs /CM and /EC at the falling edge of /E for this cycle are defined by c and e. If s is set HIGH, the instruction is the last instruction of the routine and execution of the routine is stopped after this instruction has been executed. The length of the instruction is determined by l. For the coding of the l bits refer to Table 2.

Instruction: Move data from the FIFO to DQ15–DQ0.
Binary Op Code: 0110 rrrr rrrr rrrr 0ce1 slll

- **r Reserved**
- **c The state of /CM**
- **e The state of /EC**
- **s Stop routine**
- **l Instruction length**

The "Move data from the FIFO to DQ15–DQ0" instruction places the contents of the next FIFO location on the DQ15–DQ0 lines. The control outputs /CM and /EC at the falling edge of /E for this cycle are defined by c and e. If s is set HIGH, the instruction is the last instruction of the routine and execution of the routine is stopped after this instruction has been executed. The length of the instruction is determined by l. For the coding of the l bits refer to Table 2.

Instruction: Move data from DQ15–DQ0 to the FIFO.
Binary Op Code: 0111 rrrr rrrr rrrr 1ce1 slll

- **r Reserved**
- **c The state of /CM**
- **e The state of /EC**
- **s Stop routine**
- **l Instruction length**

This instruction places the values on the DQ15–DQ0 lines into the FIFO. The control outputs /CM and /EC at the falling edge of /E for this cycle are defined by c and e. If s is set HIGH, the instruction is the last instruction of the routine and execution of the routine is stopped after this instruction has been executed. The length of the instruction is determined by l. For the coding of the l bits refer to Table 2.

lll	/E HIGH	/E LOW	Instruction Length
000B	1 MCLK	1 MCLK	2 MCLK
001B	1 MCLK	2 MCLK	3 MCLK
010B	1 MCLK	3 MCLK	4 MCLK
011B	2 MCLK	1 MCLK	3 MCLK
100B	3 MCLK	1 MCLK	4 MCLK

Note: An 300XH instruction executed after an not 300XH instruction takes one extra MCLK cycle.

Table 2: Instruction Length

REGISTER SET DESCRIPTION

BIT	NAME	DESCRIPTION
00H: Control Register		
15	RESET	If RESET is HIGH, a reset of the MU9C8248 takes place.
14	NNS	If NNS is HIGH, the MU9C8248 is programmed for the Motorola or AMD FDDI chipset. If NNS is set LOW, the MU9C8248 is programmed for the NS FDDI chipset.
13	LSASR	If LSASR is HIGH, learning of new network addresses is enabled for frames containing a RIF. If LSASR is LOW, learning of new addresses of frames with RIF is disabled. If TBO is HIGH this LSASR is "don't care".
12	TBO	If TBO is HIGH, all incoming frames are filtered by the Transparent Bridging block only. No SR bridging takes place.
11	DISSTE	If DISSTE is HIGH, all Spanning Tree Explorer frames are discarded. The MU9C8248 signals the FDDI chipset to flush these frames. If DISSTE is LOW, STE frames are accepted per the programmed filtering criteria.
10	NFF	NFF indicates the level of the /FI input.
9	/INT	/INT is read-only. If /INT is LOW an direct LANCAM access by the Host Processor has been interrupted by the execution of a MU9C8248 routine. If /INT is HIGH all direct LANCAM accesses by Host Processor were successfull. /INT is reset HIGH after read out.
8	RDFCP	If RDFCP is HIGH, access to the Error Counter 1DH is reset to point to DUPL7–0 and IRI7–0.
7	NOER	If NOER is programmed HIGH, learning of new network addresses is enabled for frames that contain errors. If NOER is LOW only network addresses from frames, not containing any errors, are learned.
6–0	APR6–0	APR6–0 point to the location in the IB which can be accessed through the IB Register.
01H: Frame Type Selection Register		
15	MSRENBL	If MSRENBL is LOW, every MAC frame containing an RIF is discarded. The FDDI chipset is signalled to flush the frame. If MSRENBL is HIGH, the MSRFILT bit determines if the frame is filtered or copied directly. MSRENBL is “don't care” if TBO is HIGH.
14	MSRFILT	If MSRFILT is LOW, the MU9C8248 signals the FDDI chipset to copy every MAC frame containing an RIF. If MSRFILT is HIGH, the MU9C8248 checks the RIF and forwards the frame if the programmed forwarding conditions are met. MSRFILT is “don't care” if TBO is HIGH.
13	LSRENBL	If LSRENBL is LOW, every LLC frame containing an RIF is discarded. The FDDI chipset is signalled to flush the frame. If LSRENBL is HIGH, the LSRFILT bit determines if the frame is filtered or copied directly. LSRENBL is “don't care” if TBO is HIGH.
12	LSRFILT	If LSRFILT is LOW, the MU9C8248 signals the FDDI chipset to copy every LLC frame containing an RIF. If LSRFILT is HIGH, the MU9C8248 checks the RIF and forwards the frame if the programmed forwarding conditions are met. LSRFILT is “don't care” if TBO is HIGH.
11	FISRENBL	If FISRENBL is LOW, every Reserved for Implementer frame containing an RIF is discarded. The FDDI chipset is signalled to flush the frame. If FISRENBL is HIGH, the FISRFILT bit determines if the frame is filtered or copied directly. This bit is “don't care” if TBO is HIGH.
10	FISRFILT	If FISRFILT is LOW, the MU9C8248 signals the FDDI chipset to copy every Reserved for Implementer frame containing an RIF. If FISRFILT is HIGH, the MU9C8248 checks the RIF and forwards the frame if the programmed forwarding conditions are met. This bit is “don't care” if TBO is HIGH.
9	FSSRENBL	If FSSRENBL is LOW, every Reserved for Future Standardization frame containing an RIF is discarded. The FDDI chipset is signalled to flush the frame. If FSSRENBL is HIGH, the FSSRFILT bit determines if the frame is filtered or copied directly. This bit is “don't care” if TBO is HIGH.
8	FSSRFILT	If FSSRFILT is LOW, the MU9C8248 signals the FDDI chipset to copy every Reserved for Future Standardization frame containing an RIF. If FSSRFILT is HIGH, the MU9C8248 checks the RIF and forwards the frame if the programmed forwarding conditions are met. This bit is “don't care” if TBO is HIGH.
7	MTRENBL	If MTRENBL is LOW, every MAC frame not containing an RIF is discarded. The FDDI chipset is signalled to flush the frame. If MTRENBL is HIGH, the MTRFILT bit determines if the frame is filtered or copied directly. If TBO is HIGH, filtering is also done on MAC frames containing an RIF.
6	MTRFILT	If MTRFILT is LOW, the MU9C8248 signals the MAC to copy every MAC frame not containing an RIF. If MTRFILT is HIGH, the MU9C8248 checks the DA and forwards the frame if the forwarding conditions are met, whether or not the frame contains an RIF.
5	LTRENBL	If LTRENBL is LOW, every LLC frame not containing an RIF is discarded. The FDDI chipset is signalled to flush the frame. If LTRENBL is HIGH, the LTRFILT bit determines if the frame is filtered or copied directly. if TBO is HIGH, filtering is also done on LLC frames containing an RIF.
4	LTRFILT	If LTRFILT is LOW, the MU9C8248 signals the FDDI chipset to copy every LLC frame not containing an RIF. If LTRFILT is HIGH, the MU9C8248 checks the DA and forwards the frame if the forwarding conditions are met, whether or not the frame contains an RIF.

REGISTER SET DESCRIPTION (CONT'D)

BIT	NAME	DESCRIPTION
3	FITRENBL	If FITRENBL is LOW, every Reserved for Implementer frame not containing an RIF is discarded. The FDDI chipset is signalled to flush the frame. If FITRENBL is HIGH, the FITRFILT bit determines if the frame is filtered or copied directly. If TBO is HIGH, filtering is also done on Reserved for Implementer frames with an RIF.
2	FITRFILT	If FITRFILT is LOW, the MU9C8248 signals the FDDI chipset to copy every Reserved for Implementer frame not containing an RIF. If FITRFILT is HIGH the MU9C8248 checks the DA and forwards the frame if the forwarding conditions are met, whether or not the frame contains an RIF.
1	FSTRENBL	If FSTRENBL is LOW, every Reserved for Future Standardization frame not containing an RIF is discarded. The FDDI chipset is signalled to flush the frame. If FITRENBL is HIGH, the FITRFILT bit determines if the frame is filtered or copied directly. If TBO is HIGH, filtering is also done on Reserved for Future Standardization frames with an RIF.
0	FSTRFILT	If FSTRFILT is LOW, the MU9C8248 signals the MAC chip to copy every Reserved for Future Standardization frame not containing an RIF. If FSTRFILT is HIGH, the MU9C8248 checks the DA and forwards the frame if the forwarding conditions are met, whether or not the frame contains an RIF.
02H: Transparent Bridging/MAC Register		
15	PONNE	If PONNE is LOW, the MU9C8248 performs negative filtering (Routine 0) for frames without an RIF, or for all frames when TBO is HIGH. If PONNE is HIGH positive filtering is performed either on frame without an RIF or on all frames.
14	DISGA	If DISGA is LOW, all frames with a group address as DA and not containing an RIF (or all frames with a group address as DA when TBO = HIGH) are filtered if PONNE is LOW. When DISGA is HIGH all frames with group addresses are discarded. If PONNE is HIGH, this bit becomes "don't care".
13	DISBA	If DISBA is LOW, all frames with a DA containing a broadcast address and not containing an RIF (or all frames with a DA containing a broadcast address when TBO = HIGH) are filtered when PONNE is also programmed LOW. When DISBA is HIGH all frames with broadcast addresses are discarded. If PONNE is set HIGH, this bit becomes "don't care".
12	DISFA	If DISFA is LOW, all frames with a functional address as DA and not containing an RIF (or all frames with a functional address as DA when TBO = HIGH) are filtered when PONNE is made LOW. When DISFA is HIGH all frames with functional addresses are discarded. If PONNE is HIGH, this bit becomes "don't care".
11	MLRN	If MLRN is LOW, no learning of network addresses from MAC frames takes place. If this bit is set HIGH, learning of addresses from MAC frames takes place by starting Routine 1 (if starting is enabled) and placing new SA's in the FIFO, if the frame doesn't contain an RIF (or for all MAC frames if TBO or LSASR is HIGH).
10	LLRN	If LLRN is LOW, no learning of addresses from LLC frames takes place. If this bit is set HIGH, learning of addresses from LLC frames takes place by starting Routine 1 (if starting is enabled) and placing new SA's in the FIFO, if the frame doesn't contain an RIF (or for all LLC frames if TBO or LSASR is HIGH).
9	FILRN	If FILRN is LOW, no learning of addresses from Reserved for Implementer frames takes place. If this bit is HIGH, learning of addresses from reserved Reserved for Implementer frames takes place by starting Routine 1 (if starting is enabled) and placing new SA's in the FIFO, if the frame doesn't contain an RIF (or for all reserved type1 frames if TBO or LSASR is HIGH).
8	FSLRN	If FSLRN is LOW, no learning of addresses from Reserved for Future Standardization frames takes place. If FSLRN is set HIGH, learning of addresses from Reserved for Future Standardization frames takes place by starting Routine 1 (if starting is enabled) and placing new SA's in the FIFO, if the frame doesn't contain an RIF (or for all Reserved for Future Standardization frames if TBO or LSASR is HIGH).
7	XDAP	This bit determines the polarity of the XDAMAT output. If this bit is set HIGH the XDAMAT signal is active HIGH. If XDAP is LOW, XDAMAT is active LOW.
6	XSAP	This bit determines the polarity of the XSAMAT output. If this bit is set HIGH the XSAMAT signal is active HIGH. If XSAP is LOW, XSAMAT is active LOW.
5	XSRP	This bit determines the polarity of the SRMAT output. If this bit is set HIGH the SRMAT signal is active HIGH. If XSRP is LOW, SRMAT is active LOW.
4	XABP	This bit determines the polarity of the ABORT output. If this bit is set HIGH the ABORT signal is active HIGH. If XABP is LOW, ABORT is active LOW.
3	XDAL	If this bit is LOW, XDAMAT is deasserted one DCLK period after it has been asserted. If this bit is HIGH, XDAMAT is deasserted at the first Control symbol received.
2	XSAL	If XSAL is LOW, XSAMAT is deasserted one DCLK period after it has been asserted. If this bit is HIGH, XSAMAT is deasserted at the first Control symbol received.
1	XSRL	If this bit is LOW, SRMAT is deasserted one DCLK period after it has been asserted. If this bit is HIGH, SRMAT is deasserted at the first Control symbol received.
0	XABL	If XABL is LOW, ABORT is deasserted one DCLK period after it has been asserted. If XABL is HIGH, ABORT is deasserted at the first Control symbol received.

REGISTER SET DESCRIPTION (CONT'D)

BIT	NAME	DESCRIPTION
03H: RIF Length/MAC Register		
15–12	SRFRD3–0	Bits SRFRD3–0 contain the maximum number of RDs–1 for an SRF frame. SRF frames containing more RDs are not copied by the MU9C8248.
11–8	ARERD3–0	Bits ARERD3–0 contain the maximum number of RDs–1 for an ARE frame. ARE frames containing more RDs are rejected.
7-4	STERD3–0	Bits STERD3–0 contain the maximum number of RDs–1 an STE frame can contain. If an STE frame contains more RDs, it is rejected.
3	EXDA	If EXDA is set HIGH, output XDAMAT is enabled. If EXDA is LOW no signalling takes place on XDAMAT.
2	EXSA	If EXSA is set HIGH, output XSAMAT is enabled. If this bit is set LOW no signalling takes place on XSAMAT.
1	EXSR	If this bit is set HIGH, output SRMAT is enabled. If EXSR is set LOW no signalling takes place on SRMAT.
0	EAB	If EAB is HIGH, output ABORT is enabled. If EAB is LOW no signalling takes place on ABORT.
04H: Source Ring Number Register		
15–12	ID3–0	ID3–0 contain the version number of the MU9C8248. The current version number is 0000B.
11–0	SR11–0	SR11–0 contain the 12-bit Ring Number for this port (Source Ring Number).
05H: Bridge/Destination Ring Number Register A		
15–12	BNA3–0	BNA3–0 contain the Bridge Number for remote port A.
11–0	DRA11–0	DRA11–0 contain the Destination Ring Number for remote port A. If DRA11–0 are all LOW, Bridge/Destination Ring combination A is disabled and doesn't take part in SRB comparisons
.		
06H: Bridge/Destination Ring Number Register B		
15–12	BNB3–0	BNB3–0 contain the Bridge Number for remote port B.
11–0	DRB11–0	DRB11–0 contain the Destination Ring Number for remote port B. If DRB11–0 are all LOW, Bridge/Destination Ring combination B is disabled and doesn't take part in SRB comparisons.
07H: Bridge/Destination Ring Number Register C		
15–12	BNC3–0	BNC3–0 contain the Bridge Number for remote port C.
11–0	DRC11–0	DRC11–0 contain the Destination Ring Number for remote port C. If DRC11–0 are all LOW, Bridge/Destination Ring combination C is disabled and doesn't take part in SRB comparisons.
08H: Bridge/Destination Ring Number Register D		
15–12	BND3–0	BND3–0 contain the Bridge Number for remote port D.
11–0	DRD11–0	DRD11–0 contain the Destination Ring Number for remote port D. If DRD11–0 are all LOW, Bridge/Destination Ring combination D is disabled and doesn't take part in SRB comparisons.
09H: Bridge/Destination Ring Number Register E		
15–12	BNE3–0	BNE3–0 contain the Bridge Number for remote port E.
11–0	DRE11–0	DRE11–0 contain the Destination Ring Number for remote port E. If DRE11–0 are all LOW, Bridge/Destination Ring combination E is disabled and doesn't take part in SRB comparisons.
0AH: Bridge/Destination Ring Number Register F		
15–12	BNF3–0	BNF3–0 contain the Bridge Number for remote port F.
11–0	DRF11–0	DRF11–0 contain the Destination Ring Number for remote port F. If DRF11–0 are all LOW, Bridge/Destination Ring combination F is disabled and doesn't take part in SRB comparisons.
0BH: Bridge/Destination Ring Number Register G		
15–12	BNG3–0	BNG3–0 contain the Bridge Number for remote port G.
11–0	DRG11–0	DRG11–0 contain the Destination Ring Number for remote port G. If DRG11–0 are all LOW, Bridge/Destination Ring combination G is disabled and doesn't take part in SRB comparisons.

REGISTER SET DESCRIPTION (CONT'D)

BIT	NAME	DESCRIPTION

0CH: Bridge/Destination Ring Number Register H

15–12	BNH3–0	BNH3–0 contain the Bridge Number for remote port H.
11–0	DRH11–0	DRH11–0 contain the Destination Ring Number for remote port H. If DRH11–0 are all LOW, Bridge/Destination Ring combination H is disabled and doesn't take part in SRB comparisons.

0DH: Bridge/Destination Ring Number Register I

15–12	BNI3–0	BNI3–0 contain the Bridge Number for remote port I.
11–0	DRI11–0	DRI11–0 contain the Destination Ring Number for remote port I. If DRI11–0 are all LOW, Bridge/Destination Ring combination I is disabled and doesn't take part in SRB comparisons.

0EH: Bridge/Destination Ring Number Register J

15–12	BNJ3–0	BNJ3–0 contain the Bridge Number for remote port J.
11–0	DRJ11–0	DRJ11–0 contain the Destination Ring Number for remote port J. If DRJ11–0 are all LOW, Bridge/Destination Ring combination J is disabled and doesn't take part in SRB comparisons.

0FH: Bridge/Destination Ring Number Register K

15–12	BNK3–0	BNK3–0 contain the Bridge Number for remote port K.
11–0	DRK11–0	DRK11–0 contain the Destination Ring Number for remote port K. If DRK11–0 are all LOW, Bridge/Destination Ring combination K is disabled and doesn't take part in SRB comparisons.

10H: Bridge/Destination Ring Number Register L

15–12	BNL3–0	BNL3–0 contain the Bridge Number for remote port L.
11–0	DRL11–0	DRL11–0 contain the Destination Ring Number for remote port L. If DRL11–0 are all LOW, Bridge/Destination Ring combination L is disabled and doesn't take part in SRB comparisons.

11H: Bridge/Destination Ring Number Register M

15–12	BNM3–0	BNM3–0 contain the Bridge Number for remote port M.
11–0	DRM11–0	DRM11–0 contain the Destination Ring Number for remote port M. If DRM11–0 are all LOW, Bridge/Destination Ring combination M is disabled and doesn't take part in SRB comparisons.

12H: Bridge/Destination Ring Number Register N

15–12	BNN3–0	BNN3–0 contain the Bridge Number for remote port N.
11–0	DRN11–0	DRN11–0 contain the Destination Ring Number for remote port N. If DRN11–0 are all LOW, Bridge/Destination Ring combination N is disabled and doesn't take part in SRB comparisons.

13H: Bridge/Destination Ring Number Register O

15–12	BNO3–0	BNO3–0 contain the Bridge Number for remote port O.
11–0	DRO11–0	DRO11–0 contain the Destination Ring Number for remote port O. If DRO11–0 are all LOW, Bridge/Destination Ring combination O is disabled and doesn't take part in SRB comparisons.

14H: Bridge/Destination Ring Number Register P

15–12	BNP3–0	BNP3–0 contain the Bridge Number for remote port P.
11–0	DRP11–0	DRP11–0 contain the Destination Ring Number for remote port P. If DRP11–0 are all LOW, Bridge/Destination Ring combination P is disabled and doesn't take part in SRB comparisons.

15H: Instruction Buffer (IB) Register

First Access

15–0	IB15–IB0	IB15–0 contain the information that is written to or read from the D15–0 bits of the IB location pointed to by the address pointer.

REGISTER SET DESCRIPTION (CONT'D)

BIT	NAME	DESCRIPTION
Second Access		
15	/W	If LOW, data is written to the LANCAM. If HIGH, data is read from the LANCAM.
14	/CM	If LOW, this instruction is a command. If HIGH, this instruction is data.
13	/EC	If LOW, the LANCAM will output /MF in the case of a match. If HIGH, /MF is held HIGH.
12	SP	Special instruction bit. If SP is HIGH, the instruction stored at the location pointed to by the address pointer is a MU9C8248 instruction. If SP is LOW, the instruction is a LANCAM instruction.
11	S	If S is HIGH, this instruction is the last instruction of this routine. Execution of the routine is stopped after this instruction has been completed.
10-8	L2-L0	The bits L2-L0 determine the length of the instruction. For detailed information refer to table 2.
7–0	Reserved	
16H: Start Register I		
15	ENABLE1	When ENABLE1 is HIGH, Routine 1 which is used for network address learning, is enabled and can be started by the Transparent Bridging Block (TBB). If ENABLE1 is LOW no start of Routine 1 can take place.
14	Reserved	
13–8	STARTI5–0	STARTI5–0 contain the Start Address of Routine 1.
7	ENABLE0	When ENABLE0 is HIGH, Routine 0 which is used for DA and SA comparisons, is enabled and can be started by the Transparent Bridging Block (TBB). If ENABLE0 is LOW no start of Routine 0 can take place.
6	Reserved	
5–0	STARTO5–0	STARTO5–0 contain the Start Address of Routine 0.
17H: Start Register II		
15	START3	When START3 is set HIGH, Routine 3 is started. START3 is reset after execution has been completed.
14	Reserved	
13–8	STARTIII5–0	STARTIII5–0 contain the Start Address of Routine 3.
7	START2	When START2 is programmed HIGH, Routine 2 is started. START2 is reset after execution of Routine 2 has been completed.
6	Reserved	
5–0	STARTII5–0	STARTII5–0 contain the Start Address of Routine 2.
18H: Start Register III		
15	START5	When START5 is set HIGH, Routine 5 is started. START5 is reset after execution has been completed.
14	Reserved	
13–8	STARTV5–0	STARTV5–0 contain the Start Address of Routine 5
7	START4	When START4 is programmed HIGH, Routine 4 is started. START4 is reset after execution of Routine 4 has been completed.
6	Reserved	
5–0	STARTIV5–0	STARTIV5–0 contain the Start Address of Routine 4.
19H: FIFO Control/Delay Register		
15–12	DELAY3-0	These bits contain the delay (in MCLK periods) of the start of routine 0 counted from the moment that the SD is received.
11	ENTRXF	If ENTRXF is HIGH, a copy of the new network address, that is learned by placing it in the LANCAM, is transferred into the external FIFO. If ENTRXF is LOW no transfer takes place.
10	ENTRIF	If ENTRIF is HIGH, a copy of the new network address, that is learned by placing it in the LANCAM, is transferred into the internal FIFO. If ENTRIF is LOW no address transfer takes place.
9	RESETIF	If RESETIF is HIGH, the FIFO read and write pointer are reset to location 3FH of the DS. All data stored in the FIFO is lost after a reset.
8	F/E	If F/E is made HIGH the /FULL, /EMPTY output functions like a FIFO full flag. At the moment the FIFO is filled, the /FULL signal is made LOW. If F/E is LOW, the /FULL, /EMPTY output acts like a FIFO empty flag. It goes LOW when the FIFO is empty.
7	ENIF	Enables/disables the FIFO function in the IB. If ENIF is HIGH, the FIFO function is active. If ENIF is LOW the FIFO function is inactive and the /FULL, /EMPTY signal is set HIGH.

REGISTER SET DESCRIPTION (CONT'D)

BIT	NAME	DESCRIPTION
6	Reserved	
5–0	LIM5–0	LIM5–0 contain the lowest location in the DS, the FIFO can use. The FIFO is located between LIM5–0 and 7FH.

1AH: FIFO Register

15–0	FF15–0	FF15–0 contain data that is written in, or read from the FIFO. This data is stored or read from in the location pointed to by the FIFO pointer. If the /FULL flag indicates that the FIFO is full, data written into the FIFO is lost. If the /EMPTY flag indicates that the FIFO is empty, no valid data can be read from the FIFO.

1BH: Frame Counter

15–0	FC15–0	The frame counter bits FC15–0 contain the number of frames counted on the FDDI port. It is a 16 bit counter which is increased every time a frame is received on the Transceiver Interface. After overflow, this counter restarts at 0000H. The type of frames that are counted by the frame counter is programmed in the Count Enable register (1EH).

1CH: Data Counter

First Access

15–0	DC31–16	DC31–16 contain the most significant part of the count of data bytes after the SA was received on the Transceiver interface. It stops counting at the reception of the ED, a new SD, Control Symbol or a symbol with an error is received. If there are other Host Processor cycles between the two consecutive accesses, the result of the second read out will repeat most significant part of the counter. After overflow, this 32-bit counter starts over at 00000000H. The type of frames from which the data bytes are counted can be programmed in the Count Enable register (1EH).

Second Access

15–0	DC15–0	DC15–0 contain the least significant part of the count of data bytes received from the FDDI port.

1DH: Error Counter

First Access

15–8	DUPL7–0	DUPL7–0 contain the value of the DUPLOUT counter, which totals the number of frames that were discarded due to a duplicate LOUT on SRF frames. After readout this error counter is reset to 00H.
7–0	IRI7–0	IRI7–0 contain the value of the INVALIDRI counter, which totals the number of frames discarded due to various format errors. After readout this error counter is reset to 00H.

Second Access

15–8	DTE7–0	DTE7–0 contain the value of the DUPLANIDORTREEERROR counter, which totals the number of STE frames that were discarded because the pre-stored LOUT already exists in the RIF. After readout this error counter is reset to 00H.
7–0	LIDM7–0	LIDM7–0 contain the value of the LAN ID MISMATCH counter, which totals the number of ARE and STE frames that were discarded because the last LAN ID in the RIF did not equal the preset LIN. After readout this error counter is reset to 00H.

Third Access

15–8	ALIM7–0	ALIM7–0 contain the value of the ARERDLIMIT EXCEEDED counter, which totals the number of ARE frames discarded due to ARERD Limit exceeded. After readout this error counter is reset to 00H.
7–0	SLIM7–0	SLIM7–0 contain the value of the STERDLIMIT EXCEEDED counter, which totals the number of STE frames discarded due to STERD Limit exceeded. After readout this error counter is reset to 00H.

REGISTER SET DESCRIPTION (CONT'D)

BIT	NAME	DESCRIPTION
1EH:	**Count Enable Register**	
15-14	Reserved	
13	ENVOFR	If ENVOFR is programmed HIGH, the frame counter is increased every time an VOID frame is received.
12	ENSTMFR	If ENSTMFR is programmed HIGH, the frame counter is increased every time an SMT frame with address length 48 bits is received.
11	ENMACFR	If ENMACFR is HIGH, the frame counter is increased every time an MAC frame with address length 48 bits is received.
10	ENLLCFR	If ENLLCFR is HIGH, the frame counter is increased every time an LLC frame with address length 48 bits is received.
9	ENFIFR	If ENFIFR is programmed HIGH, the frame counter is increased every time a Reserved for Implementer frame with address length 48 bits is received.
8	ENFSFR	If ENFSFR is programmed HIGH, the frame counter is increased every time a Reserved for Future Standardization frame with address length 48 bits is received.
7-6	Reserved	
5	ENVODA	When ENVODA is HIGH and if the VOID frame currently being received contains any data, the data counter counts the number of data bytes in the frame. If ENVODA is LOW the data counter is not increased when a VOID frame is being received.
4	ENSTMDA	When ENSTMDA is HIGH and if the Station Management frame with address length 48 bits, currently being received contains any data, the data counter counts the number of data bytes in the frame. If ENSTMDA is LOW the data counter is not increased when a Station Management frame is being received.
3	ENMACDA	When ENMACDA is HIGH and if the MAC frame with address length 48 bits, currently being received contains any data, the data counter counts the number of data bytes in the frame. If ENMACDA is LOW the data counter is not increased when a MAC frame is being received.
2	ENLLCDA	When ENLLCDA is HIGH and if the LLC frame with address length 48 bits, currently being received contains any data, the data counter counts the number of data bytes in the frame. If ENLLCDA is LOW the data counter is not increased when a LLC frame is being received.
1	ENFIDA	When ENFIDA is HIGH and if the Reserved for Implementer frame with address length 48 bits, currently being received contains any data, the data counter counts the number of data bytes in the frame. If ENFIDA is LOW the data counter is not increased when a Reserved for Implementer frame is being received.
0	ENFSDA	When ENFSDA is HIGH and if the Reserved for Future Standardization frame with address length 48 bits, currently being received contains any data, the data counter counts the number of data bytes in the frame. If ENFSDA is LOW the data counter is not increased when a Reserved for Future Standardization frame is being received.
20H: LANCAM CWEC Register		
15–0	CWEC15–0	Writing to this register starts a direct LANCAM access whereby the data written to CWEC15–0 is placed on the DQ15–0 lines and /W, /CM and /EC are held LOW. If /INT is LOW, LANCAM access is prevented.
21H: LANCAM CREC Register		
15–0	CREC15–0	Reading from this register starts a direct LANCAM access whereby the data read from CREC15–0 is data placed on the DQ15–0 lines by the LANCAM. /CM and /EC are held LOW and /W is held HIGH for this LANCAM cycle. If /INT is LOW, LANCAM access is prevented.
22H: LANCAM DWEC Register		
15–0	DWEC15–0	Writing to this register starts a direct LANCAM access whereby the data written to DWEC15–0 is placed on the DQ15–0 lines and /W and /EC are held LOW while /CM is held HIGH for this LANCAM cycle. If /INT is LOW, LANCAM access is prevented.
23H: LANCAM DREC Register		
15–0	DREC1–0	Reading from this register starts a direct LANCAM access whereby the data read from DREC15–0 is data placed on the DQ15–0 lines by the LANCAM. /EC is held LOW and /W and /CM are held HIGH for this LANCAM cycle. If /INT is LOW, LANCAM access is prevented.

REGISTER SET DESCRIPTION (CONT'D)

BIT	NAME	DESCRIPTION
24H: LANCAM CWNEC Register		
15–0	CWEC15–0	Writing to this register starts a direct LANCAM access whereby the data written to CWNEC15–0 is placed on the DQ15–0 lines and /W and /CM are held LOW while /EC is held HIGH for this LANCAM cycle. If /INT is LOW, LANCAM access is prevented.
25H: LANCAM CRNEC Register		
15–0	CRNEC15–0	Reading from this register starts a direct LANCAM access whereby the data read from CRNEC15–0 is data placed on the DQ15–0 lines by the LANCAM. /CM is held LOW and /W and /EC are held HIGH for this LANCAM cycle. If /INT is LOW, LANCAM access is prevented.
26H: LANCAM DWNEC Register		
15–0	DWNEC15–0	Writing to this register starts a direct LANCAM access whereby the data written to DWNEC15–0 is placed on the DQ15–0 lines and /W is held LOW while /CM and /EC are held HIGH for this LANCAM cycle. If /INT is LOW, LANCAM access is prevented.
27H: LANCAM DRNEC Register		
15–0	DRNEC15–0	Reading from this register starts a direct LANCAM access whereby the data read from DRNEC15–0 is data placed on the DQ15–0 lines by the LANCAM. /EC, /W and /CM are held HIGH for this LANCAM cycle. If /INT is LOW, LANCAM access is prevented.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 7.0 Volts
Voltage on all Other Pins	-0.5 to VCC+0.5 Volts (-2.0 Volts for 10 ns, measured at the 50% point)
Temperature Under Bias	-40°C to +80°C
Storage Temperature	-55°C to +125°C
DC Output Current	20 mA (per Output, one at a time, one second duration)

Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

All voltages are referenced to GND.

OPERATING CONDITIONS
(voltages referenced to GND at the device pin)

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{CC}	Operating Supply Voltage	4.5	5.0	5.5	Volts	
V_{IH}	Input Voltage Logic "1" (HIGH)	2.2		V_{CC}+0.5	Volts	
V_{IL}	Input Voltage Logic "0" (LOW)	-0.5		0.8	Volts	-1.0 Volts for 10 ns measured at 50% amplitude, Fig. 5
T_A	Ambient Operating Temperature	0		70	°C	Still Air

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typical	Max	Units	Notes
I_{CC}	Average Power Supply Current			TBD	mA	
V_{OH}	Output Voltage Logic "1" (HIGH)	2.4			Volts	I_{OH} = -2.0 mA (Excl. open-drain outputs)
V_{OL}	Output Voltage Logic "0" (LOW)			0.4	Volts	I_{OL} = 8.0 mA
I_{OH}	Output Open-drain Off Current			5	µA	$V_{OH} \le V_{CC}$
I_{IZ}	Input Leakage Current	-5		5	µA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{OZ}	Output Leakage Current	-5		5	µA	$V_{SS} \le V_{OUT} \le V_{CC}$; DQn = High Impedance

ELECTRICAL CHARACTERISTICS (CONT'D)

CAPACITANCE

Symbol	Parameter	Min	Typ	Max	Units	Notes
C_{IN}	Input Capacitance			10	pF	f=1MHz, V_{IN}=0 Volts
C_{OUT}	Output Capacitance			10	pF	f=1MHz, V_{OUT}=0 Volts

AC TEST CONDITIONS

Input Signal Transitions	0.0 to 3.0 volts
Input Signal Rise and Fall Times	≤3 ns
Input Timing reference Level	1.5 volts
Output Timing HIGH Reference level	2.4 volts
Output Timing LOW Reference Level	0.8 volts
Open-Drain Reference Level	1.5 volts
TTL Switching Test Load	Figure 2
Three-state Test Load	Figure 3
Open-Drain Test Load	Figure 4

SWITCHING CHARACTERISTICS

MAC Interface Switching Characteristics

No.	Symbol	Parameter	Min	Typ.	Max	Units	Notes
1	tCDHDCH	SRMAT, XDAMAT, SAMAT, ABORT, CIP HIGH from DCLK HIGH			10	ns	
2	tCDLDCH	SRMAT, XDAMAT, SAMAT, ABORT, CIP LOW from DCLK HIGH			10	ns	
3	tCDLDCHH	SRMAT, XDAMAT, SAMAT, ABORT, CIP LOW from DCLK HIGH			10	ns	
4	tCDHDCHH	SRMAT, XDAMAT, SAMAT, ABORT, CIP HIGH from DCLK HIGH			10	ns	

Transceiver Interface Switching Characteristics

No.	Symbol	Parameter	Min	Typ.	Max	Units	Notes
5	tDVDCH	RCDAT, RCCONT, PARITY to DCLK Setup Time	27			ns	
6	tDXDCH	RCDAT, RCCONT, PARITY from DCLK Hold Time	0			ns	
7	tDCLDCH	DCLK LOW Period	35			ns	
8	tDCHDCL	DCLK HIGH Period	35			ns	
9	tDCLDCL	DCLK period	76	80		ns	

Clocks Switching Characteristics

No.	Symbol	Parameter	Min	Typ.	Max	Units	Notes
10	tDCHMCH	DCLK HIGH after MCLK HIGH	10			ns	
11	tMCHDCH	MCLK HIGH after DCLK HIGH	10			ns	
12	tMCLMCH	MCLK LOW Period	12			ns	
13	tMCHMCL	MCLK HIGH Period	12			ns	
14	tMCLMCL	MCLK Period	38	40		ns	

SWITCHING CHARACTERISTICS (CONT'D)

FIFO Switching Characteristics

No.	Symbol	Parameter	Min	Typ.	Max	Units	Notes
15	tDVWH	DF, DFC Valid from /WF HIGH		3		ns	
16	tDXWH	DF, DFC from /WF HIGH Hold Time	0			ns	
17	tWLWL	/WF LOW Period	35			ns	
18	tWLWH	/WF HIGH Period	35			ns	
19	tWHWL	/WF Cycle	76	80		ns	

SWITCHING TEST FIGURES

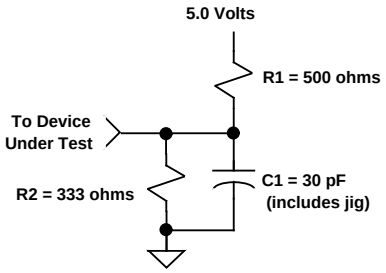


Fig. 2: TTL Switching Test Load

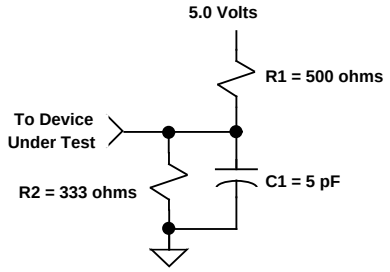


Fig. 3: Three-state Test Load

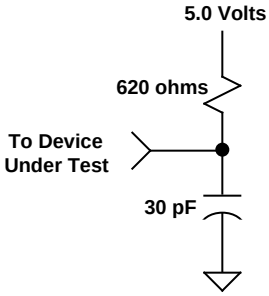


Fig. 4: Open-drain Test Load

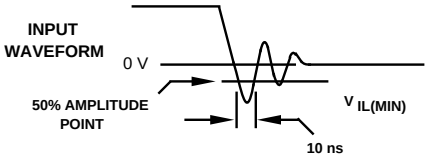


Fig. 5: Input Signal Waveform

SWITCHING CHARACTERISTICS (CONT'D)

Host Processor Interface Switching Characteristics

No.	Symbol	Parameter	Min	Typ.	Max	Units	Notes
20	tSHSL	/CS HIGH Period	0			ns	
21	tSLKL	/CS to ALE LOW Setup Time	2			ns	
22	tKHKL	ALE HIGH Period	2			ns	
23	tKLAX	Address from ALE Hold Time	0			ns	
24	tRWLKL	/RS, /WS LOW to ALE LOW Delay	0			ns	
25	tRWHRWL	/RS, /WS HIGH Period	tMCLMCL			ns	
26	tRWHAX	Address from /RS, /WS not LOW Hold Time	0			ns	
27	tAVRWL	Address to /RS, /WS LOW Setup Time	0			ns	
28	tRHDZ	Data HIGH-Z from /RS not LOW			tMCLMCL + 16	ns	
29	tAVKL	Address to ALE LOW Setup Time	2			ns	
30	tRWLRDL	Delay /HBRDY LOW after /RS, /WS LOW	4 • tMCLMCL			ns	note 1
31	tRLDV	Data valid after /RS LOW	2 • tMCLMCL			ns	note 1
32	tRWLOL	Delay /HBEN LOW after /RS, /WS LOW	3 • tMCLMCL			ns	note 1
33	tOLRDL	Delay /HBRDY LOW after /HBEN LOW			tMCLMCL + 16	ns	
34	tDVOL1	Delay /HBEN LOW after Data Valid			tMCLMCL + 16	ns	
35	tRWHOH	Delay /HBEN HIGH after /RS, /WS HIGH			tMCLMCL + 16	ns	
36	tRWHRDH	Delay from /WS, /RS HIGH to /HBRDY HIGH			tMCLMCL + 16	ns	
37	tRWHRDZ	Delay from /WS or /RS HIGH to /HBRDY HIGH-Z			2 • tMCLMCL + 16	ns	
38	tBDLOL	Delay from /HBDIR LOW to /HBEN LOW			10	ns	
39	tWHDX	Data Hold Time after /WS HIGH	25			ns	
40	tWLBDL	Delay /HBDIR LOW after /WS LOW	tMCLMCL			ns	
41	tWHBDH	Delay /WS HIGH to /HBDIR HIGH			tMCLMCL + 16	ns	
42	tDVWH	Data Setup Time before /WS HIGH	2			ns	
43	tAVDSL	Address Setup Time before /LDS, /UDS not HIGH	2			ns	
44	tDSHDSH	/LDS, /UDS HIGH Period	tMCLMCL			ns	
45	tDSHSRX	SRNW Hold Time after /LDS, /UDS HIGH	0			ns	
46	tDSHAX	Address Hold Time after /LDS, /UDS not LOW	0			ns	
47	tDSLRDZ	Delay /HBRDY LOW after /LDS, /UDS LOW	4 • tMCLMCL			ns	note 1
48	tDSLDV	Data valid after /LDS, /UDS LOW	2 • tMCLMCL			ns	note 1
49	tDSLOL	Delay /HBEN LOW after /LDS, /UDS LOW	3 • tMCLMCL			ns	note 1
50	tDVOL2	Delay /HBEN LOW after Data Valid			tMCLMCL +16	ns	
51	tOLRDL	Delay /HBRDY LOW after /HBEN LOW			tMCLMCL + 16	ns	
52	tDSHOH	Delay /HBEN HIGH after /LDS, /UDS HIGH			tMCLMCL + 16	ns	
53	tDSHDZ	Data HIGH-Z after /LDS, /UDS HIGH			tMCLMCL + 16	ns	
54	tDSHRDH	Delay from /LDS, /UDS HIGH to /HBRDY HIGH			tMCLMCL + 16	ns	
55	tDSHRDZ	Delay from /LDS, /UDS HIGH to /HBRDY HIGH-Z			2 • tMCLMCL + 16	ns	
56	tSRVDSL	Setup SRNW before /LDS, /UDS not HIGH	2			ns	
57	tBDLOL	Delay from /HBDIR LOW to /HBEN LOW			10	ns	
58	tDSLBDL	Delay /HBDIR LOW after /LDS, /UDS LOW	tMCLMCL			ns	
59	tWHBDH	Delay /LDS, /UDS HIGH to /HBDIR HIGH			tMCLMCL + 16	ns	
60	tDVDSH	Data Setup Time before /LDS, /UDS HIGH	2			ns	
61	tDSHDX	Data Hold Time after /LDS, /UDS HIGH	25			ns	

SWITCHING CHARACTERISTICS (CONT'D)

LANCAM Interface Switching Characteristics

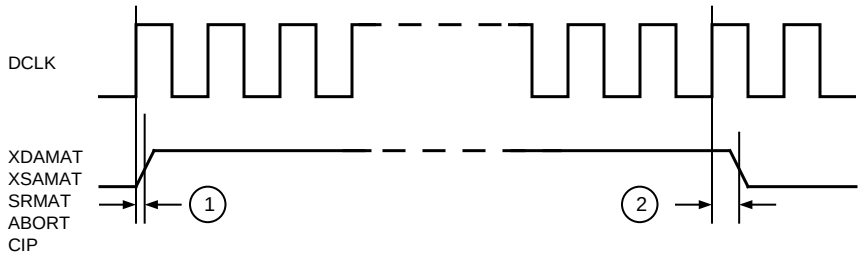
No.	Name	Parameter	Min	Typ.	Max	Units	Notes
62	tELEL	Read/Write Cycle Time	76 108 146			ns ns ns	2 3 4
63	tELEH	/E LOW Period	38 76 108			ns ns ns	5 6 7
64	tEHEL	/E HIGH Period	38 76 108			ns ns ns	8 9 10
65	tCDVEL	Control/Data Setup Time to /E LOW	1			ns	
66	tELCDX	Control/Data Hold Time from /E LOW	38			ns	
67	tDVEH	Data Setup Time to /E HIGH	3			ns	
68	tEHDX	Data Hold Time from /E HIGH	0			ns	

Notes

1. Due to internal arbitration, these values can increase by integer multiples of tMCLMCL. The differences between the minimum values of tRWLRDL, tRLDV and tRWLOL remain equal. The differences between the minimum values of tDSLRDZ, tDSLDV and tDSLOL remain equal.
2. Instructions with a length of 2 MCLK
3. Instructions with a length of 3 MCLK
4. Instructions with a length of 4 MCLK
5. Instructions with an /E LOW length of 1 MCLK
6. Instructions with an /E LOW length of 2 MCLK
7. Instructions with an /E LOW length of 3 MCLK
8. Instructions with an /E HIGH length of 1 MCLK
9. Instructions with an /E HIGH length of 2 MCLK
10. Instructions with an /E HIGH length of 3 MCLK

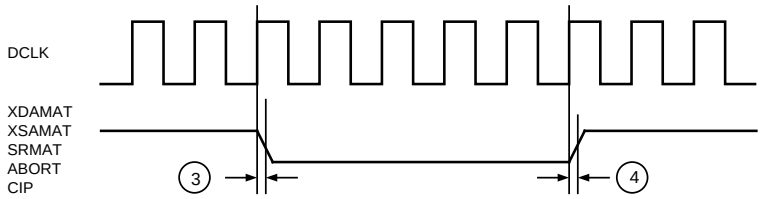
TIMING DIAGRAMS

MAC INTERFACE TIMING

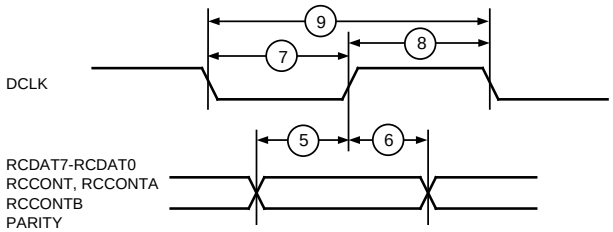


TIMING DIAGRAMS (CONT'D)

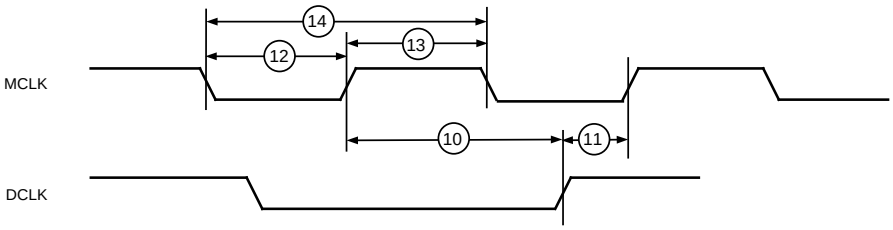
MAC INTERFACE TIMING 2



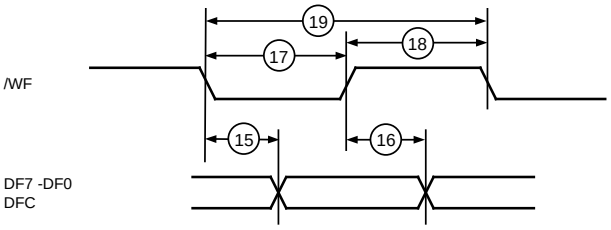
TRANSCEIVER INTERFACE TIMING



CLOCKS TIMING

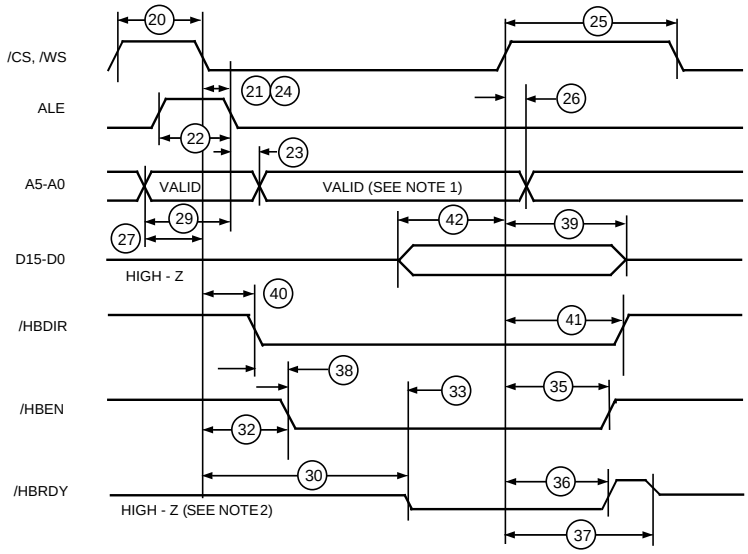


FIFO INTERFACE TIMING



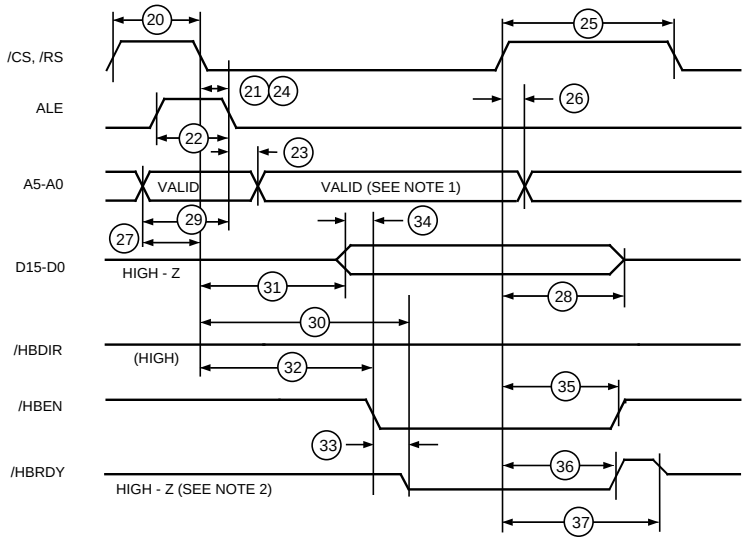
TIMING DIAGRAMS (CONT'D)

HOST PROCESSOR INTERFACE TIMING
INTEL-MODE WRITE CYCLE



Note 1: For Non-Muxed Data/Address lines
Note 2: For clarity, levels for /HBRDY are shown without the effect of the required pull-up resistor.

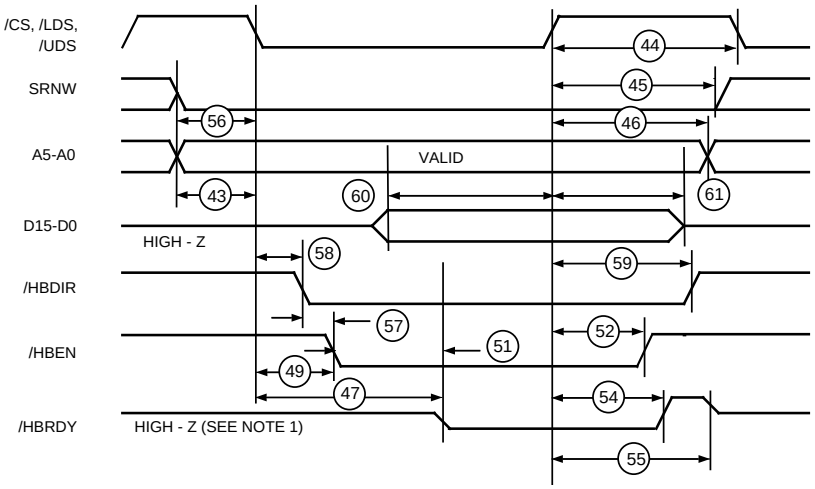
HOST PROCESSOR INTERFACE TIMING
INTEL-MODE READ CYCLE



Note 1: For Non-Muxed Data/Address lines
Note 2: For clarity, /HBRDY levels are shown without the effect of the required pull-up resistor.

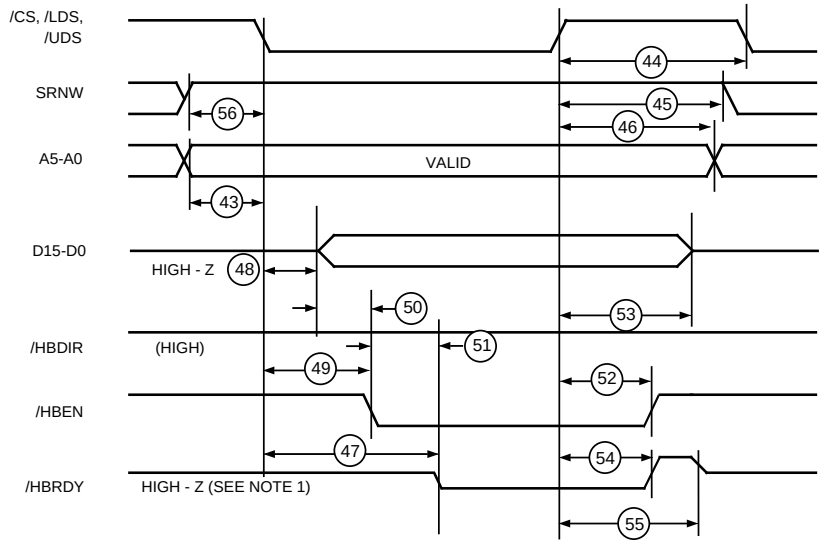
TIMING DIAGRAMS (CONT'D)

HOST PROCESSOR INTERFACE TIMING
MOTOROLA-MODE WRITE CYCLE



Note 1: For clarity, levels for /HBRDY are shown without the effect of the required pull-up resistor.

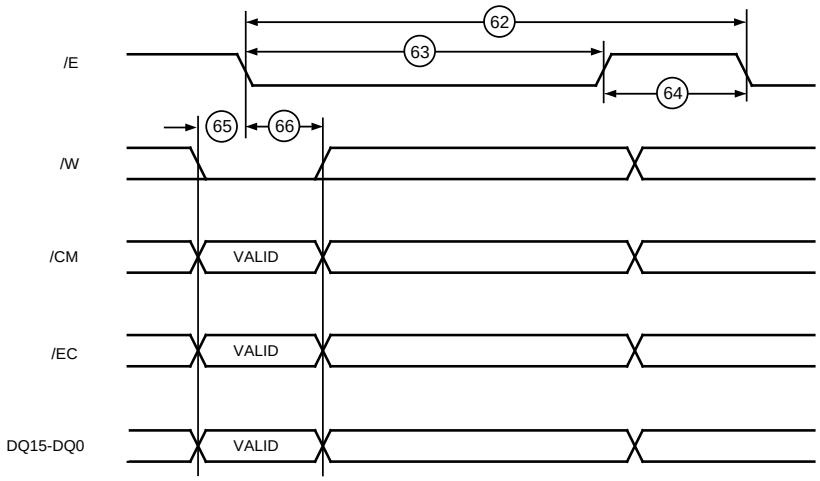
HOST PROCESSOR INTERFACE TIMING
MOTOROLA-MODE READ CYCLE



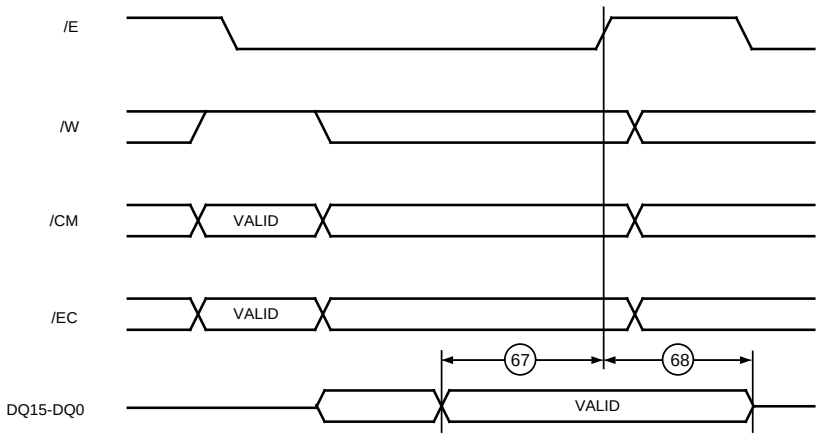
Note 1: For clarity, /HBRDY levels are shown without the effect of the required pull-up resistor.

TIMING DIAGRAMS (CONT'D)

LANCAM WRITE CYCLE TIMING



LANCAM READ CYCLE TIMING



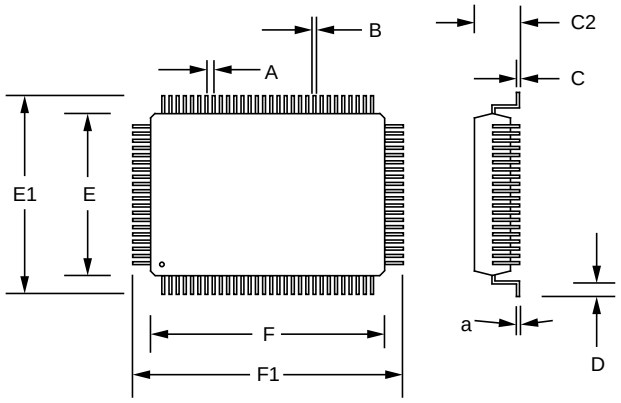
MU9C8248

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE
MU9C8248QEC	100-PIN PQFP	0-70°C

100-PIN PACKAGE OUTLINE

(All Dimensions are in millimeters)



Lead Count	Dim. A	Dim. B	Dim. C	Dim. C2	Dim. D	Dim. E	Dim. E1	Dim. F	Dim. F1	Dim. a
100	0.65 ±0.08	0.30 ±0.08	0.38 ±0.13	3.15 ±0.10	0.800 ±0.076	14.00 ±0.10	17.2 ±0.15	20.00 ±0.10	23.20 ±0.15	0° 7°

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