Filtronic

FPD1500SOT89

Datasheet v3.0

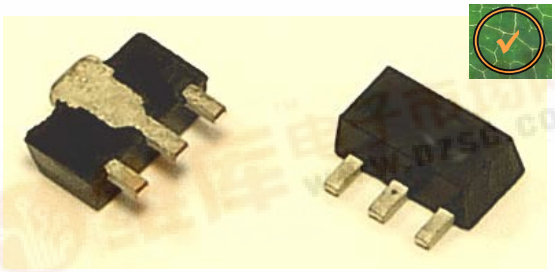
LOW NOISE HIGH LINEARITY PACKAGED PHEMT

FEATURES (1850MHZ):

- 27.5 dBm Output Power (P1dB)
- 17 dB Small-Signal Gain (SSG)
- 1.2 dB Noise Figure
- 42 dBm Output IP3
- 50% Power-Added Efficiency
- FPD1500SOT89E - RoHS compliant

PACKAGE:

RoHS



GENERAL DESCRIPTION:

The FPD1500SOT89 is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a 0.25 µm x 1500 µm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The double recessed gate structure minimizes parasitics to optimize performance, with an epitaxial structure designed for improved linearity over a range of bias conditions and i/p power levels.

TYPICAL APPLICATIONS:

- Drivers or output stages in PCS/Cellular base station transmitter amplifiers
- High intercept-point LNAs
- WLL and WLAN systems, and other types of wireless infrastructure systems.

ELECTRICAL SPECIFICATIONS:

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power at 1dB Gain Compression	P1dB	VDS = 5 V; IDS = 50% IDSS	26.0	27.5		dBm
Small-Signal Gain	SSG	VDS = 5 V; IDS = 50% IDSS	15.5	17		dB
Power-Added Efficiency	PAE	VDS = 5 V; IDS = 50% IDSS; POUT = P1dB		50		%
Noise Figure	NF	VDS = 5 V; IDS = 50% IDSS VDS = 5 V; IDS = 25% IDSS		1.0	1.2	dB
Output Third-Order Intercept Point (from 15 to 5 dB below P1dB)	IP3	VDS = 5V; IDS = 50% IDSS Matched for optimal power Matched for best IP3	38	40 42		dBm
Saturated Drain-Source Current	IDSS	VDS = 1.3 V; VGS = 0 V	375	465	550	mA
Maximum Drain-Source Current	IMAX	VDS = 1.3 V; VGS ≅ +1 V		750		mA
Transconductance	GM	VDS = 1.3 V; VGS = 0 V		400		mS
Gate-Source Leakage Current	IGSO	VGS = -5 V		1	15	µA
Pinch-Off Voltage	|VP|	VDS = 1.3 V; IDS = 1.5 mA	0.7	1.0	1.3	V
Gate-Source Breakdown Voltage	|VBDGS|	IGS = 1.5 mA	12	16		V
Gate-Drain Breakdown Voltage	|VBDGD|	IGD = 1.5 mA	12	16		V
Thermal Resistance	RθJC			60		°C/W

Note: $T_{AMBIENT}$ = 22°; RF specification measured at f = 1850 MHz using CW signal (except as noted)

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ABSOLUTE MAXIMUM RATING[1]:

PARAMETER	SYMBOL	TEST CONDITIONS	ABSOLUTE MAXIMUM
Drain-Source Voltage	VDS	-3V < VGS < +0V	8V
Gate-Source Voltage	VGS	0V < VDS < +8V	-3V
Drain-Source Current	IDS	For VDS < 2V	IDSS
Gate Current	IG	Forward or reverse current	15mA
RF Input Power[2]	PIN	Under any acceptable bias state	350mW
Channel Operating Temperature	TCH	Under any acceptable bias state	175°C
Storage Temperature	TSTG	Non-Operating Storage	-55°C to 150°C
Total Power Dissipation	PTOT	See De-Rating Note below	2.3W
Gain Compression	Comp.	Under any bias conditions	5dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits	

Notes:
[1]$T_{Ambient}$ = 22°C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device
[2]Max. RF Input Limit must be further limited if input VSWR > 2.5:1
[3]Users should avoid exceeding 80% of 2 or more Limits simultaneously
[4]Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) – P_{OUT}$,
where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power
Total Power Dissipation to be de-rated as follows above 22°C:
P_{TOT}= 2.3 - (0.016W/°C) x T_{PACK}
where T_{PACK}= source tab lead temperature above 22°C
(coefficient of de-rating formula is the Thermal Conductivity)
Example: For a 65°C carrier temperature: P_{TOT} = 2.3W – (0.016 x (65 – 22)) = 1.61W

BIASING GUIDELINES:

- Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias.
- Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices.
- For standard class A operation, a 50% of IDSS bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. A class A/B Bias of 25-33% of IDSS to achieve better OIP3, and Noise Figure performance is suggested.

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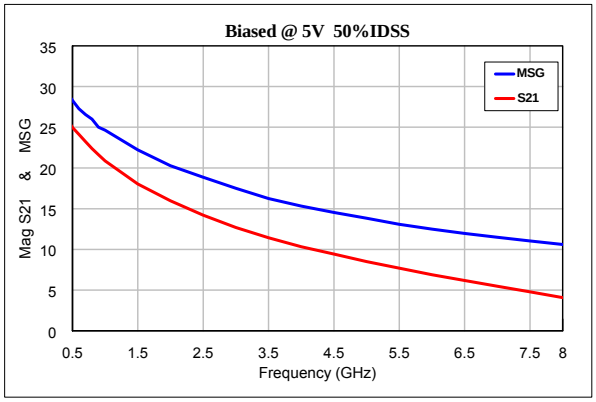
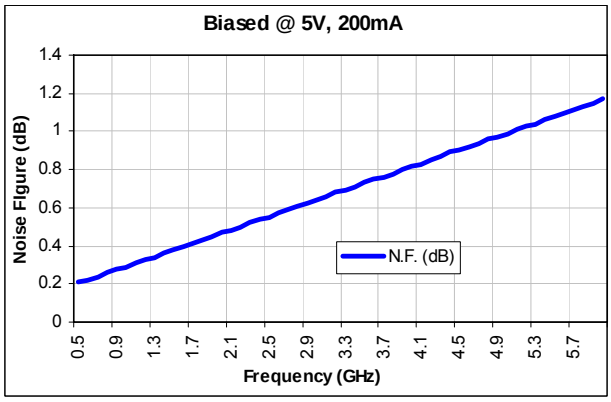
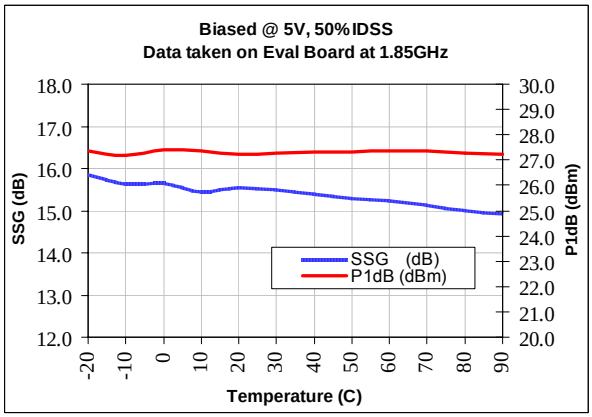
FREQUENCY RESPONSE:

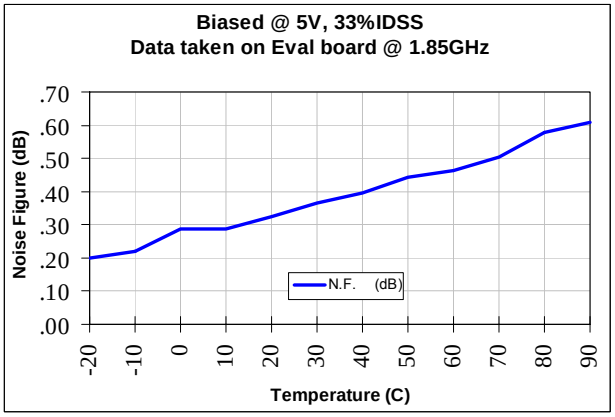




Note: Device tuned for minimum noise figure

TEMPERATURE RESPONSE:





Note: Evaluation board tuned for maximum power

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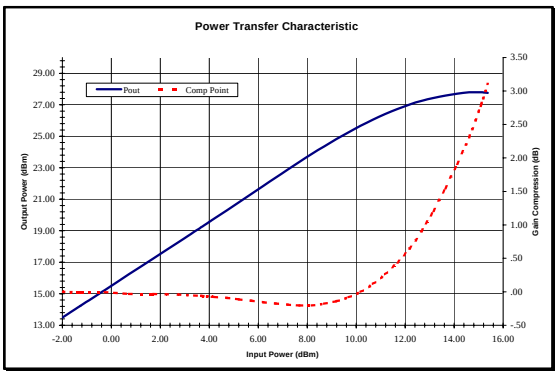
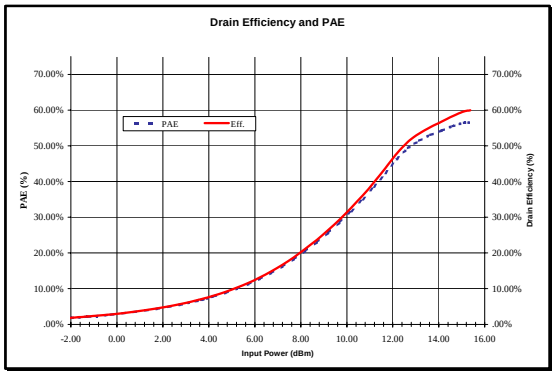
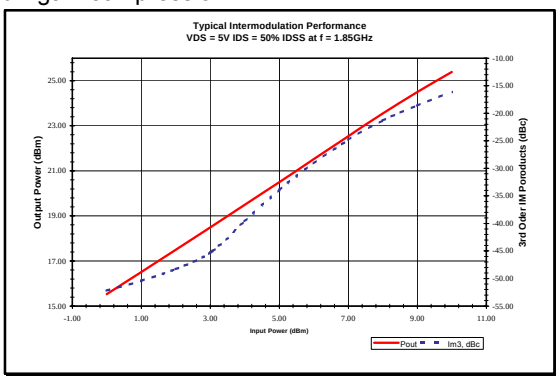
TYPICAL TUNED RF PERFORMANCE:



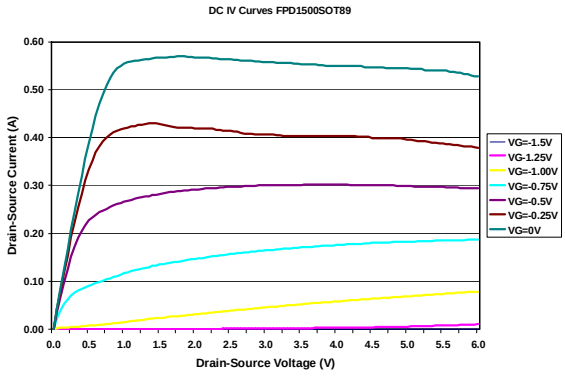


NOTE: Typical power and efficiency is shown above. The devices were biased nominally at V_{DS} = 5V, I_{DS} = 50% of I_{DSS}, at a test frequency of 1.85 GHz. The test devices were tuned (input and output tuning) for maximum output power at 1dB gain compression.



Note: pHEMT devices have enhanced intermodulation performance. This yields OIP3 values of about P_{1dB} + 14dBm. This IMD enhancement is affected by the quiescent bias and the matching applied to the device.

TYPICAL I-V CHARACTERISTICS



Note: The recommended method for measuring I_{DSS}, or any particular I_{DS}, is to set the Drain-Source voltage (V_{DS}) at 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented above). Setting the V_{DS} > 1.3V will generally cause errors in the current measurements, even in stabilized circuits.

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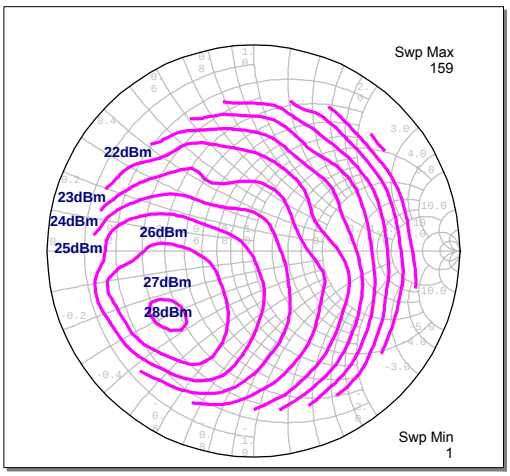
TYPICAL OUTPUT PLANE POWER CONTOURS (VDS = 5v, IDS = 50%IDSS) :



1850 MHz

Contours swept with a constant input power, set so that optimum P_{1dB} is achieved at the point of output match.

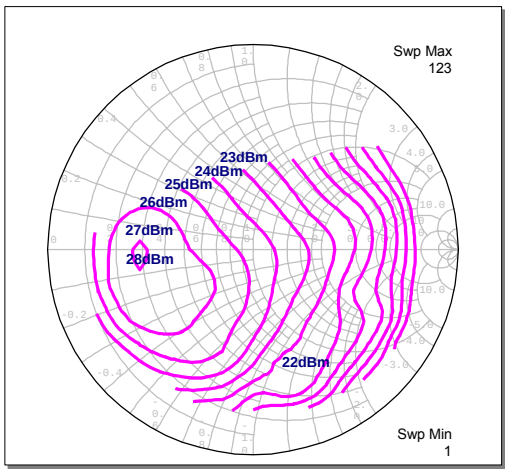
Input (Source plane) Γ_S:

0.74 ∠ 168.2º

0.15 + j0.1 (normalized)

7.5 + j5.0 Ω

Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.



900 MHz

Contours swept with a constant input power, set so that optimum P_{1dB} is achieved at the point of output match.

Input (Source plane) Γ_S:

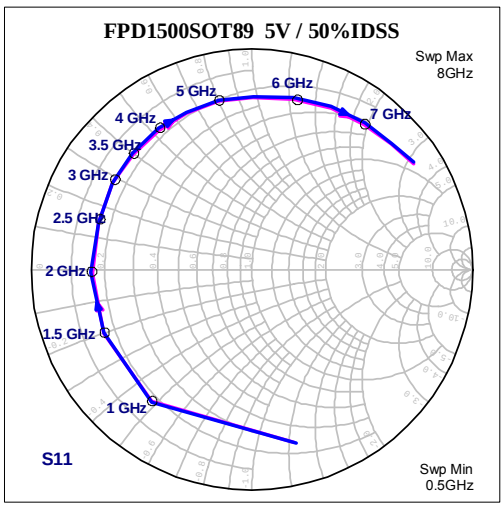
0.67 ∠ 103.6º

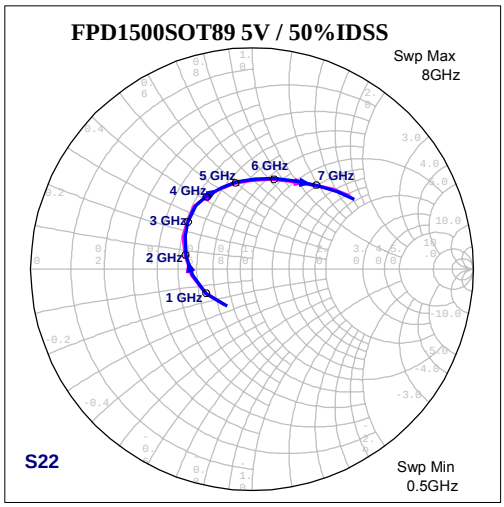
0.30 + j0.74 (normalized)

15 + j37.0 Ω

Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.

TYPICAL SCATTERING PARAMETERS (50Ω SYSTEM):





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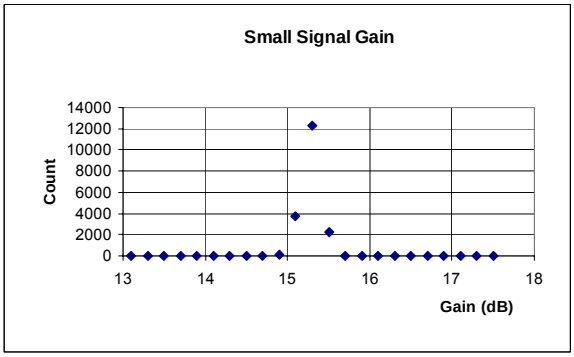
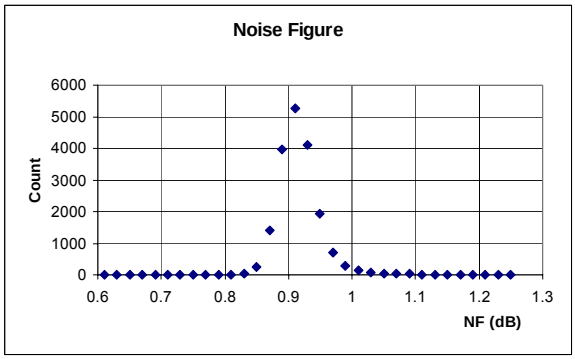
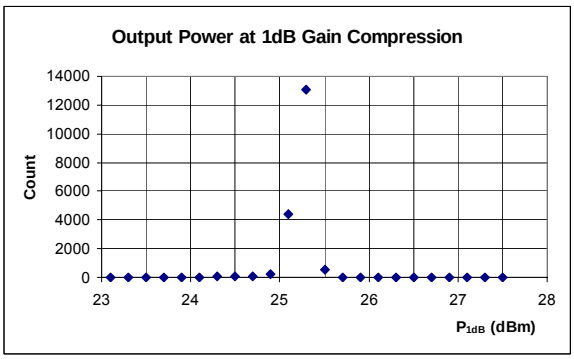
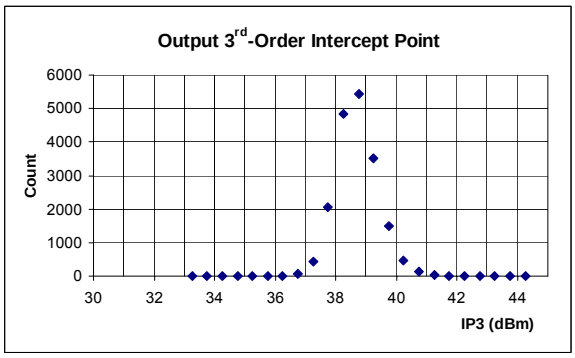
STATISTICAL SAMPLE OF RF PERFORMANCE:









Note: The devices were tested by a high-speed automatic test system, in a matched circuit based on 2GHz Evaluation Board. This circuit is a dual-bias single-pole lowpass topology, and the devices were biased at V_{DS} = 4.5V, I_{DS} = 120mA, Test Frequency = 2.0GHz. The performance data is summarized below:

Parameter	Median	Standard Deviation	Test Limit	CPK
Small-Signal Gain	15.5	0.20	14.5	1.7
Noise Figure	0.91	0.03	1.20	3.2
Output Power (P1dB)	25.2	0.25	24.5	0.93
3rd-Order Intercept	38.7	1.1	36.5	0.67

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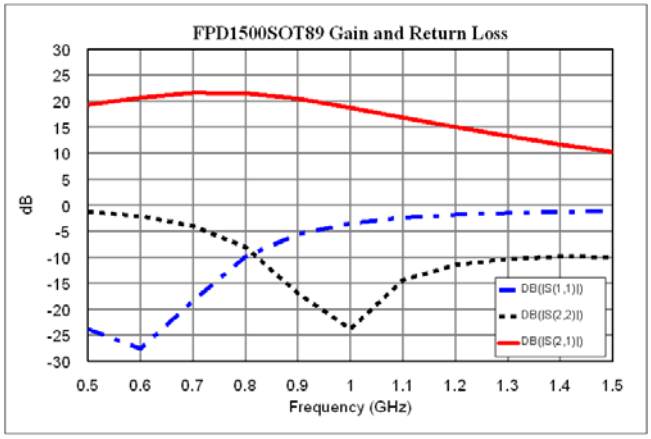
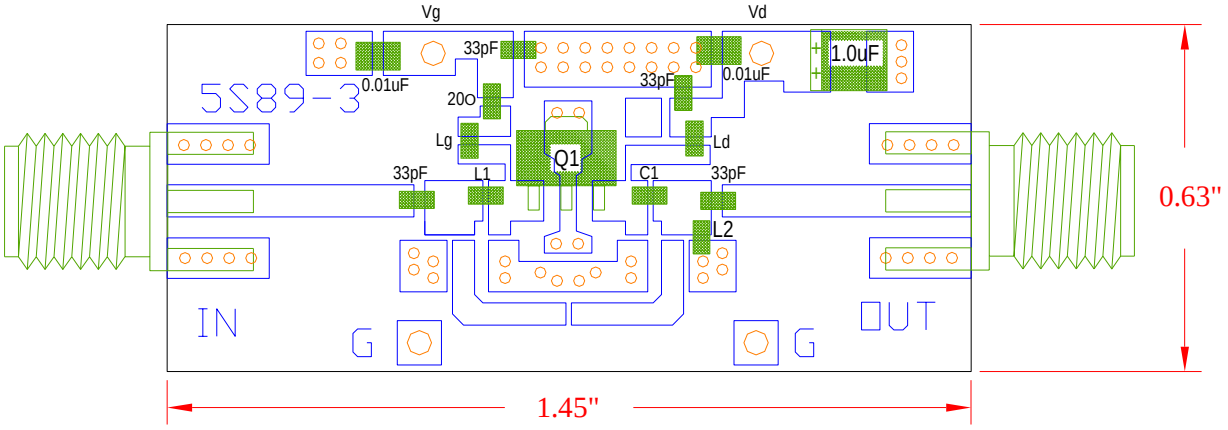
REFERENCE DESIGN 0.9GHZ

FREQUENCY	GHZ	0.9
Gain	dB	20
P1dB	dBm	27
OIP3[1]	dBm	39
N.F.	dB	0.7
S11	dB	-5
S22	dB	-15
Vd	V	5
Vg	V	-0.4 to -0.6
Id	mA	200

1. Measured at 15dBm per tone



Board Layout

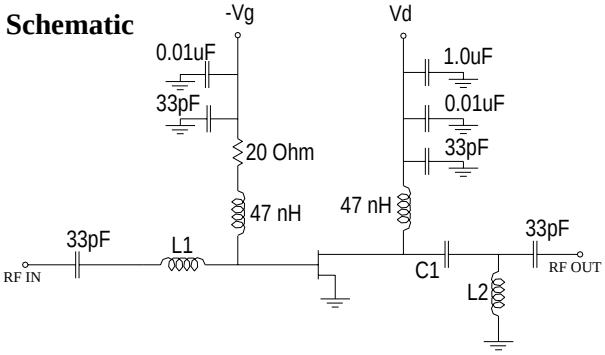


Component Values

Component	Value	Description
Lg	47nH	LL1608 Toko chip inductor
Ld	47nH	LL1608 Toko chip inductor
L1	12nH	LL1005 Toko chip inductor
L2	4.7nH	LL1005 Toko chip inductor
C1	5.6pF	ATC 600S chip capacitor

Eval board material - 31mil thick FR4 with 1/2 Ounce Cu on both sides

Schematic



D.C. Blocking capacitors are ATC series 600S. A tantalum 1.0µF is used at the drain terminal. All other capacitors are 0603 and 0805 standard chip capacitors. A 0603 size 20 Ohm Chip resistor from Vishay is used on the gate D.C. bias line for stability.

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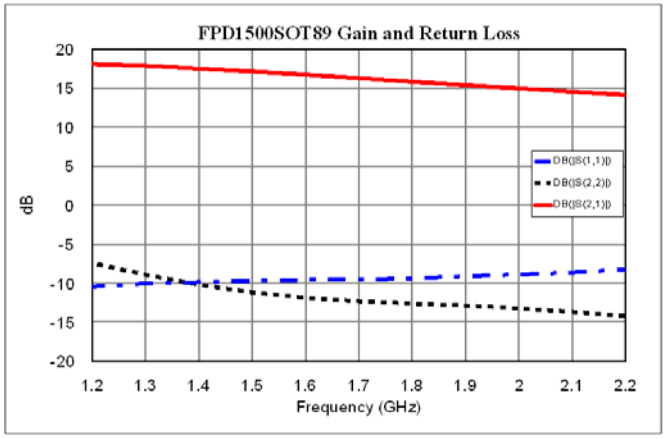
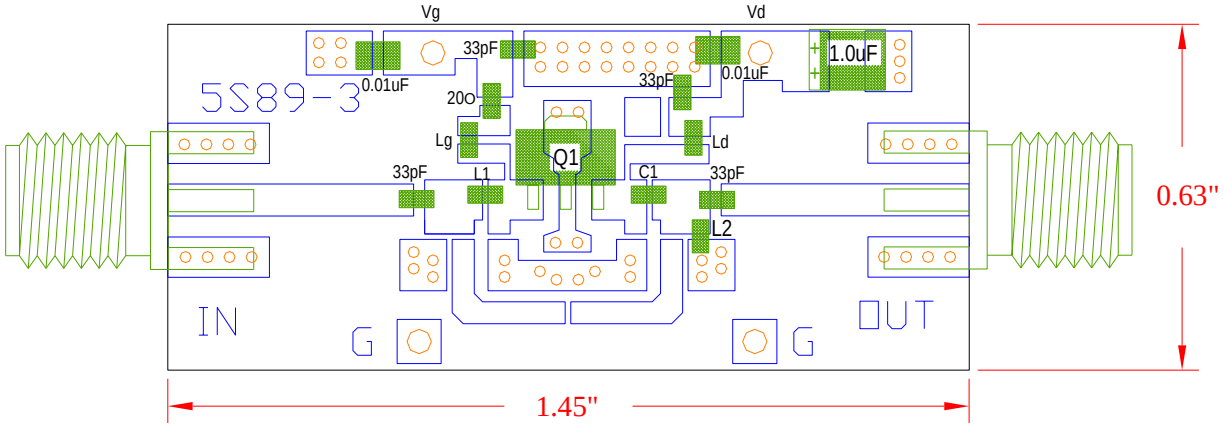
REFERENCE DESIGN 1.85GHZ

FREQUENCY	GHZ	1.85
Gain	dB	16
P1dB	dBm	27
OIP3[1]	dBm	41
N.F.	dB	0.9
S11	dB	-9
S22	dB	-14
Vd	V	5
Vg	V	-0.4 to -0.6
Id	mA	200

1. Measured 15dBm per tone



Board Layout

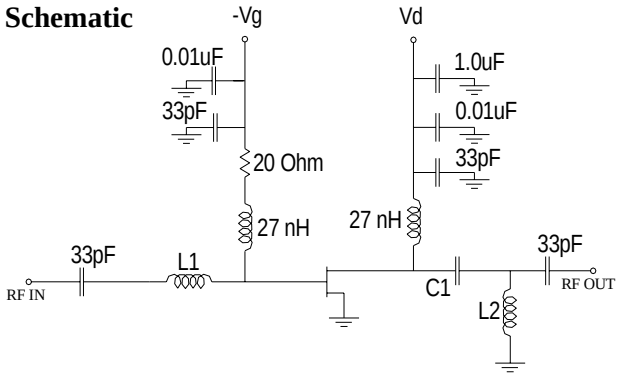


Component Values

Component	Value	Description
Lg	27nH	LL1608 Toko chip inductor
Ld	27nH	LL1608 Toko chip inductor
L1	1.5nH	LL1005 Toko chip inductor
L2	4.7nH	LL1005 Toko chip inductor
C1	2.2pF	ATC 600S chip capacitor

Eval board material - 31mil thick FR4 with 1/2 Ounce Cu on both sides

Schematic



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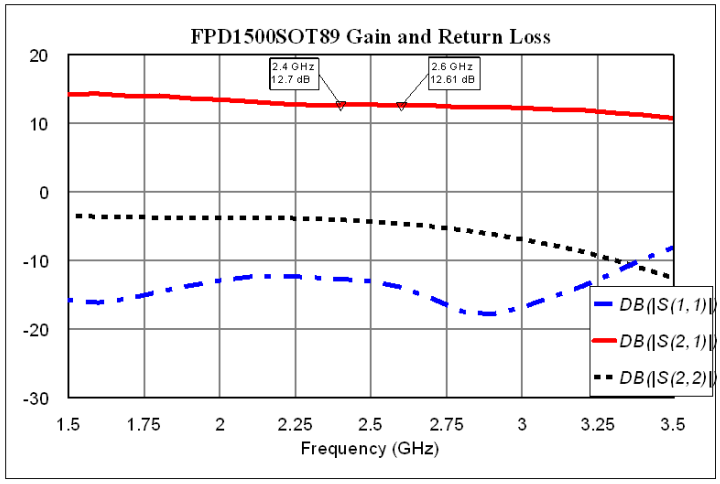
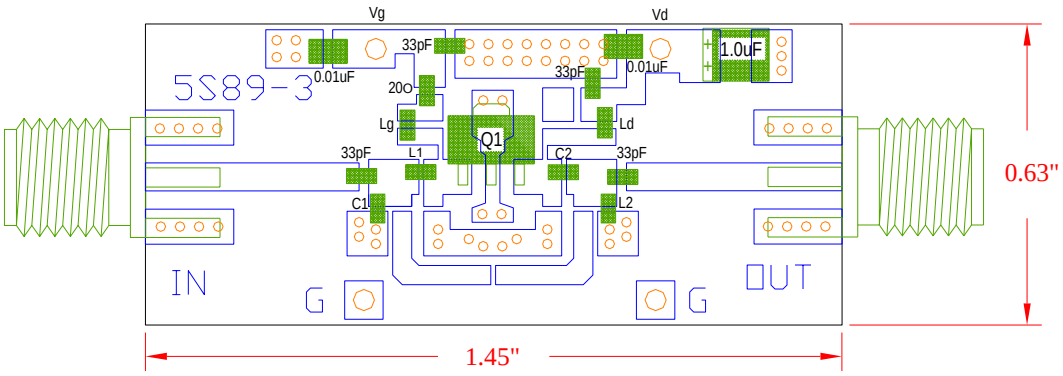
REFERENCE DESIGN 2.4 TO 2.6GHZ

FREQUENCY	GHZ	2.4	2.6
Gain	dB	12.5	12.4
P1dB	dBm	28	28
OIP3[1]	dBm	39	40
N.F.	dB	1.0	0.9
S11	dB	-14	-16
S22	dB	-5	-6
Vd	V	5	5
Vg	V	-0.4 to -0.6	-0.4 to -0.6
Id	mA	200	200

1. Measured at 15dBm per tone



Board Layout

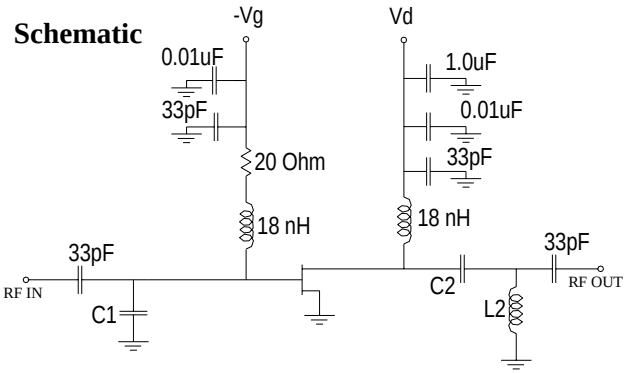


Component Values

Component	Value	Description
Lg	18nH	LL1608 Toko chip inductor
Ld	18nH	LL1608 Toko chip inductor
L1	0.0nH	No Component (Cu Tab)
L2	3.9nH	LL1005 Toko chip inductor
C1 & C2	1.0pF	ATC 600S chip capacitor

Eval board material - 31mil thick FR4 with 1/2 Ounce Cu on both sides

Schematic



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S-PARAMETERS: BIASED @ 5V, 50%IDSS:

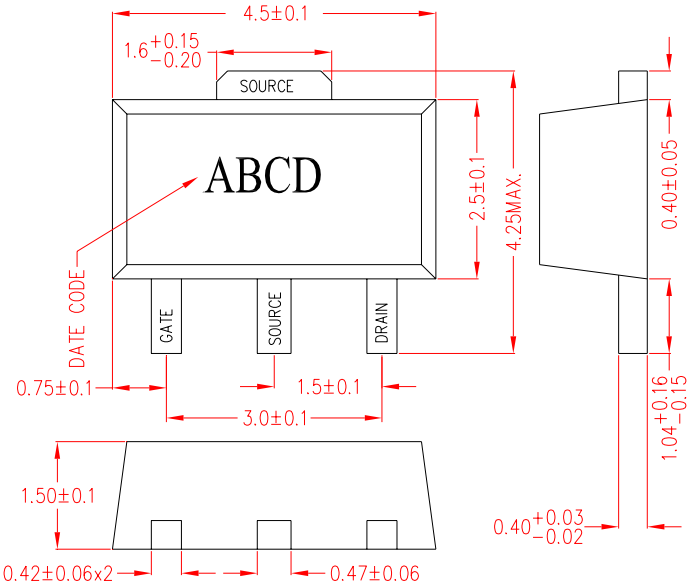
FREQ[GHz]	S11m	S11a	S21m	S21a	S12m	S12a	S22m	S22a
0.500	0.865	-91.9	18.828	121.6	0.027	52.3	0.293	-130.2
0.750	0.763	-118.7	14.373	107.4	0.033	46.3	0.287	-141.8
1.000	0.728	-136.4	11.562	95.9	0.038	42.6	0.293	-154.9
1.250	0.714	-149.6	9.707	87.0	0.043	39.6	0.285	-162.6
1.500	0.701	-162.1	8.254	79.1	0.047	37.4	0.284	-172.6
1.750	0.694	-171.3	7.225	71.2	0.052	34.6	0.288	-178.7
2.000	0.692	179.8	6.460	64.2	0.057	32.1	0.279	175.2
2.250	0.684	171.3	5.820	57.4	0.061	29.4	0.279	168.4
2.500	0.685	163.7	5.320	50.7	0.067	26.1	0.271	161.9
2.750	0.683	155.8	4.884	44.6	0.071	23.5	0.273	153.9
3.000	0.681	148.1	4.506	37.8	0.076	19.7	0.273	147.1
3.250	0.692	141.4	4.199	31.4	0.080	16.0	0.276	138.5
3.500	0.690	134.1	3.913	25.1	0.085	12.4	0.290	131.2
3.750	0.698	127.7	3.651	18.8	0.089	8.5	0.302	124.2
4.000	0.706	120.8	3.418	12.7	0.093	4.6	0.318	118.0
4.250	0.711	114.3	3.207	6.5	0.096	0.5	0.335	112.5
4.500	0.730	108.9	3.018	0.8	0.100	-3.5	0.349	107.0
4.750	0.742	103.2	2.834	-5.0	0.102	-7.4	0.367	101.4
5.000	0.757	98.2	2.672	-10.6	0.105	-11.1	0.381	96.3
5.250	0.765	92.4	2.531	-16.1	0.108	-14.6	0.396	91.7
5.500	0.769	87.7	2.408	-21.7	0.111	-18.6	0.406	87.3
5.750	0.790	83.4	2.300	-26.9	0.114	-22.2	0.417	83.2
6.000	0.847	77.1	2.263	-33.3	0.121	-27.1	0.457	79.0
6.250	0.830	73.0	2.139	-38.4	0.122	-30.6	0.457	75.1
6.500	0.850	67.3	2.046	-45.2	0.124	-36.0	0.476	68.2
6.750	0.826	63.8	1.926	-49.9	0.125	-39.1	0.471	62.2
7.000	0.829	60.2	1.839	-54.7	0.127	-42.7	0.471	55.5
7.250	0.828	56.4	1.763	-59.5	0.128	-46.1	0.470	50.2
7.500	0.823	52.8	1.698	-64.6	0.130	-49.9	0.477	44.5
7.750	0.836	48.9	1.641	-69.8	0.133	-54.2	0.491	39.2
8.000	0.855	44.5	1.580	-75.7	0.135	-58.9	0.507	33.8
8.250	0.858	38.3	1.512	-81.5	0.135	-63.5	0.531	29.3
8.500	0.855	32.9	1.442	-86.8	0.136	-68.0	0.552	24.7
8.750	0.863	27.9	1.374	-92.3	0.136	-72.8	0.575	21.2
9.000	0.874	22.0	1.311	-97.5	0.136	-77.2	0.596	17.7
9.250	0.875	16.9	1.247	-102.5	0.135	-81.6	0.618	15.4
9.500	0.885	11.9	1.182	-107.8	0.134	-86.4	0.637	13.0
9.750	0.890	7.4	1.124	-112.5	0.133	-91.4	0.652	11.0
10.000	0.895	3.8	1.069	-117.4	0.131	-96.4	0.663	8.0
10.250	0.897	0.5	1.012	-121.7	0.128	-101.8	0.673	5.1
10.500	0.899	-2.9	0.975	-126.0	0.125	-106.8	0.680	2.5
10.750	0.902	-5.6	0.928	-130.2	0.120	-111.1	0.693	0.0
11.000	0.902	-8.1	0.894	-134.3	0.117	-114.6	0.698	-2.9
11.250	0.907	-10.5	0.865	-138.4	0.115	-118.0	0.701	-6.0
11.500	0.913	-13.5	0.845	-142.1	0.114	-120.9	0.695	-9.7
11.750	0.912	-16.4	0.822	-146.4	0.114	-124.3	0.691	-13.3
12.000	0.908	-19.4	0.806	-150.7	0.117	-128.3	0.684	-18.1

Filtronic Compound Semiconductors Ltd

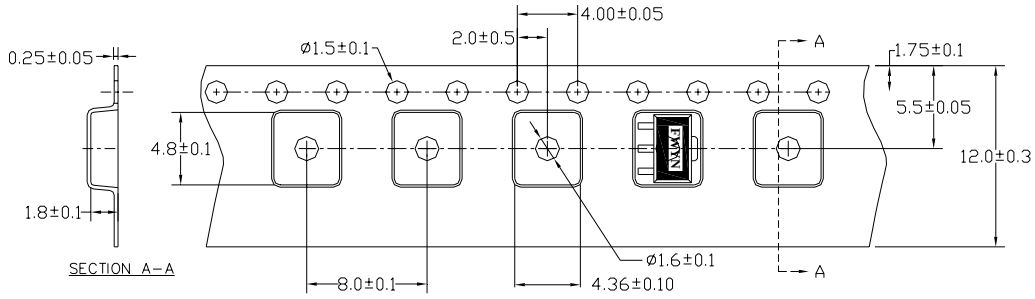
Tel: +44 (0) 1325 301111 Fax: +44 (0) 1325 306177 Email: sales@filcs.com Website: www.filtronic.com

PACKAGE OUTLINE:

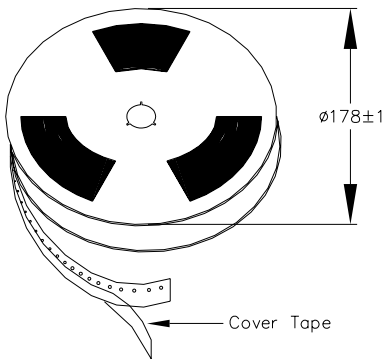
(dimensions in millimeters – mm)



TAPE DIMENSIONS AND PART ORIENTATION:



DIMENSIONS ARE IN MM



- Also available with horizontal part orientation
- Hub diameter = 80mm
- Devices per reel = 1000

Specifications subject to change without notice
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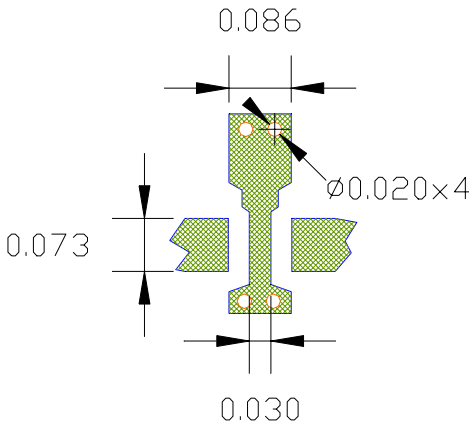
Device Foot Print:



Units in inches

NOTE: Drawing available on Website

Preferred Assembly Instructions:

This package is compatible with both lead free and leaded solder reflow processes as defined within IPC/JEDEC J-STD-020C. The maximum package temperature should not exceed 260°C.

Handling Precautions:

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing.

ESD/MSL Rating:

These devices should be treated as Class 0 (0-250 V) using the human body model as defined in JEDEC Standard No. 22-A114.

The device has a MSL rating of Level 2. To determine this rating, preconditioning was performed to the device per, the Pb-free solder profile defined within IPC/JEDEC J-STD-020C, Moisture / Reflow sensitivity classification for non-hermatic solid state surface mount devices.

Application Notes & Design Data:

Application Notes and design data including S-parameters, noise parameters and device model are available on request.

Reliability:

A MTTF of 7.4 million hours at a channel temperature of 150°C is achieved for the process used to manufacture this device.

Disclaimers:

This product is not designed for use in any space based or life sustaining/supporting equipment.

Ordering Information:

Part Number	Description
FPD1500SOT89	Packaged pHEMT
FPD1500SOT89E	RoHS Compliant Packaged pHEMT
FPD1500SOT89CE	RoHS Compliant Packaged pHEMT with enhanced passivation (Recommended for New Designs)
EB1500SOT89(E)-BB	0.9 GHz evaluation board
EB1500SOT89(E)-BA	1.85 GHz evaluation board
EB1500SOT89(E)-BC	2.0 GHz evaluation board
EB1500SOT89(E)-BD	2.2 GHz evaluation board
EB1500SOT89(E)-BE	2.4 GHz evaluation board
EB1500SOT89(E)-BG	2.6 GHz evaluation board
EB1500SOT89(E)-AJ	5.3-5.75 GHz evaluation board

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