SY88903AL

3.3V, Burst Mode 1.25Gbps PECL High-Sensitivity Limiting Post Amplifier with TTL Loss-of-Signal

General Description

The SY88903AL, burst mode, high-sensitivity limiting post amplifier is designed for use in fiber-optic receivers, specially optimized for passive optical networks (PONs). The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88903AL quantizes these signals and outputs PECL level waveforms.

The SY88903AL operates from a single +3.3V power supply, over temperatures ranging from –40°C to +85°C. Signals with data rates from 622Mbps up to 1.25Gbps, and as small as 5mV$_{pp}$, can be amplified to drive devices with PECL inputs.

The SY88903AL generates a Loss-of-Signal (LOS) open-collector TTL output. A programmable Loss-of-Signal level set pin (LOS$_{LVL}$) sets the sensitivity of the input amplitude detection. LOS asserts high if the input amplitude falls below the threshold set by LOS$_{LVL}$ and de-asserts low otherwise. The enable bar input (/EN) de-asserts the true output signal without removing the input signal. The LOS output can be fed back to the /EN input to maintain output stability under a loss-of-signal condition. Typically, 3.4dB LOS hysteresis is provided to prevent chattering.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Single 3.3V power supply
- Fast LOS release/assert (<500ns) time for PON applications
- 622Mbps to 1.25Gbps operation
- Low-noise PECL data outputs
- High gain LOS
- Chatter-free Open-Collector TTL signal detect (LOS) output with internal 4.75kΩ pull-up resistor
- TTL /EN input
- Programmable LOS level set (LOS$_{LVL}$)
- Available in a tiny 10-pin MSOP package

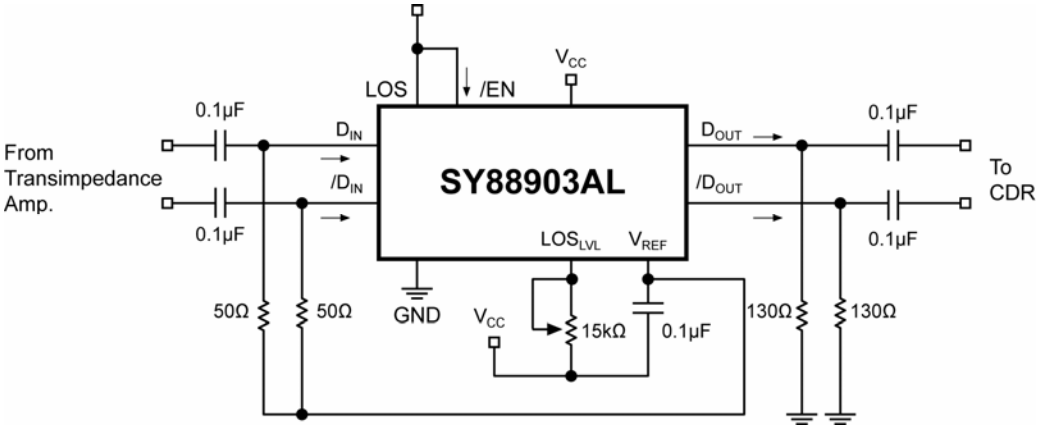
Applications

- GPON/GEPON/EPON
- Gigabit Ethernet, 1062Mbps Fibre Channel
- OC-12/24 SONET/SDH
- Low-gain TIA interface
- High-gain line driver and line receiver

Markets

- FTTH/FTTP
- Datacom/telecom
- Optical transceiver

Typical Application Circuit



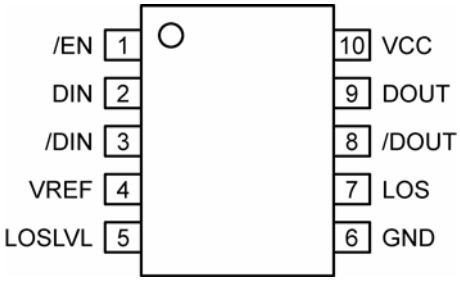
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88903ALKG	K10-1	Industrial	903A with Pb-Free bar line indicator	NiPdAu Pb-Free
SY88903ALKGTR[1]	K10-1	Industrial	903A with Pb-Free bar line indicator	NiPdAu Pb-Free

Note:

1. Tape and Reel.

Pin Configuration



10-Pin MSOP (K10-1)

Pin Description

Pin Number	Pin Name	Type	Pin Function
1	/EN	TTL Input: Default is HIGH.	/Enable: This input enables the outputs when it is LOW. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open.
2	DIN	Data Input	True data input.
3	/DIN	Data Input	Complementary data input.
4	VREF		Reference voltage: Placing a capacitor here to V_{CC} helps stabilize LOS_{LVL}.
5	LOSLVL	Input	Loss-of-Signal Level Set: a resistor from this pin to V_{CC} sets the threshold for the data input amplitude at which LOS will be asserted.
6	GND	Ground	Device ground.
7	LOS	Open-collector TTL output w/internal 4.75kΩ pull-up resistor	Loss-of-Signal: asserts high when the data input amplitude falls below the threshold set by LOS_{LVL}.
8	/DOUT	PECL Output	Complementary data output.
9	DOUT	PECL Output	True data output.
10	VCC	Power Supply	Positive power supply.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... 0V to +7.0V
Input Voltage (DIN, /DIN) ..... 0 to V_{CC}
Output Current (I_{OUT})
  Continuous ..... ±50mA
  Surge ..... ±100mA
/EN Voltage ..... 0 to V_{CC}
V_{REF} Current ..... -800µA to +500µA
LOS_{LVL} Voltage ..... V_{REF} to V_{CC}
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Temperature (T_J) ..... –40°C to +120°C
Junction Thermal Resistance
  MSOP (θ_{JA}) Still-air ..... 113°C/W

DC Electrical Characteristics

V_{CC} = 3.0 to 3.6V; R_L = 50Ω to V_{CC}-2V; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	No output load		26	39	mA
LOS_{LVL}	LOS_{LVL} Voltage		V_{REF}		V_{CC}	V
V_{OH}	PECL Output HIGH Voltage		V_{CC}-1.085	V_{CC}-0.955	V_{CC}-0.880	V
V_{OL}	PECL Output LOW Voltage		V_{CC}-1.850	V_{CC}-1.705	V_{CC}-1.555	V
V_{IHCMR}	Common Mode Range		GND+2.0		V_{CC}	V
V_{REF}	Reference Voltage		V_{CC}-1.48	V_{CC}-1.32	V_{CC}-1.16	V

TTL DC Electrical Characteristics

V_{CC} = 3.0 to 3.6V; R_L = 50Ω to V_{CC}-2V; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	/EN Input HIGH Voltage		2.0			V
V_{IL}	/EN Input LOW Voltage				0.8	V
I_{IH}	/EN Input HIGH Current	V_{IN} = 2.7V V_{IN} = V_{CC}			20 100	µA µA
I_{IL}	/EN Input LOW Current	V_{IN} = 0.5V	-0.3			mA
V_{OH}	LOS Output HIGH Level	$V_{CC} \geq$ 3.3V, I_{OH-MAX} < 160µA V_{CC} < 3.3V, I_{OH-MAX} < 160µA	2.4 2.0			V V
V_{OL}	LOS Output LOW Level	I_{OL} = +2mA			0.5	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

AC Electrical Characteristics

V_{CC} = 3.0 to 3.6V; R_L = 50Ω to V_{CC}-2V; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C.

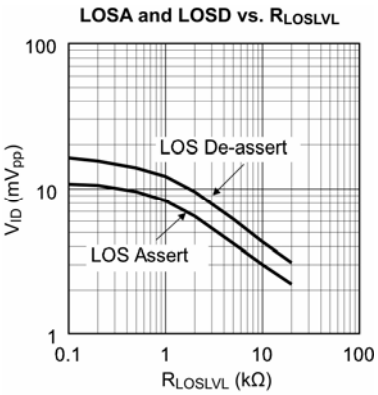
Symbol	Parameter	Condition	Min	Typ	Max	Units
t_r, t_f	Output Rise/Fall Time (20% to 80%)	Note 3			260	ps
t_{JITTER}	Deterministic Random	Note 4 Note 5		15 5		ps_{PP} ps_{RMS}
V_{ID}	Differential Input Voltage Swing	See Figure 1	5		1800	mV_{PP}
V_{OD}	Differential Output Voltage Swing	$V_{ID} \geq 18mV_{PP}$, See Figure 1		1500		mV_{PP}
t_{OFF}	LOS Release Time	Note 8		40	500	ns
t_{ON}	LOS Assert Time	Note 8		125	500	ns
LOS_{AL}	Low LOS Assert Level	R_{LOSLVL} = 15kΩ, Note 6		2.3		mV_{PP}
LOS_{DL}	Low LOS De-assert Level	R_{LOSLVL} = 15kΩ, Note 6		3.4		mV_{PP}
HSY_L	Low LOS Hysteresis	R_{LOSLVL} = 15kΩ, Note 7		3.4		dB
LOS_{AM}	Medium LOS Assert Level	R_{LOSLVL} = 5kΩ, Note 6	2	4.2		mV_{PP}
LOS_{DM}	Medium LOS De-assert Level	R_{LOSLVL} = 5kΩ, Note 6		6.2	9	mV_{PP}
HSY_M	Medium LOS Hysteresis	R_{LOSLVL} = 5kΩ, Note 7	2	3.4	5	dB
LOS_{AH}	High LOS Assert Level	R_{LOSLVL} = 100Ω, Note 6	8	10.8		mV_{PP}
LOS_{DH}	High LOS De-assert Level	R_{LOSLVL} = 100Ω, Note 6		16.4	21	mV_{PP}
HSY_H	High LOS Hysteresis	R_{LOSLVL} = 100Ω, Note 7	2	3.4	5	dB
B_{-3dB}	3dB Bandwidth			1		GHz
$A_{V(Diff)}$	Differential Voltage Gain			42		dB
S_{21}	Single-Ended Small-Signal Gain		30	36		dB

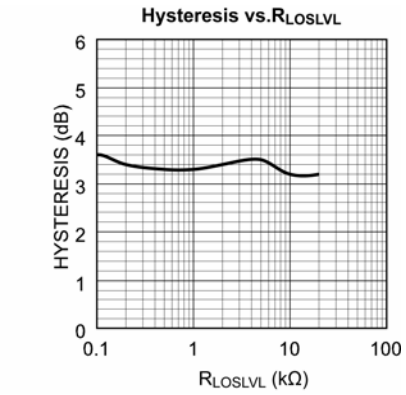
Notes:

3. Amplifier in limiting mode. Input is a 200MHz square wave.
4. Deterministic jitter measured using 1.25Gbps K28.5 pattern, V_{ID} = 10mV_{PP}.
5. Random jitter measured using 1.25Gbps K28.7 pattern, V_{ID} = 10mV_{PP}.
6. See “Typical Operating Characteristics” for a graph showing how to choose a particular R_{LOSLVL} for a particular LOS assert and its associated de-assert amplitude.
7. This specification defines electrical hysteresis as 20log (LOS De-assert/LOS Assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2 depending upon the level of received optical power and ROSA characteristics. Based on that ratio, the optical hysteresis corresponding to the electrical hysteresis range 1dB-4.5 dB, shown in the AC characteristics table, will be 0.5dB-3dB Optical Hysteresis.
8. In real world applications, the LOS Release/Assert time can be strongly influenced by the RC time constant of the AC-coupling cap and the 50Ω input termination. To keep this time low, use a decoupling cap with the lowest value that is allowed by the data rate and the number of consecutive identical bits in the application (typical values are in the range of 0.001µF to 1.0µF).

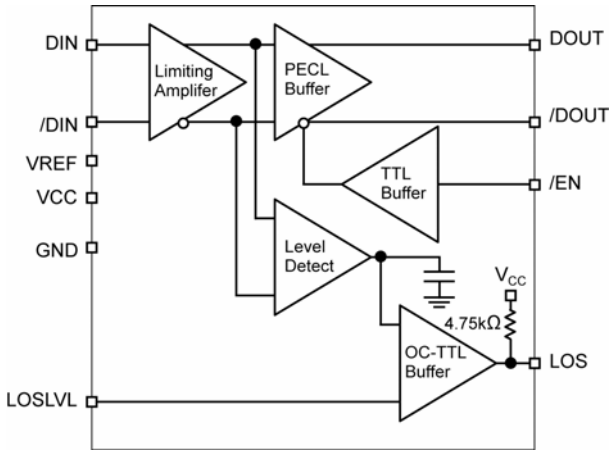
Typical Operating Characteristics

V_{CC} = 3.3V, T_A = 25°C, R_L = 50Ω to V_{CC}-2V, unless otherwise stated.





Functional Block Diagram



Detailed Description

The SY88903AL high-sensitivity limiting post amplifier operates from a single +3.3V power supply, over temperatures from –40°C to +85°C. Signals with data rates from 622Mbps up to 1.25Gbps, and as small as 5mV$_{pp}$, can be amplified. Figure 1 shows the allowed input voltage swing. The SY88903AL generates an LOS output, allowing feedback to /EN for output stability. LOS$_{LVL}$ sets the sensitivity of the input amplitude detection.

Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the input stage. The high-sensitivity of the input amplifier allows signals as small as 5mV$_{pp}$ to be detected and amplified. The input amplifier allows input signals as large as 1800mV$_{pp}$. Input signals are linearly amplified with a typically 42dB differential voltage gain. Since it is a limiting amplifier, the SY88903AL outputs typically 1500mV$_{pp}$ voltage-limited waveforms for input signals that are greater than 12mV$_{pp}$. Applications requiring the SY88903AL to operate with high-gain should have the upstream TIA placed as close as possible to the SY88903AL's input pins to ensure the best performance of the device.

Output Buffer

The SY88903AL's PECL output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V_{CC}–2V for each output pin provides this. Figure 3 shows a simplified schematic of the output stage.

Loss-of-Signal

The SY88903AL generates a chatter-free loss-of-signal (LOS) open-collector TTL output with internal 4.75kΩ pull-up resistor as shown in Figure 4. LOS is used to determine that the input amplitude is too small to be considered a valid input. LOS asserts high if the input amplitude falls below the threshold set by LOSLVL and de-asserts low otherwise. LOS can be fed back to the enable (/EN) input to maintain output stability under a loss of signal condition. /EN de-asserts low the true output signal without removing the input signals. Typically, 3.4dB LOS hysteresis is provided to prevent chattering.

Loss-of-Signal-Level Set

A programmable LOS level set pin (LOS$_{LVL}$) sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and LOS$_{LVL}$ sets the voltage at LOS$_{LVL}$. This voltage ranges from V_{CC} to V_{REF}. The external resistor creates a voltage divider between V_{CC} and V_{REF}, as shown in Figure 5.

Hysteresis

The SY88903AL provides typically 3.4dB LOS electrical hysteresis. By definition, a power ratio measured in dB is 10log (power ratio). Power is calculated as V^2_{IN}/R for an electrical signal. Hence, the same ratio can be stated as 20log (voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and hence, the ratios change linearly. Therefore, the optical hysteresis in dB is half the electrical hysteresis in dB given in the data sheet. The SY88903AL is an electrical device, this data sheet refers to hysteresis in electrical terms. With 3.4dB LOS hysteresis, a voltage factor of 1.5 is required to assert or de-assert LOS.

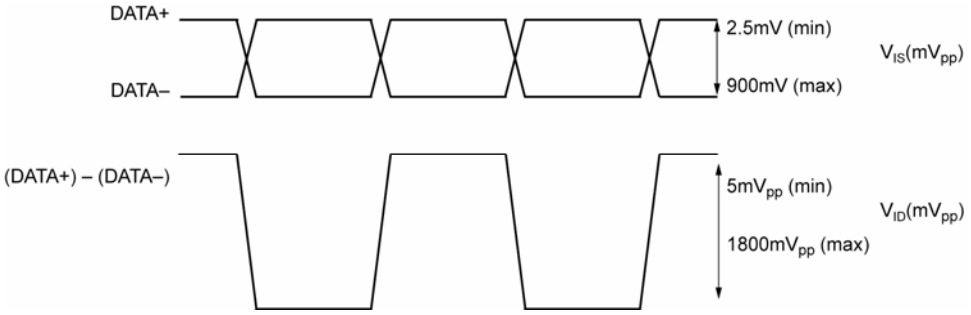


Figure 1. V_{IS} and V_{ID} Definition

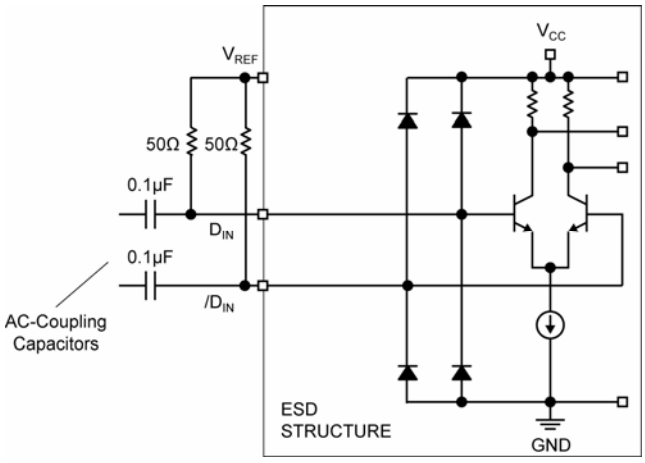


Figure 2. Input Structure

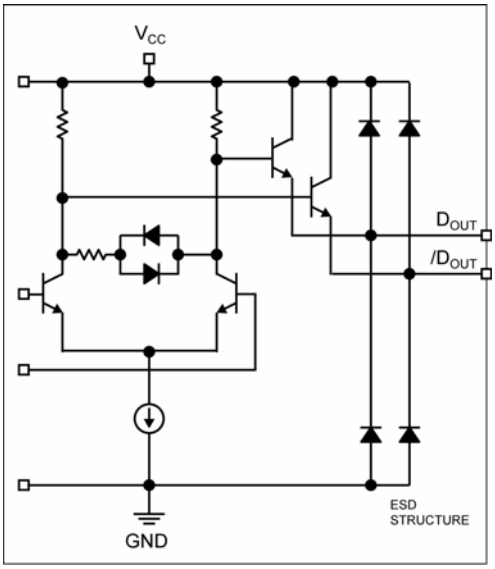


Figure 3. Output Structure

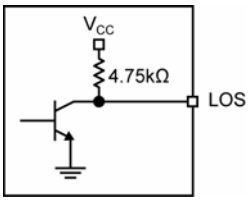


Figure 4. LOS Output Structure

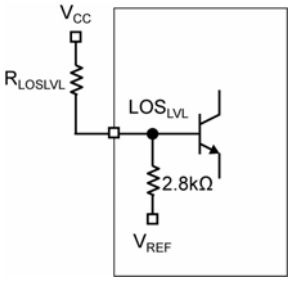


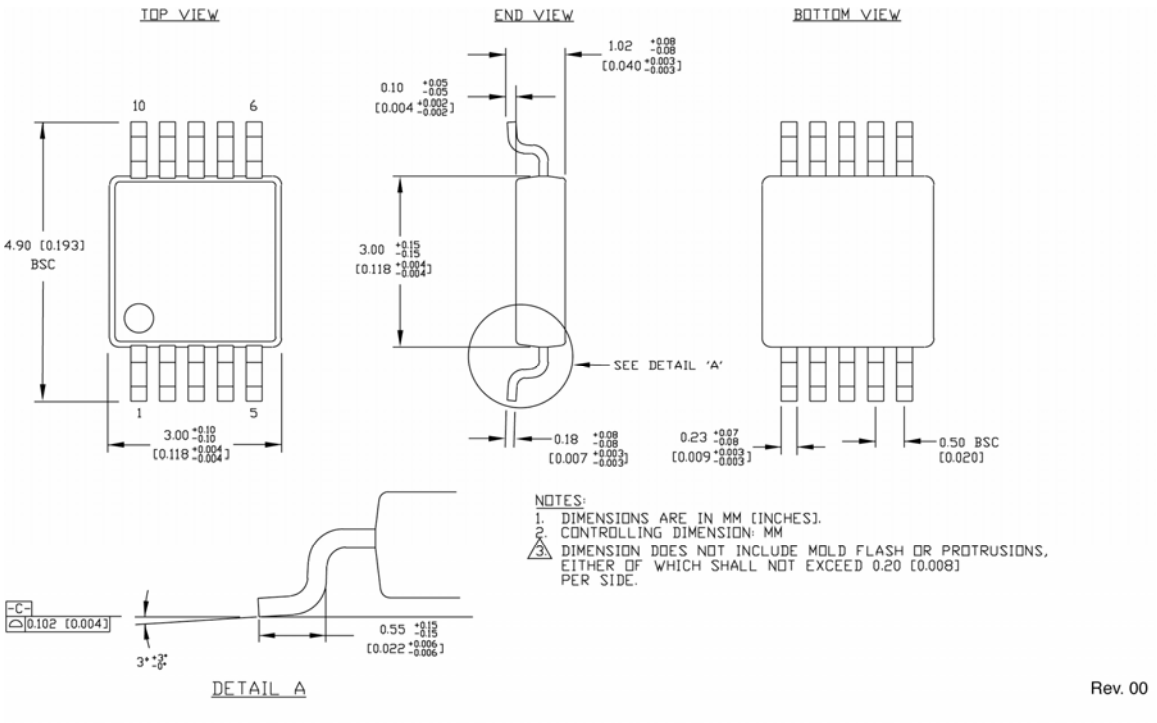
Figure 5. LOS_{LVL} Setting Circuit

Note: Recommended value for R_{LOSLVL} is 15kΩ or less.

Related Product and Support Documentation

Part Number	Function	Data Sheet Link
Application Notes	Notes on Sensitivity and Hysteresis in Micrel Post Amplifiers	http://www.micrel.com/product-info/app_hints+notes.shtml

Package Information



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MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http:/www.micrel.com