19-0291; Rev 1; 3/07

MAXIM

Hex/Quad, Power-Supply Supervisory Circuits

General Description

The MAX6887/MAX6888 multivoltage supply supervisors provide several voltage-detector inputs, one watchdog input, and three outputs. Each voltage-detector input offers a factory-set undervoltage and overvoltage threshold. Manual reset and margin disable inputs offer additional flexibility.

The MAX6887 offers six voltage-detector inputs, while the MAX6888 offers four inputs. Output $\overline{RESET}$ asserts when any input voltage drops below its respective undervoltage threshold or manual reset $\overline{MR}$ is asserted. Output $\overline{OV}$ asserts when any input voltage exceeds its respective overvoltage threshold. Monitor standard supply voltages listed in the *Selector Guide*.

The MAX6887/MAX6888 offer a watchdog timer with an initial and normal timeout periods of 102.4s and 1.6s, respectively. Watchdog output $\overline{WDO}$ asserts when the watchdog timer expires. Connect $\overline{WDO}$ to manual reset input $\overline{MR}$ to generate resets when the watchdog timer expires. $\overline{RESET}$, $\overline{OV}$, and $\overline{WDO}$ are active-low, open-drain outputs.

The MAX6887/MAX6888 are available in a 5mm x 5mm x 0.8mm, 16-pin thin QFN package and operate over the extended -40°C to +85°C temperature range.

Applications

Multivoltage Systems

Telecom

Networking

Servers/Workstations/Storage Systems

Features

- ♦ **Hex/Quad Voltage Detectors**
- ♦ **Undervoltage and Overvoltage Thresholds**
- ♦ **1% Threshold Accuracy**
- ♦ **Margining Disable and Manual Reset Input**
- ♦ **Watchdog Timer**
- ♦ **Open-Drain $\overline{RESET}$, $\overline{OV}$, and $\overline{WDO}$ Outputs**
- ♦ **180ms (min) Reset Timeout Period**
- ♦ **Few External Components**
- ♦ **Small 5mm x 5mm, 16-Pin Thin QFN Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX6887_ETE	-40°C to +85°C	16 Thin QFN	T1655-2
MAX6888_ETE	-40°C to +85°C	16 Thin QFN	T1655-2

Note: *Insert the desired letter from the Selector Guide into the blank to complete the part number.*

Pin Configurations and Typical Operating Circuit appear at end of data sheet.

Selector Guide

PART	NOMINAL INPUT VOLTAGE (V)*						TOL (%)
	IN1	IN2	IN3	IN4	IN5	IN6	
MAX6887AETE	5.0	3.3	2.5	1.8	Adj	Adj	5
MAX6887BETE	5.0	3.3	2.5	Adj	Adj	Adj	5
MAX6887CETE	5.0	3.3	1.8	Adj	Adj	Adj	5
MAX6887DETE	3.3	2.5	1.8	1.5	Adj	Adj	5
MAX6887EETE	3.3	2.5	1.8	Adj	Adj	Adj	5
MAX6887FETE	3.3	2.5	1.5	Adj	Adj	Adj	5
MAX6887GETE	3.3	2.5	Adj	Adj	Adj	Adj	5
MAX6887HETE	3.3	1.8	Adj	Adj	Adj	Adj	5
MAX6887QETE	Adj	Adj	Adj	Adj	Adj	Adj	5

PART	NOMINAL INPUT VOLTAGE (V)*						TOL (%)
	IN1	IN2	IN3	IN4	IN5	IN6	
MAX6887IETE	5.0	3.3	2.5	1.8	Adj	Adj	10
MAX6887JETE	5.0	3.3	2.5	Adj	Adj	Adj	10
MAX6887KETE	5.0	3.3	1.8	Adj	Adj	Adj	10
MAX6887LETE	3.3	2.5	1.8	1.5	Adj	Adj	10
MAX6887METE	3.3	2.5	1.8	Adj	Adj	Adj	10
MAX6887NETE	3.3	2.5	1.5	Adj	Adj	Adj	10
MAX6887OETE	3.3	2.5	Adj	Adj	Adj	Adj	10
MAX6887PETE	3.3	1.8	Adj	Adj	Adj	Adj	10
MAX6887RETE	Adj	Adj	Adj	Adj	Adj	Adj	10

**See thresholds options tables (Tables 1 and 2) for actual undervoltage and overvoltage thresholds.*

Selector Guides continued at end of data sheet.

Hex/Quad, Power-Supply Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
IN1–IN6, V_{CC}, $\overline{RESET}$, $\overline{OV}$, $\overline{WDO}$ .....-0.3V to +6V
WDI, $\overline{MR}$, $\overline{MARGIN}$ .....-0.3V to +6V
BP .....-0.3V to +3V
Input/Output Current (all pins).....±20mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin 5mm x 5mm Thin QFN
(derate 20.8mW/°C above +70°C).....1667mW
Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN1}–V_{IN4} or V_{CC} = 2.7V to 5.8V, WDI = GND, $\overline{MARGIN}$ = $\overline{MR}$ = BP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 3)		Voltage on either one of IN1–IN4 or V_{CC} to guarantee the part is fully operational	2.7		5.8	V
Supply Current	I_{CC}	V_{IN1} = 5.8V, IN2–IN6 = GND, no load		0.9	1.2	mA
Threshold Accuracy (See the *Selector Guide*)	V_{TH}	IN1–IN6, IN_ falling, T_A = +25°C to +85°C	-1		+1	% V_{TH}
		IN1–IN6, IN_ falling, T_A = -40°C to +85°C	-1.5		+1.5	
Threshold Hysteresis	$V_{TH-HYST}$			0.3		% V_{TH}
Threshold Tempco	ΔV_{TH}/°C			10		ppm/°C
IN_ Input Impedance	R_{IN}	For $V_{IN\_}$ < highest $V_{IN1–IN4}$ and $V_{IN\_}$ < V_{CC} (not ADJ), thresholds are not set as adjustable	130	200	300	kΩ
IN_ Input Leakage Current	I_{IN}	IN5, IN6 (MAX6887 only)	-150		+150	nA
		IN1–IN4 set as adjustable thresholds				
Power-Up Delay	t_{D-PO}	V_{CC} ≥ 2.5V			2.5	ms
IN_ to $\overline{RESET}$ or $\overline{OV}$ Delay	t_{D-R}	IN_ falling/rising, 100mV overdrive		20		µs
$\overline{RESET}$ Timeout Period	t_{RP}		180	200	220	ms
$\overline{OV}$ Timeout Period	t_{OP}			25		µs
$\overline{RESET}$, $\overline{OV}$, and $\overline{WDO}$ Output Low	V_{OL}	I_{SINK} = 4mA, output asserted			0.4	V
$\overline{RESET}$, $\overline{OV}$, and $\overline{WDO}$ Output Open-Drain Leakage Current	I_{LKG}	Output high impedance	-1		+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1}–V_{IN4} or V_{CC} = 2.7V to 5.8V, WDI = GND, $\overline{MARGIN}$ = $\overline{MR}$ = BP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

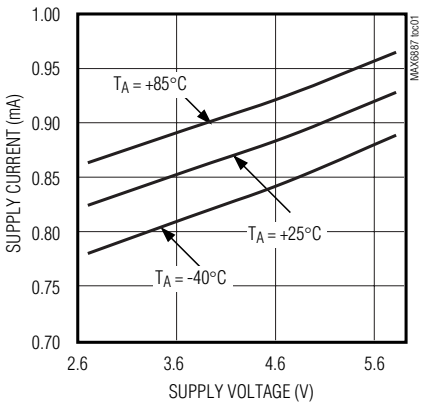
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{MR}$, $\overline{MARGIN}$, WDI Input Voltage	V_{IL}				0.6	V
	V_{IH}		1.4			
$\overline{MR}$ Input Pulse Width	$t_{\overline{MR}}$		1			µs
$\overline{MR}$ Glitch Rejection				100		ns
$\overline{MR}$ to $\overline{RESET}$ or $\overline{OV}$ Delay	$t_{D\text{-}\overline{MR}}$			200		ns
$\overline{MR}$ to Internal BP Pullup Current	$I_{\overline{MR}}$	$V_{\overline{MR}}$ = 1.4V	5	10	15	µA
$\overline{MARGIN}$ to Internal BP Pullup Current	$I_{\overline{MARGIN}}$	$V_{\overline{MARGIN}}$ = 1.4V	5	10	15	µA
WDI Pulldown Current	I_{WDI}	V_{WDI} = 0.6V	5	10	15	µA
WDI Input Pulse Width			50			ns
Watchdog Timeout Period	t_{WDI}	Initial	92.16	102.4	112.64	s
	t_{WD}	Normal	1.44	1.6	1.76	

Note 1: 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C are guaranteed by design.
Note 2: Device may be supplied from any one of IN1–IN4 or V_{CC}.
Note 3: The internal supply voltage, measured at V_{CC}, equals the maximum of IN1–IN4.
Note 4: Versions Q and R require that power be applied through V_{CC}.

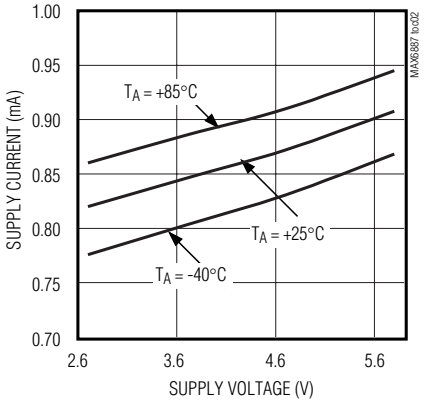
Typical Operating Characteristics

(V_{IN1}–V_{IN4} or V_{CC} = 5V, WDI = GND, $\overline{MARGIN}$ = $\overline{MR}$ = BP, T_A = +25°C, unless otherwise noted.)

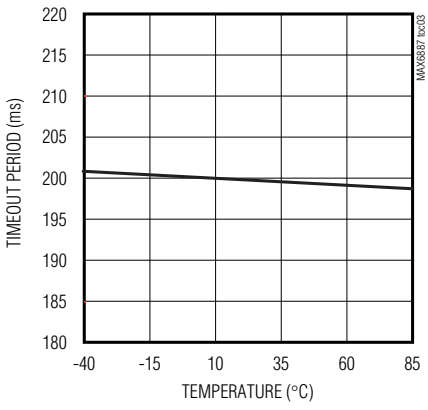
IN1–IN4 SUPPLY CURRENT vs. IN1–IN4 SUPPLY VOLTAGE



V_{CC} SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE



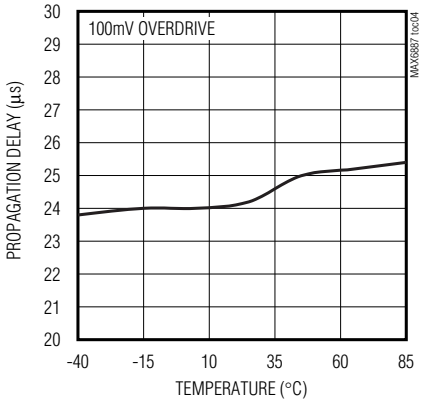
RESET TIMEOUT PERIOD vs. TEMPERATURE



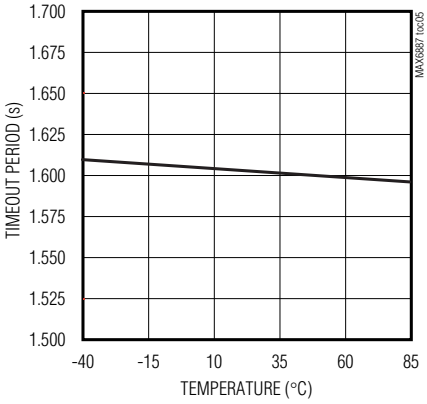
Typical Operating Characteristics (continued)

(V_{IN1}–V_{IN4} or V_{CC} = 5V, WDI = GND, $\overline{MARGIN}$ = $\overline{MR}$ = BP, T_A = +25°C, unless otherwise noted.)

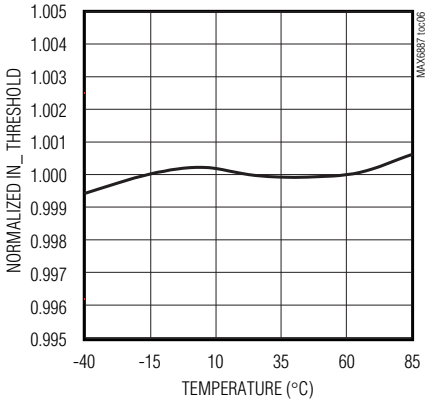
IN_ TO $\overline{RESET}$ OR $\overline{OV}$ PROPAGATION DELAY vs. TEMPERATURE



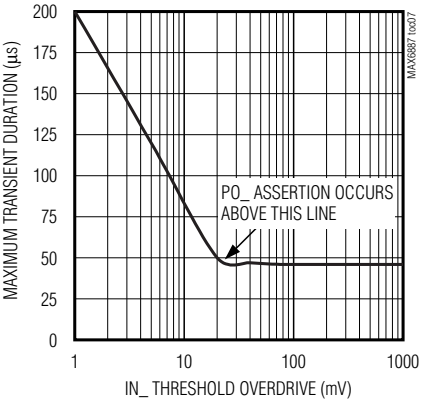
WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



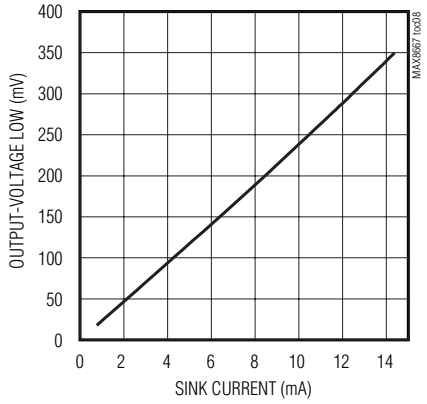
NORMALIZED IN_ THRESHOLD vs. TEMPERATURE



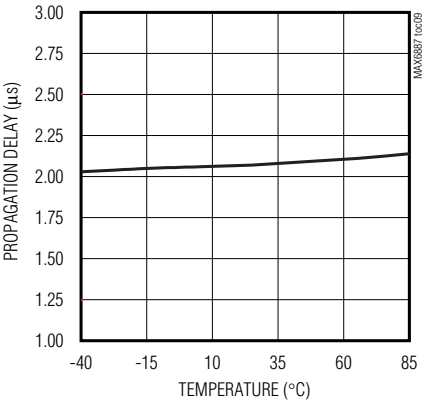
MAXIMUM IN_ TRANSIENT vs. IN_THRESHOLD OVERDRIVE



OUTPUT-VOLTAGE LOW vs. SINK CURRENT



$\overline{MR}$ TO $\overline{RESET}$ OUTPUT PROPAGATION DELAY vs. TEMPERATURE



Pin Description

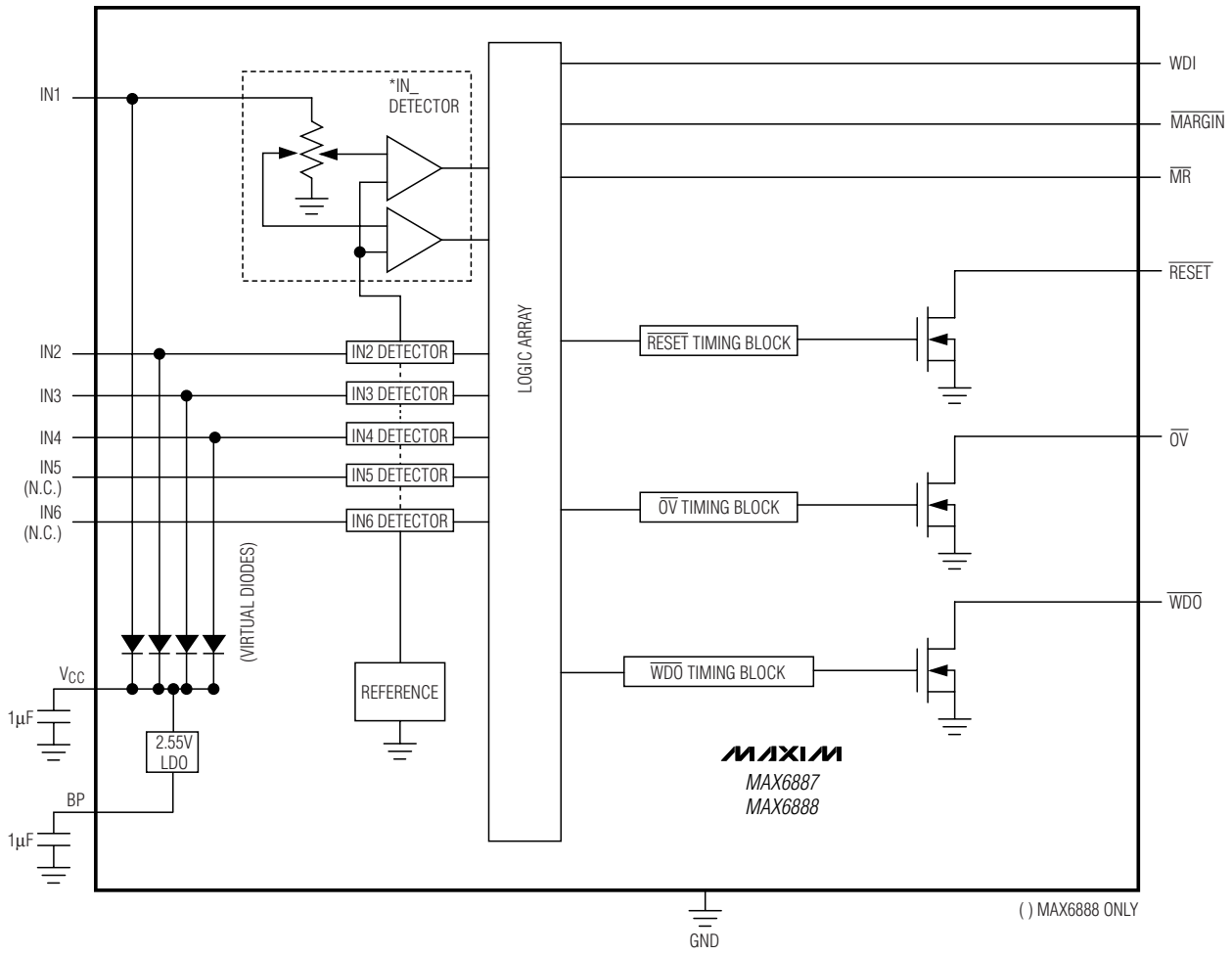
PIN		NAME	FUNCTION
MAX6887	MAX6888		
1	1	$\overline{RESET}$	Open-Drain, Active-Low Reset Output. $\overline{RESET}$ asserts when any input voltage falls below its undervoltage threshold or when $\overline{MR}$ is pulled low. $\overline{RESET}$ remains low for 200ms after all assertion-causing conditions are cleared. An external pullup resister is required.
2	2	$\overline{WDO}$	Open-Drain, Active-Low Watchdog Timer Output. Logic output for the watchdog timer function. $\overline{WDO}$ goes low when $\overline{WDI}$ is not strobed high-to-low or low-to-high within the watchdog timeout period.
3	3	$\overline{OV}$	Open-Drain Active-Low Overvoltage Output. $\overline{OV}$ asserts when any input voltage exceeds its overvoltage threshold. $\overline{OV}$ remains low for 25µs after all overvoltage conditions are cleared. An external pullup resistor is required.
4	4	GND	Ground

Pin Description (continued)

PIN		NAME	FUNCTION
MAX6887	MAX6888		
5	5	$\overline{MR}$	Manual Reset Input. Pull $\overline{MR}$ low to assert $\overline{RESET}$. Connect $\overline{MR}$ to $\overline{WDO}$ to generate resets when the watchdog timer expires. Leave $\overline{MR}$ unconnected or connect to DBP if unused. $\overline{MR}$ is internally pulled up to BP through a 10µA current source.
6	6	$\overline{MARGIN}$	Margin Input. When $\overline{MARGIN}$ is pulled low, $\overline{RESET}$ is held in its existing state independent of subsequent changes in monitored input voltages or the watchdog timer expiration. $\overline{MARGIN}$ is internally pulled up to BP through a 10µA current source. Leave $\overline{MARGIN}$ unconnected or connect to BP if unused. $\overline{MARGIN}$ overrides $\overline{MR}$ if both are asserted at the same time.
7	7	WDI	Watchdog Timer Input. Logic input for the watchdog timer function. If WDI is not strobed with a valid low-to-high or high-to-low transition within the selected watchdog timeout period, $\overline{WDO}$ asserts. WDI is internally pulled down to GND through a 10µA current sink.
8	8	I.C.	Internal Connection. Leave unconnected.
9	9	V_{CC}	Internal Power-Supply Voltage. Bypass V_{CC} to GND with a 1µF ceramic capacitor as close to the device as possible. V_{CC} supplies power to the internal circuitry. V_{CC} is internally powered from the highest of the monitored IN1–IN4 voltages. Do not use V_{CC} to supply power to external circuitry. To externally supply V_{CC}, see the *Powering the MAX6887/MAX6888* section.
10	10	BP	Bypass Voltage. The internally generated voltage at BP supplies power to internal logic and output $\overline{RESET}$. Connect a 1µF capacitor from BP to GND as close to the device as possible. Do not use BP to supply power to external circuitry.
11	—	IN6	Input Voltage Detector 6. IN6 monitors both undervoltage and overvoltage conditions. See the thresholds options (Tables 1 and 2) for available thresholds. IN6 cannot power the device. For improved noise immunity, bypass IN6 to GND with a 0.1µF capacitor installed as close to the device as possible.
12	—	IN5	Input Voltage Detector 5. IN5 monitors both undervoltage and overvoltage conditions. See the thresholds options (Tables 1 and 2) for available thresholds. IN5 cannot power the device. For improved noise immunity, bypass IN5 to GND with a 0.1µF capacitor installed as close to the device as possible.
13	13	IN4	Input Voltage Detector 4. IN4 monitors both undervoltage and overvoltage conditions. See the thresholds options (Tables 1 and 2) for available thresholds. Power the device through IN1–IN4 or V_{CC} (see the *Powering the MAX6887/MAX6888* section). For improved noise immunity, bypass IN4 to GND with a 0.1µF capacitor installed as close to the device as possible.
14	14	IN3	Input Voltage Detector 3. IN3 monitors both undervoltage and overvoltage conditions. See the thresholds options (Tables 1 and 2) for available thresholds. Power the device through IN1–IN4 or V_{CC} (see the *Powering the MAX6887/MAX6888* section). For improved noise immunity, bypass IN3 to GND with a 0.1µF capacitor installed as close to the device as possible.
15	15	IN2	Input Voltage Detector 2. IN2 monitors both undervoltage and overvoltage conditions. See the thresholds options (Tables 1 and 2) for available thresholds. Power the device through IN1–IN4 or V_{CC} (see the *Powering the MAX6887/MAX6888* section). For improved noise immunity, bypass IN2 to GND with a 0.1µF capacitor installed as close to the device as possible.
16	16	IN1	Input Voltage Detector 1. IN1 monitors both undervoltage and overvoltage conditions. See the thresholds options (Tables 1 and 2) for available thresholds. Power the device through IN1–IN4 or V_{CC} (see the *Powering the MAX6887/MAX6888* section). For improved noise immunity, bypass IN1 to GND with a 0.1µF capacitor installed as close to the device as possible.
—	11, 12	N.C.	No Connection. Not internally connected.
—	—	EP	Exposed Paddle. Internally connected to GND. Connect EP to GND or leave unconnected.

Hex/Quad, Power-Supply Supervisory Circuits

Functional Diagram



*FOR ADJUSTABLE INPUTS REFER TO THE *ADJUSTABLE THRESHOLD INPUTS* SECTION.

Detailed Description

The MAX6887/MAX6888 provide several supply-detector inputs, one watchdog input, and three outputs for power-supply monitoring applications. The MAX6887 offers six voltage-detector inputs, while the MAX6888 offers four. Each voltage-detector input offers both an undervoltage and overvoltage threshold.

The undervoltage and overvoltage thresholds are factory-set for monitoring standard supply voltages (see the *Selector Guide*). Inputs in the *Selector Guide* that contain "Adj" allow an external voltage-divider to be connected to set a user-defined threshold.

$\overline{RESET}$ goes low when any input voltage drops below its undervoltage threshold or when $\overline{MR}$ is brought low. $\overline{RESET}$ stays low for 200ms after all assertion-causing conditions have been cleared. $\overline{OV}$ goes low when an input voltage rises above its overvoltage threshold. $\overline{OV}$ typically stays low for 25µs (typ) after all inputs fall back under their overvoltage thresholds.

The MAX6887/MAX6888 offer a watchdog timer with initial and normal timeout periods of 102.4s and 1.6s, respectively. $\overline{WDO}$ goes low when the watchdog timer expires and deasserts when WDI transitions from low-to-high or high-to-low.

Powering the MAX6887/MAX6888

The MAX6887/MAX6888 derive power from the voltage-detector inputs IN1–IN4 or through an externally supplied V_{CC}. A virtual diode-ORing scheme selects the positive input that supplies power to the device (see the *Functional Diagram*). The highest input voltage on IN1–IN4 supplies power to the device. One of IN1–IN4 must be at least 2.7V to ensure proper operation.

Internal hysteresis ensures that the supply input that initially powered the device continues to power the device when multiple input voltages are within 50mV of each other.

V_{CC} powers the analog circuitry and is the bypass connection for the MAX6887/MAX6888 internal supply. Bypass V_{CC} to GND with a 1µF ceramic capacitor installed as close to the device as possible. The internal supply voltage, measured at V_{CC}, equals the maximum of IN1–IN4. If V_{CC} is externally supplied, V_{CC} must be at least 200mV higher than any voltage applied to IN1–IN4 and V_{CC} must be brought up first. V_{CC} always powers the device when all IN_ are factory set as "Adj." Do not use the internally generated V_{CC} to provide power to external circuitry.

The MAX6887/MAX6888 generate a supply voltage at BP for the internal logic circuitry. Bypass BP to GND with a 1µF ceramic capacitor installed as close to the device as possible. The nominal BP output voltage is +2.55V. Do not use BP to provide power to external circuitry.

Inputs

The MAX6887 offers six voltage-detector inputs, while the MAX6888 offers four voltage-detector inputs. Each voltage-detector input offers an undervoltage and overvoltage threshold set at the factory to monitor standard supply voltages (see the *Selector Guide*). The 5% and 10% tolerances are based on maximum and minimum threshold values. Actual thresholds for the MAX6887/MAX6888 are shown in Tables 1 and 2. Inputs in the *Selector Guide* listing "Adj" allow an external voltage-divider to be connected to set a user-defined threshold.

Adjustable Threshold Inputs

Inputs listed in the *Selector Guide* containing "Adj" for inputs allow external resistor voltage-dividers to be connected at the voltage-detector inputs. These inputs monitor any voltage supply higher than 0.6V (see Figure 1). Use the following equation to set a voltage-

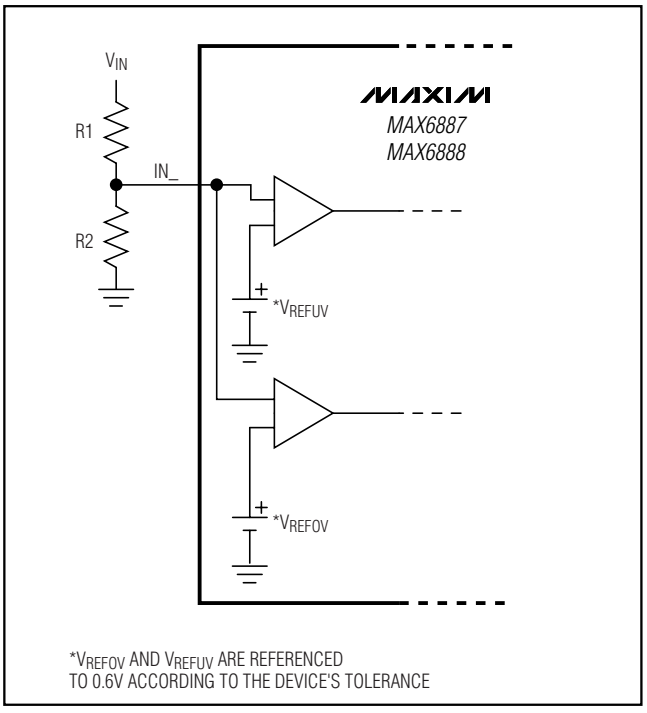


Figure 1. Adjusting the Monitored Threshold

detector input (IN1–IN6) to monitor a user-defined supply voltage:

$$0.6V = V_{MON} \times \left(\frac{R2}{R1+R2} \right)$$

where V_{MON} is the desired voltage to be monitored. Use the following procedure to design the proper voltage-divider and calculate thresholds:

1) Pick a value for R2. Use the equation above with the desired supply voltage to be monitored and solve for R1. Use high-value resistors R1 and R2 to minimize current consumption due to low leakage currents.
2) To find the actual undervoltage and overvoltage thresholds, use the following equations:

$$V_{ACTUALUV} = V_{MON} \times \left(\frac{V_{REFUV}}{0.6V} \right)$$

$$V_{ACTUALOV} = V_{MON} \times \left(\frac{V_{REFOV}}{0.6V} \right)$$

V_{REFUV} and V_{REFOV} are the undervoltage and overvoltage thresholds listed in Tables 1 and 2 that allow adjustable thresholds. Their values are based on tolerances of ±7.5% and ±12.5% from a 0.6V reference. See the *Selector Guide* to find which thresholds in Tables 1 and 2 are adjustable.

Manual Reset ($\overline{MR}$)

Many µP-based products require manual reset capability to allow an operator or external logic circuitry to initiate a reset. The manual reset input ($\overline{MR}$) can be connected directly to a switch without an external pullup resistor or debouncing network. $\overline{MR}$ is internally pulled up to BP. Leave unconnected if not used. $\overline{MR}$ is internally pulled up to BP through a 10µA current source. $\overline{MR}$ is designed to reject fast, falling transients (typically 100ns pulses) and $\overline{MR}$ must be held low for a minimum of 1µs to assert $\overline{RESET}$. Connect a 0.1µF capacitor from $\overline{MR}$ to ground to provide additional noise immunity. After $\overline{MR}$ transitions from low to high, $\overline{RESET}$ remains asserted for the duration of its time delay.

Margin Output Disable ($\overline{MARGIN}$)

$\overline{MARGIN}$ allows system-level testing while power supplies exceed the normal operating ranges. Drive $\overline{MARGIN}$ low to hold $\overline{RESET}$, $\overline{OV}$, and $\overline{WDO}$ in their

Table 1. MAX6887 Threshold Options

PART	UV THRESHOLDS (V)						OV THRESHOLDS (V)					
	IN1	IN2	IN3	IN4	IN5	IN6	IN1	IN2	IN3	IN4	IN5	IN6
MAX6887AETE	4.620	3.060	2.310	1.670	0.557	0.557	5.360	3.540	2.680	1.930	0.643	0.643
MAX6887BETE	4.620	3.060	2.310	0.557	0.557	0.557	5.360	3.540	2.680	0.643	0.643	0.643
MAX6887CETE	4.620	3.060	1.670	0.557	0.557	0.557	5.360	3.540	1.930	0.643	0.643	0.643
MAX6887DETE	3.060	2.310	1.670	1.390	0.557	0.557	3.540	2.680	1.930	1.610	0.643	0.643
MAX6887EETE	3.060	2.310	1.670	0.557	0.557	0.557	3.540	2.680	1.930	0.643	0.643	0.643
MAX6887FETE	3.060	2.310	1.390	0.557	0.557	0.557	3.540	2.680	1.610	0.643	0.643	0.643
MAX6887GETE	3.060	2.310	0.557	0.557	0.557	0.557	3.540	2.680	0.643	0.643	0.643	0.643
MAX6887HETE	3.060	1.670	0.557	0.557	0.557	0.557	3.540	1.930	0.643	0.643	0.643	0.643
MAX6887QETE	0.557	0.557	0.557	0.557	0.557	0.557	0.643	0.643	0.643	0.643	0.643	0.643
MAX6887IETE	4.380	2.880	2.190	1.580	0.527	0.527	5.620	3.700	2.810	2.020	0.673	0.673
MAX6887JETE	4.380	2.880	2.190	0.527	0.557	0.557	5.620	3.700	2.810	0.673	0.673	0.673
MAX6887KETE	4.380	2.880	1.580	0.527	0.557	0.557	5.620	3.700	2.020	0.673	0.673	0.673
MAX6887LETE	2.880	2.190	1.580	1.310	0.557	0.557	3.700	2.810	2.020	1.680	0.673	0.673
MAX6887METE	2.880	2.190	1.580	0.527	0.557	0.557	3.700	2.810	2.020	0.673	0.673	0.673
MAX6887NETE	2.880	2.190	1.310	0.527	0.557	0.557	3.700	2.810	1.680	0.673	0.673	0.673
MAX6887OETE	2.880	2.190	0.527	0.527	0.557	0.557	3.700	2.810	0.673	0.673	0.673	0.673
MAX6887PETE	2.880	1.580	0.527	0.527	0.557	0.557	3.700	2.020	0.673	0.673	0.673	0.673
MAX6887RETE	0.527	0.527	0.527	0.527	0.527	0.527	0.673	0.673	0.673	0.673	0.673	0.673

Table 2. MAX6888 Threshold Options

PART	UV THRESHOLDS (V)				OV THRESHOLDS (V)			
	IN1	IN2	IN3	IN4	IN1	IN2	IN3	IN4
MAX6888AETE	4.620	3.060	2.310	1.670	5.360	3.540	2.680	1.930
MAX6888BETE	4.620	3.060	2.310	0.557	5.360	3.540	2.680	0.643
MAX6888CETE	4.620	3.060	1.670	0.557	5.360	3.540	1.930	0.643
MAX6888DETE	3.060	2.310	1.670	1.390	3.540	2.680	1.930	1.610
MAX6888EETE	3.060	2.310	1.670	0.557	3.540	2.680	1.930	0.643
MAX6888FETE	3.060	2.310	1.390	0.557	3.540	2.680	1.610	0.643
MAX6888GETE	3.060	2.310	0.557	0.557	3.540	2.680	0.643	0.643
MAX6888HETE	3.060	1.670	0.557	0.557	3.540	1.930	0.643	0.643
MAX6888QETE	0.527	0.527	0.527	0.527	0.673	0.673	0.673	0.673
MAX6888IETE	4.380	2.880	2.190	1.580	5.620	3.700	2.810	2.020
MAX6888JETE	4.380	2.880	2.190	0.527	5.620	3.700	2.810	0.673
MAX6888KETE	4.380	2.880	1.580	0.527	5.620	3.700	2.020	0.673
MAX6888LETE	2.880	2.190	1.580	1.310	3.700	2.810	2.020	1.680
MAX6888METE	2.880	2.190	1.580	0.527	3.700	2.810	2.020	0.673
MAX6888NETE	2.880	2.190	1.310	0.527	3.700	2.810	1.680	0.673
MAX6888OETE	2.880	2.190	0.527	0.527	3.700	2.810	0.673	0.673
MAX6888PETE	2.880	1.580	0.527	0.527	3.700	2.020	0.673	0.673
MAX6888RETE	0.557	0.557	0.557	0.557	0.643	0.643	0.643	0.643

existing state while system-level testing occurs. Leave $\overline{\text{MARGIN}}$ unconnected or connect to BP if unused. An internal 10µA current source pulls $\overline{\text{MARGIN}}$ to BP. $\overline{\text{MARGIN}}$ overrides $\overline{\text{MR}}$ if both are asserted at the same time. The state of $\overline{\text{RESET}}$, $\overline{\text{OV}}$, and $\overline{\text{WDO}}$ does not change while $\overline{\text{MARGIN}}$ = GND.

$\overline{\text{RESET}}$, $\overline{\text{OV}}$, and $\overline{\text{WDO}}$ Outputs

The MAX6887/MAX6888 feature three active-low open-drain outputs: $\overline{\text{RESET}}$, $\overline{\text{OV}}$, and $\overline{\text{WDO}}$. After power-up or overvoltage/undervoltage conditions, $\overline{\text{RESET}}$ and $\overline{\text{OV}}$ remain in their active states until their timeout periods expire and no undervoltage/overvoltage conditions are present (see Figure 2).

$\overline{\text{OV}}$ asserts when any monitored input is above its overvoltage threshold and remains asserted until all inputs are below their thresholds and its respective 25µs timeout period expires. Connect $\overline{\text{OV}}$ to $\overline{\text{MR}}$ to bring $\overline{\text{RESET}}$ low during an overvoltage condition. $\overline{\text{OV}}$ requires a pullup resistor (unless connected to $\overline{\text{MR}}$).

$\overline{\text{RESET}}$ asserts when any monitored input is below its undervoltage threshold or $\overline{\text{MR}}$ is asserted. $\overline{\text{RESET}}$ remains asserted for 200ms after all assertion-causing conditions have been cleared. Configure $\overline{\text{RESET}}$ to assert when the watchdog timer expires by connecting $\overline{\text{WDO}}$ to $\overline{\text{MR}}$. $\overline{\text{RESET}}$ requires a pullup resistor.

$\overline{\text{WDO}}$ asserts when the watchdog timer expires. See the *Configuring the Watchdog Timer* section for a complete description. $\overline{\text{WDO}}$ requires a pullup resistor.

Configuring the Watchdog Timer

A watchdog timer monitors microprocessor (µP) software execution for a stalled condition and resets the µP if it stalls. Connect the watchdog timer output $\overline{\text{WDO}}$ to the reset input or a nonmaskable interrupt of the µP. The watchdog timer features independent initial and normal watchdog timeout periods of 102.4s and 1.6s, respectively.

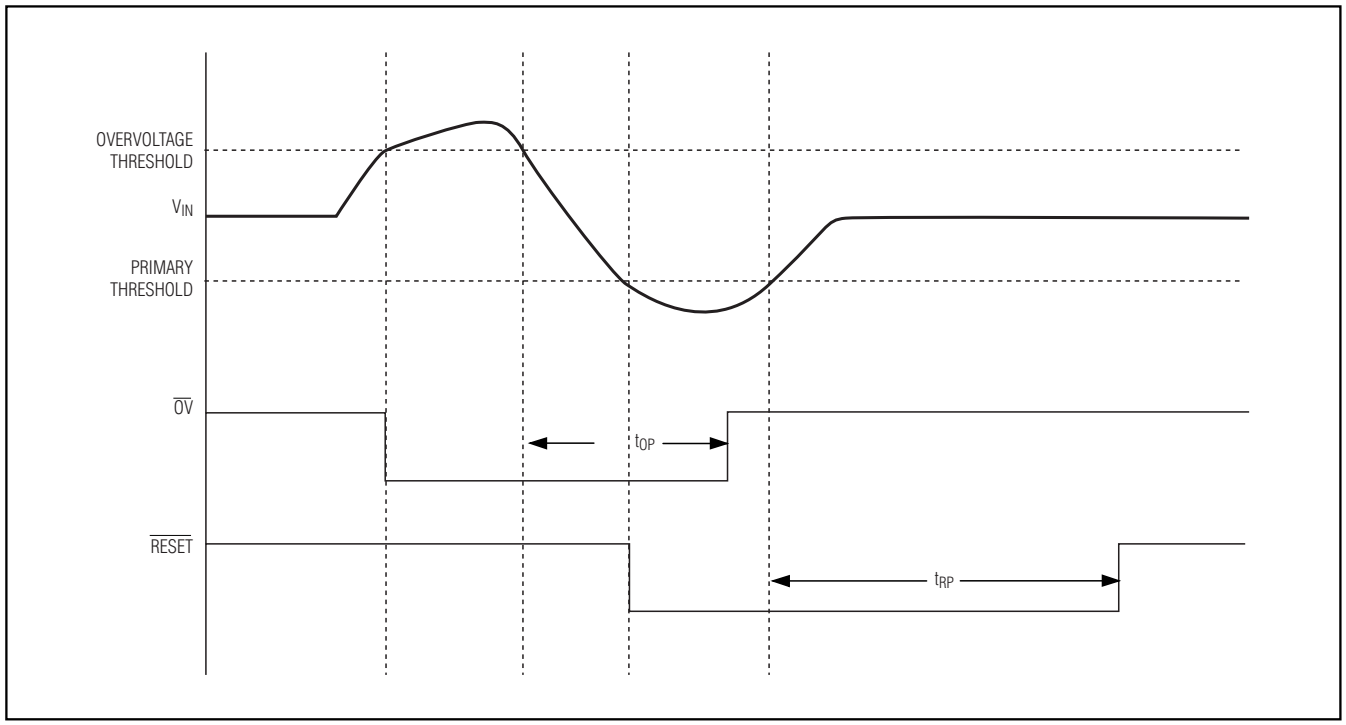


Figure 2. Output Timing Diagram

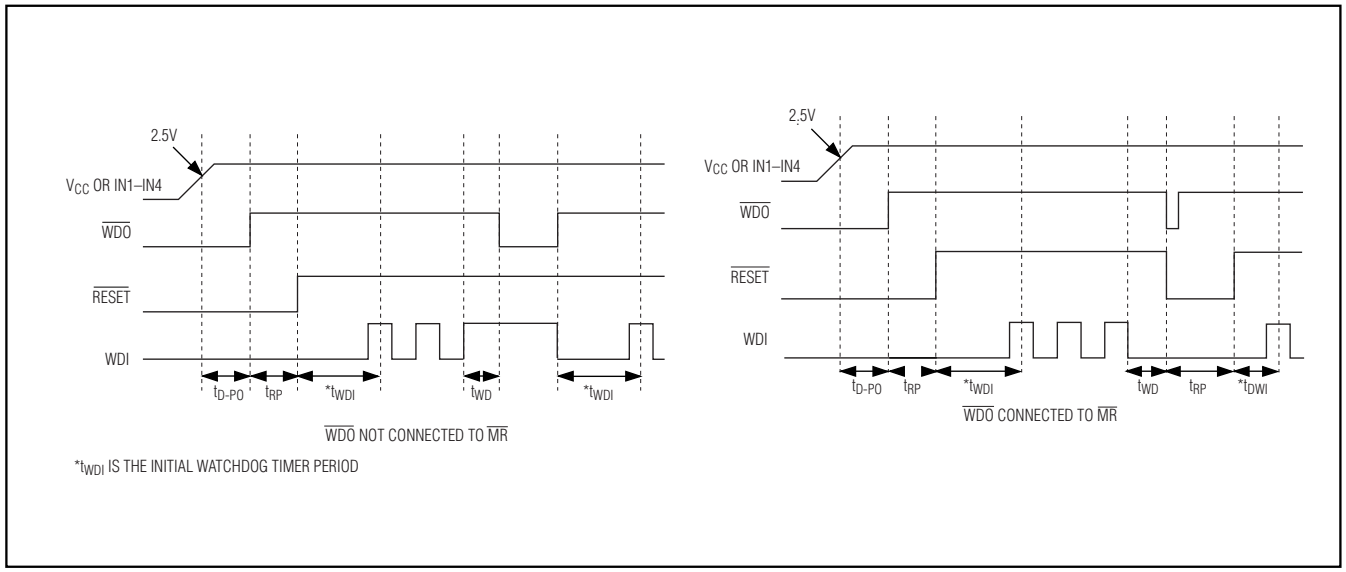


Figure 3. Watchdog, Reset, and Power-Up Timing Diagram

At power-up, $\overline{WDO}$ goes high after t_{D-PO} (see Figure 3). The initial watchdog timeout period (t_{WDI}) applies immediately after $\overline{WDO}$ is high. The initial watchdog timeout period allows the µP to perform its initialization process. A normal watchdog timeout period (t_{WD}) applies whenever WDI transitions from high to low after the initial watchdog timeout period occurs. WDI monitors the toggling output of the µP, indicating normal processor behavior. If WDI does not toggle during the normal watchdog timeout period (t_{WD}), indicating that the processor has stopped operating or is stuck in an infinite execution loop, $\overline{WDO}$ goes low. $\overline{WDO}$ stays low until the next transition on WDI. An initial watchdog timeout period (t_{WDI}) starts when $\overline{WDO}$ goes high.

If $\overline{WDO}$ is connected to $\overline{MR}$, the $\overline{WDO}$ will assert for a short duration (~5µs), long enough to assert the $\overline{RESET}$ output. Asserting $\overline{RESET}$ clears the watchdog timer and $\overline{WDO}$ goes high. The reset output will remain asserted for its timeout period after a watchdog fault. The watchdog timer stays cleared as long as $\overline{RESET}$ is low.

Applications Information

Layout and Bypassing

For better noise immunity, bypass each of the voltage-detector inputs to GND with 0.1µF capacitors installed as close to the device as possible. Bypass V_{CC} and BP to GND with 1µF capacitors installed as close to the device as possible. V_{CC} (when not externally supplied) and BP are internally generated voltages and should not be used to supply power to external circuitry.

Selector Guide (continued)

PART	NOMINAL INPUT VOLTAGE (V)*				TOLERANCE (%)
	IN1	IN2	IN3	IN4	
MAX6888AETE	5.0	3.3	2.5	1.8	5
MAX6888BETE	5.0	3.3	2.5	Adj	5
MAX6888CETE	5.0	3.3	1.8	Adj	5
MAX6888DETE	3.3	2.5	1.8	1.5	5
MAX6888EETE	3.3	2.5	1.8	Adj	5
MAX6888FETE	3.3	2.5	1.5	Adj	5
MAX6888GETE	3.3	2.5	Adj	Adj	5
MAX6888HETE	3.3	1.8	Adj	Adj	5
MAX6888QETE	Adj	Adj	Adj	Adj	5
MAX6888IETE	5.0	3.3	2.5	1.8	10
MAX6888JETE	5.0	3.3	2.5	Adj	10
MAX6888KETE	5.0	3.3	1.8	Adj	10
MAX6888LETE	3.3	2.5	1.8	1.5	10
MAX6888METE	3.3	2.5	1.8	Adj	10
MAX6888NETE	3.3	2.5	1.5	Adj	10
MAX6888OETE	3.3	2.5	Adj	Adj	10
MAX6888PETE	3.3	1.8	Adj	Adj	10
MAX6888RETE	Adj	Adj	Adj	Adj	10

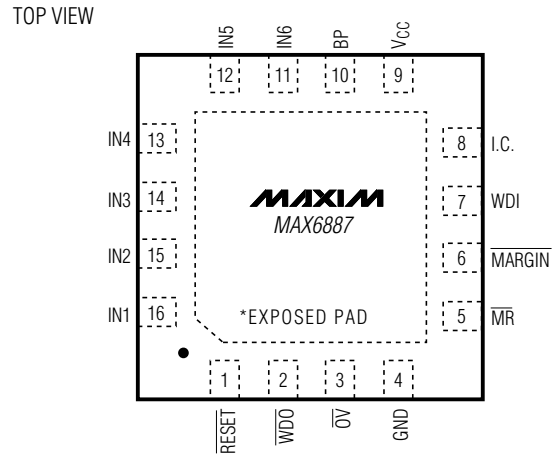
**See thresholds options tables (Tables 1 and 2) for actual undervoltage and overvoltage thresholds.*

Chip Information

PROCESS: BiCMOS

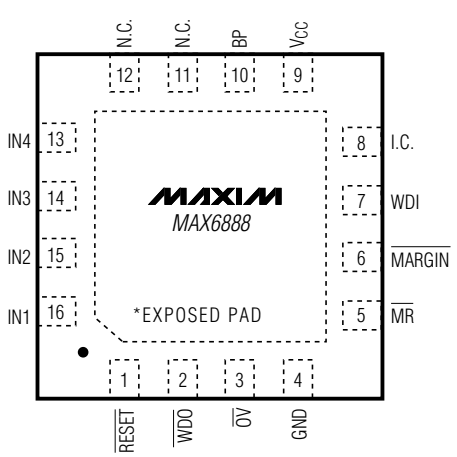
Hex/Quad, Power-Supply Supervisory Circuits

Pin Configurations



THIN QFN

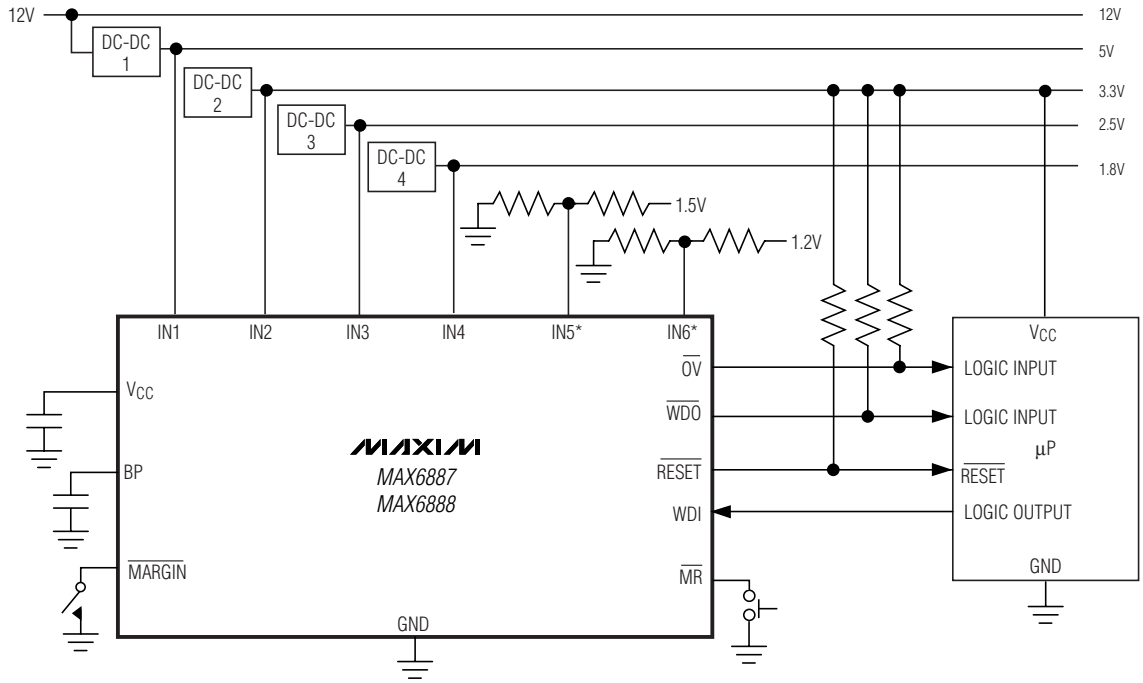
*EXPOSED PAD CONNECTED TO GND.



THIN QFN

*EXPOSED PAD CONNECTED TO GND.

Typical Operating Circuit

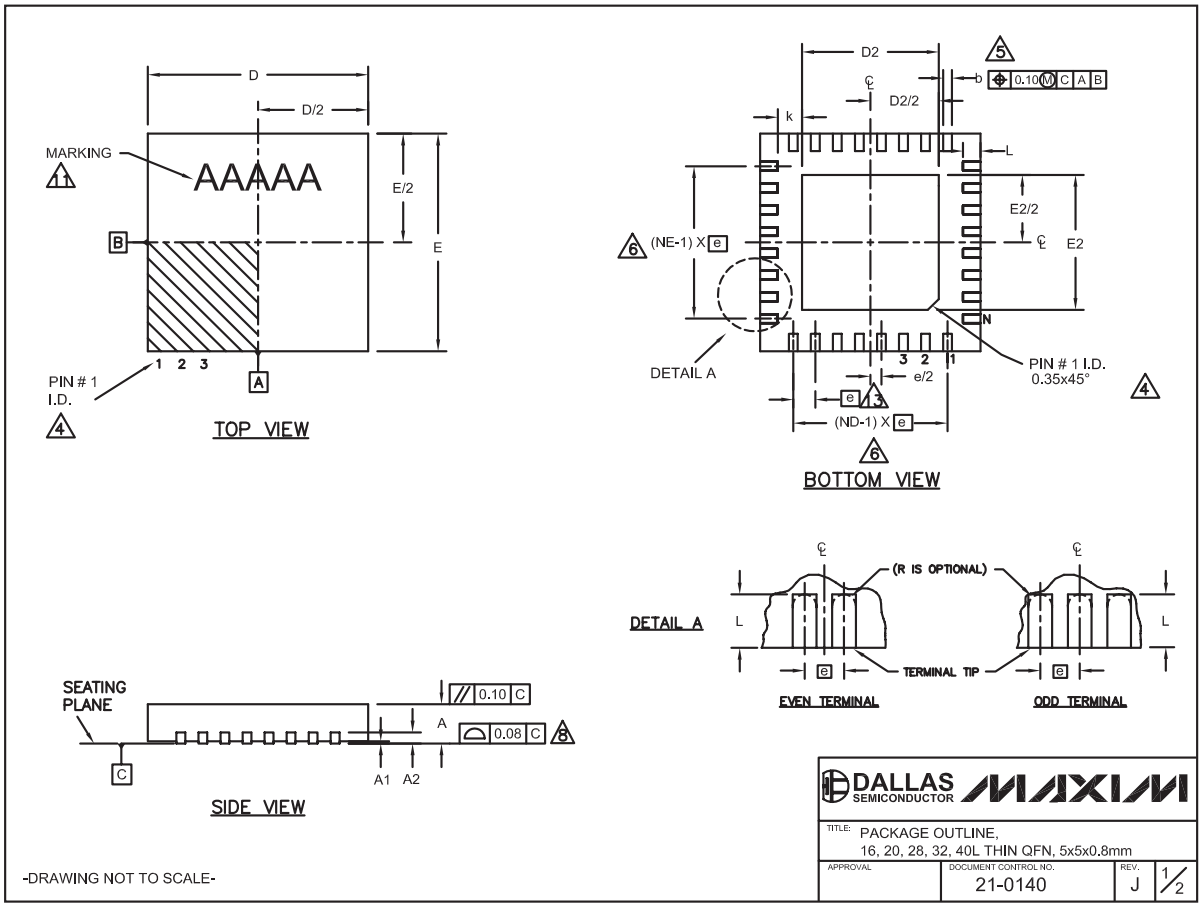


*MAX6887 ONLY

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



Hex/Quad, Power-Supply Supervisory Circuits

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			----			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	J	2/2

Revision History

Pages changed at Rev 1: 1, 5, 14