*PRELIMINARY CUSTOMER PROCUREMENT SPECIFICATION*

# Z86E02 SL1925

## CMOS Z8® OTP MICROCONTROLLER

## FEATURES

| Part Number | ROM (Kilobytes) | RAM* (Bytes) | Speed (MHz) |
|---|---|---|---|
| Z86E02 | 0.5 | 61 | 8 |

* General-Purpose

- 18-Pin DIP and SOIC Packages
- 3.5V to 5.5V Operating Range @ 0°C to +70°C
  4.5V to 5.5V Operating Range @ -40°C to +105°C
- 14 Input / Output Lines
- Five Vectored, Prioritized Interrupts with Programmable Polarity
- Two Analog Comparators
- WDT/Power-On Reset (POR)
- Program Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Permanent Watch-Dog Timer (WDT)
  - EPROM/TEST Mode Disable
  - RC Oscillator
- One Programmable 8-Bit Counter/Timer, with 6-Bit Programmable Prescaler
- On-Chip Oscillator that Accepts RC, XTAL, Ceramic Resonance, LC, or External Clock
- Clock-Free WDT Reset
- Low-Power Consumption (50 mw)
- Fast Instruction Pointer (1.5 µs @ 8 MHz)

## GENERAL DESCRIPTION

Zilog's Z86E02 Microcontroller (MCU) is a One-Time Programmable (OTP) member of the Z8 single-chip microcontroller family which allow easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E02's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

An on-chip counter/timer, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

**Note:** All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

| Connection | Circuit | Device |
|---|---|---|
| Power | $V_{CC}$ | $V_{DD}$ |
| Ground | GND | $V_{SS}$ |

## GENERAL DESCRIPTION (Continued)

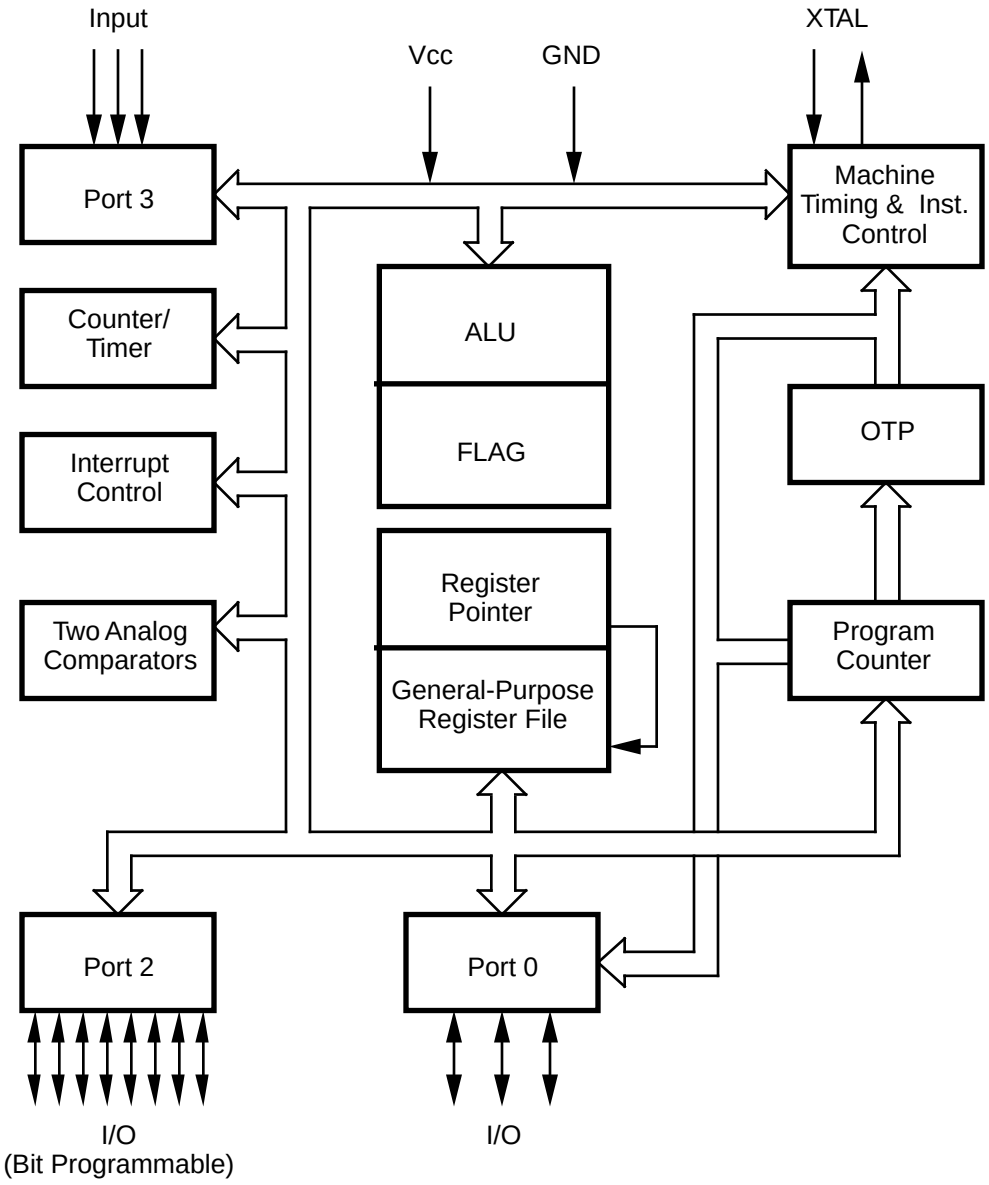


**Figure 1. Functional Block Diagram**

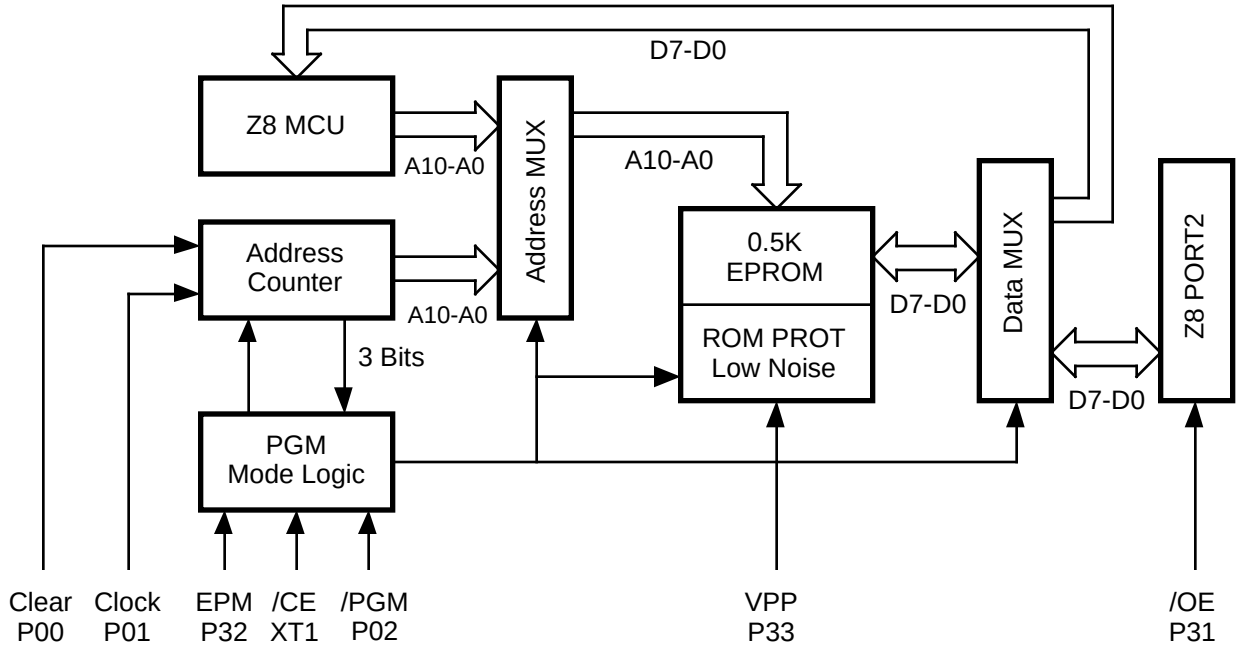


**Figure 2. EPROM Programming Mode Block Diagram**

## PIN DESCRIPTION

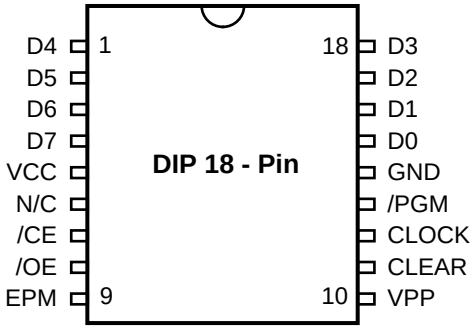


**Figure 3. 18-Pin EPROM Mode Configuration**

**Table 1. 18-Pin DIP Pin Identification**

| EPROM Programming Mode | | | |
|---|---|---|---|
| **Pin #** | **Symbol** | **Function** | **Direction** |
| 1–4 | D4–D7 | Data 4, 5, 6, 7 | In/Output |
| 5 | $V_{CC}$ | Power Supply | |
| 6 | N/C | No Connection | |
| 7 | /CE | Chip Enable | Input |
| 8 | /OE | Output Enable | Input |
| 9 | EPM | EPROM Prog Mode | Input |
| 10 | $V_{PP}$ | Prog Voltage | Input |
| 11 | Clear | Clear Clock | Input |
| 12 | Clock | Address | Input |
| 13 | /PGM | Prog Mode | Input |
| 14 | GND | Ground | |
| 15–18 | D3–D0 | Data 0,1, 2, 3 | In/Output |

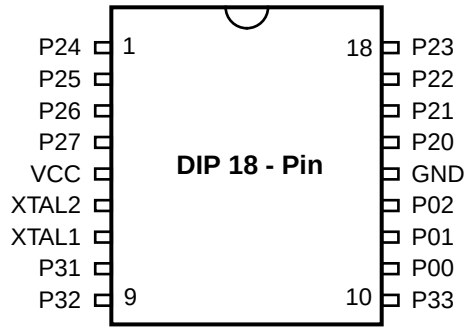


**Figure 4. 18-Pin DIP/SOIC Standard Mode Configuration**

**Table 2. 18-Pin DIP/SOIC Pin Identification**

| Standard Mode | | | |
|---|---|---|---|
| **Pin #** | **Symbol** | **Function** | **Direction** |
| 1–4 | P24–P27 | Port 2, Pins 4,5,6,7 | In/Output |
| 5 | $V_{cc}$ | Power Supply | |
| 6 | XTAL2 | Crystal Osc. Clock | Output |
| 7 | XTAL1 | Crystal Osc. Clock | Input |
| 8 | P31 | Port 3, Pin 1, AN1 | Input |
| 9 | P32 | Port 3, Pin 2, AN2 | Input |
| 10 | P33 | Port 3, Pin 3, REF | Input |
| 11–13 | P00–P02 | Port 0, Pins 0,1,2 | In/Output |
| 14 | GND | Ground | |
| 15–18 | P20–P23 | Port 2, Pins 0,1,2,3 | In/Output |

## ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

Total Power Dissipation = $V_{DD}$ x [$I_{DD}$ - (sum of $I_{OH}$)]
+ sum of [($V_{DD}$ - $V_{OH}$) x $I_{OH}$]
+ sum of ($V_{0L}$ x $I_{0L}$)

| Parameter | Min | Max | Units | Note |
|---|---|---|---|---|
| Ambient Temperature under Bias | –40 | +105 | C | |
| Storage Temperature | –65 | +150 | C | |
| Voltage on any Pin with Respect to $V_{SS}$ | –0.7 | +12 | V | 1 |
| Voltage on $V_{DD}$ Pin with Respect to $V_{SS}$ | –0.3 | +7 | V | |
| Voltage on Pins 7, 8, 9, 10 with Respect to $V_{SS}$ | –0.6 | $V_{DD}$+1 | V | 2 |
| Total Power Dissipation | | 462 | mW | |
| Maximum Allowable Current out of $V_{SS}$ | | 240 | mA | |
| Maximum Allowable Current into $V_{DD}$ | | 240 | mA | |
| Maximum Allowable Current into an Input Pin | –600 | +600 | µA | 3 |
| Maximum Allowable Current into an Open-Drain Pin | –600 | +600 | µA | 4 |
| Maximum Allowable Output Current Sinked by Any I/O Pin | | 20 | mA | |
| Maximum Allowable Output Current Sourced by Any I/O Pin | | 20 | mA | |

**Notes:**
[1] This applies to all pins except where otherwise noted. Maximum current into pin must be ±600 µA.
[2] There is no input protection diode from pin to $V_{DD}$ (not applicable to EPROM Mode).
[3] This excludes Pin 6 and Pin 7.
[4] Device pin is not at an output Low state.

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 5).

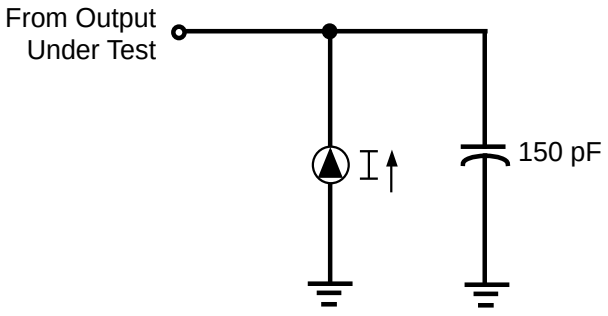


**Figure 5. Test Load Diagram**

## CAPACITANCE

**$T_A$ = 25°C, $V_{CC}$ = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.**

| Parameter | Min | Max |
|---|---|---|
| Input capacitance | 0 | 10 pF |
| Output capacitance | 0 | 20 pF |
| I/O capacitance | 0 | 25 pF |

## DC ELECTRICAL CHARACTERISTICS

| | | | $T_A$ = 0°C to +70°C | | Typical Note 4 | | | |
|---|---|---|---|---|---|---|---|---|
| Sym | Parameter | $V_{CC}$ [4] | Min | Max | @ 25°C | Units | Conditions | Notes |
| $V_{inmax}$ | Max Input Voltage | 3.5V | | 12 | | V | $I_{In}$<250 µA | 1 |
| | | 5.5V | | 12 | | V | $I_{In}$<250µA | 1 |
| $V_{CH}$ | Clock Input High Voltage | 3.5V | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 1.7 | V | Driven by External Clock Generator | |
| | | 5.5V | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 3.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 0.8 | V | Driven by External Clock Generator | |
| | | 5.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.7 | V | Driven by External Clock Generator | |
| $V_{IH}$ | Input High Voltage | 3.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 1.8 | V | | |
| | | 5.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | | |
| $V_{IL}$ | Input Low Voltage | 3.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 0.8 | V | | |
| | | 5.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.5 | V | | |
| $V_{OH}$ | Output High Voltage | 3.5V | $V_{CC}$–0.4 | | 3.0 | V | $I_{OH}$ = –2.0 mA | 5 |
| | | 5.5V | $V_{CC}$–0.4 | | 4.8 | V | $I_{OH}$ = –2.0 mA | 5 |
| | | 3.5V | $V_{CC}$–0.4 | | 3.0 | V | Low Noise @ $I_{OH}$ = –0.5 mA | |
| | | 5.5V | $V_{CC}$–0.4 | | 4.8 | V | Low Noise @ $I_{OH}$ = –0.5 mA | |
| $V_{OL1}$ | Output Low Voltage | 3.5V | | 0.8 | 0.2 | V | $I_{OL}$ = +4.0 mA | 5 |
| | | 5.5V | | 0.4 | 0.1 | V | $I_{OL}$ = +4.0 mA | 5 |
| | | 3.5V | | 0.4 | 0.2 | V | Low Noise @ $I_{OL}$ = 1.0 mA | |
| | | 5.5V | | 0.4 | 0.1 | V | Low Noise @ $I_{OL}$ = 1.0 mA | |
| $V_{OL2}$ | Output Low Voltage | 3.5V | | 1.2 | 1.0 | V | $I_{OL}$ = +10 mA, | 5 |
| | | 5.5V | | 1.2 | 0.8 | V | $I_{OL}$ = +10 mA, | 5 |
| $V_{OFFSET}$ | Comparator Input Offset Voltage | 3.5V | | 25.0 | 10.0 | mV | | |
| | | 5.5V | | 25.0 | 10.0 | mV | | |
| $V_{LV}$ | $V_{CC}$ Low Voltage Protection | | 2.6 | 3.2 | 2.9 | V | @ 4 MHz Max. Int. CLK Freq. | |
| $I_{IL}$ | Input Leakage (Input Bias Current of Comparator) | 3.5V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |

| Sym | Parameter | $V_{CC}$ [4] | $T_A$ = 0°C to +70°C Min | Max | Typical Note 4 @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $I_{OL}$ | Output Leakage | 3.5V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | –1.0 | 1.0 | | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $V_{VICR}$ | Comparator Input Common Mode Voltage Range | | $V_{SS}$–0.3 | $V_{CC}$ –1.0 | | V | | |
| $I_{CC}$ | Supply Current | 3.5V | | 3.5 | 1.5 | mA | All Output and I/O Pins Floating @ 2 MHz | 5,7 |
| | | 5.5V | | 7.0 | 6.8 | mA | All Output and I/O Pins Floating @ 2 MHz | 5,7 |
| | | 3.5V | | 8.0 | 3.0 | mA | All Output and I/O Pins Floating @ 8 MHz | 5,7 |
| | | 5.5V | | 11.0 | 8.2 | mA | All Output and I/O Pins Floating @ 8 MHz | 5,7 |
| $I_{CC1}$ | Standby Current | 3.5V | | 2.5 | 0.7 | mA | HALT mode $V_{IN}$ = 0V,$V_{CC}$ @ 2 MHz | 5,7 |
| | | 5.5V | | 4.0 | 2.5 | mA | HALT mode $V_{IN}$ = 0V,$V_{CC}$ @ 2 MHz | 5,7 |
| | | 3.5V | | 4.0 | 1.0 | mA | HALT mode $V_{IN}$ = 0V,$V_{CC}$ @ 8 MHz | 5,7 |
| | | 5.5V | | 5.0 | 3.0 | mA | HALT mode $V_{IN}$ = 0V,$V_{CC}$ @ 8 MHz | 5,7 |
| CC | Supply Current (Low Noise Mode) | 3.5V | | 3.5 | 1.5 | mA | All Output and I/O Pins Floating @ 1 MHz | 7 |
| | | 5.5V | | 7.0 | 6.8 | mA | All Output and I/O Pins Floating @ 1 MHz | 7 |
| CC | Supply Current (Low Noise Mode) | 3.5V | | 5.8 | 2.5 | mA | All Output and I/O Pins Floating @ 2 MHz | 7 |
| | | 5.5V | | 9.0 | 7.5 | mA | All Output and I/O Pins Floating @ 2 MHz | 7 |
| | | 3.5V | | 8.0 | 3.0 | mA | All Output and I/O Pins Floating @ 4 MHz | 7 |
| | | 5.5V | | 11.0 | 8.2 | mA | All Output and I/O Pins Floating @ 4 MHz | 7 |

## DC ELECTRICAL CHARACTERISTICS (Continued)

| Sym | Parameter | $V_{CC}$ [4] | $T_A$ = 0°C to +70°C Min | Max | Typical Note 4 @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $I_{CC1}$ | Standby Current (Low Noise Mode) | 3.5V | | 1.2 | 0.4 | mA | HALT mode $V_{IN}$ = 0V,$V_{CC}$ @ 1 MHz | 7 |
| | | 5.5V | | 1.6 | 0.9 | mA | HALT mode $V_{IN}$ = 0V,$V_{CC}$ @ 1 MHz | 7 |
| | | 3.5V | | 1.5 | 0.5 | mA | HALT mode $V_{IN}$ = 0V,$V_{CC}$ @ 2 MHz | 7 |
| | | 5.5V | | 1.9 | 1.0 | mA | HALT mode $V_{IN}$ = 0V,$V_{CC}$ @ 2 MHz | 7 |
| | | 3.5V | | 2.0 | 0.8 | mA | HALT mode $V_{IN}$ = 0V,$V_{CC}$ @ 4 MHz | 7 |
| | | 5.5V | | 2.4 | 0.3 | mA | HALT mode $V_{IN}$ = 0V,$V_{CC}$ @ 4 MHz | 7 |
| $I_{CC2}$ | Standby Current | 3.5V | | 10.0 | 1.0 | µA | STOP mode $V_{IN}$ = 0V, $V_{CC}$ WDT is not Running | 7,8 |
| | | 5.5V | | 10.0 | 1.0 | µA | STOP mode $V_{IN}$ = 0V, $V_{CC}$ WDT is not Running | 7,8 |
| $I_{ALL}$ | Auto Latch Low Current | 3.5V | | 12.0 | 3.0 | µA | 0V < $V_{IN}$ < $V_{CC}$ | 6 |
| | | 5.5V | | 32 | 16 | µA | 0V < $V_{IN}$ < $V_{CC}$ | 6 |
| $I_{ALH}$ | Auto Latch High Current | 3.5V | | –8.0 | –1.5 | µA | 0V < $V_{IN}$ < $V_{CC}$ | 6 |
| | | 5.5V | | –16.0 | –8.0 | µA | 0V < $V_{IN}$ < $V_{CC}$ | 6 |

**Notes:**

1. Port 2 and Port 0 only.
2. $V_{SS}$ = 0V = GND.
3. The device operates down to $V_{RST}$ of the specified frequency for $V_{RST.}$ The minimum operational $V_{CC}$ is determined on the value of the voltage $V_{RST}$ at the ambient temperature. The $V_{RST}$ increases as the temperature decreases.
4. $V_{CC}$ = 4.5V to 5.5V, typical values measured at $V_{CC}$ = 5.0V.
5. Standard Mode (not Low EMI mode).
6. Autolatches are enabled.
7. All outputs unloaded and all inputs are at $V_{CC}$ or $V_{SS}$ level.
8. If analog comparator is selected, then the comparator inputs must be at $V_{CC}$ level.

| Sym | Parameter | $V_{CC}$ [4] | $T_A$ = -40°C to +105°C Min | Max | Typical Note 4 @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| | Max Input Voltage | 4.5V | | 12.0 | | V | $I_{IN}$ < 250 µA | 1 |
| | | 5.5V | | 12.0 | | V | $I_{IN}$ < 250 µA | 1 |
| $V_{CH}$ | Clock Input High Voltage | 4.5V | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | Driven by External Clock Generator | |
| | | 5.5V | 0.8 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | Driven by External Clock Generator | |
| $V_{CL}$ | Clock Input Low Voltage | 4.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.7 | V | Driven by External Clock Generator | |
| | | 5.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.7 | V | Driven by External Clock Generator | |
| $V_{IH}$ | Input High Voltage | 4.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | | |
| | | 5.5V | 0.7 $V_{CC}$ | $V_{CC}$+0.3 | 2.8 | V | | |
| $V_{IL}$ | Input Low Voltage | 4.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.5 | V | | |
| | | 5.5V | $V_{SS}$–0.3 | 0.2 $V_{CC}$ | 1.5 | V | | |
| $V_{OH}$ | Output High Voltage | 4.5V | $V_{CC}$–0.4 | | 4.8 | V | $I_{OH}$ = –2.0 mA | 5 |
| | | 5.5V | $V_{CC}$–0.4 | | 4.8 | V | $I_{OH}$ = –2.0 mA | 5 |
| | | 4.5V | $V_{CC}$–0.4 | | | V | Low Noise @ $I_{OH}$ = –0.5 mA | |
| | | 5.5V | $V_{CC}$–0.4 | | | V | Low Noise @ $I_{OH}$ = –0.5 mA | |
| $V_{OL1}$ | Output Low Voltage | 4.5V | | 0.8 | 0.1 | V | $I_{OL}$ = +4.0 mA | 5 |
| | | 5.5V | | 0.4 | 0.1 | V | $I_{OL}$ = +4.0 mA | 5 |
| | | 4.5V | | 0.4 | 0.1 | V | Low Noise @ $I_{OL}$ = 1.0 mA | |
| | | 5.5V | | 0.4 | 0.1 | V | Low Noise @ $I_{OL}$ = 1.0 mA | |
| $V_{OL2}$ | Output Low Voltage | 4.5V | | 1.2 | 1.0 | V | $I_{OL}$ = +10 mA, | 5 |
| | | 5.5V | | 1.2 | 0.8 | V | $I_{OL}$ = +10 mA, | 5 |
| $V_{OFFSET}$ | Comparator Input Offset Voltage | 4.5V | | 25.0 | 10.0 | mV | | |
| | | 5.5V | | 25.0 | 10.0 | mV | | |
| $V_{LV}$ | $V_{CC}$ Low Voltage Protection | | 2.3 | 3.5 | 2.9 | V | @ 4 MHz Max. Int. CLK Freq. | 3 |
| $I_{IL}$ | Input Leakage (Input Bias Current of Comparator) | 4.5V | | –1.0 | 1.0 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | | –1.0 | 1.0 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $I_{OL}$ | Output Leakage | 4.5V | | –1.0 | 1.0 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| | | 5.5V | | –1.0 | 1.0 | µA | $V_{IN}$ = 0V, $V_{CC}$ | |
| $V_{VICR}$ | Comparator Input Common Mode Voltage Range | | $V_{SS}$ –0.3 | $V_{CC}$ –1.5 | | V | | |
| $I_{CC}$ | Supply Current | 4.5V | | 7.0 | 6.8 | mA | All Output and I/O Pins Floating @ 2 MHz | 5,7 |
| | | 5.5V | | 7.0 | 6.8 | mA | All Output and I/O Pins Floating @ 2 MHz | 5,7 |
| | | 4.5V | | 11.0 | 8.2 | mA | All Output and I/O Pins Floating @ 8 MHz | 5,7 |
| | | 5.5V | | 11.0 | 8.2 | mA | All Output and I/O Pins Floating @ 8 MHz | 5,7 |

## DC ELECTRICAL CHARACTERISTICS (Continued)

| Sym | Parameter | $V_{CC}$ [4] | $T_A$ = -40°C to +105°C Min | Max | Typical Note 4 @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $I_{CC1}$ | Standby Current | 4.5V | | 3.0 | 2.5 | mA | HALT mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 5,7 |
| | | 5.5V | | 3.0 | 2.5 | mA | HALT mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 5,7 |
| | | 4.5V | | 5.0 | 3.0 | mA | HALT mode $V_{IN}$ = 0V, $V_{CC}$ @ 8 MHz | 5,7 |
| | | 5.5V | | 5.0 | 3.0 | mA | HALT mode $V_{IN}$ = 0V, $V_{CC}$ @ 8 MHz | 5,7 |
| $I_{CC}$ | Supply Current (Low Noise Mode) | 4.5V | | 7.0 | 6.8 | mA | All Output and I/O Pins Floating @ 1 MHz | 7 |
| | | 5.5V | | 7.0 | 6.8 | mA | All Output and I/O Pins Floating @ 1 MHz | 7 |
| | | 4.5V | | 9.0 | 7.5 | mA | All Output and I/O Pins Floating @ 2 MHz | 7 |
| | | 5.5V | | 9.0 | 7.5 | mA | All Output and I/O Pins Floating @ 2 MHz | 7 |
| | | 4.5V | | 11.0 | 8.2 | mA | All Output and I/O Pins Floating @ 4 MHz | 7 |
| | | 5.5V | | 11.0 | 8.2 | mA | All Output and I/O Pins Floating @ 4 MHz | 7 |

| Sym | Parameter | $V_{CC}$ [4] | $T_A$ = -40°C to +105°C Min | Max | Typical Note 4 @ 25°C | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|
| $I_{CC1}$ | Standby Current (Low Noise Mode) | 4.5V | | 1.6 | 0.9 | mA | HALT mode $V_{IN}$ = 0V, $V_{CC}$ @ 1 MHz | 7 |
| | | 5.5V | | 1.6 | 0.9 | mA | HALT mode $V_{IN}$ = 0V, $V_{CC}$ @ 1 MHz | 7 |
| | | 4.5V | | 1.9 | 1 | mA | HALT mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 7 |
| | | 5.5V | | 1.9 | 1 | mA | HALT mode $V_{IN}$ = 0V, $V_{CC}$ @ 2 MHz | 7 |
| $I_{CC2}$ | Standby Current | 4.5V | | 20 | 1.0 | µA | STOP mode $V_{IN}$ = 0V, $V_{CC}$ WDT is not Running | 7,8 |
| | | 5.5V | | 20 | 1.0 | µA | STOP mode $V_{IN}$ = 0V, $V_{CC}$ WDT is not Running | 7,8 |
| $_{ALL}$ | Auto Latch Low Current | 4.5V | | 40 | 16 | µA | $0V < V_{IN} < V_{CC}$ | 6 |
| | | 5.5V | | 40 | 16 | µA | $0V < V_{IN} < V_{CC}$ | 6 |
| $I_{ALH}$ | Auto Latch High Current | 4.5V | | –20.0 | –8.0 | µA | $0V < V_{IN} < V_{CC}$ | 6 |
| | | 5.5V | | –20.0 | –8.0 | µA | $0V < V_{IN} < V_{CC}$ | 6 |

**Notes:**

1. Port 2 and Port 0 only.
2. $V_{SS}$ = 0V = GND.
3. The device operates down to $V_{RST}$ of the specified frequency for $V_{RST.}$ The minimum operational $V_{CC}$ is determined on the value of the voltage $V_{RST}$ at the ambient temperature. The $V_{RST}$ increases as the temperature decreases.
4. $V_{CC}$ = 4.5V to 5.5V, typical values measured at $V_{CC}$ = 5.0V.
5. Standard Mode (not Low EMI mode).
6. Autolatches are enabled.
7. All outputs unloaded and all inputs are at $V_{CC}$ or $V_{SS}$ level.
8. If analog comparator is selected, then the comparator inputs must be at $V_{CC}$ level.

## AC ELECTRICAL CHARACTERISTICS

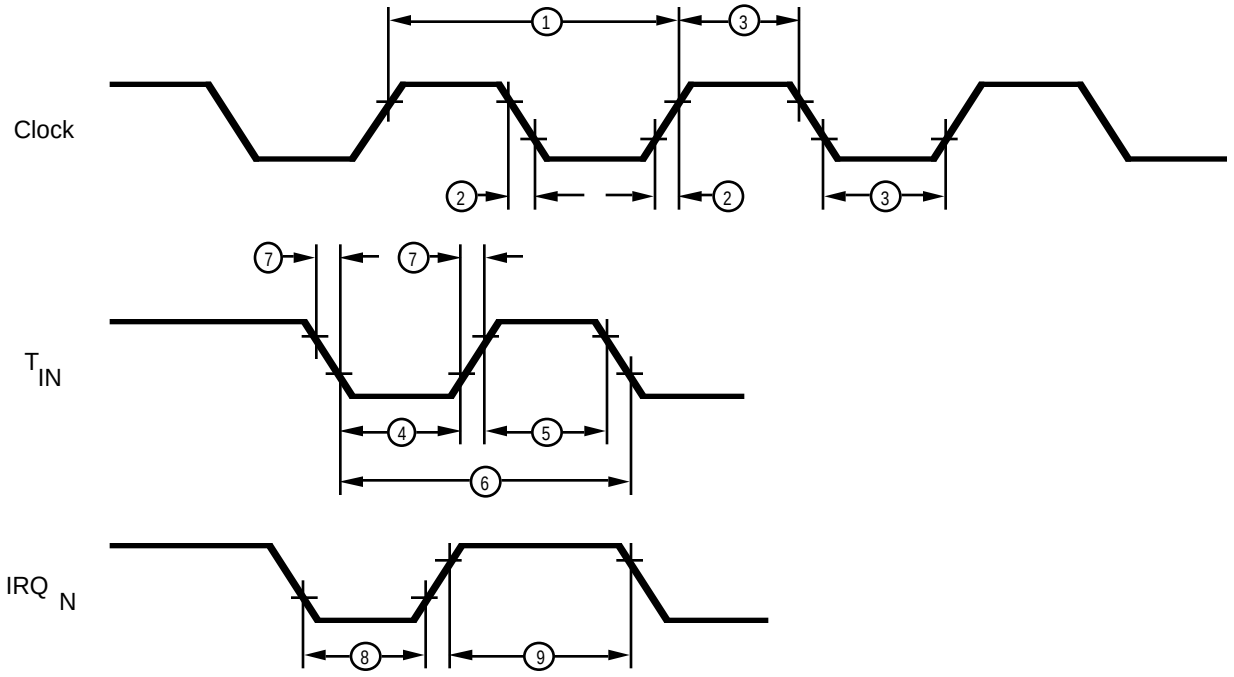


**Figure 6. AC Electrical Timing Diagram**

## AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

| | | | $T_A$= 0°C to +70°C 8 MHz | | | | |
|---|---|---|---|---|---|---|---|
| **No** | **Symbol** | **Parameter** | **$V_{CC}$** | **Min** | **Max** | **Units** | **Notes** |
| 1 | TpC | Input Clock Period | 3.5V | 125 | DC | ns | 1 |
| | | | 5.5V | 125 | DC | ns | 1 |
| 2 | TrC,TfC | Clock Input Rise and Fall Times | 3.5V | | 25 | ns | 1 |
| | | | 5.5V | | 25 | ns | |
| 3 | TwC | Input Clock Width | 3.5V | 62 | | ns | 1 |
| | | | 5.5V | 62 | | ns | 1 |
| 4 | TwTinL | Timer Input Low Width | 3.5V | 100 | | ns | [ |
| | | | 5.5V | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 3.5V | 5TpC | | | 1 |
| | | | 5.5V | 5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 3.5V | | 8TpC | | 1 |
| | | | 5.5V | | 8TpC | | [ |
| 7 | TrTin, TtTin | Timer Input Rise and Fall Time | 3.5V | | 100 | ns | 1 |
| | | | 5.5V | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 3.5V | 100 | | ns | 1,2 |
| | | | 5.5V | 70 | | ns | 1,2 |
| 9 | TwIH | Int. Request Input High Time | 3.5V | | 5TpC | | 1 |
| | | | 5.5V | | 5TpC | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time for Timeout | 3.5V | 10 | | ms | 1 |
| | | | 5.5V | 5 | | ms | 1 |
| 11 | Tpor | Power-On Reset Time | 3.5V | 4 | 36 | ms | 1 |
| | | | 5.5V | 2 | 18 | ms | 1 |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request through Port 3 (P33-P31).

## AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

| | | | $T_A$= –40°C to +105°C 8 MHz | | | | |
|---|---|---|---|---|---|---|---|
| **No** | **Symbol** | **Parameter** | **$V_{CC}$** | **Min** | **Max** | **Units** | **Notes** |
| 1 | TpC | Input Clock Period | 4.5V | 125 | DC | ns | 1 |
| | | | 5.5V | 125 | DC | ns | 1 |
| 2 | TrC,TfC | Clock Input Rise and Fall Times | 4.5V | | 25 | ns | 1 |
| | | | 5.5V | | 25 | ns | |
| 3 | TwC | Input Clock Width | 4.5V | | 62 | ns | 1 |
| | | | 5.5V | | 62 | ns | 1 |
| 4 | TwTinL | Timer Input Low Width | 4.5V | 70 | | ns | 1 |
| | | | 5.5V | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 4.5V | 5TpC | | | 1 |
| | | | 5.5V | 5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 4.5V | 8TpC | | | 1 |
| | | | 5.5V | 8TpC | | | 1 |
| 7 | TrTin, TtTin | Timer Input Rise and Fall Timer | 4.5V | | 100 | ns | 1 |
| | | | 5.5V | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 4.5V | 70 | | ns | 1,2 |
| | | | 5.5V | 70 | | ns | 1,2 |
| 9 | TwIH | Int. Request Input High Time | 4.5V | 5TpC | | | 1 |
| | | | 5.5V | 5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time for Timeout | 4.5V | 5 | | ms | 1 |
| | | | 5.5V | 5 | | ms | 1 |
| 11 | Tpor | Power-On Reset Time | 4.5V | 2 | 20 | ms | 1 |
| | | | 5.5V | 2 | 20 | ms | 1 |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request through Port 3 (P33-P31).

## AC ELECTRICAL CHARACTERISTICS

Low Noise Mode

| | | | | $T_A$= 0°C to +70°C | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 1 MHz | | 4 MHz | | | |
| **No** | **Symbol** | **Parameter** | **$V_{CC}$** | **Min** | **Max** | **Min** | **Max** | **Units** | **Notes** |
| 1 | TPC | Input Clock Period | 3.5V | 1000 | DC | 250 | DC | ns | 1 |
| | | | 5.5V | 1000 | DC | 250 | DC | ns | 1 |
| 2 | TrC<br>TfC | Clock Input Rise and Fall Times | 3.5V | | 25 | | 25 | ns | 1 |
| | | | 5.5V | | 25 | | 25 | ns | 1 |
| 3 | TwC | Input Clock Width | 3.5V | 500 | | 125 | | ns | 1 |
| | | | 5.5V | 500 | | 125 | | ns | 1 |
| 4. | TwTinL | Timer Input Low Width | 3.5V | 100 | | 100 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 3.5V | 2.5TpC | | 2.5TpC | | | 1 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 3.5V | 4TpC | | 4TpC | | | 1 |
| | | | 5.5V | 4TpC | | 4TpC | | | 1 |
| 7 | TrTin,<br>TtTin | Timer Input Rise and Fall Timer | 3.5V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |
| 8 | TwIL<br>Low Time | Int. Request Input | 3.5V | 100 | | 100 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | TwIH<br>High Time | Int. Request Input | 3.5V | 2.5TpC | | 2.5TpC | | | 1 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time for Timeout | 3.5V | 10 | | 10 | | ms | 1 |
| | | | 5.5V | 5 | | 5 | | ms | 1 |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request through Port 3 (P33-P31).

## AC ELECTRICAL CHARACTERISTICS

Low Noise Mode

| | | | | $T_A$= –40°C to +105°C 1 MHz | | 4 MHz | | | |
|---|---|---|---|---|---|---|---|---|---|
| **No** | **Symbol** | **Parameter** | **$V_{CC}$** | **Min** | **Max** | **Min** | **Max** | **Units** | **Notes** |
| 1 | TPC | Input Clock Period | 4.5V | 1000 | DC | 250 | DC | ns | 1 |
| | | | 5.5V | 1000 | DC | 250 | DC | ns | 1 |
| 2 | TrC<br>TfC | Clock Input Rise and Fall Times | 4.5V | | 25 | | 25 | ns | 1 |
| | | | 5.5V | | 25 | | 25 | ns | 1 |
| 3 | TwC | Input Clock Width | 4.5V | 500 | | 125 | | ns | 1 |
| | | | 5.5V | 500 | | 125 | | ns | 1 |
| 4. | TwTinL | Timer Input Low Width | 4.5V | 70 | | 70 | | ns | 1 |
| | | | 5.5V | 70 | | 70 | | ns | 1 |
| 5 | TwTinH | Timer Input High Width | 4.5V | 2.5TpC | | 2.5TpC | | | 1 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | | 1 |
| 6 | TpTin | Timer Input Period | 4.5V | | 4TpC | 4TpC | | | 1 |
| | | | 5.5V | | 4TpC | 4TpC | | | 1 |
| 7 | TrTin,<br>TtTin | Timer Input Rise and Fall Timer | 4.5V | | 100 | | 100 | ns | 1 |
| | | | 5.5V | | 100 | | 100 | ns | 1 |
| 8 | TwIL | Int. Request Input Low Time | 4.5V | 70 | | 70 | | ns | 1,2 |
| | | | 5.5V | 70 | | 70 | | ns | 1,2 |
| 9 | TwIH | Int. Request Input High Time | 4.5V | 2.5TpC | | 2.5TpC | | | 1 |
| | | | 5.5V | 2.5TpC | | 2.5TpC | | | 1,2 |
| 10 | Twdt | Watch-Dog Timer Delay Time for Timeout | 4.5V | 5 | | 5 | | ms | 1 |
| | | | 5.5V | 5 | | 5 | | ms | 1 |

**Notes:**

1. Timing Reference uses 0.7 $V_{CC}$ for a logic 1 and 0.2 $V_{CC}$ for a logic 0.
2. Interrupt request through Port 3 (P33-P31).

# LOW NOISE VERSION

## Low EMI Emission

The Z86E02 can be programmed to operate in a Low EMI emission mode by means of a mask ROM bit option. Use of this feature results in:

- All pre-driver slew rates reduced to 10 ns typical.
- Internal SCLK/TCLK operation limited to a maximum of 4 MHz - 250 ns cycle time.
- Output drivers have resistances of 200 ohms (typical).
- Oscillator divide-by-two circuitry eliminated.

The Low EMI mode is mask-programmable to be selected by the customer at the time the ROM code is submitted.



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