MUSIC SEMICONDUCTORS

Preliminary Data Sheet

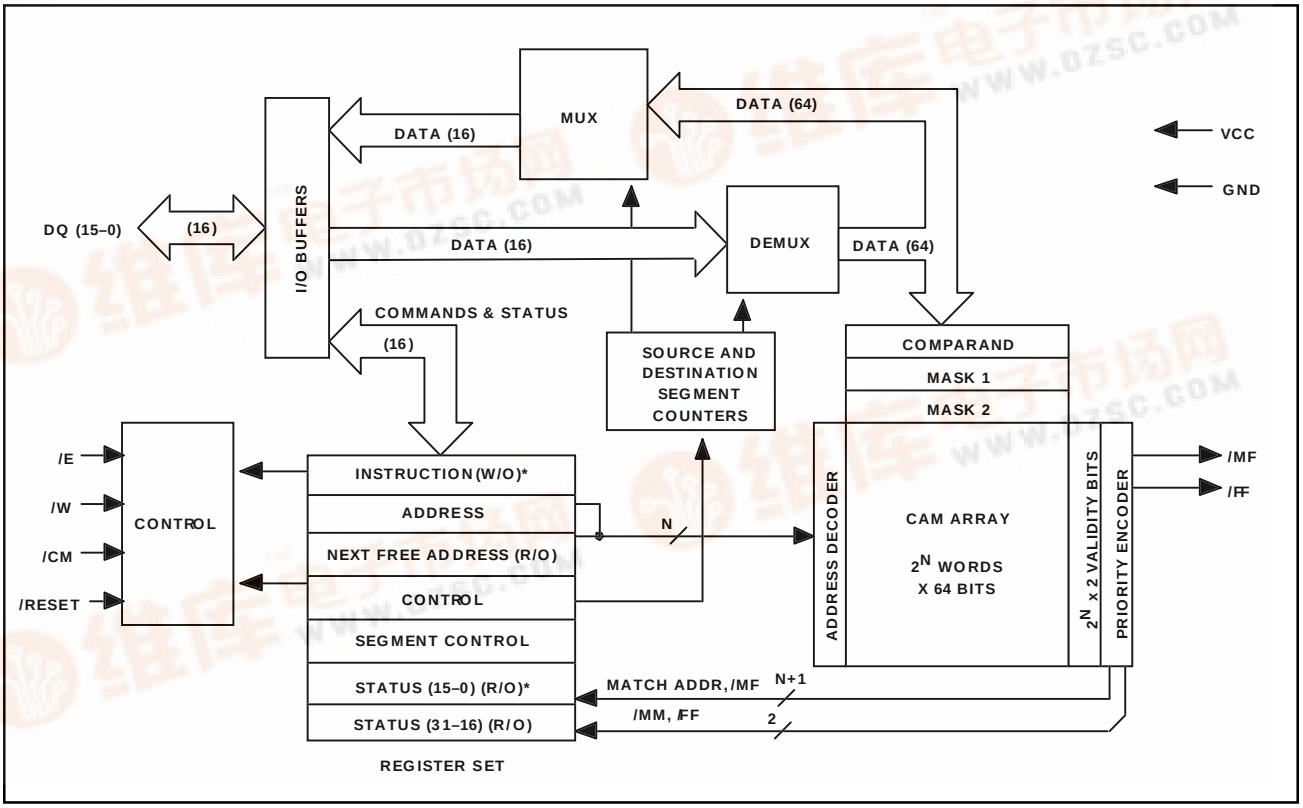
LANCAM® 1ST Family

FEATURES AND BENEFITS

- Full compatibility among all LANCAM 1ST devices, allowing CAM density variations within any application
- Full CAM technology for simplicity and speed: one single cycle to find, learn, or delete an entry
- 3.3 volt operation for low power dissipation
- Powerful LANCAM instruction set for application flexibility
- Partionable CAM/RAM array for associated data storage
- Low cost per entry for cost sensitive applications

DISTINCTIVE CHARACTERISTICS

- High density content-addressable memory (CAM) family
- 2K (2481L), 4K (4481L), and 8K (8481L) words
- 64-bit per word memory organization
- Fast 100 ns compare speed
- MUSIC's patented CAM/RAM partitioning
- Powerful LANCAM instruction set
- 16-bit I/O
- 3.3 volt operation
- 44 pin PLCC



Block Diagram

LANCAM 1ST Family

GENERAL DESCRIPTION

The LANCAM 1ST family consists of high density content-addressable memories (CAMs) in a variety of depths. Like the other LANCAM series from MUSIC Semiconductors, the LANCAM 1ST is ideal for time critical applications requiring intensive list processing.

Content-addressable memories, also known as associative memories, operate in the converse way to random access memories (RAM). In RAM, the input to the device is an address and the output is the data stored at that address. In CAM, the input is a data sample and the output is a flag to indicate a match and the address of the matching data. As a result, CAM searches large databases for matching data in a short, constant time period, no matter how many entries are in the database. The ability to search data words up to 64 bits wide allows large address spaces to be searched rapidly and efficiently. A patented architecture links each CAM entry to associated data and makes this data available for use after a successful compare operation.

The MUSIC LANCAM 1ST is ideal for address filtering and translation applications in LAN switches and routers. The LANCAM 1ST is also well suited to encryption, data caches, and branch tables.

OPERATIONAL OVERVIEW

To use the LANCAM 1ST, the user loads the data into the Comparand register, which is automatically compared to all valid CAM locations. The device then indicates whether or not one or more of the valid CAM locations contains data that match the target data. The status of each CAM location is determined by two validity bits at each memory location. The two bits are encoded to render four validity conditions: Valid, Skip, Empty, and Random Access, as shown in Table 1. The memory can be partitioned into CAM and associated RAM segments on 16-bit boundaries, but by using one of the two available mask registers, the CAM/RAM partitioning can be set at any arbitrary size between zero and 64 bits.

The LANCAM 1ST's internal data path is 64 bits wide for rapid internal comparison and data movement. Loading data to the Control, Comparand, and mask registers automatically triggers a compare. Compares may also be initiated by a command to the device. Associated RAM data is available immediately after a successful compare operation. The Status register reports the results of compares including all flags and addresses. Two Mask registers are available and can be used in two different ways: to mask comparisons or to mask data writes. The random access validity type allows additional masks to be stored in the CAM array where they may be retrieved rapidly.

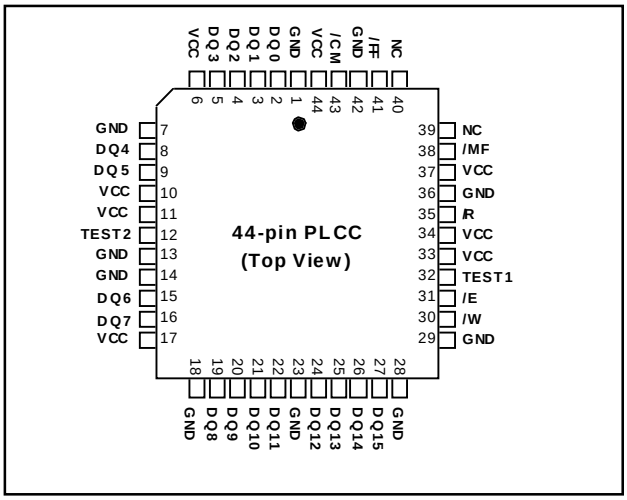
A simple three-wire control interface and commands loaded into the Instruction decoder control the device. A powerful instruction set increases the control flexibility and minimizes software overhead. These and other features make the LANCAM 1ST a powerful associative memory that drastically reduces search delays.

Skip Bit	Empty Bit	Entry Type
0	0	Valid
0	1	Empty
1	0	Skip
1	1	RAM

Table 1: Entry Types vs. Validity Bits

/W	/CM	Cycle Type
LOW	LOW	Command Write Cycle
LOW	HIGH	Data Write Cycle
HIGH	LOW	Command Read Cycle
HIGH	HIGH	Data Read Cycle

Table 2: I/O Cycles



Pinout Diagram

PIN DESCRIPTIONS

All signals are implemented in CMOS technology with TTL levels. Signal names that start with a slash ("/") are active LOW. Inputs should never be left floating. The CAM architecture draws large currents during compare operations, mandating the use of good layout and bypassing techniques. Refer to the Electrical Characteristics section for more information.

/E (Chip Enable, Input, TTL)

The /E input enables the device while LOW. The falling edge registers the control signals /W and /CM. The rising edge turns off the DQ pins and clocks the Destination and Source Segment counters. The four cycle types enabled by /E are shown in Table 2 on page 2.

/W (Write Enable, Input, TTL)

The /W input selects the direction of data flow during a device cycle. /W LOW selects a Write cycle and /W HIGH selects a Read cycle.

/CM (Data/Command Select, Input, TTL)

The /CM input selects whether the input signals on DQ15–0 are data or commands. /CM LOW selects Command cycles and /CM HIGH selects Data cycles.

DQ15–0 (Data Bus, I/O, TTL)

The DQ15–0 lines convey data, commands, and status to and from the LANCAM 1ST. /W and /CM control the direction and nature of the information that flows to or from the device. When /E is HIGH, DQ15–0 go to Hi-Z.

/MF (Match Flag, Output, TTL)

The /MF output goes LOW when one or more valid matches occur during a compare cycle. /MF is HIGH if there is no match. /MF will be reset when the active configuration register set is changed.

/FF (Full Flag, Output, TTL)

The /FF output goes LOW when no empty memory locations exist within the device.

/RESET (Reset, Input, TTL)

/RESET must be driven LOW to place the device in a known state before operation, which will reset the device to the conditions shown in Table 4 on page 8. The /RESET pin should be driven by TTL levels, not directly by an RC time-out. /E must be kept HIGH during /RESET.

TEST1, TEST2 (Test, Input, TTL)

These pins enable MUSIC production test modes that are not usable in an application. They should be connected to ground, either directly or through a pull-down resistor, or they may be left unconnected. These pins may not be implemented on all versions of these products.

VCC, GND (Positive Power Supply, Ground)

These pins are the power supply connections to the LANCAM 1ST. VCC must meet the voltage supply requirements in the Operating Conditions section relative to the GND pins, which are at 0 Volts (system reference potential), for correct operation of the device. All the ground and power pins must be connected to their respective planes with adequate bulk and high frequency bypassing capacitors in close proximity to the device.

FUNCTIONAL DESCRIPTION

The LANCAM 1ST is a content-addressable memory (CAM) with 16-bit I/O for network address filtering and translation, virtual memory, data compression, caching, and table lookup applications. The memory consists of static CAM, organized in 64-bit data fields. Each data field can be partitioned into a CAM and a RAM subfield on 16-bit boundaries. The contents of the memory can be randomly accessed or associatively accessed by the use of a compare. During automatic comparison cycles, data in the Comparand register is automatically compared with the "Valid" entries in the memory array. The Device ID can be read using a TCO PS instruction (see Table 11 on page 16).

The data inputs and outputs of the LANCAM 1ST are multiplexed for data and instructions over a 16-bit I/O bus. Internally, data is handled on a 64-bit basis, since the Comparand register, the mask registers, and each memory entry are 64 bits wide. Memory entries are globally configurable into CAM and RAM segments on 16-bit boundaries, as described in US Patent 5,383,146 assigned to MUSIC Semiconductors. Seven different CAM/RAM splits are possible, with the CAM width going from one to four segments, and the remaining RAM width going from three to zero segments. Finer resolution on compare width is possible by invoking a mask register during a compare, which does global masking on a bit basis. The CAM subfield contains the associative data, which enters into compares, while the RAM subfield contains the associated data, which is not compared. In LAN bridges, the RAM subfield could hold, for example, port-address and aging information related to the destination or source address information held in the CAM subfield of a given location. In a translation application, the CAM field could hold the dictionary entries, while the RAM field holds the translations, with almost instantaneous response.

Each entry has two validity bits (known as Skip bit and Empty bit) associated with it to define its particular type: empty, valid, skip, or RAM. When data is written to the active Comparand register, and the active Segment Control register reaches its terminal count, the contents of the Comparand register are automatically compared with the CAM portion of all the valid entries in the memory array. For added versatility, the Comparand register can be barrel-shifted right or left one bit at a time. A Compare instruction can then be used to force another compare between the Comparand register and the CAM portion of memory entries of any one of the four validity types. After a Read or Move from Memory operation, the validity bits of the location read or moved will be copied into the Status register, where they can be read using Command Read cycles.

Data can be moved from one of the data registers (CR, MR1, or MR2) to a memory location that is based on the results of the last comparison (Highest-Priority Match or Next Free), or to an absolute address, or to the location pointed to by the active Address register. Data can also be written directly to the memory from the DQ bus using any of the above addressing modes. The Address register may be directly loaded and may be set to increment or decrement, allowing DMA-type reading or writing from memory.

Two sets of configuration registers (Control, Segment Control, Address, Mask Register 1, and Persistent Source and Destination) are provided to permit rapid context switching between foreground and background activities. The currently active set of configuration registers control writes, reads, moves, and compares. The foreground set would typically be pre-loaded with values useful for comparing input data, often called filtering, while the background set would be pre-loaded with values useful for housekeeping activities such as purging old entries. Moving from the foreground task of filtering to the background task of purging can be done by issuing a single instruction to change the current set of configuration registers. The match condition of the device is reset whenever the active register set is changed.

The active Control register determines the operating conditions within the device. Conditions set by this register's contents are reset, CAM/RAM partitioning, disable or select masking conditions, and disable or select auto-incrementing or -decrementing the Address register. The active Segment Control register contains separate counters to control the writing of 16-bit data segments to the selected persistent destination, and to control the reading of 16-bit data segments from the selected persistent source.

There are two active mask registers at any one time, which can be selected to mask comparisons or data writes. Mask Register 1 has both a foreground and background mode to support rapid context switching. Mask Register 2 does not have this mode, but can be shifted left or right one bit at a time. For masking comparisons, data stored in the active selected mask register determines which bits of the comparand are

FUNCTIONAL DESCRIPTION *Continued*

compared against the valid contents of the memory. If a bit is set HIGH in the mask register, the same bit position in the Comparand register becomes a "don't care" for the purpose of the comparison with all the memory locations. During a Data Write cycle or a MOV instruction, data in the specified active mask register can also determine which bits in the destination will be updated. If a bit is HIGH in the mask register, the corresponding bit of the destination is unchanged.

The match line associated with each memory address is fed into a priority encoder where multiple responses are resolved, and the address of the highest-priority responder (the lowest numerical match address) is generated. In LAN applications, a multiple response might indicate an error. In other applications the existence of multiple responders may be valid.

Three input control signals and commands loaded into an instruction decoder control the LANCAM 1ST. Two of the three input control signals determine the cycle type. The control signals tell the device whether the data on the I/O bus represents data or a command, and is input or output. Commands are decoded by instruction logic and control moves, forced compares, validity bit manipulations, and the data path within the device. Registers (Control, Segment Control, Address, Next Free Address, etc.) are accessed using Temporary Command Override instructions. The data path from the DQ bus to/from data resources (comparand, masks, and memory) within the device are set until changed by Select Persistent Source and Destination instructions.

After a Compare cycle (caused by either a data write to the Comparand or mask registers, a write to the Control register, or a forced compare), the status register contains the address of the Highest-Priority Matching location, along with flags indicating match, multiple match, and full. The /MF and /FF flags are also available directly on output pins.

OPERATIONAL CHARACTERISTICS

Throughout the following, "aaaH" represents a three-digit hexadecimal number "aaa," while "bbB" represents a two-digit binary number "bb." All memory locations are written to or read from in 16-bit segments. Segment 0 corresponds to the lowest order bits (bits 15–0) and Segment 3 corresponds to the highest order bits (bits 63–48).

THE CONTROL BUS

Refer to the Block Diagram on page 1 for the following discussion. The inputs Chip Enable (/E), Write Enable (/W), and Command Enable (/CM) are the primary control mechanism for the LANCAM 1ST. Instructions are the secondary control mechanism. Logical combinations of the Control Bus inputs, coupled with the execution of Select Persistent Source (SPS), Select Persistent Destination (SPD), and Temporary Command Override (TCO) instructions allow the I/O operations to and from the DQ15–0 lines to the internal resources, as shown in Table 3 on page 7.

The Comparand register is the default source and destination for Data Read and Write cycles. This default state can be overridden independently by executing a Select Persistent Source or Select Persistent Destination instruction, selecting a different source or destination for data. Subsequent Data Read or Data Write cycles will access that source or destination until another SPS or SPD instruction is executed. The currently selected persistent source or destination can be read back through a TCO PS or PD instruction. The sources and destinations available for persistent access are those resources on the 64-bit bus: Comparand register, Mask Register 1, Mask Register 2, and the Memory array.

The default destination for Command Write cycles is the Instruction decoder, while the default source for Command Read cycles is the Status register.

Temporary Command Override (TCO) instructions provide access to the Control register, the Segment Control register, the Address register, and the Next Free Address register. TCO instructions are only active for one Command Read or Write cycle after being loaded into the Instruction decoder.

The data and control interfaces to the LANCAM 1ST are synchronous. During a Write cycle, the Control and Data inputs are registered by the falling edge of /E. When writing to the persistently selected data destination, the Destination Segment counter is clocked by the rising edge of /E. During a Read cycle, the Control inputs are registered by the falling edge of /E, and the Data outputs are enabled while /E is LOW. When reading from the persistently selected data source, the Source Segment counter is clocked by the rising edge of /E.

OPERATIONAL CHARACTERISTICS *Continued*

THE REGISTER SET

The Control, Segment Control, Address, Mask Register 1, and the Persistent Source and Destination registers are duplicated, with one set termed the Foreground set, and the other the Background set. The active set is chosen by issuing Select Foreground Registers or Select Background Registers instructions. By default, the Foreground set is active after a reset. Having two alternate sets of registers that determine the device configuration allows for a rapid return to a foreground network filtering task from a background housekeeping task.

Writing a value to the Control register or writing data to the last segment of the Comparand or either mask register will cause an automatic comparison to occur between the contents of the Comparand register and the words in the CAM segments of the memory marked valid, masked by MR1 or MR2 if selected in the Control register.

Instruction Decoder

The Instruction decoder is the write-only decode logic for instructions and is the default destination for Command Write cycles. If an instruction's Address Field flag (bit 11) is set to a 1, it is a two-cycle instruction that is not executed immediately. For the next cycle only, the data from a Command Write cycle is loaded into the Address register and the instruction then completes at that address. The Address register will then increment, decrement, or stay at the same value depending on the setting of Control Register bits CT3 and CT2. If the Address Field flag is not set, the memory access occurs at the address currently contained in the Address register.

Control Register (CT)

The Control register is composed of a number of switches that configure the LANCAM 1ST, as shown in Table 7 on page 15. It is written or read using a TCO CT instruction. If bit 15 of the value written during a TCO CT is a 0, the device is reset (and all other bits are ignored). See Table 4 for the Reset states. Bit 15 always reads back as a 0. A write to the Control register causes an automatic compare to occur (except in the case of a reset). Either the Foreground or Background Control register will be active, depending on which register set has been selected, and only the active Control register will be written to or read from.

Control Register bits 8–6 control the CAM/RAM partitioning. The CAM portion of each word may be sized from a full 64 bits down to 16 bits in 16-bit increments. The RAM portion can be at either end of the 64-bit word.

Compare masks may be selected by bits 5 and 4. Mask Register 1, Mask Register 2, or neither may be selected to mask compare operations. The address register behavior is controlled by bits 3 and 2, and may be set to increment, decrement, or neither after a memory access.

Segment Control Register (SC)

The Segment Control register, as shown in Table 8 on page 16, is accessed using a TCO SC instruction. On read cycles, D15, D10, D5, and D2 will always read back as 0s. Either the Foreground or Background Segment Control register will be active, depending on which register set has been selected, and only the active Segment Control register will be written to or read from.

The Segment Control register contains dual independent incrementing counters with limits, one for data reads and one for data writes. These counters control which 16-bit segment of the 64-bit internal resource is accessed during a particular data cycle on the 16-bit data bus. The actual destination for data writes and source for data reads (called the persistent destination and source) are set independently with SPD and SPS instructions, respectively.

Each of the two counters consists of a start limit, an end limit, and the current count value that points to the segment to be accessed on the next data cycle. The current count value can be set to any segment, even if it is outside the range set by the start and end limits. The counters count up from the current count value to the end limit and then jump back to the start limit. If the current count is greater than the end limit, the current count value will increment to 3, then roll over to 0 and continue incrementing until the end limit is reached; it then jumps back to the start limit.

If a sequence of data writes or reads is interrupted, the Segment Control register can be reset to its initial start limit values by using an RSC instruction. After the LANCAM 1ST is reset, both Source and Destination counters are set to count from Segment 0 to Segment 3 with an initial value of 0.

Address Register (AR)

The Address register points to the CAM memory location to be operated upon when M@[AR] or M@aaaH is part of the instruction. It can be loaded directly by using a TCO AR instruction or indirectly by using an instruction requiring an absolute address, such as MOV aaaH, CR,V. After being loaded, the Address register value will then be used for the next memory access referencing the Address register. A reset sets the Address register to zero.

OPERATIONAL CHARACTERISTICS *Continued*

Cycle Type	/E	/CM	/W	I/O Status	SPS	SPD	TCO	Operation	Notes
Cmd Write	L	L	L	IN				Load Instruction decoder	1
				IN			✓	Load Address register	2,3
				IN			✓	Load Control register	3
				IN			✓	Load Segment Control register	3
Cmd Read	L	L	H	OUT			✓	Read Next Free Address register	3
				OUT			✓	Read Address register	3
				OUT				Read Status Register bits 15–0	4
				OUT				Read Status Register bits 31–16	5
				OUT			✓	Read Control register	3
				OUT			✓	Read Segment Control register	3
				OUT			✓	Read Current Persistent Source or Destination	3,10
Data Write	L	H	L	IN		✓		Load Comparand register	6,9
				IN		✓		Load Mask Register 1	7,9
				IN		✓		Load Mask Register 2	7,9
				IN		✓		Write Memory Array at address	7,9
				IN		✓		Write Memory Array at Next Free address	7,9
				IN		✓		Write Memory Array at Highest-Priority match	7,9
Data Read	L	H	H	OUT	✓			Read Comparand register	6, 9
				OUT	✓			Read Mask Register 1	8, 9
				OUT	✓			Read Mask Register 2	8, 9
				OUT	✓			Read Memory Array at address	8, 9
				OUT	✓			Read Memory Array at Highest-Priority match	7, 8
	H	X	X	HIGH-Z				Deselected	

Notes:
1. Default Command Write cycle destination (does not require a TCO instruction).
2. Default Command Write cycle destination (no TCO instruction required) if Address Field flag was set in bit 11 of the instruction loaded in the previous cycle.
3. Loaded or read on the Command Write or Read cycle immediately following a TCO instruction. Active for one Command Write or Read cycle only. NFA register cannot be loaded this way.
4. Default Command Read cycle source (does not require a TCO instruction).
5. Default Command Read cycle source (does not require a TCO instruction) if the previous cycle was a Command Read of Status Register bits 15–0. If next cycle is not a Command Read cycle, any subsequent Command Read cycle will access the Status Register bits 15–0.
6. Default persistent source and destination on power-up and after Reset. If other resources were sources or destinations, SPD CR or SPS CR restores the Comparand register as the destination or source.
7. Selected by executing a Select Persistent Destination instruction.
8. Selected by executing a Select Persistent Source instruction.
9. Access may require multiple 16-bit Read or Write cycles. The Segment Control register is used to control the selection of the desired 16-bit segment(s) by establishing the Segment counters' start and end limits and count values.
10. A Command Read cycle after a TCO PS or TCO PD reads back the Instruction decoder bits that were last set to select a persistant source or destination. The TCO PS instruction will also read back the Device ID.

Table 3: Input/Output Operations

Control Register bits CT3 and CT2 set the Address register to automatically increment or decrement (or not change) during sequences of Command or Data cycles. The Address register will change after executing an instruction that includes M@[AR] or M@aaaH, or after a data access to the end limit segment (as set in the Segment Control register) when the persistent source or destination is M@[AR] or M@aaaH.

Either the Foreground or Background Address register will be active, depending on which register set has been selected, and only the active Address register will be written to or read from.

Next Free Address Register (NF)

The LANCAM 1ST automatically stores the address of the first empty memory location in the Next Free Address register, which is then used as a memory address pointer for M@NF operations. The Next Free Address register, shown in Table 9 on page 16, can be read using a TCO NF instruction. After a reset, the Next Free Address register is set to zero.

OPERATIONAL CHARACTERISTICS *Continued*

CAM Status	After /RESET Is Asserted or Software Reset
Validity bits at all memory locations	Skip = 0, Empty = 1 (empty)
CAM/RAM Partitioning	64 bits CAM, 0 bits RAM
Comparison Masking	Disabled
Address register auto-increment or -decrement	Disabled
Source and Destination Segment counters count ranges	00B to 11B; loaded with 00B
Address register and Next Free Address register	Contains all 0s
Control register after reset (including CT15)	Contains 0008H
Persistent Destination for Command writes	Instruction decoder
Persistent Source for Command reads	Status register
Persistent Source and Destination for Data reads and writes	Comparand register
Configuration Register set	Foreground

Table 4: Device Control State after Reset

Status Register

The 32-bit Status register, as shown in Table 10 on page 16, is the default source for Command Read cycles. Bit 31 is the internal Full flag, which will go LOW if there are no empty memory locations. Bit 30 is the internal Multiple Match flag, which will go LOW if a Multiple match was detected. Bits 29 and 28 are the Skip and Empty Validity bits, which reflect the validity of the last memory location read. After a reset, the Skip and Empty bits will read 11 until a read or move from memory has occurred. The rest of the Status register down to bit 1 contains the address of the Highest-Priority match. After a reset or a no-match condition, the match address bits will be all 1s. Bit 0 is the internal Match flag, which will go LOW if a match was found.

Comparand Register (CR)

The 64-bit Comparand register is the default destination for data writes and reads, using the Segment Control register to select which 16-bit segment of the Comparand register is to be loaded or read out. The persistent source and destination for data writes and reads can be changed to the mask registers or memory by SPS and SPD instructions. During an automatic or forced compare, the Comparand register is simultaneously compared against the CAM portion of all memory locations with the correct validity condition. Automatic compares always compare against valid memory locations, while forced compares, using CMP instructions, can compare against memory locations tagged with any specific validity condition.

The Comparand register may be shifted one bit at a time to the right or left by issuing a Shift Right or Shift Left instruction, with the right and left limits for the wrap-around determined by the CAM/RAM partitioning set in the Control register. During shift rights, bits shifted off the LSB of the CAM partition will reappear at the MSB of the CAM partition. Likewise, bits shifted off the MSB of the CAM partition will reappear at the LSB during shift lefts.

Mask Registers (MR1, MR2)

The Mask registers can be used in two different ways, either to mask compares or to mask data writes and moves. Either mask register can be selected in the Control register to mask every compare, or selected by instructions to participate in data writes or moves to and from memory. If a bit in the selected mask register is set to a 0, the corresponding bit in the Comparand register will enter into a masked compare operation. If a Mask bit is a 1, the corresponding bit in the Comparand register will not enter into a masked compare operation. Bits set to 0 in the mask register cause corresponding bits in the destination register or memory location to be updated when masking data writes or moves, while a bit set to 1 will prevent that bit in the destination from being changed.

Either the Foreground or Background MR1 can be set active, but after a reset, the Foreground MR1 is active by default. MR2 incorporates a sliding mask, where the data can be replicated one bit at a time to the right or left with no wrap-around by issuing a Shift Right or Shift Left instruction. The right and left limits are determined by the CAM/RAM partitioning set in the Control register. For a Shift Right the upper limit bit is replicated to the next lower bit, while for a Shift Left the lower limit bit is replicated to the next higher bit.

THE MEMORY ARRAY

Memory Organization

The Memory array is organized into 64-bit words with each word having an additional two validity bits (Skip and Empty). By default, all words are configured to be 64 CAM cells. However, bits 8–6 of the Control register can divide each word into a CAM field and a RAM field. The RAM field can be assigned to the least-significant or

most-significant portion of each entry. The CAM/RAM partitioning is allowed on 16-bit boundaries, permitting selection of the configuration shown in Table 7 on page 15, bits 8–6 (e.g., 001 sets the 48 MSBs to CAM and the 16 LSBs to RAM). Memory Array bits designated as RAM can be used to store and retrieve data associated with the CAM content at the same memory location.

Memory Access

There are two general ways to get data into and out of the memory array: directly or by moving the data via the Comparand or mask registers.

The first way, through direct reads or writes, is set up by issuing a Set Persistent Destination (SPD) or Set Persistent Source (SPS) command. The addresses for the direct access can be directly supplied; supplied from the Address register, supplied from the Next Free Address register, or supplied as the Highest-Priority Match address. Additionally, all the direct writes can be masked by either mask register.

The second way is to move data via the Comparand or mask registers. This is accomplished by issuing Data Move commands (MOV). Moves using the Comparand register can also be masked by either of the mask registers.

I/O CYCLES

The LANCAM 1ST supports four basic I/O cycles: Data Read, Data Write, Command Read, and Command Write. The type of cycle is determined by the states of the /W and /CM control inputs. These signals are registered at the beginning of a cycle by the falling edge of /E. Table 2 on page 2 shows how the /W and /CM lines select the cycle type.

During Read cycles, the DQ15–0 outputs are enabled after /E goes LOW. During Write cycles, the data or command to be written is captured from DQ15–0 at the beginning of the cycle by the falling edge of /E. Figures 1 and 2 show Read and Write cycles respectively. Figure 3 shows typical cycle-to-cycle timing with the Match flag valid at the end of the Comparand Write cycle. Data writes and reads to the comparand, mask registers, or memory occur in one to four 16-bit cycles, depending on the settings in the Segment Control register. The Compare operation automatically occurs during Data writes to the Comparand or mask registers when the destination segment counter reaches the end count set in the Segment Control register. If there was a match, the second cycle reads status or associated data, depending on the state of /CM.

The minimum timings for the /E control signal are given in the Switching Characteristics section on page 18. Note that at minimum timings the /E signal is non-symmetrical, and that different cycle types have different timing requirements, as given in Table 6 on page 15.

COMPARE OPERATIONS

During a Compare operation, the data in the Comparand register is compared to all locations in the Memory array simultaneously. Any mask register used during compares must be selected beforehand in the Control register. There are two ways compares are initiated: Automatic and Forced compares.

Automatic compares perform a compare of the contents of the Comparand register against Memory locations that are tagged as "Valid," and occur whenever the following happens:

- The Destination Segment counter in the Segment Control register reaches its end limit during writes to the Comparand or mask registers.
- After a command write of a TCO CT is executed (except for a software reset), so that a compare is executed with the new settings of the Control register.

Forced compares are initiated by CMP instructions using one of the four validity conditions, V, R, S, and E. The forced compare against "Empty" locations automatically masks all 64 bits of data to find all locations with the validity bits set to "Empty," while the other forced compares are only masked as selected in the Control register.

INITIALIZING THE LANCAM 1ST

Initialization of the LANCAM 1ST is required to configure the various registers on the device. Since a Control register reset establishes the operating conditions shown in Table 4 on page 8, restoration of operating conditions better suited for the application may be required after a reset, whether using the Control Register reset or the /RESET pin. When the device powers up, the memory and registers are in an unknown state, so the /RESET pin must be asserted to place the device in a known state.

OPERATIONAL CHARACTERISTICS *Continued*

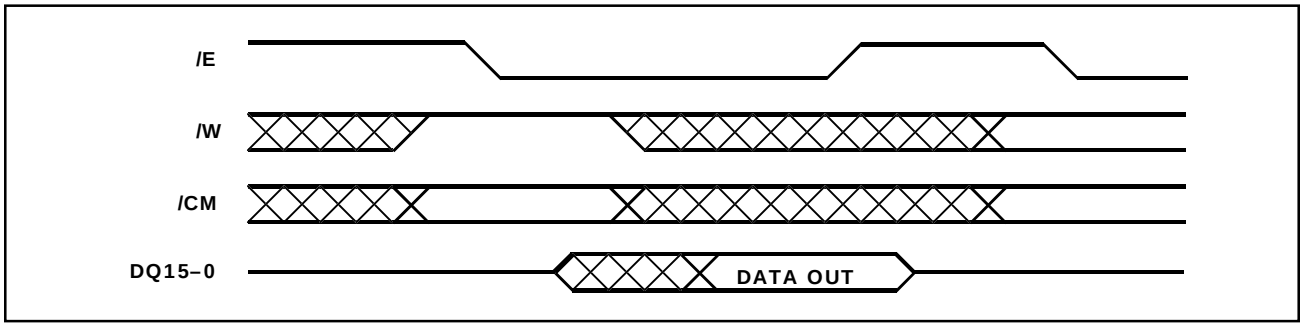


Figure 1: Read Cycle

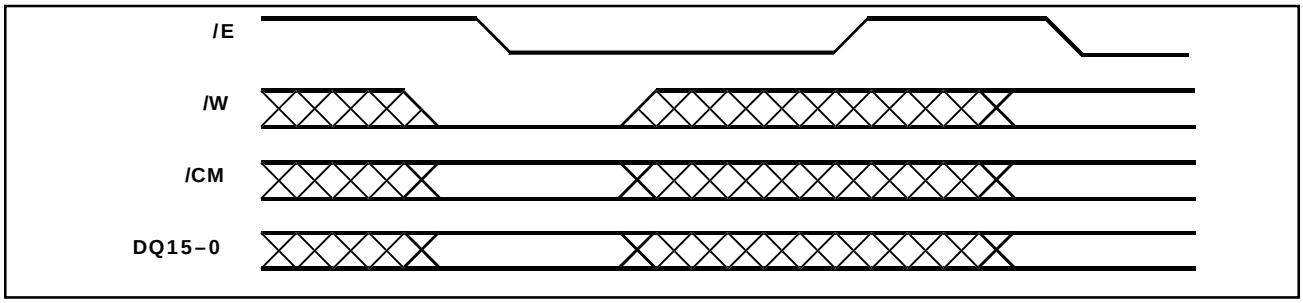


Figure 2: Write Cycle

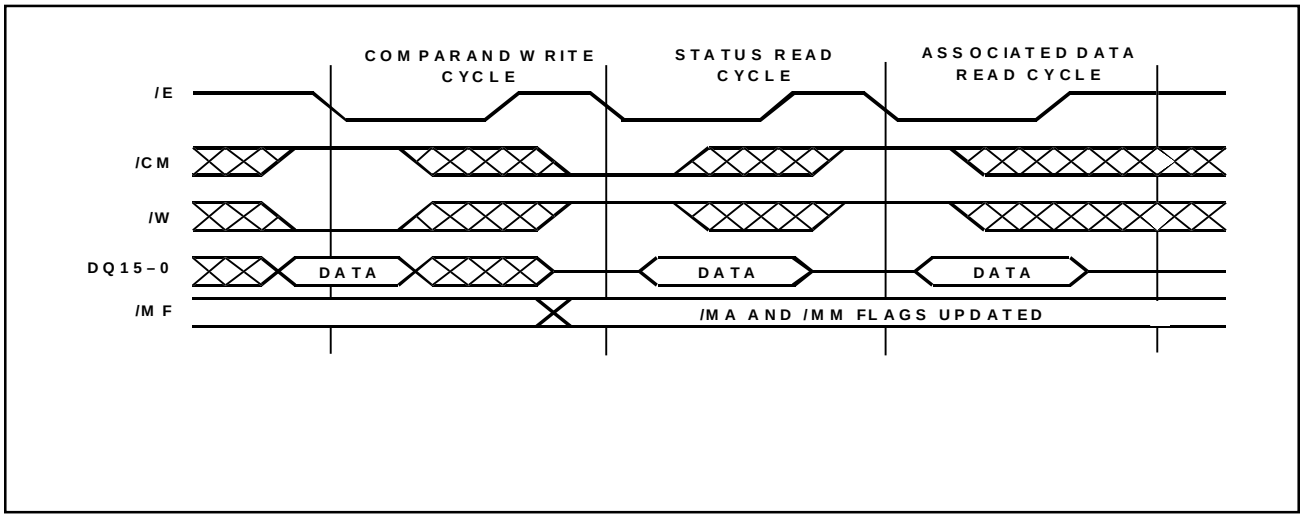


Figure 3: Cycle to Cycle Timing Example

OPERATIONAL CHARACTERISTICS *Continued*

Cycle Type	Opcode on DQ Bus	Control Bus /E	/CM	/W	Comments	Notes
Command read		L	L	H	Clears power-up anomalies	
Command write	TCO CT	L	L	L	Target Control register for reset	
Command write	0000H	L	L	L	Causes reset	1
Command write	TCO CT	L	L	L	Target Control register for initial values	
Command write	8040H	L	L	L	Control Register value	2
Command write	TCO SC	L	L	L	Target Segment Counter Control register	
Command write	3808H	L	L	L	Set Segment counters to write to Segment 1, 2, and 3, and read from Segment 0.	
Command write	SPS M@HM	L	L	L	Set Data Reads from Segment 0 of the Highest-priority match	

Notes:

1. A software reset using a TCO CT followed by 0000H puts the device in a known state. Good programming practice dictates a software reset for initialization to account for all possible conditions.
2. A typical LANCAM 1ST control environment: 48 CAM bits, 16 RAM bits; Disable comparison masking; and Enable address increment. See Table 7 on page 15 for Control Register Bit assignments.

Table 5: Example Initialization Routine

INSTRUCTION SET DESCRIPTIONS*

Instruction: Select Persistent Source (SPS)
Binary Op-Code: 0000 f000 0000 0sss

f **Address Field flag†**
sss **Selected source**

This instruction selects a persistent source for data reads, until another SPS instruction changes it or a reset occurs. The default source after reset for Data Read cycles is the Comparand register. Setting the persistent source to M@aaaH loads the Address register with "aaaH" and the first access to that persistent source will be at aaaH, after which the AR value increments or decrements as set in the Control register. The SPS M@[AR] instruction does the same except the current Address Register value is used.

Instruction: Select Persistent Destination (SPD)
Binary Op-Code: 0000 f001 mmdd dvvv

f **Address Field flag†**
mm **Mask Register select**
ddd **Selected destination**
vvv **Validity setting for Memory Location destinations**

This instruction selects a persistent destination for data writes, which remains until another SPD instruction changes it or a reset occurs. The default destination for Data Write cycles is the Comparand register after a reset. When the destination is the Comparand register or the memory array, the data written may be masked by either Mask Register 1 or Mask Register 2, so that only destination bits corresponding to bits in the mask register set to 0 will be modified. An automatic compare will occur after writing the last segment of the Comparand or mask registers, but not after writing to memory. Setting the persistent destination to M@aaaH loads the Address register with aaaH, and the first access to that persistent destination will be at aaaH, after which the AR value increments or decrements as set in the Control register. The SPD M@[AR] instruction does the same except the current Address Register value is used.

Instruction: Temporary Command Override (TCO)
Binary Op-Code: 0000 0010 00dd d000

ddd **Register selected as source or destination for only the next Command Read or Write cycle**

The TCO instruction selects a register as the source or destination for only the next Command Read or Write cycle, so a value can be loaded or read out of the register. Subsequent Command Read or Write Cycles revert to reading the Status register and writing to the Instruction decoder. All registers but the NF, PS, and PD can be written to, and all can be read from. The Status register is only available via non-TCO Command Read cycles. Reading the PS register also outputs the Device ID on bits 15–4 as shown in Table 11 on page 16.

INSTRUCTION SET DESCRIPTIONS* *Continued*

Instruction: Data Move (MOV)
Binary Op-Code: 0000 f011 mmdd dsss or
0000 f011 mmdd dvss

f	**Address Field flag†**
mm	**Mask Register select**
ddd	**Destination of data**
sss	**Source of data**
v	**Validity setting if destination is a Memory location**

The MOV instruction performs a 64-bit move of the data in the selected source to the selected destination. If the source or destination is aaaH, the Address register is set to aaaH. For MOV instructions to or from aaaH or [AR], the Address register will increment or decrement from that value after the move completes, as set in the Control register. Data transfers between the Memory array and the Comparand register may be masked by either Mask Register 1 or Mask Register 2, in which case, only those bits in the destination which correspond to bits in the selected mask register set to 0 will be changed. A Memory location used as a destination for a MOV instruction may be set to Valid or left unchanged. If the source and destination are the same register, no net change occurs (a NOP).

Instruction: Validity Bit Control (VBC)
Binary Op-Code: 0000 f100 00dd dvvv

f	**Address Field flag†**
ddd	**Destination of data**
vvv	**Validity setting for Memory location**

The VBC instruction sets the Validity bits at the selected memory locations to the selected state. This feature can be used to find all valid entries by using a repetitive sequence of CMP V through a mask of all 1s followed by a VBC HM, S. If the VBC target is aaaH, the Address register is set to aaaH. For VBC instructions to or from aaaH or [AR], the Address register will increment or decrement from that value after the operation completes, as set in the Control register.

Instruction: Compare (CMP)
Binary Op-Code: 0000 0101 0000 0vvv

vvv	**Validity condition**

A CMP V, S, or R instruction forces a Comparison of Valid, Skipped, or Random entries against the Comparand register through a mask register, if one is selected. During a CMP E instruction, the compare is only done on the Validity bits and all data bits are automatically masked.

Instruction: Special Instructions
Binary Op-Code: 0000 0110 00dd drrr

ddd	**Target resource**
rrr	**Operation**

Two alternate sets of configuration registers can be selected by using the Select Foreground and Select Background Registers instructions. These registers are the Control, Segment Control, Address, Mask Register 1, and the PS and PD registers. An RSC instruction resets the Segment Control register count values for both the Destination and Source counters to the original Start limits. The Shift instructions shift the designated register one bit right or left. The right and left limits for shifting are determined by the CAM/RAM partitioning set in the Control register. The Comparand register is a barrel-shifter, and for the example of a device set to 64 bits of CAM executing a Shift Comparand Right instruction, bit 0 is moved to bit 63, bit 1 is moved to bit 0, and bit 63 is moved to bit 62. For a Shift Comparand Left instruction, bit 63 is moved to bit 0, bit 0 is moved to bit 1, and bit 62 is moved to bit 63. MR2 acts as a sliding mask, where for a Shift Right instruction bit 1 is moved to bit 0, while bit 0 "falls off the end," and bit 63 is replicated to bit 62. For a Shift Mask Left instruction, bit 0 is replicated to bit 1, bit 62 is moved to bit 63, and bit 63 "falls off the end." With shorter width CAM fields, the bit limits on the right or left move to match the width of CAM field.

Notes:

* Instruction cycle lengths given in Table 6 on page 15.
† If f =1, the instruction requires an absolute address to be supplied on the following cycle as a Command write. The value supplied on the second cycle will update the address register. After operations involving M@[AR] or M@aaaH, the Address register will be incremented or decremented depending on the setting in the Control register.

INSTRUCTION SET SUMMARY

MNEMONIC FORMAT
INS dst,src[msk],val

INS: Instruction mnemonic
dst: Destination of the data
src: Source of the data
msk: Mask register used
val: Validity condition set at the location written

Instruction: Select Persistent Source

Operation	Mnemonic	Op-Code
Comparand Register	SPS CR	0000H
Mask Register 1	SPS MR1	0001H
Mask Register 2	SPS MR2	0002H
Memory Array at Addr. Reg.	SPS M@[AR]	0004H
Memory Array at Address	SPS M@aaaH	0804H
Mem. at Highest-Prio. Match	SPS M@HM	0005H

Instruction: Select Persistent Destination

Operation	Mnemonic	Op-Code
Comparand Register	SPD CR	0100H
Masked by MR1	SPD CR[MR1]	0140H
Masked by MR2	SPD CR[MR2]	0180H
Mask Register 1	SPD MR1	0108H
Mask Register 2	SPD MR2	0110H
Mem. at Addr. Reg. set Valid	SPD M@[AR],V	0124H
Masked by MR1	SPD M@[AR][MR1],V	0164H
Masked by MR2	SPD M@[AR][MR2],V	01A4H
Mem. at Addr. Reg. set Empty	SPD M@[AR],E	0125H
Masked by MR1	SPD M@[AR][MR1],E	0165H
Masked by MR2	SPD M@[AR][MR2],E	01A5H
Mem. at Addr. Reg. set Skip	SPD M@[AR],S	0126H
Masked by MR1	SPD M@[AR][MR1],S	0166H
Masked by MR2	SPD M@[AR][MR2],S	01A6H
Mem. at Addr. Reg. set Random	SPD M@[AR],R	0127H
Masked by MR1	SPD M@[AR][MR1],R	0167H
Masked by MR2	SPD M@[AR][MR2],R	01A7H
Memory at Address set Valid	SPD M@aaaH,V	0924H
Masked by MR1	SPD M@aaaH[MR1],V	0964H
Masked by MR2	SPD M@aaaH[MR2],V	09A4H
Memory at Addr. set Empty	SPD M@aaaH,E	0925H
Masked by MR1	SPD M@aaaH[MR1],E	0965H
Masked by MR2	SPD M@aaaH[MR2],E	09A5H
Memory at Address set Skip	SPD M@aaaH,S	0926H
Masked by MR1	SPD M@aaaH[MR1],S	0966H
Masked by MR2	SPD M@aaaH[MR2],S	09A6H
Mem. at Address set Random	SPD M@aaaH,R	0927H
Masked by MR1	SPD M@aaaH[MR1],R	0967H
Masked by MR2	SPD M@aaaH[MR2],R	09A7H
Mem. at Highest-Prio. Match, Valid	SPD M@HM,V	012CH
Masked by MR1	SPD M@HM[MR1],V	016CH
Masked by MR2	SPD M@HM[MR2],V	01ACH

Instruction: Select Persistent Destination *Cont.*

Operation	Mnemonic	Op-Code
Mem. at Highest-Prio. Match, Emp.	SPD M@HM,E	012DH
Masked by MR1	SPD M@HM[MR1],E	016DH
Masked by MR2	SPD M@HM[MR2],E	01ADH
Mem. at Highest-Prio. Match, Skip	SPD M@HM,S	012EH
Masked by MR1	SPD M@HM[MR1],S	016EH
Masked by MR2	SPD M@HM[MR2],S	01AEH
Mem. at High.-Prio. Match, Random	SPD M@HM,R	012FH
Masked by MR1	SPD M@HM[MR1],R	016FH
Masked by MR2	SPD M@HM[MR2],R	01AFH
Mem. at Next Free Addr., Valid	SPD M@NF,V	0134H
Masked by MR1	SPD M@NF[MR1],V	0174H
Masked by MR2	SPD M@NF[MR2],V	01B4H
Mem. at Next Free Addr., Empty	SPD M@NF,E	0135H
Masked by MR1	SPD M@NF[MR1],E	0175H
Masked by MR2	SPD M@NF[MR2],E	01B5H
Mem. at Next Free Addr., Skip	SPD M@NF,S	0136H
Masked by MR1	SPD M@NF[MR1],S	0176H
Masked by MR2	SPD M@NF[MR2],S	01B6H
Mem. at Next Free Addr., Random	SPD M@NF,R	0137H
Masked by MR1	SPD M@NF[MR1],R	0177H
Masked by MR2	SPD M@NF[MR2],R	01B7H

Instruction: Temporary Command Override

Operation	Mnemonic	Op-Code
Control Register	TCO CT	0200H
Segment Control Register	TCO SC	0210H
Read Next Free Address	TCO NF	0218H
Address Register	TCO AR	0220H
Read Persistent Source	TCO PS	0230H
Read Persistent Destination	TCO PD	0238H

Instruction: Data Move

Operation	Mnemonic	Op-Code
Comparand Register from:		
No Operation	NOP	0300H
Mask Register 1	MOV CR,MR1	0301H
Mask Register 2	MOV CR,MR2	0302H
Memory at Address Reg.	MOV CR,[AR]	0304H
Masked by MR1	MOV CR,[AR][MR1]	0344H
Masked by MR2	MOV CR,[AR][MR2]	0384H
Memory at Address	MOV CR,aaaH	0B04H
Masked by MR1	MOV CR,aaaH[MR1]	0B44H
Masked by MR2	MOV CR,aaaH[MR2]	0B84H
Mem. at Highest-Prio. Match	MOV CR,HM	0305H
Masked by MR1	MOV CR,HM[MR1]	0345H
Masked by MR2	MOV CR,HM[MR2]	0385H

INSTRUCTION SET SUMMARY *Continued*

Instruction: Data Move *Cont.*

Operation	Mnemonic	OpCode
Mask Register 1 from:		
Comparand Register	MOV MR1,CR	0308H
No Operation	NOP	0309H
Mask Register 2	MOV MR1,MR2	030AH
Memory at Address Reg.	MOV MR1,[AR]	030CH
Memory at Address	MOV MR1,aaaH	0B0CH
Mem. at Highest-Prio. Match	MOV MR1,HM	030DH
Mask Register 2 from:		
Comparand Register	MOV MR2,CR	0310H
Mask Register 1	MOV MR2,MR1	0311H
No Operation	NOP	0312H
Memory at Address Reg.	MOV MR2,[AR]	0314H
Memory at Address	MOV MR2,aaaH	0B14H
Mem. at Highest-Prio. Match	MOV MR2,HM	0315H
Memory at Address Register, No Change to Validity bits, from:		
Comparand Register	MOV [AR],CR	0320H
Masked by MR1	MOV [AR],CR[MR1]	0360H
Masked by MR2	MOV [AR],CR[MR2]	03A0H
Mask Register 1	MOV [AR],MR1	0321H
Mask Register 2	MOV [AR],MR2	0322H
Memory at Address Register, Location set Valid, from:		
Comparand Register	MOV [AR],CR,V	0324H
Masked by MR1	MOV [AR],CR[MR1],V	0364H
Masked by MR2	MOV [AR],CR[MR2],V	03A4H
Mask Register 1	MOV [AR],MR1,V	0325H
Mask Register 2	MOV [AR],MR2,V	0326H
Memory at Address, No Change to Validity bits, from:		
Comparand Register	MOV aaaH,CR	0B20H
Masked by MR1	MOV aaaH,CR[MR1]	0B60H
Masked by MR2	MOV aaaH,CR[MR2]	0BA0H
Mask Register 1	MOV aaaH,MR1	0B21H
Mask Register 2	MOV aaaH,MR2	0B22H
Memory at Address, Location set Valid, from:		
Comparand Register	MOV aaaH,CR,V	0B24H
Masked by MR1	MOV aaaH,CR[MR1],V	0B64H
Masked by MR2	MOV aaaH,CR[MR2],V	0BA4H
Mask Register 1	MOV aaaH,MR1,V	0B25H
Mask Register 2	MOV aaaH,MR2,V	0B26H
Memory at Highest-Priority Match, No Change to Validity bits, from:		
Comparand Register	MOV HM,CR	0328H
Masked by MR1	MOV HM,CR[MR1]	0368H
Masked by MR2	MOV HM,CR[MR2]	03A8H
Mask Register 1	MOV HM,MR1	0329H
Mask Register 2	MOV HM,MR2	032AH
Memory at Highest-priority Match, Location set Valid, from:		
Comparand Register	MOV HM,CR,V	032CH
Masked by MR1	MOV HM,CR[MR1],V	036CH
Masked by MR2	MOV HM,CR[MR2],V	03ACH
Mask Register 1	MOV HM,MR1,V	032DH
Mask Register 2	MOV HM,MR2,V	032EH
Memory at Next Free Address, No Change to Validity bits, from:		
Comparand Register	MOV NF,CR	0330H
Masked by MR1	MOV NF,CR[MR1]	0370H
Masked by MR2	MOV NF,CR[MR2]	03B0H
Mask Register 1	MOV NF,MR1	0331H
Mask Register 2	MOV NF,MR2	0332H
Memory at Next Free Address, Location set Valid, from:		
Comparand Register	MOV NF,CR,V	0334H
Masked by MR1	MOV NF,CR[MR1],V	0374H
Masked by MR2	MOV NF,CR[MR2],V	03B4H
Mask Register 1	MOV NF,MR1,V	0335H
Mask Register 2	MOV NF,MR2,V	0336H

Instruction: Validity Bit Control

Operation	Mnemonic	Op-Code
Set Validity bits at Address Register		
Set Valid	VBC [AR],V	0424H
Set Empty	VBC [AR],E	0425H
Set Skip	VBC [AR],S	0426H
Set Random Access	VBC [AR],R	0427H
Set Validity bits at Address		
Set Valid	VBC aaaH,V	0C24H
Set Empty	VBC aaaH,E	0C25H
Set Skip	VBC aaaH,S	0C26H
Set Random Access	VBC aaaH,R	0C27H
Set Validity bits at Highest-Priority Match		
Set Valid	VBC HM,V	042CH
Set Empty	VBC HM,E	042DH
Set Skip	VBC HM,S	042EH
Set Random Access	VBC HM,R	042FH
Set Validity bits at All Matching Locations		
Set Valid	VBC ALM,V	043CH
Set Empty	VBC ALM,E	043DH
Set Skip	VBC ALM,S	043EH
Set Random Access	VBC ALM,R	043FH

Instruction: Compare

Operation	Mnemonic	Op-Code
Compare Valid Locations	CMP V	0504H
Compare Empty Locations	CMP E	0505H
Compare Skipped Locations	CMP S	0506H
Comp. Random Access Locations	CMP R	0507H

Instruction: Special Instructions

Operation	Mnemonic	Op-Code
Shift Comparand Right	SFT CR, R	0600H
Shift Comparand Left	SFT CR, L	0601H
Shift Mask Register 2 Right	SFT M2, R	0610H
Shift Mask Register 2 Left	SFT M2, L	0611H
Select Foreground Registers	SFR	0618H
Select Background Registers	SBR	0619H
Reset Seg. Cont. Reg. to Initial Val.	RSC	061AH

INSTRUCTION SET SUMMARY *Continued*

CYCLE LENGTH	CYCLE TYPE			
	Command Write	**Command Read**	**Data Write**	**Data Read**
Short	MOV reg, reg TCO reg (except CT) TCO CT (non-reset, HMA invalid) SPS, SPD, SFR SBR, RSC, NOP		Comparand register (not last segment) Mask register (not last segment)	
Medium	MOV reg, mem TCO CT (reset) VBC (NFA invalid) SFT	Status register or 16-bit register	Memory array (NFA invalid)	Comparand register Mask register
Long	MOV mem, reg TCO CT (non-reset, HMA valid) CMP VBC (NFA valid)		Memory array (NFA valid) Comparand register (last segment) Mask register (last segment)	Memory array
Note: The specific timing requirements for Short, Medium, and Long cycles are given in the Switching Characteristics Section under the tELEH parameter. For two cycle Command Writes (TCO reg or any instruction with “aaaH” as the source or destination), the first cycle is short, and the second cycle will be the length given.				

Table 6: Instruction Cycle Lengths

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	Reserved						CAM/RAM Part.			Comp. Mask		AR Inc/Dec		Reserved	
RESET = 0	Must be set =000000						64 CAM/0 RAM = 000 48 CAM/16 RAM = 001 32 CAM/32 RAM = 010 16 CAM/48 RAM = 011 48 RAM/16 CAM = 100 32 RAM/32 CAM = 101 16 RAM/48 CAM = 110 No Change = 111			None = 00 MR1 = 01 MR2 = 10 No Change = 11		Increment = 00 Decrement = 01 Disable = 10 No Change = 11		Must be set =00	
Note: D15 reads back as 0.															

Table 7: Control Register Bit Assignments

REGISTER BIT ASSIGNMENTS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDL	DCSL		DCEL		SSL	SCSL		SCEL		LDC	DSCV		LSC	SSCV	
Set Dest. Seg. Limits = 0 No Chng. = 1	Destination Count Start Limit 00–11		Destination Count End Limit 00–11		Set Source Seg. Limits = 0 No Chng. = 1	Source Count Start Limit 00–11		Source Count End Limit 00–11		Load Dest. Seg. Count = 0 No Chng. = 1	Destination Seg. Count Value 00–11		Load Src. Seg. Count = 0 No Chng. = 1	Source Seg. Count Value 00–11	

Note: D15, D10, D5, and D2 read back as 0s.

Table 8: Segment Control Register Bit Assignments

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2481L	0	0	0	0	0	Next Free Address, NF10–0										
4481L	0	0	0	0	Next Free Address, NF11–0											
8481L	0	0	0	Next Free Address, NF12–0												

Note: The Next Free Address register is read only, and is accessed by performing a Command Read cycle immediately following a TCO NF instruction.

Table 9: Next Free Address Register Bit Assignments

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ALL	/FF	/MM	Skip	Empty	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2481L	0	0	0	0	Match Address, AM10–AM0											/MF
4481L	0	0	0	Match Address, AM11–AM0												/MF
8481L	0	0	Match Address, AM12–AM0													/MF

Note: The Status register is read only, and is accessed by performing Command Read cycles. On the first cycle, bits 15–0 will be output, and if a second Command Read cycle is issued immediately after the first Command Read cycle, bits 31–16 will be output.

Table 10: Status Register Bit Assignments

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2481L	Device ID = 241H												PS			
4481L	Device ID = 441H												PS			
8481L	Device ID = 841H												PS			

Note: The Persistent Source register is read only, and is accessed by performing a Command Read cycle immediately following a TCO PS instruction.

Table 11: Persistent Source Register Bit Assignments

OPERATIONAL CHARACTERISTICS *Continued*

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 4.6 Volts
Voltage on all other pins	-0.5 to VCC +0.5 Volts (-2 Volts for 10 ns, measured at the 50% point)
Temperature under bias	-40°C to +85°C
Storage Temperature	-55°C to 125°C
DC Output Current	20 mA (per output, one at a time, one second duration.

Stresses exceeding those listed under Absolute Maximum Ratings may include failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

All voltages referenced to GND.

OPERATING CONDITIONS (voltages referenced to GND at the device pin)

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{CC}	Operating Supply Voltage	3.0	3.3	3.6	Volts	
V_{IH}	Input Voltage Logic 1	2.0		V_{CC} + 0.5	Volts	
V_{IL}	Input Voltage Logic 0	-0.5		0.8	Volts	1, 2
T_A	Ambient Operating Temperature	0		70	°C	Still Air

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min	Typical	Max	Units	Notes
I_{CC}	Average Power Supply Current	2481L		85	125	mA	t_{ELEL}= t_{ELEL}(min); 9
		4481L		90	160	mA	
		8481L		TBD	TBD	mA	
$I_{CC(SB)}$	Stand-by Power Supply Current				2	mA	/E = HIGH
V_{OH}	Output Voltage Logic 1		2.4			Volts	I_{OH} = -2.0mA
V_{OL}	Output Voltage Logic 0				0.4	Volts	I_{OL} = 4.0mA
I_{IZ}	Input Leakage Current	/RESET	6	9	12	Kohms	V_{IN} = 0 V
		TEST1, TEST2	6	10	13	Kohms	V_{IN} = V_{cc}; 10
		Others	-2		+2	µA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{OZ}	Output Leakage Current		-10		10	µA	$V_{SS} \le V_{OUT} \le V_{CC}$; DQ_N = High Impedance

CAPACITANCE

Symbol	Parameter	Max	Units	Notes
C_{IN}	Input Capacitance	6	pF	f = 1 MHz, V_{IN} = 0 V
C_{OUT}	Output Capacitance	7	pF	f = 1 MHz, V_{OUT} = 0 V

AC TEST CONDITIONS

Input Signal Transitions	0.0 Volts to 3.0 Volts
Input Signal Rise Time	< 3 ns
Input Signal Fall Time	< 3 ns
Input Timing Reference Level	1.5 Volts
Output Timing Reference Level	1.5 Volts

SWITCHING CHARACTERISTICS *(see note 3)*

		Cycle Time	-10		
No	**Symbol**	**Parameter (all times in nanoseconds)**	**Min**	**Max**	**Notes**
1	t_{ELEL}	Chip Enable Compare Cycle Time	100		
2	t_{ELEH}	Chip Enable LOW Pulse Width Short Cycle:	30		4
		Medium Cycle:	55		4
		Long Cycle:	75		4
3	t_{EHEL}	Chip Enable HIGH Pulse Width	15		
4	t_{CVEL}	Control Input to Chip Enable LOW Set-up Time	0		5
5	t_{ELCX}	Control Input from Chip Enable LOW Hold Time	10		5
6	t_{ELQX}	Chip Enable LOW to Outputs Active	3		6
7	t_{ELQV}	Chip Enable LOW to Outputs Valid		55	4,6
				75	4,6
8	t_{EHQZ}	Chip Enable HIGH to Outputs High-Z	3	15	7
9	t_{DVEL}	Data to Chip Enable LOW Set-up Time	0		
10	t_{ELDX}	Data from Chip Enable LOW Hold Time	10		
11	t_{ELFFV}	Chip Enable LOW to Full Flag Valid		75	
12	t_{EHMFX}	Chip Enable HIGH to /MF Invalid	0		
13	t_{EHMFV}	Chip Enable HIGH to /MF Valid		25	
14	t_{RLRH}	Reset LOW Pulse Width	100		8

Notes:
1. -1.0V for a duration of 10 ns measured at the 50% amplitude points for Input-only lines (Figure 5).
2. Common I/O lines are clamped, so that signal transients cannot fall below -0.5V.
3. At 0 – 70°C and Vcc(min) to Vcc(max).
4. See Table 6.
5. Control signals are /W and /CM.
6. With load specified in Figure 4, Test Load A.
7. With load specified in Figure 4, Test Load B.
8. /E must be HIGH during this period to ensure accurate default values in the configuration registers.
9. With output and I/O pins unloaded.
10. TEST1 and/or TEST2 may not be implemented on all versions of these products.

SWITCHING TEST FIGURES

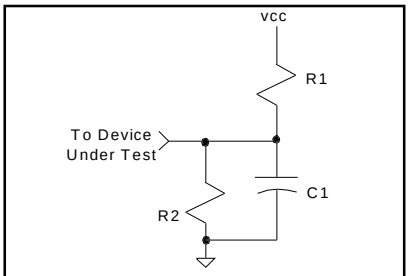


Figure 4: AC Test Load

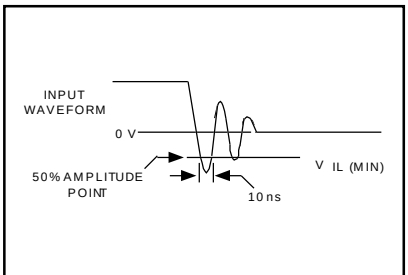


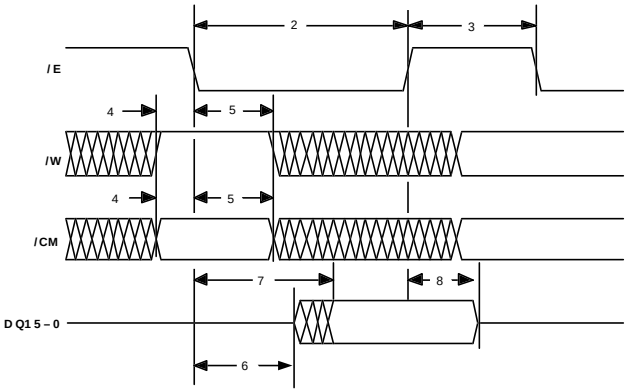
Figure 5: Input Signal Waveform

SWITCHING TEST FIGURES COMPONENT VALUES

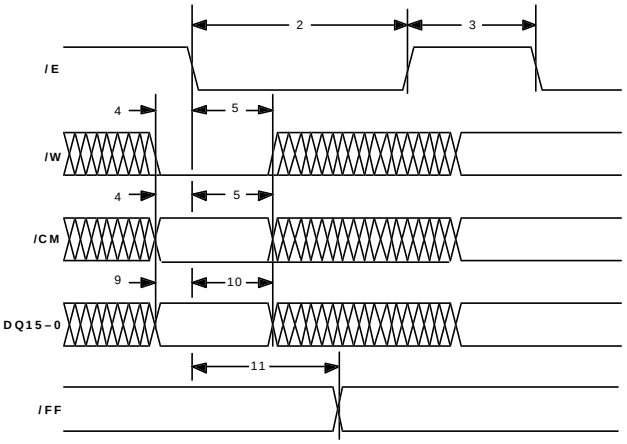
Component		Value	Units
VCC		3.3	Volts
R1		635	Ohms
R2		702	Ohms
C1 (includes jig)	Test Load A	30	pF
	Test Load B	5	pF

TIMING DIAGRAMS

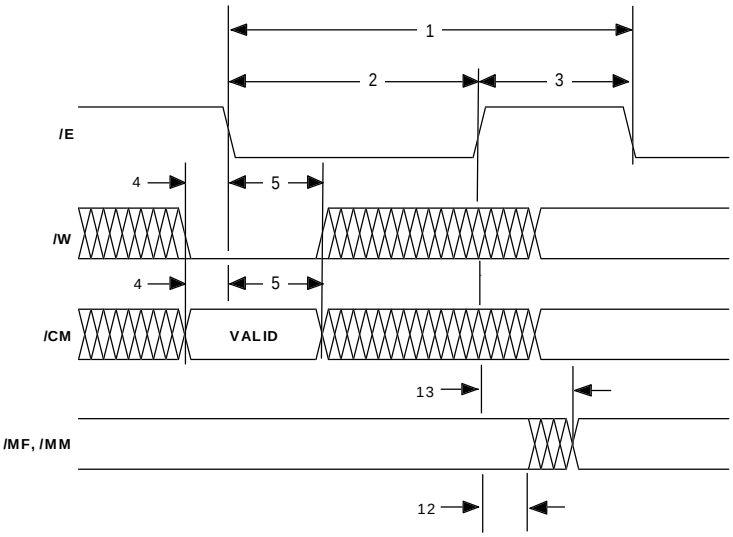
READ CYCLE



WRITE CYCLE



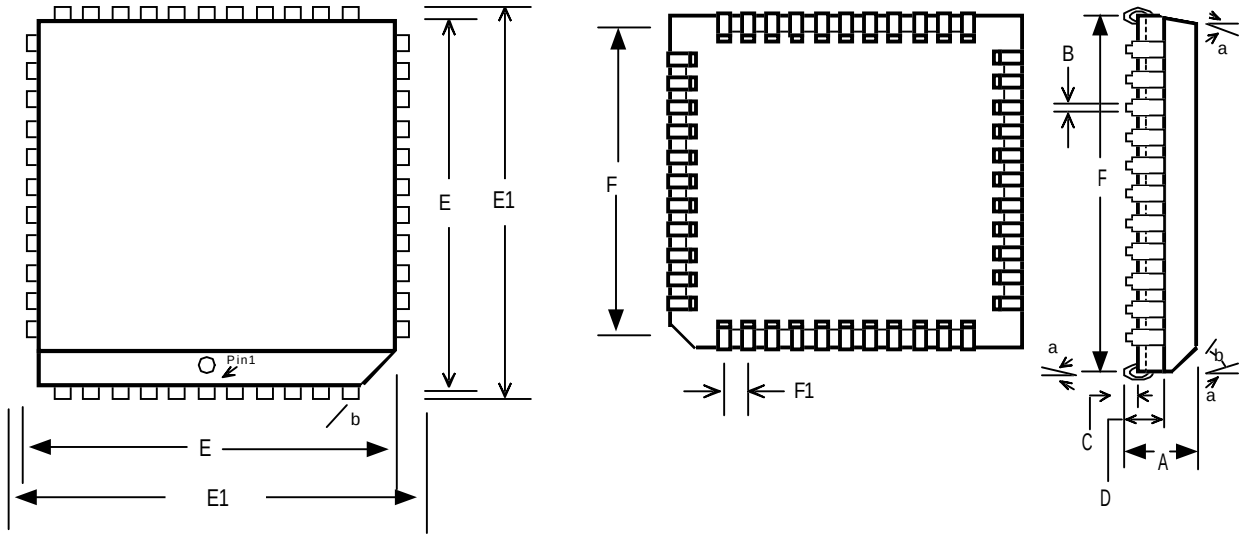
COMPARE CYCLE



ORDERING INFORMATION

PART NUMBER	ORGANIZATION	CYCLE TIME	PACKAGE	TEMPERATURE	VOLTAGE
MU9C2481L - 10DC	2048 x 64	100ns	44-PIN PLCC	0-70° C	3.3 ± 0.3
MU9C4481L - 10DC	4096 x 64	100ns	44-PIN PLCC	0-70° C	3.3 ± 0.3
MU9C8481L - 10DC	8192 x 64	100ns	44-PIN PLCC	0-70° C	3.3 ± 0.3

PACKAGE OUTLINE



Dimensions are in inches

	Dim. A	Dim. B	Dim. C	Dim. D	Dim. E	Dim. E1	Dim. F	Dim. F1	Dim. a	Dim. b	
44-pin PLCC	.170 / .180	.017 / TYP	.018 / .032	.100 / TYP	.650 / .656	.685 / .695	.590 / .630	.05 / TYP	3° / 6°	43° / 47°	

MUSIC Semiconductors Agent or Distributor:

MUSIC SEMICONDUCTORS

http://www.music-ic.com
email: info@music-ic.com

USA Headquarters
MUSIC Semiconductors
254 B Mountain Avenue
Hackettstown, New Jersey 07840
USA
Tel: 908/979-1010
Fax: 908/979-1035
USA Only: 800/933-1550 Tech. Support
888/226-6874 Product Info.

Asian Headquarters
MUSIC Semiconductors
Special Export Processing Zone 1
Carmelray Industrial Park
Canlubang, Calamba, Laguna
Philippines
Tel: +63 49 549 1480
Fax: +63 49 549 1023
Sales Tel/Fax: +632 723 62 15

European Headquarters
MUSIC Semiconductors
Torenstraat 28
6471 JX Eygelshoven
Netherlands
Tel: +31 45 5462177
Fax: +31 45 5463663