



CYPRESS

CY7C1019BV33

CY7C1018BV33

128K x 8 Static RAM

Features

- High speed
 - $t_{AA} = 10$ ns
- CMOS for optimum speed/power
- Center power/ground pinout
- Automatic power-down when deselected
- Easy memory expansion with CE and OE options
- Functionally equivalent to CY7C1019V33 and/or CY7C1018V33

Functional Description

The CY7C1019BV33/CY7C1018BV33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

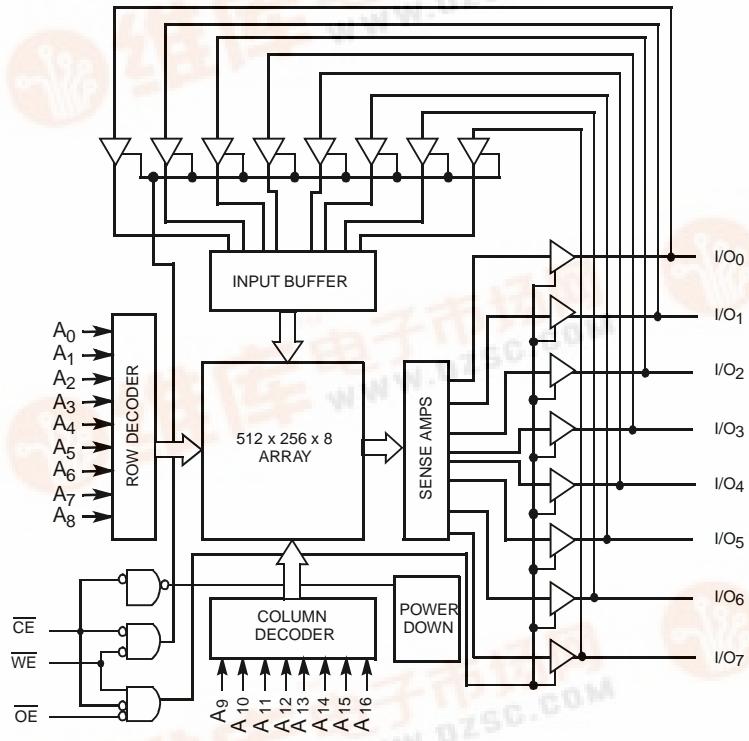
Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW, and WE LOW).

The CY7C1019BV33 is available in standard 32-pin TSOP Type II and 400-mil-wide package. The CY7C1018BV33 is available in a standard 300-mil-wide package.

Logic Block Diagram



Pin Configurations

SOJ / TSOPII

Top View

A_0	1	32	A_{16}
A_1	2	31	A_{15}
A_2	3	30	A_{14}
A_3	4	29	A_{13}
\overline{CE}	5	28	\overline{OE}
I/O_0	6	27	I/O_7
I/O_1	7	26	I/O_6
V_{CC}	8	25	V_{SS}
V_{SS}	9	24	V_{CC}
I/O_2	10	23	I/O_5
I/O_3	11	22	I/O_4
WE	12	21	A_{12}
A_4	13	20	A_{11}
A_5	14	19	A_{10}
A_6	15	18	A_9
A_7	16	17	A_8

Selection Guide

	7C1019BV33-10 7C1018BV33-10	7C1019BV33-12 7C1018BV33-12	7C1019BV33-15 7C1018BV33-15
Maximum Access Time (ns)	10	12	15
Maximum Operating Current (mA)	175	160	145
Maximum Standby Current (mA)	5	5	5
	L	—	0.5
			0.5

**CY7C1019BV33****CY7C1018BV33**

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with

Power Applied -55°C to $+125^{\circ}\text{C}$

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to $+7.0\text{V}$

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to $V_{\text{CC}} + 0.5\text{V}$

DC Input Voltage^[1] -0.5V to $V_{\text{CC}} + 0.5\text{V}$

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage $>2001\text{V}$
(per MIL-STD-883, Method 3015)

Latch-Up Current $>200\text{ mA}$

Operating Range

Range	Ambient Temperature ^[2]	V_{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$3.3\text{V} \pm 10\%$

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C1019BV33-10 7C1018BV33-10		7C1019BV33-12 7C1018BV33-12		7C1019BV33-15 7C1018BV33-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{\text{CC}} = \text{Min.}$, $I_{\text{OH}} = -4.0\text{ mA}$	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{\text{CC}} = \text{Min.}$, $I_{\text{OL}} = 8.0\text{ mA}$		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{\text{CC}} + 0.3$	2.2	$V_{\text{CC}} + 0.3$	2.2	$V_{\text{CC}} + 0.3$	V
V_{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I_{IX}	Input Load Current	$\text{GND} \leq V_{\text{I}} \leq V_{\text{CC}}$	-1	+1	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$\text{GND} \leq V_{\text{I}} \leq V_{\text{CC}}$, Output Disabled	-5	+5	-5	+5	-5	+5	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{\text{CC}} = \text{Max.}$, $I_{\text{OUT}} = 0\text{ mA}$, $f = f_{\text{MAX}} = 1/t_{\text{RC}}$		175		160		145	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	$\text{Max. } V_{\text{CC}}, \bar{C}\bar{E} \geq V_{\text{IH}}$ $V_{\text{IN}} \geq V_{\text{IH}}$ or $V_{\text{IN}} \leq V_{\text{IL}}, f = f_{\text{MAX}}$		20		20		20	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	$\text{Max. } V_{\text{CC}},$ $\bar{C}\bar{E} \geq V_{\text{CC}} - 0.3\text{V}$, $V_{\text{IN}} \geq V_{\text{CC}} - 0.3\text{V}$, or $V_{\text{IN}} \leq 0.3\text{V}, f = 0$	L	5		5		5	mA
				-		0.5		0.5	

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^{\circ}\text{C}, f = 1\text{ MHz}$, $V_{\text{CC}} = 5.0\text{V}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

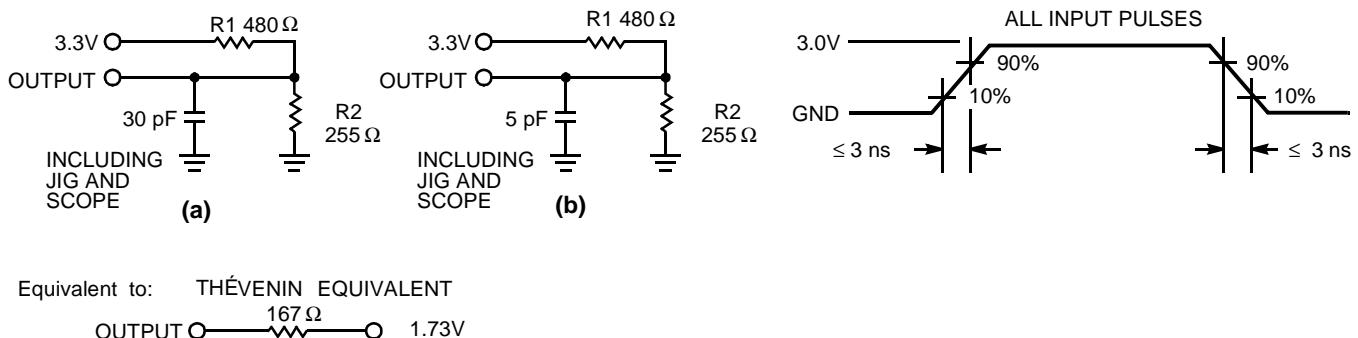
1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
2. T_A is the "Instant On" case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.



CY7C1019BV33

CY7C1018BV33

AC Test Loads and Waveforms



Switching Characteristics^[4] Over the Operating Range

Parameter	Description	7C1019BV33-10 7C1018BV33-10		7C1019BV33-12 7C1018BV33-12		7C1019BV33-15 7C1018BV33-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		10		12		15	ns
t_{DOE}	\overline{OE} LOW to Data Valid		5		6		7	ns
t_{LZOE}	\overline{OE} LOW to Low Z	0		0		0		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[5, 6]		5		6		7	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[6]	3		3		3		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[5, 6]		5		6		7	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		10		12		15	ns
WRITE CYCLE^[7, 8]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	\overline{CE} LOW to Write End	8		9		10		ns
t_{AW}	Address Set-Up to Write End	7		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	7		8		10		ns
t_{SD}	Data Set-Up to Write End	5		6		8		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[6]	3		3		3		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[5, 6]		5		6		7	ns

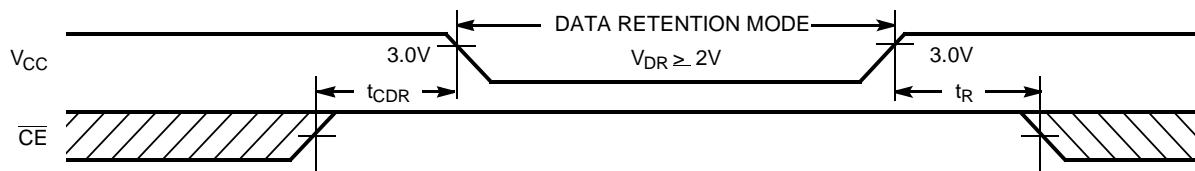
Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 (WE controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Data Retention Characteristics Over the Operating Range (L Version Only)

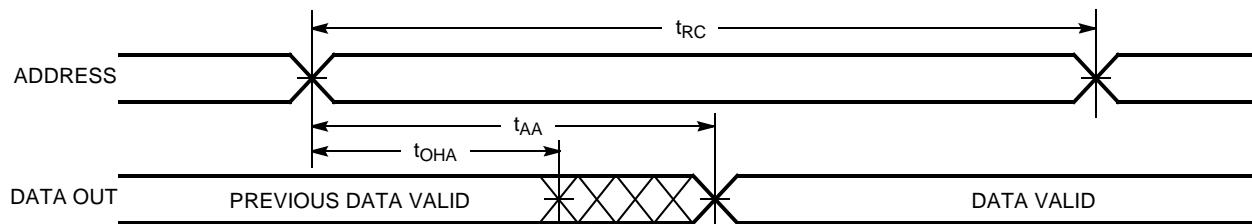
Parameter	Description	Conditions	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	$V_{CC} = V_{DR} = 2.0V$, $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	2.0		V
I_{CCDR}	Data Retention Current			150	μA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
t_R	Operation Recovery Time			200	μs

Data Retention Waveform

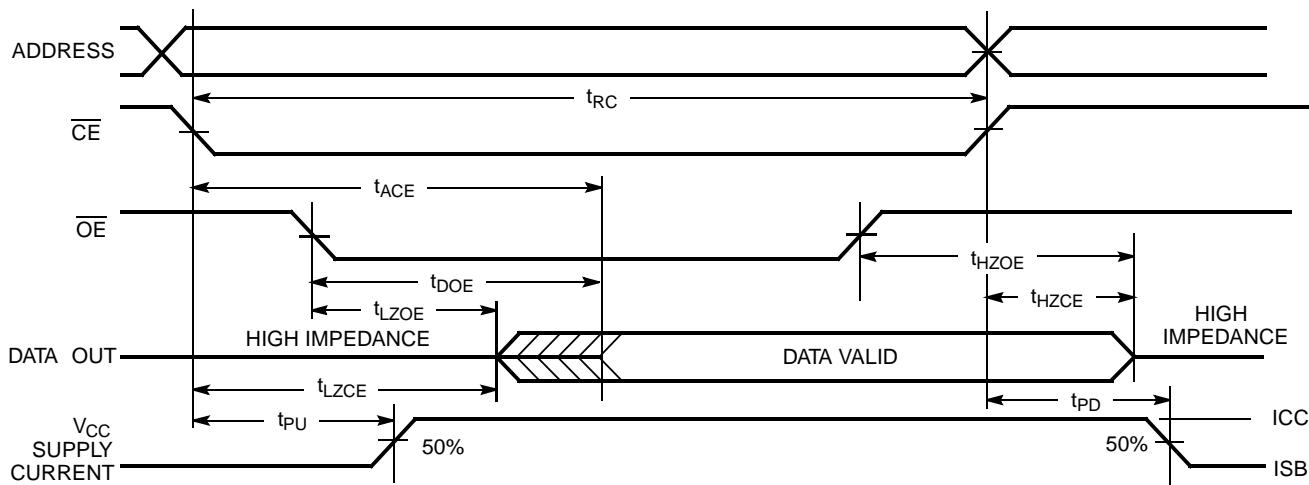


Switching Waveforms

Read Cycle No. 1^[9, 10]



Read Cycle No. 2 (OE Controlled)^[10, 11]

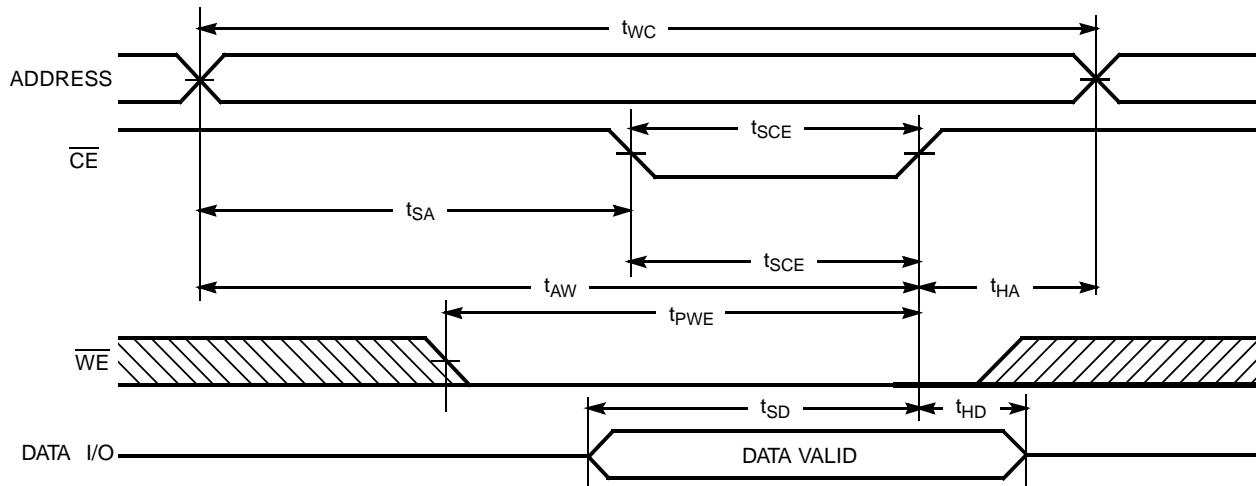


Notes:

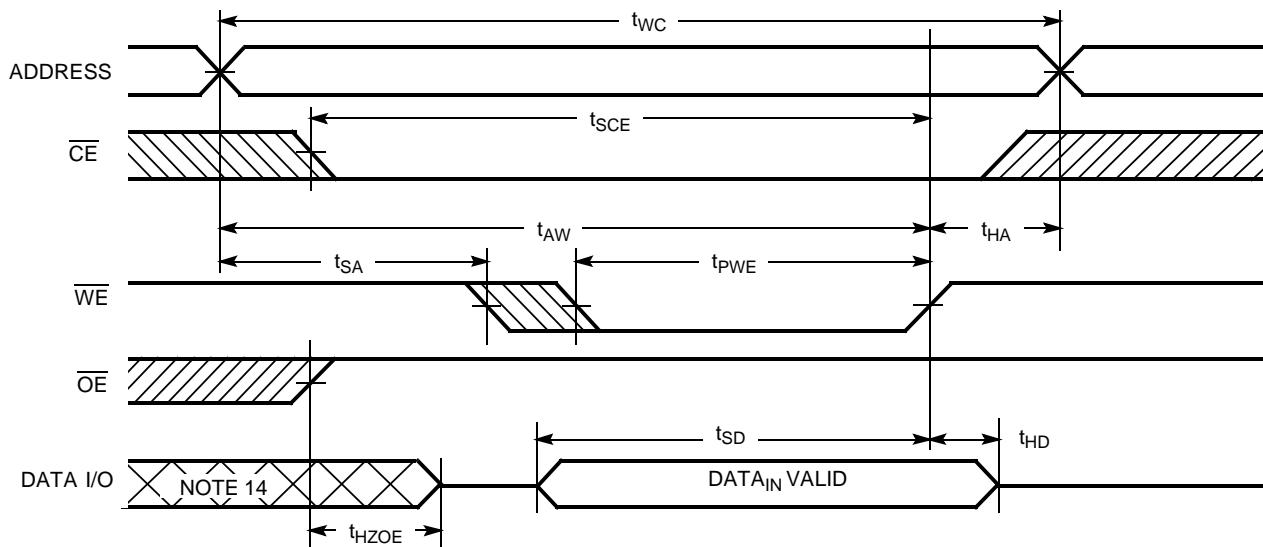
- 9. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
 - 10. WE is HIGH for read cycle.
 - 11. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[12, 13]



Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write)^[12, 13]

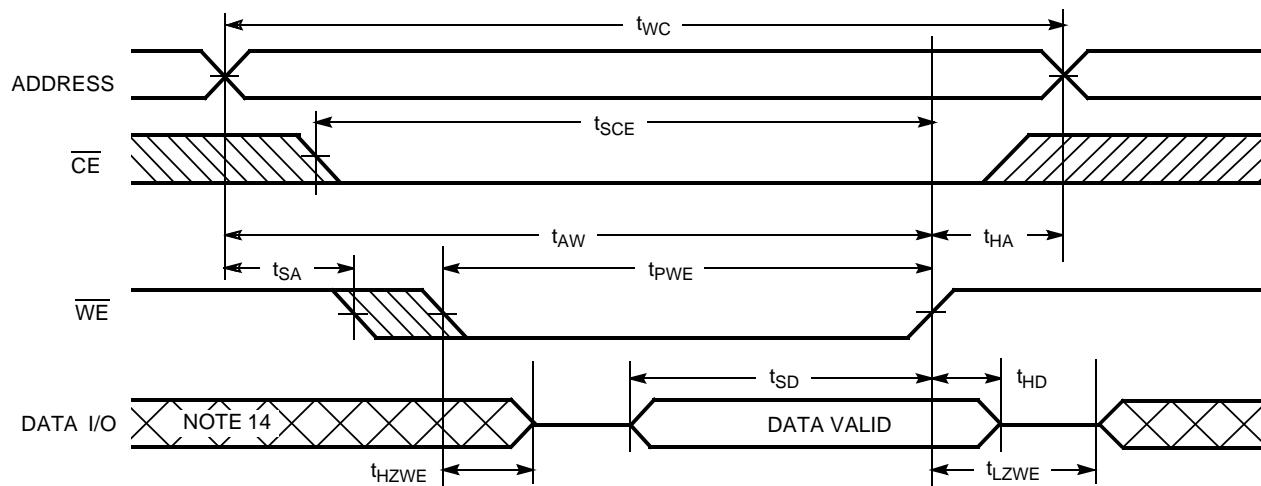


Notes:

12. Data I/O is high impedance if $\overline{\text{OE}} = \text{V}_{\text{IH}}$.
13. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.
14. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[13]



Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\text{I/O}_0\text{-}\text{I/O}_7$	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
X	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})



CY7C1019BV33

CY7C1018BV33

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1018V33-10VC	V32	32-Lead 300-Mil Molded SOJ	Commercial
	CY7C1019BV33-10VC	V33	32-Lead 400-Mil Molded SOJ	
	CY7C1019BV33-10ZC	ZS32	32-Lead TSOP Type II	
12	CY7C1018BV33-12VC	V32	32-Lead 300-Mil Molded SOJ	
	CY7C1018BV33L-12VC	V32	32-Lead 300-Mil Molded SOJ	
	CY7C1019BV33-12VC	V33	32-Lead 400-Mil Molded SOJ	
	CY7C1019BV33-12ZC	ZS32	32-Lead TSOP Type II	
	CY7C1019BV33L-12VC	V33	32-Lead 400-Mil Molded SOJ	
	CY7C1019BV33L-12ZC	ZS32	32-Lead TSOP Type II	
15	CY7C1018BV33-15VC	V32	32-Lead 300-Mil Molded SOJ	
	CY7C1018BV33L-15VC	V32	32-Lead 300-Mil Molded SOJ	
	CY7C1018BV33-15VI	V32	32-Lead 300-Mil Molded SOJ	
	CY7C1019BV33-15VC	V33	32-Lead 400-Mil Molded SOJ	
	CY7C1019BV33-15ZC	ZS32	32-Lead TSOP Type II	
	CY7C1019BV33L-15VC	V33	32-Lead 400-Mil Molded SOJ	
	CY7C1019BV33L-15ZC	ZS32	32-Lead TSOP Type II	
	CY7C1019BV33-15VI	V33	32-Lead 400-Mil Molded SOJ	
	CY7C1019BV33-15ZI	ZS32	32-Lead TSOP Type II	Industrial

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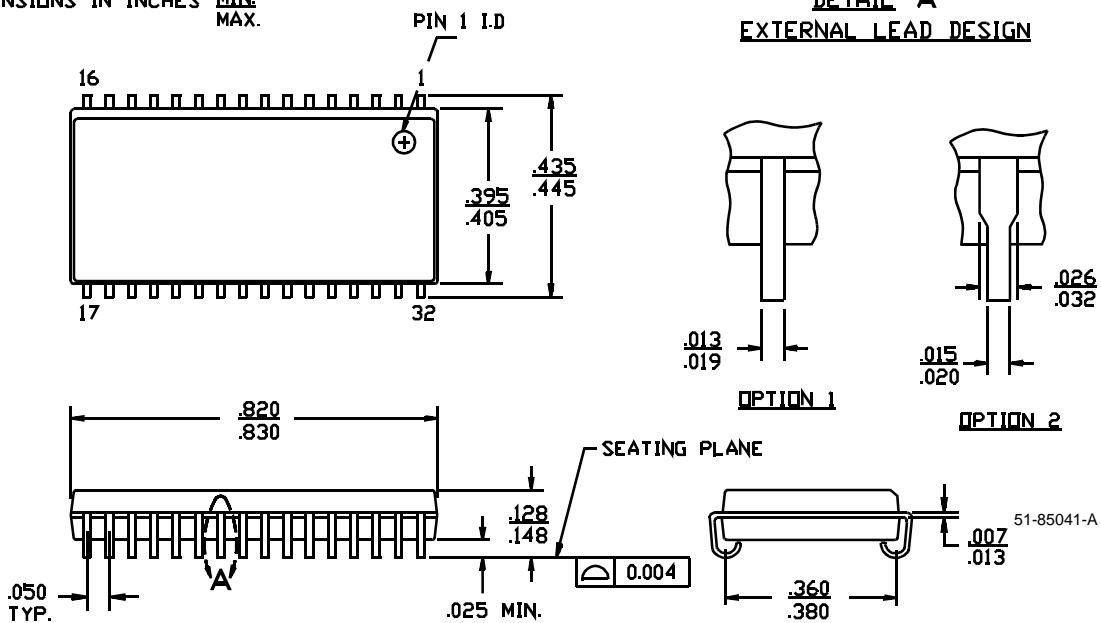
CY7C1019BV33

CY7C1018BV33

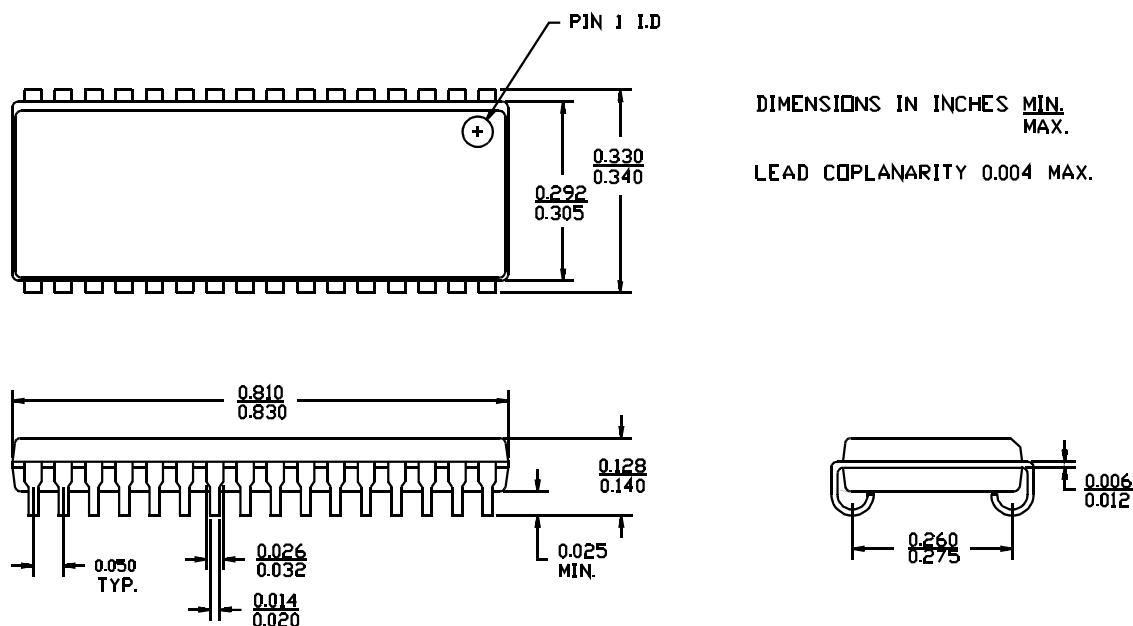
Package Diagram

32-Lead (400-Mil) Molded SOJ V33

DIMENSIONS IN INCHES MIN. MAX.



32-Lead (300-Mil) Molded SOJ V32





CY7C1019BV33

CY7C1018BV33

Package Diagram

32-Lead TSOP II ZS32

