



October 2007

LP3918 Battery Charge Management and Regulator Unit

General Description

The LP3918 is a fully integrated charger and multi-regulator unit designed for CDMA cellular phones. The LP3918 contains a Li-Ion battery charger, 7 low noise low dropout (LDO) voltage regulators and a high-speed serial interface to program on/off conditions and output voltages of individual regulators, and also to read status information from the PMU.

The Li-Ion charger integrates a power FET, reverse current blocking diode, sense resistor with current monitor output, and requires only a few external components. Charging is thermally regulated to obtain the most efficient charging rate for a given ambient temperature.

LDO regulators provide high PSRR and low noise ideally suited for supplying power to both analog and digital loads.

Applications

- CDMA Phone Handsets
- Low Power Wireless Handsets
- Handheld Information Appliances
- Personal Media Players
- Digital Cameras

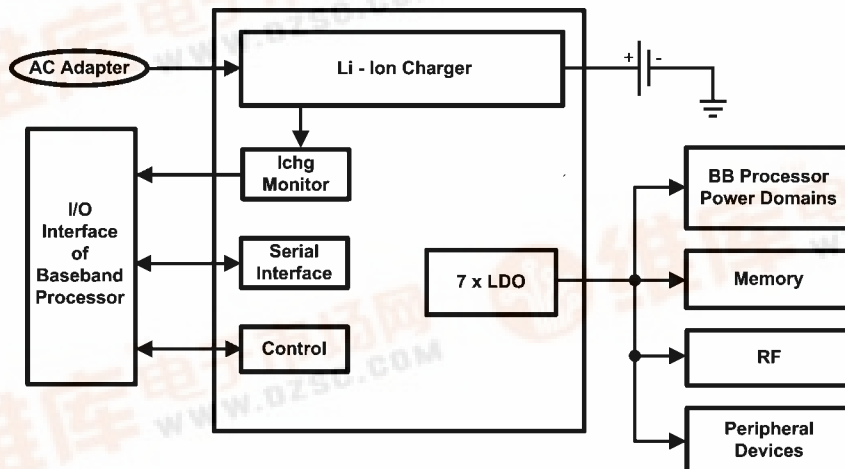
Features

- Fully integrated Li-Ion battery charger with thermal regulation
- USB Charge Mode.
- 7 Low Noise LDO's
 - 2 x 300 mA
 - 3 x 150 mA
 - 2 x 80 mA
- I2C compatible interface for controlling LDO outputs and charger operation
- Thermal shutdown
- Under Voltage Lockout
- 25-bump Thin micro-SMD package 2.5 x 2.5 mm
- Options available on request, please contact sales office for further information;
 - Level detect on HF_PWR & PWR_ON
 - LDO Charging mode
 - Custom Default Settings on Charger, and LDO O/P's.

Key Specifications

- 50mA to 950mA Programmable Charge Current
- 3.0V to 5.5V Input Voltage Range
- 200mV typ. Dropout Voltage on 300 mA LDO's
- 2% (typ) Output Voltage Accuracy on LDO's

Simplified Functional Block Diagram



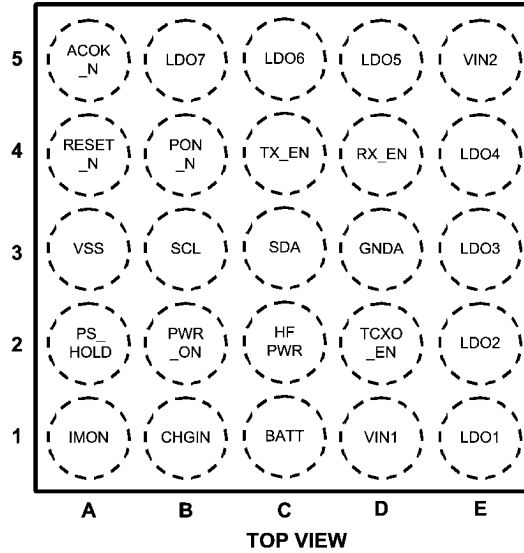
20211601

LP3918 Battery Charge Management and Regulator Unit



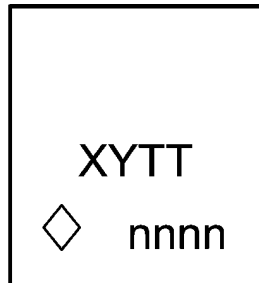
Device Pin Diagram

LP3918 25 pin micro-SMD Package
TOP VIEW



20211634

Package Marking Information



20211604

- The physical placement of the package marking will vary from part to part.
- Date Code. XYTT format. 'XY' 2 digit date code; 'TT' – die run code
- MNK - Package Marking
- See National web page for more info - http://www.national.com/quality/marketing_conventions.html

Ordering Information

| Order Number | Connector Debounce | LDO MODE | Package Marking | Supplied As |
|--------------|--------------------|----------|-----------------|-------------------------|
| LP3918TL | NO | NO | 3918 | 250 units, Tape & Reel |
| LP3918TLX | | | | 1000 units, Tape & Reel |
| LP3918TL-L | NO | YES | 3918L | 250 units, Tape & Reel |
| LP3918TLX-L | | | | 1000 units, Tape & Reel |
| LP3918TL-A | YES | NO | 3918A | 250 units, Tape & Reel |
| LP3918TLX-A | | | | 1000 units, Tape & Reel |

LP3918 Pin Descriptions

| Pin # | Name | Type | Description |
|-------|---------|------|---|
| A1 | IMON | A | Charge current monitor output. This pin presents an analog voltage representation of the input charging current. $V_{IMON}(mV) = (2.47 \times I_{CHG})(mA)$. |
| A2 | PS_HOLD | DI | Input for power control from external processor/controller. |
| A3 | VSS | G | Digital Ground pin |
| A4 | RESET_N | DO | Reset Output. Pin stays LOW during power up sequence. 60ms after LDO1 (CORE) is stable this pin is asserted HIGH. |
| A5 | ACOK_N | DO | AC Adapter indicator, LOW when 4.5V – 6.0V present at CHG_IN. |
| B1 | CHG_IN | P | DC power input to charger block from wall or car power adapters. |
| B2 | PWR_ON | DI | Power up sequence starts when this pin is set HIGH. Internal 500k Ω pull-down resistor. |
| B3 | SCL | DI | Serial Interface Clock input. External pull up resistor is needed, typ 1.5k Ω |
| B4 | PON_N | DO | Active low signal is PWR_ON inverted |
| B5 | LDO7 | A | LDO7 Output (GP) |
| C1 | BATT | P | Main battery connection. Used as a power connection for current delivery to the battery. |
| C2 | HF_PWR | DI | Power up sequence starts when this pin is set HIGH. Internal 500k Ω pull-down resistor. |
| C3 | SDA | DI/O | Serial Interface, Data Input/Output Open Drain output, external pull up resistor is needed, typ 1.5k Ω . |
| C4 | TX_EN | DI | Enable control for LDO6 (TX). HIGH = Enable, LOW = Disable. |
| C5 | LDO6 | A | LDO6 Output (TX) |
| D1 | VIN1 | P | Battery Input for LDO1 - 2 |
| D2 | TCXO_EN | DI | Enable control for LDO4 (TCXO). HIGH = Enable, LOW = Disable. |
| D3 | GNDA | G | Analog Ground pin |
| D4 | RX_EN | DI | Enable control for LDO5 (RX). HIGH = Enable, LOW = Disable. |
| D5 | LDO5 | A | LDO5 Output (RX) |
| E1 | LDO1 | A | LDO1 Output (CORE) |
| E2 | LDO2 | A | LDO2 Output (DIGI) |
| E3 | LDO3 | A | LDO3 Output (ANA) |
| E4 | LDO4 | A | LDO4 Output (TCXO) |
| E5 | VIN2 | P | Battery Input for LDO3 - 7 |

A: Analog. D: Digital. I: Input. DI/O: Digital Input/Output.
 G: Ground. O: Output. P: Power.

POWER SUPPLY CONFIGURATIONS

At PMU start up, LDO1, LDO2 and LDO3 are always started with their default voltages. The start up sequence of the LDO's is given below.

Startup Sequence

LDO1 -> LDO2 -> LDO3

LDO's with external enable control (LDO4, LDO5, LDO6) start immediately after LDO2 if enabled by logic high at their respective control inputs.

LDO7 (and LDO1 and 3) may be programmed to enable/disable once PS_HOLD has been asserted.

Default voltages for the LDOs are shown in *Table 1* and *Table 2* shows the voltages that may be programmed via the Serial Interface.

DEVICE PROGRAMMABILITY

An I²C compatible Serial Interface is used to communicate with the device to program a series of registers and also to read status registers. These internal registers allow control over LDO outputs and their levels. The charger functions may also be programmed to alter termination voltage, end of charge current, charger restart voltage, full rate charge current, and also the charging mode.

This device internal logic is powered from LDO2.

TABLE 1. LDO Default Voltages

| LDO | Function | mA | Default Voltage (V) | Startup Default | Enable Control |
|-----|----------|-----|---------------------|-----------------|----------------|
| 1 | CORE | 300 | 1.8 | ON | SI |
| 2 | DIGI | 300 | 3.0 | ON | - |
| 3 | ANA | 80 | 3.0 | ON | SI |
| 4 | TCXO | 80 | 3.0 | OFF | TCXO_EN |
| 5 | RX | 150 | 3.0 | OFF | RX_EN |
| 6 | TX | 150 | 3.0 | OFF | TX_EN |
| 7 | GP | 150 | 3.0 | OFF | SI |

TABLE 2. LDO Output Voltages Selectable via Serial Interface

| LDO | mA | 1.5 | 1.8 | 1.85 | 2.5 | 2.6 | 2.7 | 2.75 | 2.8 | 2.85 | 2.9 | 2.95 | 3.0 | 3.05 | 3.1 | 3.2 | 3.3 |
|-----|------|-----|-----|------|-----|-----|-----|------|-----|------|-----|------|-----|------|-----|-----|-----|
| 1 | CORE | 300 | + | + | + | + | + | + | + | + | + | + | + | + | + | + | + |
| 2 | DIGI | 300 | | | | + | + | + | + | + | + | + | + | + | + | + | + |
| 3 | ANA | 80 | | | | | + | + | + | + | + | + | + | + | | | |
| 4 | TCXO | 80 | + | + | + | + | + | + | + | + | + | + | + | + | + | + | + |
| 5 | RX | 150 | | | | | | + | + | + | + | + | + | + | | | |
| 6 | TX | 150 | | | | | | + | + | + | + | + | + | + | | | |
| 7 | GP | 150 | + | + | + | + | + | + | + | + | + | + | + | + | + | + | + |

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|--|
| CHG-IN, | -0.3 to +6.5V |
| VBATT =VIN1/2, BATT,HF_PWR | -0.3 to +6V |
| All other Inputs | -0.3 to V _{BATT} +0.3V, max 6.0V |
| Junction Temperature (T _{J-MAX}) | 150°C |
| Storage Temperature | -40°C to +150°C |
| Max Continuous Power Dissipation (P _{D-MAX}) (Note 3) | Internally Limited |
| ESD (Note 4) | |
| Batt, VIN1, VIN2, HF_PWR, CHG_IN, PWR_ON | 8kV HBM |
| All other pins | 2kV HBM |

| | |
|---|----------------------------------|
| HF_PWR, PWR_ON | 0V to 5.5V |
| ACOK_N, SDA, SCL, RX_EN, TX_EN, TCXO_EN, PS_HOLD, RESET_N | 0V to (V _{LDO2} + 0.3V) |
| All other pins | 0V to (V _{BATT} + 0.3V) |
| Junction Temperature (T _J) | -40°C to +125°C |
| Ambient Temperature (T _A) | -40 to 85°C |

Thermal Properties (Note 9)

| | |
|--|--------|
| Junction to Ambient Thermal Resistance θ_{JA} | |
| Jedec Standard Thermal PCB | 37°C/W |
| 4L Cellphone Board | 66°C/W |

Operating Ratings (Notes 1, 2)

| | |
|---------------------|-------------|
| CHG_IN | 4.5 to 6.0V |
| VBATT =VIN1/2, BATT | 3.0 to 5.5V |

General Electrical Characteristics

Unless otherwise noted, V_{IN} (= VIN1 = VIN2 = BATT) = 3.6V, GND = 0V, C_{VIN1-2}=10 μ F, C_{LDOX}=1 μ F. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_a = T_J = -40°C to +125°C. (Note 6)

| Symbol | Parameter | Condition | Typ | Limit | | Units |
|-------------------------|------------------------|--|-----|-------|-----------|---------|
| | | | | Min | Max | |
| I _{Q(STANDBY)} | Standby Supply Current | V _{IN} = 3.6V, UVLO on, internal logic circuit on, all other circuits off | 2 | | 10 | μ A |

Power Monitor Functions

Battery Under-Voltage Lockout

| | | | | | | |
|---------------------|------------------------|------------------------|------|-----|-----|---|
| V _{UVLO-R} | Under Voltage Lock-out | V _{IN} Rising | 2.85 | 2.7 | 3.0 | V |
|---------------------|------------------------|------------------------|------|-----|-----|---|

Thermal Shutdown

| | | | | | | |
|--|---------------|----------|-----|--|--|----|
| | TSD Threshold | (Note 7) | 160 | | | °C |
|--|---------------|----------|-----|--|--|----|

| Symbol | Parameter | Condition | Typ | Limit | | Units |
|---|---------------------|--|-----|----------------------------|----------------------------|-------|
| | | | | Min | Max | |
| LOGIC AND CONTROL INPUTS (LDO2 at 3.0V) | | | | | | |
| V _{IL} | Input Low Level | PS_HOLD, SDA, SCL, RX_EN, TCXO_EN, TX_EN | | | 0.25* V _{LDO2} | V |
| | | PWR_ON, HF_PWR | | | 0.25* V _{BATT} | V |
| V _{IH} | Input High Level | PS_HOLD, SDA, SCL, RX_EN, TCXO_EN, TX_EN | | 0.75* V _{LDO2} | | V |
| | | PWR_ON, HF_PWR | | 0.75* V _{BATT} | | V |
| I _{IL} | Logic Input Current | All logic inputs except PWR_ON and HF_PWR 0V ≤ V _{INPUT} ≤ V _{BATT} | | -5 | +5 | μA |
| R _{IN} | Input Resistance | PWR_ON, HF_PWR Pull-Down resistance to GND(Note 7) | 500 | | | kΩ |
| LOGIC AND CONTROL OUTPUTS (LDO2 at 3.0V) | | | | | | |
| V _{OL} | Output Low Level | PON_N, RESET_N, SDA, ACOK_N I _{OUT} = 2mA | | | 0.25* V _{LDO2} | V |
| V _{OH} | Output High Level | PON_N, RESET_N, ACOK_N I _{OUT} = 2mA (Not applicable to Open Drain Output SDA) | | 0.75* V _{LDO2} | | V |

LDO1 (CORE) Electrical Characteristics

Unless otherwise noted, V_{IN} (= VIN1 = VIN2 = BATT) = 3.6V, GND = 0V, C_{VIN1-2} = 10μF, C_{LDOX} = 1μF. V_{OUT1} set to 3.0V output. Note V_{INMIN} is the greater of 3.0V or V_{OUT1} + 0.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_a = T_J = -40°C to +125°C. (Note 6)

| Symbol | Parameter | Condition | Typ | Limit | | Units |
|------------------------|------------------------------|--|-----|-------|------------|-------------------|
| | | | | Min | Max | |
| V _{OUT1} | Output Voltage Accuracy | I _{OUT1} = 1mA, V _{OUT1} = 3.0V | | -2 | +2 | % |
| | Output Voltage | Default | 1.8 | | | V |
| I _{OUT1} | Output Current | V _{INMIN} ≤ V _{IN} ≤ 5.5V | | | 300 | mA |
| | Output Current Limit | V _{OUT1} = 0V | 600 | | | |
| V _{DO1} | Dropout Voltage | I _{OUT1} = 300mA, (Note 8) | 200 | | 280 | mV |
| ΔV _{OUT1} | Line Regulation | V _{INMIN} ≤ V _{IN} ≤ 5.5V I _{OUT1} = 1mA | 2 | | | mV |
| | Load Regulation | 1mA ≤ I _{OUT1} ≤ 300mA | 20 | | | mV |
| e _{n1} | Output Noise Voltage | 10Hz ≤ f ≤ 100KHz, C _{OUT} = 1μF (Note 7) | 45 | | | μV _{RMS} |
| PSRR | Power Supply Rejection Ratio | F = 10kHz, C _{OUT} = 1μF I _{OUT1} = 20mA (Note 7) | 65 | | | dB |
| t _{START-UP} | Start-Up Time from Shut-down | C _{OUT} = 1μF, I _{OUT1} = 300mA (Note 7) | 60 | | 170 | μs |
| T _{Transient} | Start-Up Transient Overshoot | C _{OUT} = 1μF, I _{OUT1} = 300mA (Note 7) | 60 | | 120 | mV |

LDO2 (DIGI) Electrical Characteristics

Unless otherwise noted, V_{IN} (= $V_{IN1} = V_{IN2} = BATT$) = 3.6V, $GND = 0V$, $C_{VIN1-2} = 10\mu F$, $C_{LDOX} = 1\mu F$. Note V_{INMIN} is the greater of 3.0V or $V_{OUT2} + 0.5V$. Typical values and limits appearing in normal type apply for $T_J = 25^\circ C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_a = T_J = -40^\circ C$ to $+125^\circ C$. (Note 6)

| Symbol | Parameter | Condition | Typ | Limit | | Units |
|-------------------|------------------------------|--|-----|-----------|------------|---------------|
| | | | | Min | Max | |
| V_{OUT2} | Output Voltage Accuracy | $I_{OUT2} = 1mA$, $V_{OUT2} = 3.0V$ | | -2 | +2 | % |
| | | | | -3 | +3 | |
| | Output Voltage | Default | 3.0 | | | V |
| I_{OUT2} | Output Current | $V_{INMIN} \leq V_{IN} \leq 5.5V$ | | | 300 | mA |
| | Output Current Limit | $V_{OUT2} = 0V$ | 600 | | | |
| V_{DO2} | Dropout Voltage | $I_{OUT2} = 300mA$ (Note 8) | 200 | | 280 | mV |
| ΔV_{OUT2} | Line Regulation | $V_{INMIN} \leq V_{IN} \leq 5.5V$ $I_{OUT2} = 1mA$ | 2 | | | mV |
| | Load Regulation | $1mA \leq I_{OUT2} \leq 300mA$ | 20 | | | mV |
| e_{n2} | Output Noise Voltage | $10Hz \leq f \leq 100KHz$, $C_{OUT} = 1\mu F$ (Note 7) | 45 | | | μV_{RMS} |
| PSRR | Power Supply Rejection Ratio | $F = 10kHz$, $C_{OUT} = 1\mu F$ $I_{OUT2} = 20mA$ (Note 7) | 65 | | | dB |
| $t_{START-UP}$ | Start-Up Time from Shut-down | $C_{OUT} = 1\mu F$, $I_{OUT2} = 300mA$ (Note 7) | 40 | | 60 | μs |
| $t_{Transient}$ | Start-Up Transient Overshoot | $C_{OUT} = 1\mu F$, $I_{OUT2} = 300mA$ (Note 7) | 5 | | 30 | mV |

LDO3 (ANA), LDO4 (TCXO) Electrical Characteristics

Unless otherwise noted, V_{IN} (= $V_{IN1} = V_{IN2} = BATT$) = 3.6V, $GND = 0V$, $C_{VIN1-2} = 10\mu F$, $C_{LDOX} = 1\mu F$. $TCXO_EN$ high. Note V_{INMIN} is the greater of 3.0V or $V_{OUT3/4} + 0.5V$. Typical values and limits appearing in normal type apply for $T_J = 25^\circ C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_a = T_J = -40^\circ C$ to $+125^\circ C$. (Note 6)

| Symbol | Parameter | Condition | Typ | Limit | | Units |
|--|------------------------------|--|------------|-----------|-----------|---------------|
| | | | | Min | Max | |
| V_{OUT3} , V_{OUT4} | Output Voltage Accuracy | $I_{OUT3/4} = 1mA$, $V_{OUT3/4} = 3.0V$ | | -2 | +2 | % |
| | | | | -3 | +3 | |
| | Output Voltage | LDO3 default LDO4 default | 3.0 3.0 | | | V |
| I_{OUT3} , I_{OUT4} | Output Current | $V_{INMIN} \leq V_{IN} \leq 5.5V$ | | | 80 | mA |
| | Output Current Limit | $V_{OUT3/4} = 0V$ | 160 | | | |
| V_{DO3} , V_{DO4} | Dropout Voltage | $I_{OUT3/4} = 80mA$ (Note 8) | 180 | | 220 | mV |
| ΔV_{OUT3} , ΔV_{OUT4} | Line Regulation | $V_{INMIN} \leq V_{IN} \leq 5.5V$ $I_{OUT3/4} = 1mA$ | 2 | | | mV |
| | Load Regulation | $1mA \leq I_{OUT3/4} \leq 80mA$ | 20 | | | mV |
| e_{n3} , e_{n4} | Output Noise Voltage | $10Hz \leq f \leq 100kHz$, $C_{OUT} = 1\mu F$ (Note 7) | 45 | | | μV_{RMS} |
| PSRR | Power Supply Rejection Ratio | $F = 10kHz$, $C_{OUT} = 1\mu F$ $I_{OUT3/4} = 20mA$ (Note 7) | 65 | | | dB |
| $t_{START-UP}$ | Start-Up Time from Shut-down | $C_{OUT} = 1\mu F$, $I_{OUT3/4} = 80mA$ (Note 7) | 40 | | 60 | μs |
| $t_{Transient}$ | Start-Up Transient Overshoot | $C_{OUT} = 1\mu F$, $I_{OUT3/4} = 80mA$ (Note 7) | 5 | | 30 | mV |

LDO5 (RX), LDO6 (TX), LDO7 (GP) Electrical Characteristics

Unless otherwise noted, V_{IN} (= VIN1 = VIN2 = BATT) = 3.6V, GND = 0V, C_{VIN1-2} = 10 μ F, C_{LDOX} = 1 μ F. RX_EN, TX_EN high. LDO7 Enabled via Serial Interface. Note V_{INMIN} is the greater of 3.0V or $V_{OUT5/6/7} + 0.5V$. Typical values and limits appearing in normal type apply for $T_J = 25^\circ\text{C}$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_a = T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$. (Note 6)

| Symbol | Parameter | Condition | Typ | Limit | | Units |
|---|------------------------------|--|-----|-----------|------------|----------------------------|
| | | | | Min | Max | |
| V_{OUT5} , V_{OUT6} , V_{OUT7} | Output Voltage | $I_{OUT5/6/7} = 1\text{mA}$, $V_{OUT5/6/7} = 3.0V$ | | -2 | +2 | % |
| | | | | -3 | +3 | |
| | Output Voltage | LDO5 default | 3.0 | | | V |
| | | LDO6 default | 3.0 | | | |
| | | LDO7 default | 3.0 | | | |
| I_{OUT5} , I_{OUT6} , I_{OUT7} | Output Current | $V_{INMIN} \leq V_{IN} \leq 5.5V$ | | | 150 | mA |
| | Output Current Limit | $V_{OUT5/6/7} = 0V$ | 300 | | | |
| V_{DO5} , V_{DO6} , V_{DO7} | Dropout Voltage | $I_{OUT5/6/7} = 150\text{mA}$ (Note 8) | 180 | | 240 | mV |
| ΔV_{OUT5} , ΔV_{OUT6} , ΔV_{OUT7} | Line Regulation | $V_{INMIN} \leq V_{IN} \leq 5.5V$ $I_{OUT5/6/7} = 1\text{mA}$ | 2 | | | mV |
| | Load Regulation | $1\text{mA} \leq I_{OUT5/6/7} \leq 150\text{mA}$ | 20 | | | mV |
| e_{n5} , e_{n6} , e_{n7} | Output Noise Voltage | $10\text{Hz} \leq f \leq 100\text{kHz}$, $C_{OUT} = 1\mu\text{F}$ (Note 7) | 45 | | | μV_{RMS} |
| PSRR | Power Supply Rejection Ratio | $F = 10\text{kHz}$, $C_{OUT} = 1\mu\text{F}$ $I_{OUT5/6/7} = 20\text{mA}$ (Note 7) | 65 | | | dB |
| $t_{\text{START-UP}}$ | Start-Up Time from Shut-down | $C_{OUT} = 1\mu\text{F}$, $I_{OUT5/6/7} = 150\text{mA}$ (Note 7) | 40 | | 60 | μs |
| $t_{\text{Transient}}$ | Start-Up Transient Overshoot | $C_{OUT} = 1\mu\text{F}$, $I_{OUT5/6/7} = 150\text{mA}$ (Note 7) | 5 | | 30 | mV |

Charger Electrical Characteristics

Unless otherwise noted, $V_{CHG_IN} = 5V$, V_{IN} (= $V_{IN1} = V_{IN2} = BATT$) = 3.6V. $C_{CHG_IN} = 10\mu F$, $C_{BATT} = 30\mu F$. Charger set to default settings unless otherwise noted. Typical values and limits appearing in normal type apply for $T_J = 25^\circ C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_a = T_J = -25^\circ C$ to $+85^\circ C$. (Notes 6, 9)

| Symbol | Parameter | Condition | Typ | Limit | | Units |
|--------------------------------------|---|--|-------|-------------|-------------|------------|
| | | | | Min | Max | |
| V_{CHG_IN} | Input Voltage Range | | | 4.5 | 6.5 | V |
| | Operating Range | | | 4.5 | 6 | |
| V_{OK_CHG} | CHG_IN OK trip-point | $V_{CHG_IN} - V_{BATT}$ (Rising) | 200 | | | mV |
| | | $V_{CHG_IN} - V_{BATT}$ (Falling) | 50 | | | |
| V_{TERM} | Battery Charge Termination voltage | Default | 4.2 | | | V |
| | V_{TERM} voltage tolerance | $T_J = 25^\circ C$ | | -0.35 | +0.35 | % |
| | | $T_J = 0^\circ C$ to $85^\circ C$ | | | -1 | |
| I_{CHG} | Fast Charge Current Accuracy | $I_{CHG} = 450mA$ | | -10 | +10 | % |
| | Programmable full-rate charge current range (default 100mA) | $6.0V \geq V_{CHG_IN} \geq 4.5V$ $V_{BATT} < (V_{CHG_IN} - V_{OK_CHG})$ $V_{FULL_RATE} < V_{BATT} < V_{TERM}$ (Note 10) | | 50 | 950 | mA |
| | | Default | 100 | | | |
| | Charge current programming step | | 50 | | | |
| $I_{PREQUAL}$ | Pre-qualification current | $V_{BATT} = 2V$ | 50 | 40 | 60 | mA |
| I_{CHG_USB} | CHG_IN programmable current in USB mode | $5.5V \geq V_{CHG_IN} \geq 4.5V$ $V_{BATT} < (V_{CHG_IN} - V_{OK_CHG})$ $V_{FULL_RATE} < V_{BATT} < V_{TERM}$ Default = 100mA | Low | 100 | | mA |
| | | | High | 450 | | |
| | | | | 100 | | |
| V_{FULL_RATE} | Full-rate qualification threshold | V_{BATT} rising, transition from pre-qual to full-rate charging | 3.0 | 2.9 | 3.1 | V |
| I_{EOC} | End of Charge Current, % of full-rate current | 0.1C option selected | 10 | | | % |
| $V_{RESTART}$ | Restart threshold voltage | V_{BATT} falling, transition from EOC to full-rate charge mode. Default options selected - 4.05V | 4.05 | 3.97 | 4.13 | V |
| I_{MON} | I_{MON} Voltage 1 | $I_{CHG} = 100mA$ | 0.247 | | | V |
| | I_{MON} Voltage 2 | $I_{CHG} = 450mA$ | 1.112 | 0.947 | 1.277 | |
| T_{REG} | Regulated junction temperature | (Note 7) | 115 | | | $^\circ C$ |
| Detection and Timing (Note 7) | | | | | | |
| T_{POK} | Power OK deglitch time | $V_{BATT} < (V_{CC} - V_{OK_CHG})$ | 32 | | | mS |
| T_{PQ_FULL} | Deglitch time | Pre-qualification to full-rate charge transition | 230 | | | mS |
| T_{CHG} | Charge timer | Precharge mode | 1 | | | Hrs |
| | | Full Rate Charging Timeout | 5 | | | |
| | | Constant Voltage Timeout | 5 | | | |
| T_{EOC} | Deglitch time for end-of-charge transition | | 230 | | | mS |

Serial Interface

Unless otherwise noted, V_{IN} (= $V_{IN1} = V_{IN2} = BATT$) = 3.6V, $GND = 0V$, $C_{VIN1-2} = 10\mu F$, $C_{LDOX} = 1\mu F$, and V_{LDO2} (DIG) = 3.0V. Typical values and limits appearing in normal type apply for $T_J = 25^\circ C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_a = T_J = -40^\circ C$ to $+125^\circ C$. (Notes 6, 7)

| Symbol | Parameter | Condition | Typ | Limit | | Units |
|-----------------|--|-----------|-----|-------|-----|---------|
| | | | | Min | Max | |
| f_{CLK} | Clock Frequency | | | | 400 | kHz |
| t_{BF} | Bus-Free Time between START and STOP | | | 1.3 | | μs |
| t_{HOLD} | Hold Time Repeated START Condition | | | 0.6 | | μs |
| t_{CLK-LP} | CLK Low Period | | | 1.3 | | μs |
| t_{CLK-HP} | CLK High Period | | | 0.6 | | μs |
| t_{SU} | Set-Up Time Repeated START Condition | | | 0.6 | | μs |
| $t_{DATA-HOLD}$ | Data Hold Time | | | 50 | | ns |
| $t_{DATA-SU}$ | Data Set-Up Time | | | 100 | | ns |
| t_{SU} | Set-Up Time for STOP Condition | | | 0.6 | | μs |
| t_{TRANS} | Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter of both DATA & CLK Signals | | 50 | | | ns |

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal Thermal Shutdown circuitry protects the device from permanent damage.

Note 4: The human-body model is 100pF discharged through 1.5k Ω . The machine model is a 200pF capacitor discharged directly into each pin, MIL-STD-883 3015.7.

Note 5: Care must be exercised where high power dissipation is likely. The maximum ambient temperature may have to be derated.

Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. In applications where high power dissipation and/or poor thermal dissipation exists, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A_MAX}) is dependent on the maximum power dissipation of the device in the application (P_{D_MAX}), and the junction to ambient thermal resistance of the device/package in the application (θ_{JA}), as given by the following equation:

$$T_{A_MAX} = T_{J_MAX-OP} - (\theta_{JA} \times P_{D_MAX})$$

Note 6: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with $T_J = 25^\circ C$. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 7: Guaranteed by design.

Note 8: Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the 3.0V minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.

Note 9: Junction-to-ambient thermal resistance (θ_{JA}) is taken from thermal modelling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The value of (θ_{JA}) of this product could fall within a wide range, depending on PWB material, layout, and environmental conditions. In applications where high maximum power dissipation exists (high V_{IN} , high I_{OUT}), special care must be paid to thermal dissipation issues in board design.

Note 10: Full charge current is guaranteed for $CHG_IN = 4.5$ to $6.0V$. At higher input voltages, increased power dissipation may cause the thermal regulation to limit the current to a safe level, resulting in longer charging time.

Register Information, Slave Address Code 7h'7E

TABLE 3. Control Registers

| Addr | Register (default value) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------|-----------------------------|-------------------|------------------|-----------------|-------------------|------------------|------------------|--------------------|--------------------|
| 8h'00 | OP_EN (0000 0101) | X | X | X | X | LDO7_EN | LDO3_EN | X | LDO1_EN |
| 8h'01 | LDO1PGM O/P (0000 0001) | X | X | X | X | V1_OP[3] | V1_OP[2] | V1_OP[1] | V1_OP[0] |
| 8h'02 | LDO2PGM O/P (0000 1011) | X | X | X | X | V2_OP[3] | V2_OP[2] | V2_OP[1] | V2_OP[0] |
| 8h'03 | LDO3PGM O/P (0000 1011) | X | X | X | X | V3_OP[3] | V3_OP[2] | V3_OP[1] | V3_OP[0] |
| 8h'04 | LDO4PGM O/P (0000 1011) | X | X | X | X | V4_OP[3] | V4_OP[2] | V4_OP[1] | V4_OP[0] |
| 8h'05 | LDO5PGM O/P (0000 1011) | X | X | X | X | V5_OP[3] | V5_OP[2] | V5_OP[1] | V5_OP[0] |
| 8h'06 | LDO6PGM O/P (0000 1011) | X | X | X | X | V6_OP[3] | V6_OP[2] | V6_OP[1] | V6_OP[0] |
| 8h'07 | LDO7PGM O/P (0000 1011) | X | X | X | X | V7_OP[3] | V7_OP[2] | V7_OP[1] | V7_OP[0] |
| 8h'0C | STATUS (0000 0000) | PWR_ON _TRIG | HF_PWR _TRIG | CHG_IN _TRIG | X | X | X | X | X |
| 8h'10 | CHGCNTL1 (0000 1001) | USBMODE _EN | CHGMODE _EN | Force EOC | TOUT_ doubling | EN_Tout | En_EOC | X | EN_CHG |
| 8h'11 | CHGCNTL2 (0000 0001) | | | | Prog_ ICHG[4] | Prog_ ICHG[3] | Prog_ ICHG[2] | Prog_ ICHG[1] | Prog_ ICHG[0] |
| 8h'12 | CHGCNTL3 (0001 0010) | | | VTERM[1] | VTERM[0] | Prog_ EOC[1] | Prog_ EOC[0] | Prog_ VRSTRT[1] | Prog_ VRSTRT[0] |
| 8h'13 | CHGSTATUS1 | Batt_Over _Out | CHGIN_ OK_Out | EOC | Tout_ Fullrate | Tout_ Prechg | LDO Mode | Fullrate | PRECHG |
| 8h'14 | CHGSTATUS2 | | | | | | | Tout_ ConstV | Bad_Batt |
| 8h'1C | MISC Control1 | | | | | | | APU_TSD_EN | PS_HOLD _DELAY |

X Not Used
(R/O) Bits are Read Only type.
 Codes other than those shown in the table are disallowed.

Note that for Serial Interface operation and thus register control, LDO2 must be active to provide the power for the internal logic.

LDO Output Voltage Programming

The following table summarizes the supported output voltages for the LP3918. Default voltages after startup are highlighted in **bold**.

TABLE 4.

| Data Code (Reg 01 - 07) | LDO1 V | LDO2 V | VLDO3 V | LDO4 V | LDO5 V | LDO6 V | LDO7 V |
|----------------------------|------------|------------|------------|------------|------------|------------|------------|
| 8h'00 | 1.5 | | | 1.5 | | | 1.5 |
| 8h'01 | 1.8 | | | 1.8 | | | 1.8 |
| 8h'02 | 1.85 | | | 1.85 | | | 1.85 |
| 8h'03 | 2.5 | 2.5 | | 2.5 | | | 2.5 |
| 8h'04 | 2.6 | 2.6 | | 2.6 | | | 2.6 |
| 8h'05 | 2.7 | 2.7 | 2.7 | 2.7 | 2.7 | 2.7 | 2.7 |
| 8h'06 | 2.75 | 2.75 | 2.75 | 2.75 | 2.75 | 2.75 | 2.75 |
| 8h'07 | 2.8 | 2.8 | 2.8 | 2.8 | 2.8 | 2.8 | 2.8 |
| 8h'08 | 2.85 | 2.85 | 2.85 | 2.85 | 2.85 | 2.85 | 2.85 |
| 8h'09 | 2.9 | 2.9 | 2.9 | 2.9 | 2.9 | 2.9 | 2.9 |
| 8h'0A | 2.95 | 2.95 | 2.95 | 2.95 | 2.95 | 2.95 | 2.95 |
| 8h'0B | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 |
| 8h'0C | 3.05 | 3.05 | 3.05 | 3.05 | 3.05 | 3.05 | 3.05 |
| 8h'0D | 3.1 | 3.1 | | 3.1 | | | 3.1 |
| 8h'0E | 3.2 | 3.2 | | 3.2 | | | 3.2 |
| 8h'0F | 3.3 | 3.3 | | 3.3 | | | 3.3 |

Charger Control Register 2

Note that Bits 7,6,5 are not used and must be set to 0 during write to this register.

CHARGER CURRENT PROGRAMMING

The following table summarizes the supported charging current values for the LP3918.

Default charge current after startup is highlighted in **bold**

TABLE 5. LP3918 Charger Current Programming

| Address | Register ID | Current Selection Prog_ICHG<4..0> Bit 0 to Bit 4 | | | | | | |
|---------|-------------|--|--------------|-------|-------|-------|-------|-------|
| 8h'11 | CHGCNTL2 | 00000 | 00001 | 00010 | 00011 | 00100 | 00101 | 00110 |
| | | 50mA | 100mA | 150mA | 200mA | 250mA | 300mA | 350mA |
| Address | Register ID | Current Selection Prog_ICHG<4..0> Bit 0 to Bit 4 | | | | | | |
| 8h'11 | CHGCNTL2 | 00111 | 01000 | 01001 | 01010 | 01011 | 01100 | 01101 |
| | | 400mA | 450mA | 500mA | 550mA | 600mA | 650mA | 700mA |
| Address | Register ID | Current Selection Prog_ICHG<4..0> Bit 0 to Bit 4 | | | | | | |
| 8h'11 | CHGCNTL2 | 01110 | 01111 | 10000 | 10001 | 10010 | | |
| | | 750mA | 800mA | 850mA | 900mA | 950mA | | |

Charger Control Register 3

CHARGER TERMINATION VOLTAGE PROGRAMMING

TABLE 6. LP3918 Charger Termination Voltage Control

| Address | Register ID | V_{TERM} Selection Bits | | |
|---------|-------------|---------------------------|-------------------------|------------------------|
| | | VTERM[1] CHGCNTL3<5> | VTERM[0] CHGCNTL3<4> | Termination Voltage(V) |
| 8h'12 | CHGCNTL3 | 0 | 0 | 4.1 |
| | | 0 | 1 | 4.2 (Default) |
| | | 1 | 0 | 4.3 |
| | | 1 | 1 | 4.4 |

END OF CHARGE CURRENT PROGRAMMING

TABLE 7. LP3918 EOC Current Control

| Address | Register ID | End Of Charge Current Selection Bits | | |
|---------|-------------|--------------------------------------|----------------------------|-----------------------|
| | | PROG_EOC[1] CHGCNTL3<3> | PROG_EOC[0] CHGCNTL3<2> | End Of Charge Current |
| 8h'12 | CHGCNTL3 | 0 | 0 | 0.1 (Default) |
| | | 0 | 1 | 0.15C |
| | | 1 | 0 | 0.2C |
| | | 1 | 1 | 0.25C |

CHARGING RESTART VOLTAGE PROGRAMMING

TABLE 8. LP3918 Charging Restart Voltage

| Address | Register ID | Charging Restart Voltage Selection Bits | | |
|---------|-------------|---|-------------------------------|--------------------------------------|
| | | PROG_VRSTRT[1] CHGCNTL3<1> | PROG_VRSTRT[0] CHGCNTL3<0> | Restart Voltage(V) |
| 8h'12 | CHGCNTL3 | 0 | 0 | $V_{TERM} - 50mV$ |
| | | 0 | 1 | $V_{TERM} - 100mV$ |
| | | 1 | 0 | $V_{TERM} - 150mV$ |
| | | 1 | 1 | $V_{TERM} - 200mV$ |

Charger Control Register 1

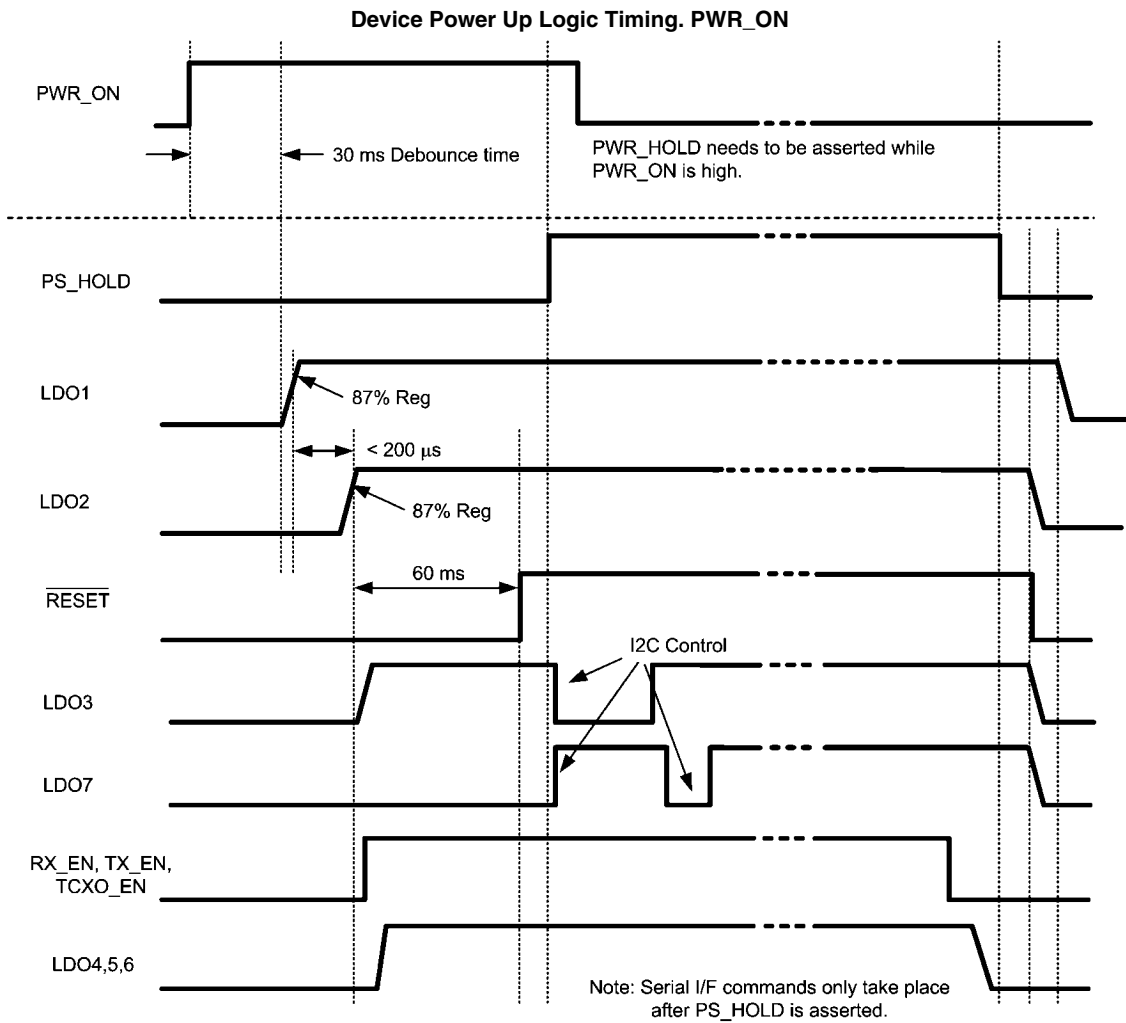
CHARGING MODE SELECTION

Charging mode selection changes will only take place when the battery voltage is above the 3.0V pre-charge/Full-rate charge threshold.

TABLE 9. LP3918 USB Charging Selection

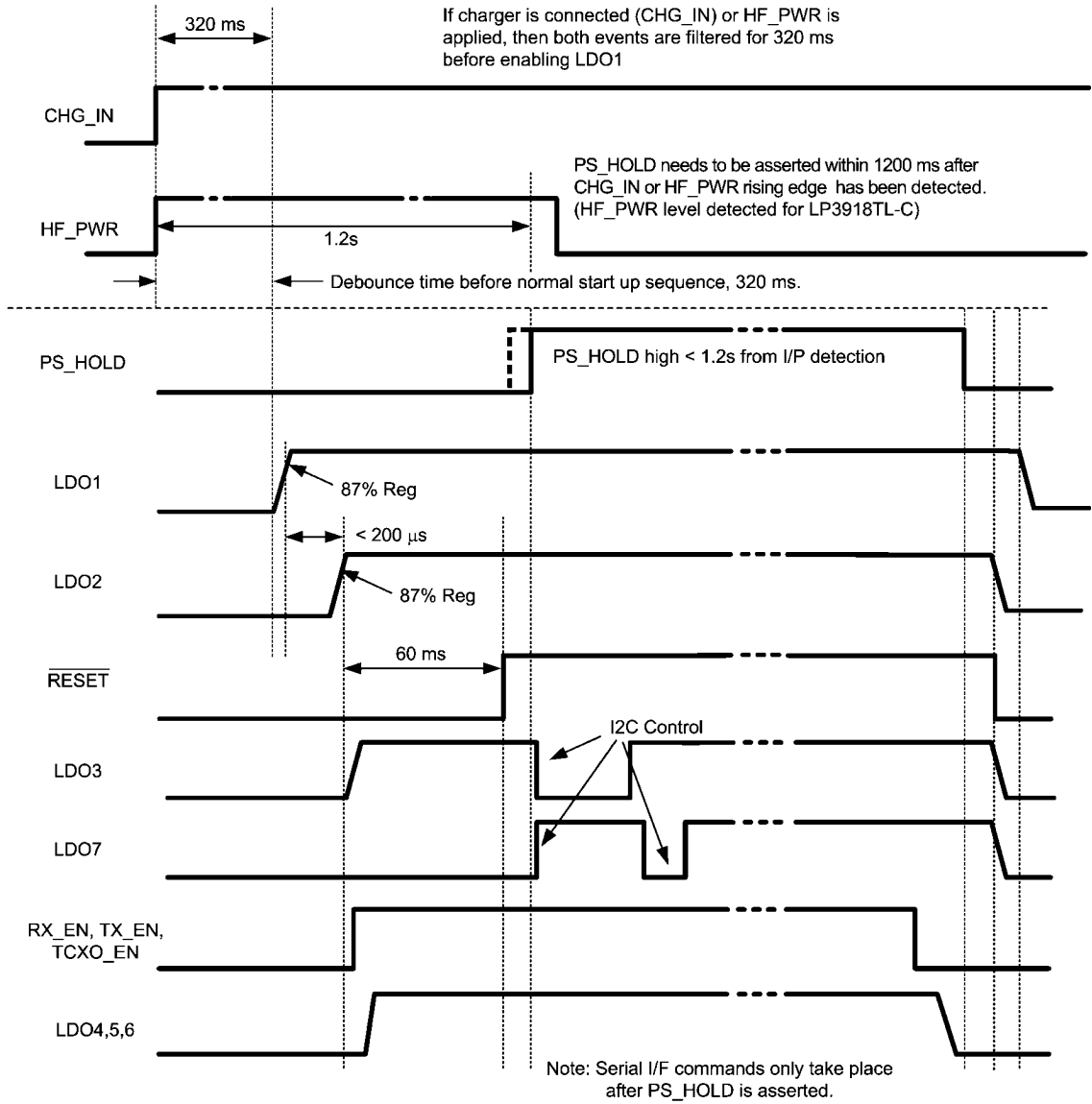
| Address | Register ID | USB Charge Mode Control Bits | | | |
|---------|-------------|------------------------------|----------------------------|-------------|----------------------|
| | | USB_Mode_En CHGCNTL1<7> | CHG_Mode_En CHGCNTL1<6> | Mode | Current |
| 8h'10 | CHGCNTL1 | 0 | 0 | Fast Charge | Default or Selection |
| | | 1 | 0 | Fast Charge | Default or Selection |
| | | 0 | 1 | USB | 100mA |
| | | 1 | 1 | USB | 450mA |

Device Power Up and Shutdown Timing



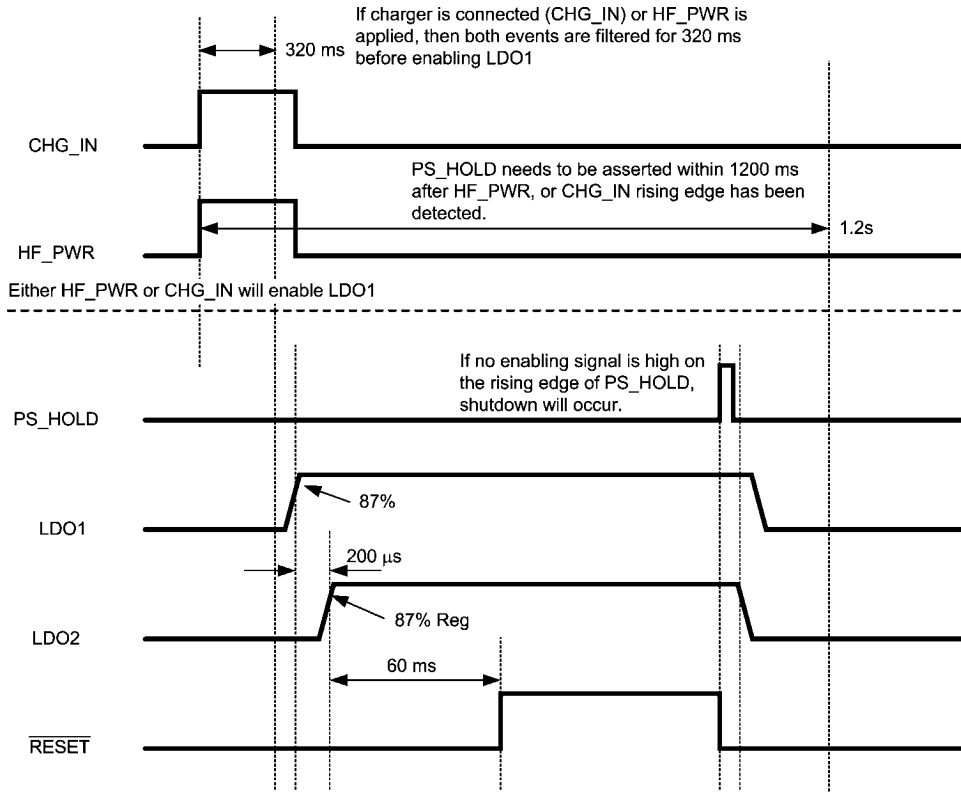
20211637

Device Power Up Logic Timing. CHG_IN, HF_PWR



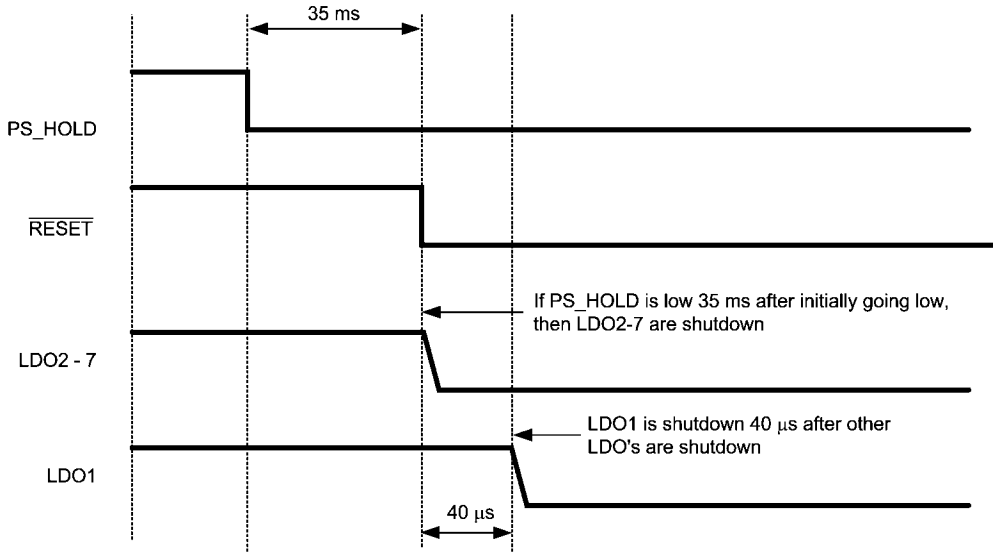
20211607

LP3918 Power On Behaviour (Failed PS_Hold)



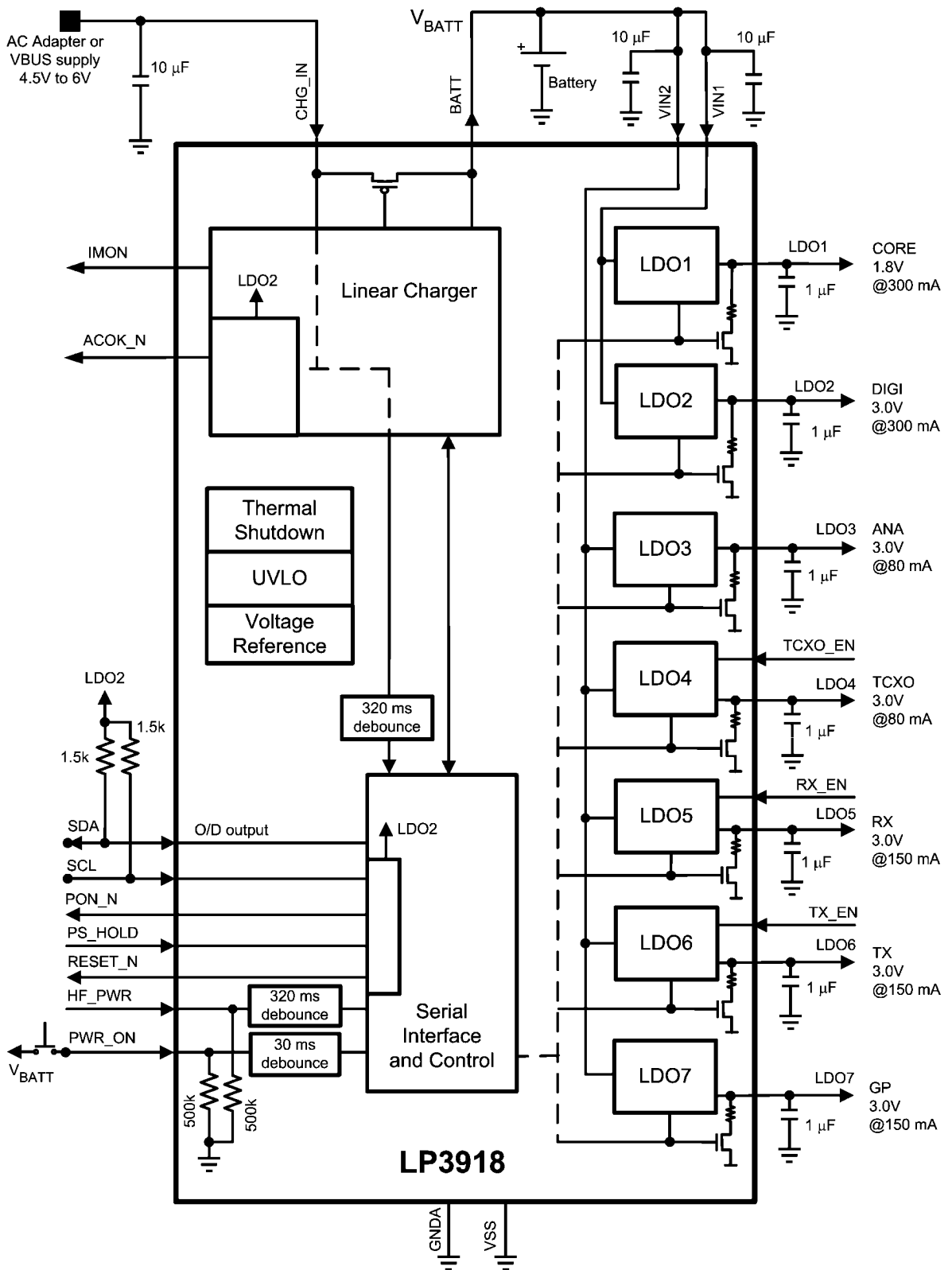
20211608

LP3918 Normal Shutdown Behaviour



20211633

Functional Block Diagram



LP3918 Functional Block Diagram

20211602

Technical Description

BATTERY CHARGE MANAGEMENT

A charge management system allowing the safe charge and maintenance of a Li-Ion battery is implemented on the LP3918. This has a CC/CV linear charge capability with programmable battery regulation voltage and end of charge current threshold. The charge current in the constant current mode is programmable and a maintenance mode monitors for battery voltage drop to restart charging at a preset level. A USB charging mode is also available with 2 charge current levels.

CHARGER FUNCTION

Following the correct detection of an input voltage at the charger pin the charger enters a pre-charge mode. In this mode a constant current of 50mA is available to charge the battery to 3.0V. At this voltage level the charge management applies the default (100mA) full rate constant current to raise the battery voltage to the termination voltage level (default 4.2V). The full rate charge current may be programmed to a different level at this stage. When termination voltage (V_{TERM}) is reached, the charger is in constant voltage mode and a constant voltage of 4.2V is maintained. This mode is complete when the end of charge current (default 0.1C) is detected and the charge management enters the maintenance mode. In maintenance mode the battery voltage is monitored for the restart level (4.05V at the default settings) and the charge cycle is re-initiated to re-establish the termination voltage level.

For start up the EOC function is disabled. This function should be enabled once start up is complete and a battery has been detected. EOC is enabled via register CHGCNTL1, *Table 10*.

The full rate constant current rate of charge may be programmed to 19 levels from 50mA to 950mA. These values are given in *Table 5*, and *Table 12*

The charge mode may be programmed to USB mode when the charger input is applied and the battery voltage is above 3.0V. This provides two programmable current levels of 100mA and 450mA for a USB sourced supply input at CHG_IN. *Table 9*

LDO Mode on device option LP3918TL-L

The charger circuit automatically enters an LDO mode if no battery is detected on insertion of the charger input voltage. In LDO mode the battery pin is regulated to 4.2V and can source up to 1.0A of current. Normal operation with a battery connected can be re-established via the serial interface. The serial interface allows the device to switch between modes as required however care is required to ensure that LDO mode is not initiated while a battery is present.

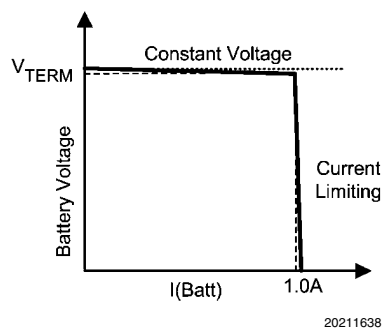


FIGURE 1. LDO Mode Diagram

EOC

EOC is disabled by default and should be enabled when the system processor is awake and the system detects that a battery is present.

Programming Information

TABLE 10. Register Address 8h'10: CHGCNTL1

| BIT | NAME | FUNCTION |
|-----|--------|---|
| 2 | En_EOC | Enables the End Of Charge current level threshold detection. When set to '0' the EOC is disabled. |

The End Of Charge current threshold default setting is at 0.1C. This EOC value is set relative to C the set full rate constant current. This threshold can be set to 0.1C, 0.15C, 0.2C or 0.25C by changing the contents of the PROG_EOC[1:0] register bits.

TABLE 11. Register Address 8h'12: CHGCNTL3

| BIT | NAME | FUNCTION |
|-----|-------------|--------------------------------|
| 2 | Prog_EOC[0] | Set the End Of Charge Current. |
| 3 | Prog_EOC[1] | See <i>Table 9</i> |

CHARGER FULL RATE CURRENT

Programming Information

TABLE 12. Register Address 8h'11: CHGCNTL2

| Data BITS | HEX | NAME | FUNCTION |
|------------|-----|-----------|----------|
| 000[00000] | 00 | Prog_ICHG | 50mA |
| 000[00001] | 01 | | 100mA |
| 000[00010] | 02 | | 150mA |
| 000[00011] | 03 | | 200mA |
| 000[00100] | 04 | | 250mA |
| 000[00101] | 05 | | 300mA |
| 000[00110] | 06 | | 350mA |
| 000[00111] | 07 | | 400mA |
| 000[01000] | 08 | | 450mA |
| 000[01001] | 09 | | 500mA |
| 000[01010] | 0A | | 550mA |
| 000[01011] | 0B | | 600mA |
| 000[01100] | 0C | | 650mA |
| 000[01101] | 0D | | 700mA |
| 000[01110] | 0E | | 750mA |
| 000[01111] | 0F | | 800mA |
| 000[10000] | 10 | 850mA | |
| 000[10001] | 11 | 900mA | |
| 000[10010] | 12 | 950mA | |

Charger Operation

The operation of the charger with EOC enabled is shown in this simplified flow diagram.

TERMINATION AND RESTART

The termination and restart voltage levels are determined by the data in the VTERM[1:0] and PROG_VSTRT[1:0] bits in the control register. The restart voltage is programmed relative to the selected termination voltage.

The Termination voltages available are 4.1V, 4.2V (default), 4.3V, and 4.4V.

The Restart voltages are determined relative to the termination voltage level and may be set to 50mV, 100mV, 150mV (default), and 200mV below the set termination voltage level.

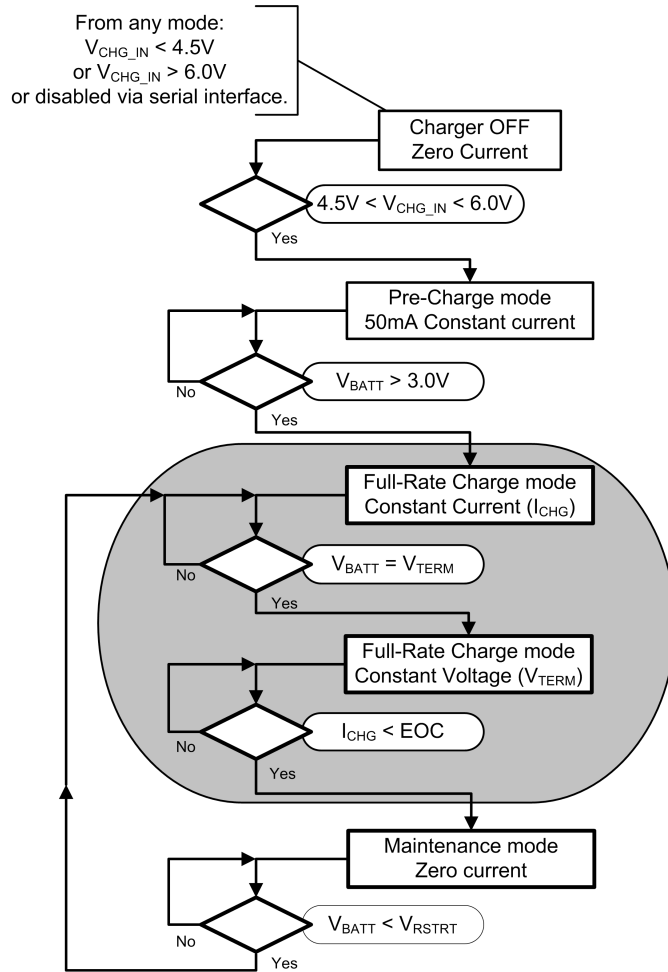
Programming Information

TABLE 13. Register Address 8h'12: CHGCNTL3

| BIT | NAME | FUNCTION |
|-----|----------|--|
| 4 | VTERM[0] | Set the charging termination voltage. See Table 6 |
| 5 | VTERM[1] | |

TABLE 14. Register Address 8h'12: CHGCNTL3

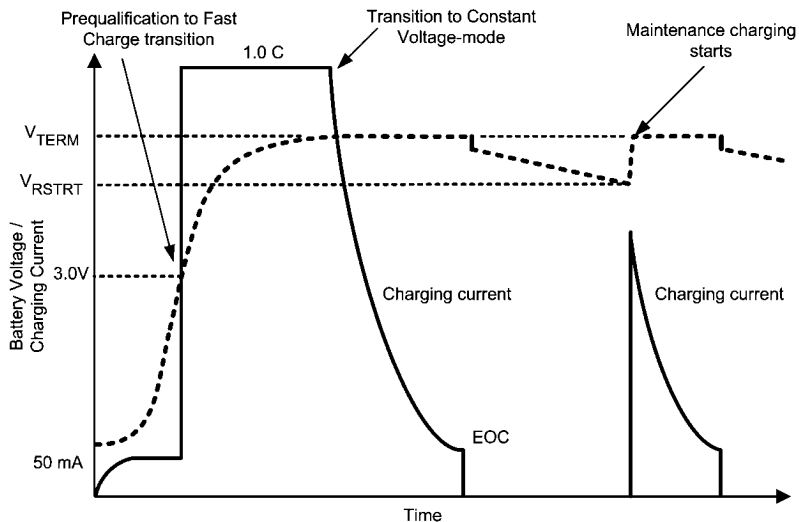
| BIT | NAME | FUNCTION |
|-----|-----------|--|
| 0 | VRSTRT[0] | Set the charging restart voltage. See Table 8 |
| 1 | VRSTRT[1] | |



20211636

FIGURE 2. Simplified Charger Functional Flow Diagram (EOC is enabled)

The charger operation may be depicted by the following graphical representation of the voltage and current profiles.



20211635

FIGURE 3. Charge Cycle Diagram

Further Charger Register Information
Charger Control Register 1

TABLE 15. Register Address 8h'10: CHGCNTL1

| BIT | NAME | FUNCTION (if bit = '1') |
|-----|---------------|--|
| 7 | USB_MODE_EN | Sets the Current Level in USB mode. |
| 6 | CHG_MODE_EN | Forces the charger into USB mode when active high. If low, charger is in normal charge mode. |
| 5 | FORCE_EOC | Forces an EOC event. |
| 4 | TOUT_Doubling | Doubles the timeout delays for all timeout signals. |
| 3 | EN_Tout | Enables the timeout counters. When set to '0' the timeout counters are disabled. |
| 2 | EN_EOC | Enables the End of Charge current level threshold detection. When set to '0' the functions are disabled. |
| 1 | Set_LDOfmode | Forces the charger into LDO mode. Function available on LP3918TL_L. |
| 0 | EN_CHG | Charger enable. |

Charger Status Register 1 Read only

TABLE 16. Register Address 8h'13: CHGSTATUS1

| BIT | NAME | FUNCTION (if bit = '1') |
|-----|----------------|--|
| 7 | BAT_OVER_OUT | Is set when battery voltage exceeds 4.7V. |
| 6 | CHGIN_OK_Out | Is set when a valid input voltage is detected at CHG_IN pin. |
| 5 | EOC | Is set when the charging current decreases below the programmed End Of Charge level. |
| 4 | Tout_Fullrate | Set after timeout on full rate charge. |
| 3 | Tout_Precharge | Set after timeout for precharge mode. |
| 2 | LDO_Mode | Only available on LP3918TL_L. |
| 1 | Fullrate | Set when the charger is in CC/CV mode. |
| 0 | PRECHG | Set during precharge. |

Charger Status Register 2 Read only

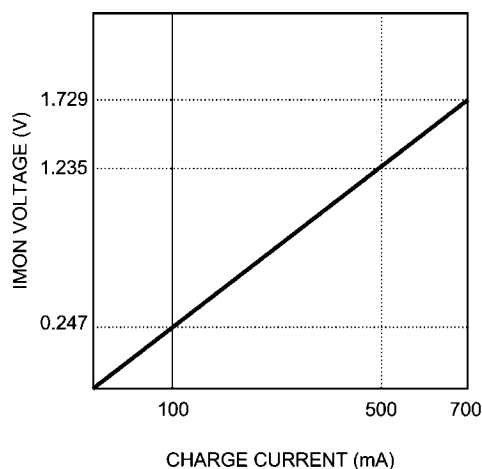
TABLE 17. Register Address 8h'13: CHGSTATUS2

| BIT | NAME | FUNCTION (if bit = '1') |
|-----|-------------|--------------------------------|
| 1 | Tout_ConstV | Set after timeout in CV phase. |
| 0 | BAD_BATT | Set at bad battery state. |

IMON CHARGE CURRENT MONITOR

Charge current is monitored within the charger section and a proportional voltage representation of the charge current is presented at the IMON output pin. The output voltage relationship to the actual charge current is represented in the following graph and by the equation:

$$V_{\text{IMON}}(\text{mV}) = (2.47 \times I_{\text{CHG}})(\text{mA})$$



20211611

FIGURE 4. IMON Voltage vs Charge Current

Note that this function is not available if there is no input at CHG_IN or if the charger is off due to the input at CHG_IN being outwith the operating voltage range.

LDO Information

OPERATIONAL INFORMATION

The LP3918 has 7 LDO's of which 3 are enabled by default, LDO's 1,2 and 3 are powered up during the power up sequence. LDO4, 5 and 6 are separately, externally enabled and will follow LDO2 in start up if their respective enable pin is pulled high. LDO2, LDO3 and LDO7 can be enabled/disabled via the serial interface.

LDO2 must remain in regulation otherwise the device will power down. While LDO1 is enabled this must also be in regulation for the device to remain powered. If LDO1 is disabled via I2C interface the device will not shut down.

INPUT VOLTAGES

There are two input voltage pins used to power the 7LDO's on the LP3918. $V_{\text{IN}2}$ is the supply for LDO3, LDO4, LDO5, LDO6 and LDO7. $V_{\text{IN}1}$ is the supply for LDO1 and LDO2. These input voltages should be tied to the Batt pin in the application.

PROGRAMMING INFORMATION

Enable via Serial Interface

TABLE 18. Register Address 8h'00: OP_EN

| BIT | NAME | FUNCTION |
|-----|---------|-------------------------------|
| 0 | LDO1_EN | Bit set to '0' - LDO disabled |
| 2 | LDO3_EN | Bit set to '1' - LDO enabled |
| 3 | LDO7_EN | |

Note that the default setting for this Register is [0000 0101]. This shows that LDO1 and 3 are enabled by default whereas LDO7 is not enabled by default on start up.

LDO OUTPUT PROGRAMMING

TABLE 19.

| Register Add (hex) | NAME | Data Range (hex) | Output Voltage |
|--------------------|----------------|------------------|-----------------------------|
| 01 | LDO1PGM O/P | 03 - 0F | 1.5V to 3.3V (def. 1.8V) |
| 02 | LDO2PGM O/P | 00 - 0F | 2.5V to 3.3V (def 3.0V) |
| 03 | LDO3PGM O/P | 05 - 0C | 2.7V to 3.05V (def 3.0V) |
| 04 | LDO4PGM O/P | 00 - 0F | 1.5V to 3.3V (def 3.0V) |
| 05 | LDO5PGM O/P | 05 - 0C | 2.7V to 3.05V (def 3.0V) |
| 06 | LDO6PGM O/P | 05 - 0C | 2.7V to 3.05V (def 3.0V) |
| 07 | LDO7PGM O/P | 00 - 0F | 1.5V to 3.3V (def 3.0V) |

See Table 2 for full programmable range of values.

EXTERNAL CAPACITORS

The Low Drop Out Linear Voltage regulators on the LP3918 require external capacitors to ensure stable outputs. The LDO's on the LP3918 are specifically designed to use small surface mount ceramic capacitors which require minimum board space. These capacitors must be correctly selected for good performance

INPUT CAPACITOR

Input capacitors are required for correct operation. It is recommended that a 10 μ F capacitor be connected between each of the voltage input pins and ground (this capacitance value may be increased without limit). This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analogue ground. A ceramic capacitor is recommended although a good quality tantalum or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have surge current rating sufficient for the application. There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain within its operational range over the entire operating temperature range and conditions.

Output Capacitor

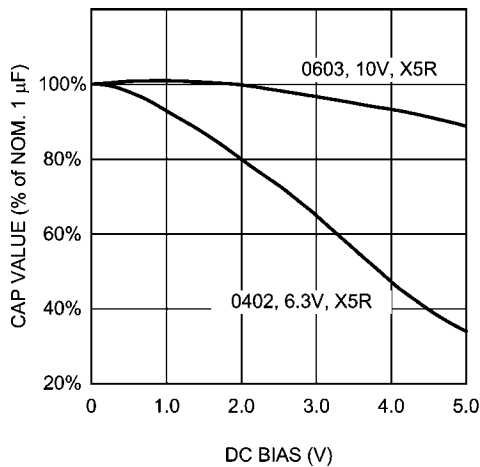
Correct selection of the output capacitor is critical to ensure stable operation in the intended application. The output capacitor must meet all the requirements specified in the recommended capacitor table over all conditions in the application. These conditions include DC-bias, frequency and temperature. Unstable operation will result if the capacitance

drops below the minimum specified value. The LP3918 is designed specifically to work with very small ceramic output capacitors. The LDO's on the LP3918 are specifically designed to be used with X7R and X5R type capacitors. With these capacitors selection of the capacitor for the application is dependant on the range of operating conditions and temperature range for that application. (See section on Capacitor Characteristics). It is also recommended that the output capacitor be placed within 1cm from the output pin and returned to a clean ground line.

Capacitor Characteristics

The LDO's on the LP3918 are designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values around 1µF, ceramic capacitors give the circuit designer the best design options in terms of low cost and minimal area. For both input and output capacitors careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly dependant on the conditions of operation and capacitor type. In particular to ensure stability, the output capacitor selection should take account of all the capacitor parameters to ensure that the specification is met within the application. Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller sizes giving poorer performance figures in general.

As an example *Figure 5* shows a typical graph showing a comparison of capacitor case sizes in a Capacitance vs DC Bias plot. As shown in the graph, as a result of DC Bias condition the capacitance value may drop below minimum capacitance value given in the recommended capacitor table (0.7µF in this case). Note that the graph shows the capacitance out of spec for 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers specifications for the nominal value capacitor are consulted for all conditions as some capacitor sizes (e.g 0402) may not be suitable in the actual application. Ceramic capacitors have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1µF ceramic capacitor is in the range of 20mΩ to 40mΩ, and also meets the ESR requirements for stability. The temperature performance of ceramic capacitors varies by type. Capacitor type X7R is specified with a tolerance of ±15% over temperature range -55°C to +125°C. The X5R has similar tolerance over the reduced temperature range -55°C to +85°C. Most large value ceramic capacitors (<2.2µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C. Therefore X7R is recommended over these other capacitor types in applications where the temperature will change significantly above or below 25°C.



20211612

FIGURE 5. Graph Showing A Typical Variation in Capacitance vs DC Bias

No-Load Stability

The LDO's on the LP3918 will remain stable in regulation with no external load.

TABLE 20. LDO Output Capacitors Recommended Specification

| Symbol | Parameter | Capacitor Type | Typ | Limit | | Units |
|----------------------|-------------|----------------|-----|-------|-----|-------|
| | | | | Min | Max | |
| C _{o(LDO1)} | Capacitance | X5R. X74 | 1.0 | 0.7 | 2.2 | μF |
| C _{o(LDO2)} | Capacitance | X5R. X74 | 1.0 | 0.7 | 2.2 | μF |
| C _{o(LDO3)} | Capacitance | X5R. X74 | 1.0 | 0.7 | 2.2 | μF |
| C _{o(LDO4)} | Capacitance | X5R. X74 | 1.0 | 0.7 | 2.2 | μF |
| C _{o(LDO5)} | Capacitance | X5R. X74 | 1.0 | 0.7 | 2.2 | μF |
| C _{o(LDO6)} | Capacitance | X5R. X74 | 1.0 | 0.7 | 2.2 | μF |
| C _{o(LDO7)} | Capacitance | X5R. X74 | 1.0 | 0.7 | 2.2 | μF |

Note: The capacitor tolerance should be 30% or better over the full temperature range. X7R or X5R capacitors should be used. These specifications are given to ensure that the capacitance remains within these values over all conditions within the application. See Capacitor Characteristics section in Application Information.

Thermal Shutdown

The LP3918 has internal limiting for high on-chip temperatures caused by high power dissipation etc. This Thermal Shutdown, TSD, function monitors the temperature with respect to a threshold and results in a device power-down.

If the threshold of +160°C has been exceeded then the device will power down. Recovery from this TSD event can only be initiated after the chip has cooled below +115°C. This device recovery is controlled by the APU_TSD_EN bit (bit 1) in control register MISC, 8h'1C. See *Table 22* If the APU_TSD_EN is set low then the device will shutdown requiring a new start up event initiated by PWR_ON, HF_PWR, or CHG_IN. If APU_TSD_EN is set high then the device will power up automatically when the shutdown condition clears. In this case the control register settings are preserved for the device restart.

The threshold temperature for the device to clear this TSD event is 115°C. This threshold applies for any start up thus the device temperature must be below this threshold to allow a start up event to initiate power up.

Further Register Information

STATUS REGISTER READ ONLY

TABLE 21. Register Address 8h'0C: Status

| BIT | NAME | FUNCTION (if bit = '1') |
|-----|-------------|--------------------------------------|
| 7 | PWR_ON_TRIG | PMU start up is initiated by PWR_ON. |
| 6 | HF_PWR_TRIG | PMU start up is initiated by HF_PWR. |
| 5 | CHG_IN_TRIG | PMU start up is initiated by CHG_IN. |

Bits <4..0> are not used.

MISC CONTROL REGISTER

TABLE 22. Register Address 8h'1C: Misc

| BIT | NAME | FUNCTION (if bit = '1') |
|-----|----------------|---|
| 1 | APU_TSD_EN | 1b'0: Device will shutdown completely if thermal shutdown occurs. Requires a new start up event to restart the PMU. 1b'1: Device will start up automatically after thermal shutdown condition is removed. (Device tries to keep its internal state.) |
| 0 | PWR_HOLD_DELAY | 1b'0: If PWR_HOLD is low for 35ms the device will shutdown. (Default) 1b'1: If PWR_HOLD is low for 350ms the device will shutdown. |

Bits <7..2> are not used.

I²C Compatible Serial Bus Interface

INTERFACE BUS OVERVIEW

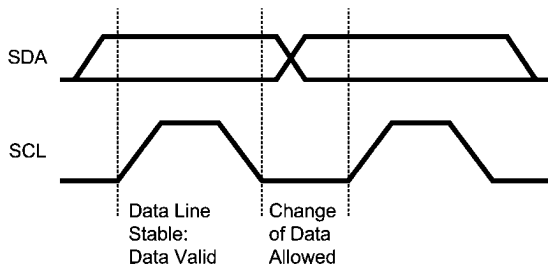
The I²C compatible synchronous serial interface provides access to the programmable functions and registers on the device.

This protocol uses a two-wire interface for bi-directional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pull-up resistor of 1.5KΩ, and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock (SCL).

DATA TRANSACTIONS

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.



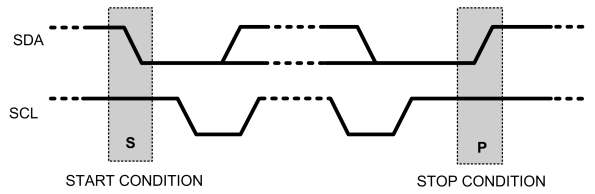
20211613

FIGURE 6. Bit Transfer

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

START AND STOP

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.



20211610

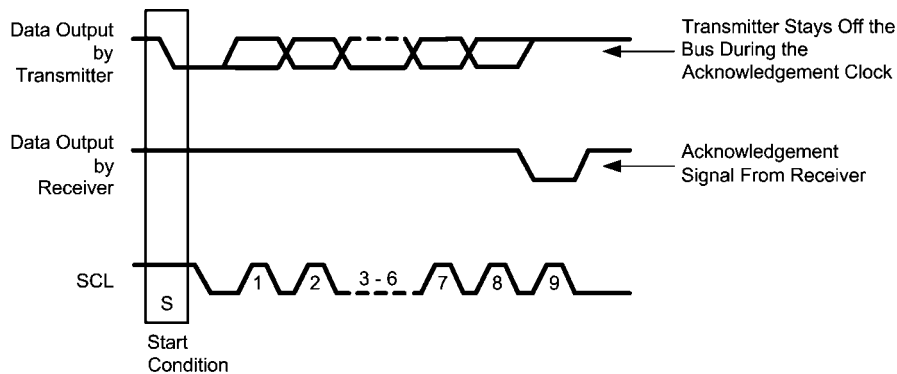
FIGURE 7. Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

ACKNOWLEDGE CYCLE

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.



20211628

FIGURE 8. Bus Acknowledge Cycle

“ACKNOWLEDGE AFTER EVERY BYTE” RULE

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the “acknowledge after every byte” rule.

When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

ADDRESSING TRANSFER FORMATS

Each device on the bus has a unique slave address. The LP3918 operates as a slave device with the address 7h7E

(binary 1111110). Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

CONTROL REGISTER WRITE CYCLE

- Master device generates start condition.

- Master device sends slave address (7 bits) and the data direction bit (r/w = "0").
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

CONTROL REGISTER READ CYCLE

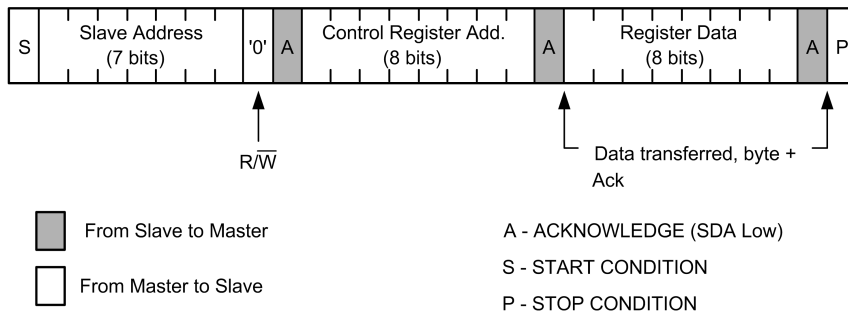
- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = "0").
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = "1").
- Slave sends acknowledge signal if the slave address is correct.

- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

| | Address Mode |
|------------|--|
| Data Read | <Start Condition> <Slave Address><r/w = '0'>[Ack] <Register Addr.>[Ack] <Repeated Start Condition> <Slave Address><r/w = '1'>[Ack] [Register Data]<Ack or nAck> ... additional reads from subsequent register address possible <Stop Condition> |
| Data Write | <Start Condition> <Slave Address><r/w = '0'>[Ack] <Register Addr.>[Ack] <Register Data>[Ack] ... additional writes to subsequent register address possible <Stop Condition> |

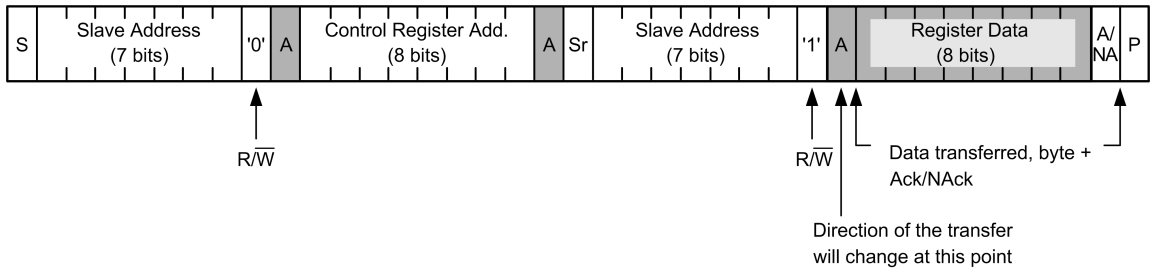
< > Data from master [] Data from slave

REGISTER READ AND WRITE DETAIL



20211629

FIGURE 9. Register Write Format



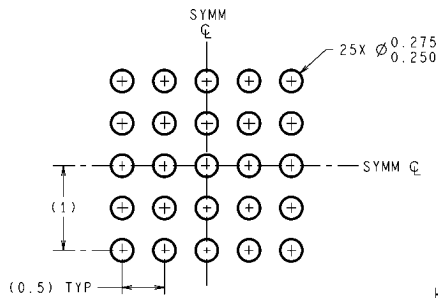
From Slave to Master
 From Master to Slave

A - ACKNOWLEDGE (SDA Low)
 NA - ACKNOWLEDGE (SDA High)
 S - START CONDITION
 Sr - REPEATED START CONDITION
 P - STOP CONDITION

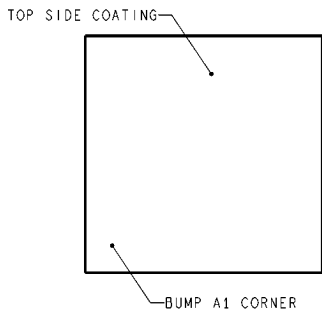
20211630

FIGURE 10. Register Read Format

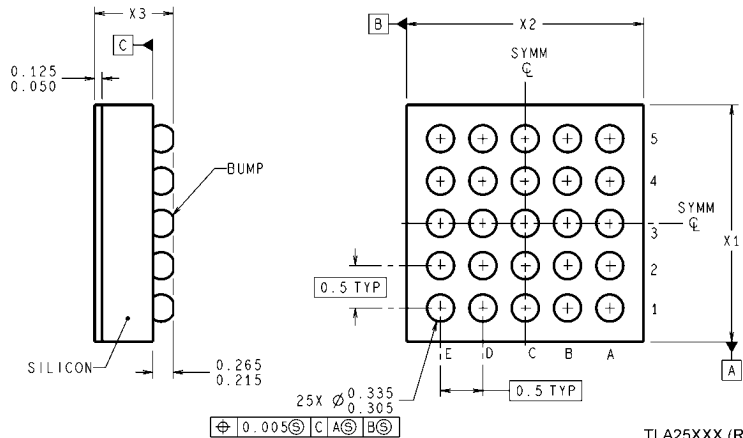
Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



TLA25XXX (Rev D)

Thin micro-SMD25 Package
NS Package Number MKT-TLA2511A
X1 = 2.465mm ± 0.030mm
X2 = 2.465mm ± 0.030mm
X3 = 0.600mm ± 0.075mm

Notes

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2007 National Semiconductor Corporation

For the most current product information visit us at www.national.com



National Semiconductor Americas Customer Support Center
 Email: new.feedback@nsc.com
 Tel: 1-800-272-9959

National Semiconductor Europe Customer Support Center
 Fax: +49 (0) 180-530-85-86
 Email: europe.support@nsc.com
 Deutsch Tel: +49 (0) 69 9508 6208
 English Tel: +49 (0) 870 24 0 2171
 Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Support Center
 Email: ap.support@nsc.com

National Semiconductor Japan Customer Support Center
 Fax: 81-3-5639-7507
 Email: jpn.feedback@nsc.com
 Tel: 81-3-5639-7560