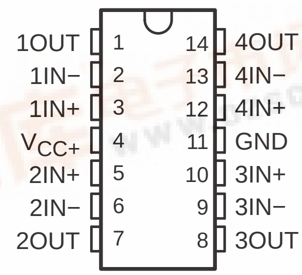
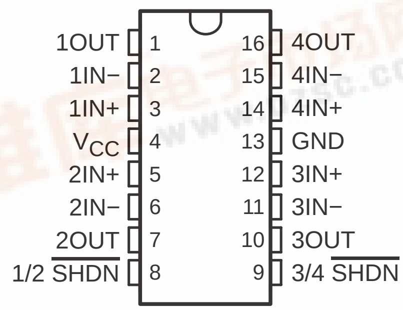
- **2.7-V and 5-V Performance**
- **−40°C to 125°C Operation**
- **Low-Power Shutdown Mode (LMV324S)**
- **No Crossover Distortion**
- **Low Supply Current**
  - **LMV321 . . . 130 μA Typ**
  - **LMV358 . . . 210 μA Typ**
  - **LMV324 . . . 410 μA Typ**
  - **LMV324S . . . 410 μA Typ**
- **Rail-to-Rail Output Swing**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **1000-V Charged-Device Model (C101)**

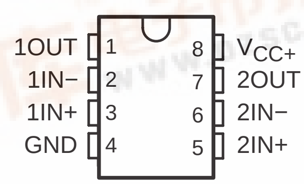
LMV324 . . . D (SOIC) OR PW (TSSOP) PACKAGE (TOP VIEW)



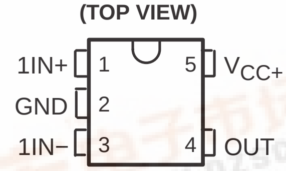
LMV324S . . . D (SOIC) OR PW (TSSOP) PACKAGE (TOP VIEW)



LMV358 . . . D (SOIC), DDU (VSSOP), DGK (MSOP), OR PW (TSSOP PACKAGE (TOP VIEW)



LMV321 . . . DBV (SOT-23) OR DCK (SC-70) PACKAGE (TOP VIEW)



description/ordering information

The LMV321, LMV358, and LMV324/LMV324S are single, dual, and quad low-voltage (2.7 V to 5.5 V), operational amplifiers with rail-to-rail output swing. The LMV324S, which is a variation of the standard LMV324, includes a power-saving shutdown feature that reduces supply current to a maximum of 5 μA per channel when the amplifiers are not needed. Channels 1 and 2 together are put in shutdown, as are channels 3 and 4. While in shutdown, the outputs actively are pulled low.

The LMV321, LMV358, LMV324, and LMV324S are the most cost-effective solutions for applications where low-voltage operation, space saving, and low cost are needed. These amplifiers were designed specifically for low-voltage (2.7 V to 5 V) operation, with performance specifications meeting or exceeding the LM358 and LM324 devices that operate from 5 V to 30 V. Additional features of the LMV3xx devices are a common-mode input voltage range that includes ground, 1-MHz unity-gain bandwidth, and 1-V/μs slew rate.

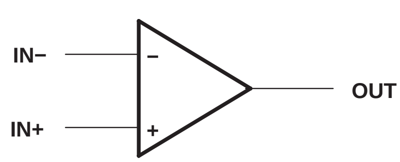
The LMV321 is available in the ultra-small DCK (SC-70) package, which is approximately one-half the size of the DBV (SOT-23) package. This package saves space on printed circuit boards and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

ORDERING INFORMATION

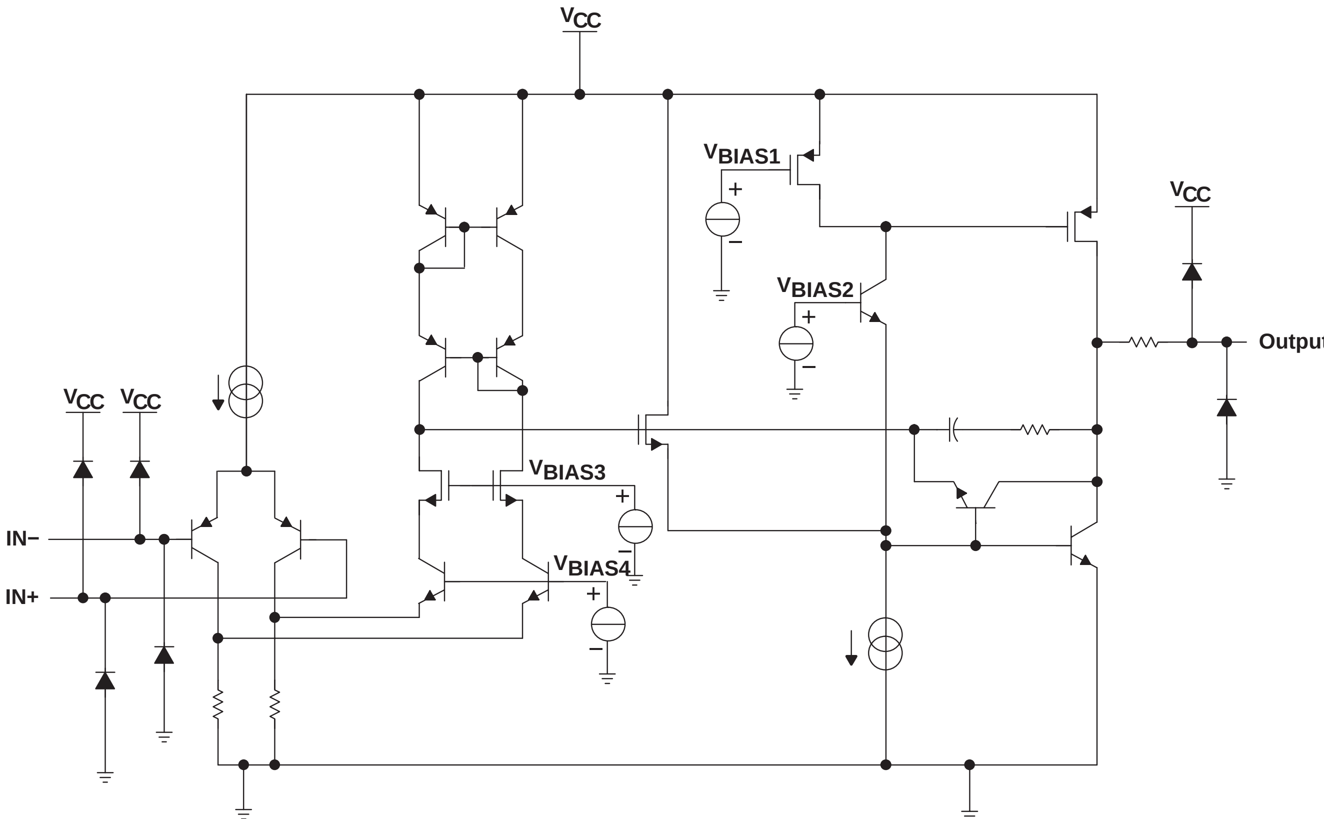
T_A		PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	Single	SC-70 (DCK)	Reel of 3000	LMV321IDCKR	R3_
			Reel of 250	LMV321IDCKT	
		SOT23-5 (DBV)	Reel of 3000	LMV321IDBVR	RC1_
			Reel of 250	LMV321IDBVT	
	Dual	MSOP/VSSOP (DGK)	Reel of 2500	LMV358IDGKR	R5_
			Reel of 250	LMV358IDGKT	PREVIEW
		SOIC (D)	Tube of 75	LMV358ID	MV358I
			Reel of 2500	LMV358IDR	
		TSSOP (PW)	Tube of 150	LMV358IPW	MV358I
			Reel of 2000	LMV358IPWR	
		VSSOP (DDU)	Reel of 3000	LMV358IDDUR	RA56
	Quad	SOIC (D)	Tube of 50	LMV324ID	LMV324I
			Reel of 2500	LMV324IDR	
			Tube of 40	LMV324SID	LMV324SI
			Reel of 2500	LMV324SIDR	
		TSSOP (PW)	Reel of 2000	LMV324IPWR	MV324I
				LMV324SIPWR	MV324SI
−40°C to 125°C	Dual	MSOP/VSSOP (DGK)	Reel of 2500	LMV358QDGKR	RH_
			Reel of 250	LMV358QDGKT	
		SOIC (D)	Tube of 75	LMV358QD	MV358Q
			Reel of 2500	LMV358QDR	
		TSSOP (PW)	Tube of 150	LMV358QPW	MV358Q
			Reel of 2000	LMV358QPWR	
		VSSOP (DDU)	Reel of 3000	LMV358QDDUR	RAH_
	Quad	SOIC (D)	Tube of 50	LMV324QD	LMV324Q
			Reel of 2500	LMV324QDR	
		TSSOP (PW)	Tube of 90	LMV324QPW	MV324Q
			Reel of 2000	LMV324QPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
‡ DBV/DCK/DGK: The actual top-side marking has one additional character that designates the assembly/test site.

symbol (each amplifier)



LMV324 simplified schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . 5.5 V
Differential input voltage, V_{ID} (see Note 2) . . . ±5.5 V
Input voltage, V_I (either input) . . . 0 to 5.5 V
Duration of output short circuit (one amplifier) to ground at (or below) T_A = 25°C,
$V_{CC} \leq 5.5$ V (see Note 3) . . . Unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5):
- D (8-pin) package . . . 97°C/W
- D (14-pin) package . . . 86°C/W
- D (16-pin) package . . . 73°C/W
- DBV (5-pin) package . . . 206°C/W
- DCK (5-pin) package . . . 252°C/W
- DDU (8-pin) package . . . TBD°C/W
- DGK (8-pin) package . . . 172°C/W
- PW (8-pin) package . . . 149°C/W
- PW (14-pin) package . . . 113°C/W
- PW (16-pin) package . . . 108°C/W

Operating virtual junction temperature, T_J . . . 150°C
Storage temperature range, T_{stg} . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
2. Differential voltages are at IN+ with respect to IN−.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage (single-supply operation)		2.7	5.5	V
V_{IH}	Amplifier turnon voltage level (LMV324S)‡	V_{CC} = 2.7 V	1.7		V
		V_{CC} = 5 V	3.5		
V_{IL}	Amplifier turnoff voltage level (LMV324S)	V_{CC} = 2.7 V		0.7	V
		V_{CC} = 5 V		1.5	
T_A	Operating free-air temperature	I-Temp	−40	85	°C
		Q-Temp	−40	125	

‡ V_{IH} should not be allowed to exceed V_{CC}.

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics at T_A = 25°C and V_{CC+} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage				1.7	7	mV
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage				5		μV/°C
I_{IB}	Input bias current				11	250	nA
I_{IO}	Input offset current				5	50	nA
CMRR	Common-mode rejection ratio	V_{CM} = 0 to 1.7 V		50	63		dB
k_{SVR}	Supply-voltage rejection ratio	V_{CC} = 2.7 V to 5 V, V_O = 1 V		50	60		dB
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		0 to 1.7	−0.2 to 1.9		V
	Output swing	R_L = 10 kΩ to 1.35 V	High level	V_{CC} − 100	V_{CC} − 10		mV
			Low level		60	180	
I_{CC}	Supply current	LMV321I			80	170	μA
		LMV358I (both amplifiers)			140	340	
		LMV324I/LMV324SI (all four amplifiers)			260	680	
B_1	Unity-gain bandwidth	C_L = 200 pF			1		MHz
Φ_m	Phase margin				60		deg
G_m	Gain margin				10		dB
V_n	Equivalent input noise voltage	f = 1 kHz			46		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz			0.17		pA/√Hz

shutdown characteristics (LMV324S) at T_A = 25°C and V_{CC+} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode (per channel)	$\overline{SHDN}$ ≤ 0.6 V			5	μA
$t_{(on)}$	Amplifier turnon time	A_V = 1, R_L = Open (measured at 50% point)		2		μs
$t_{(off)}$	Amplifier turnoff time	A_V = 1, R_L = Open (measured at 50% point)		40		ns

electrical characteristics at specified free-air temperature range, V_{CC+} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage			25°C		1.7	7	mV
				Full range			9	
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage			25°C		5		μV/°C
I_{IB}	Input bias current			25°C		15	250	nA
				Full range			500	
I_{IO}	Input offset current			25°C		5	50	nA
				Full range			150	
CMRR	Common-mode rejection ratio	V_{CM} = 0 to 4 V		25°C	50	65		dB
k_{SVR}	Supply-voltage rejection ratio	V_{CC}= 2.7 V to 5 V, V_O = 1 V, V_{CM} = 1 V		25°C	50	60		dB
V_{ICR}	Common-mode input voltage range	CMMR ≥ 50 dB		25°C	0 to 4	−0.2 to 4.2		V
	Output swing	R_L = 2 kΩ to 2.5 V	High level	25°C	V_{CC} − 300	V_{CC} − 40		mV
				Full range	V_{CC} − 400			
			Low level	25°C		120	300	
				Full range			400	
		R_L = 10 kΩ to 2.5 V	High level	25°C	V_{CC} − 100	V_{CC} − 10		
				Full range	V_{CC} − 200			
			Low level	25°C		65	180	
				Full range			280	
A_{VD}	Large-signal differential voltage gain	R_L = 2 kΩ		25°C	15	100		V/mV
				Full range	10			
I_{OS}	Output short-circuit current	Sourcing, V_O = 0 V		25°C	5	60		mA
		Sinking, V_O = 5 V			10	160		
I_{CC}	Supply current	LMV321I		25°C		130	250	μA
				Full range			350	
		LMV358I (both amplifiers)		25°C		210	440	
				Full range			615	
		LMV324I/LMV324SI (all four amplifiers)		25°C		410	830	
				Full range			1160	
B_1	Unity-gain bandwidth	C_L = 200 pF		25°C		1		MHz
Φ_m	Phase margin			25°C		60		deg
G_m	Gain margin			25°C		10		dB
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		39		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.21		pA/√Hz
SR	Slew rate			25°C		1		V/μs

† Full range: −40°C to 85°C for I-temp, −40°C to 125°C for Q-temp.

shutdown characteristics (LMV324S) at T_A = 25°C and V_{CC+} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode (per channel)	$\overline{SHDN}$ ≤ 0.6 V	−40°C to 85°C			5	μA
$t_{(on)}$	Amplifier turnon time	A_V = 1, R_L = Open (measured at 50% point)			2		μs
$t_{(off)}$	Amplifier turnoff time	A_V = 1, R_L = Open (measured at 50% point)			40		ns

TYPICAL CHARACTERISTICS

LMV321 FREQUENCY RESPONSE vs RESISTIVE LOAD

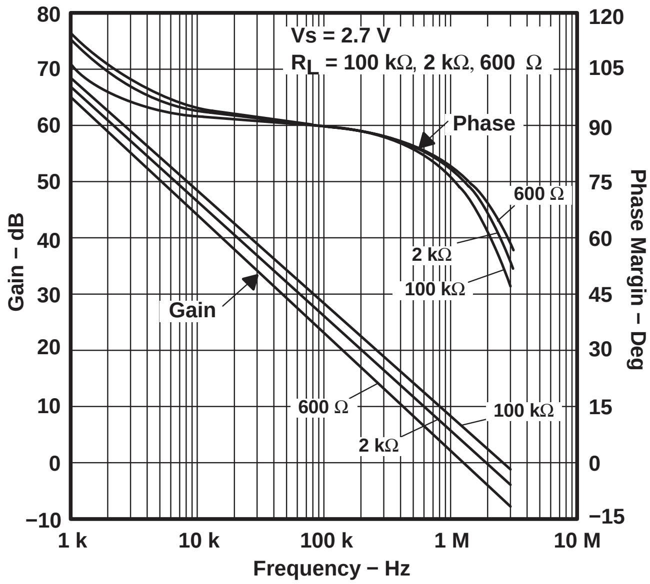


Figure 1

LMV321 FREQUENCY RESPONSE vs RESISTIVE LOAD

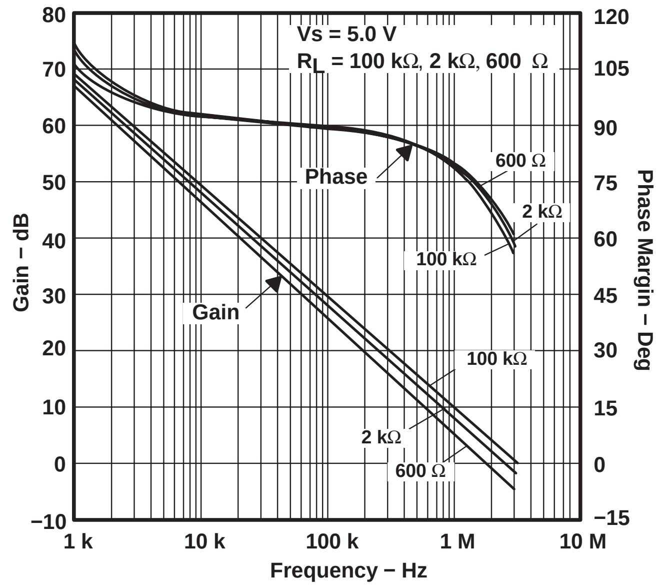


Figure 2

LMV321 FREQUENCY RESPONSE vs CAPACITIVE LOAD

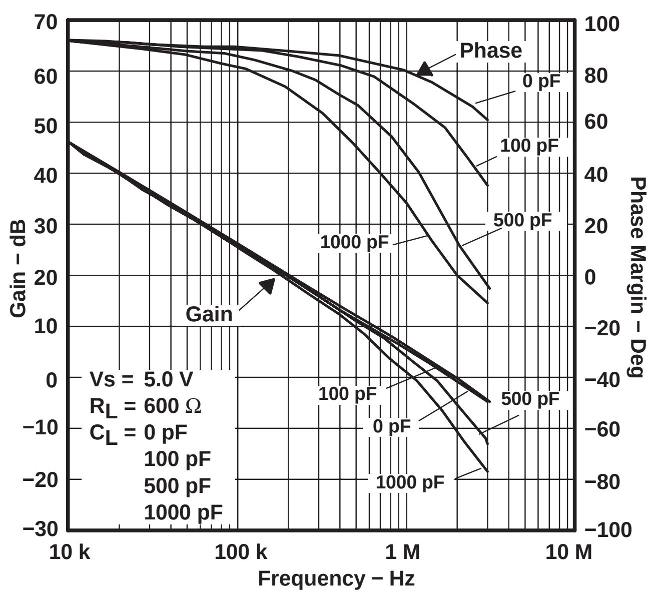


Figure 3

LMV321 FREQUENCY RESPONSE vs CAPACITIVE LOAD

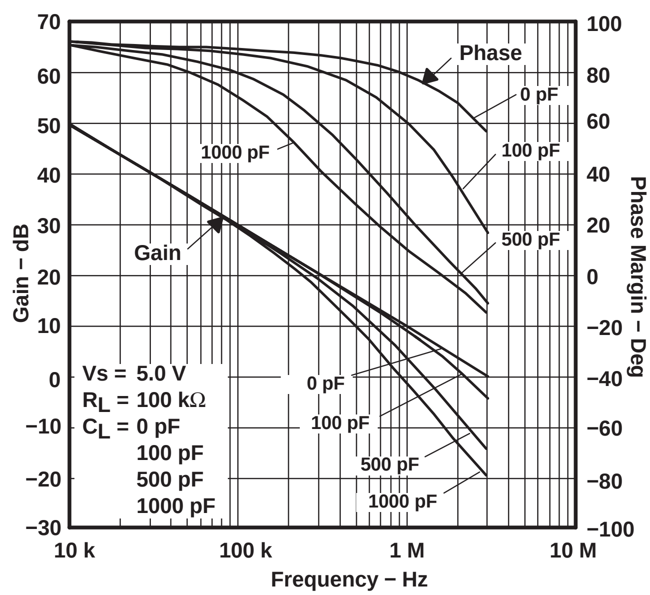


Figure 4

TYPICAL CHARACTERISTICS

LMV321 FREQUENCY RESPONSE vs TEMPERATURE

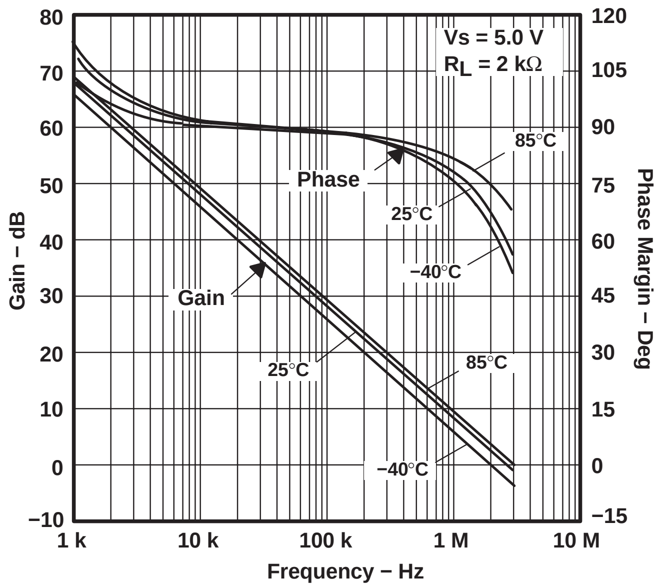


Figure 5

STABILITY vs CAPACITIVE LOAD

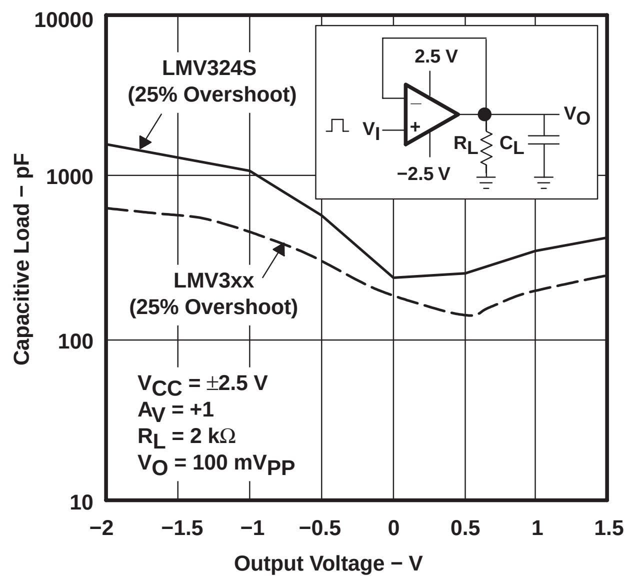


Figure 6

STABILITY vs CAPACITIVE LOAD

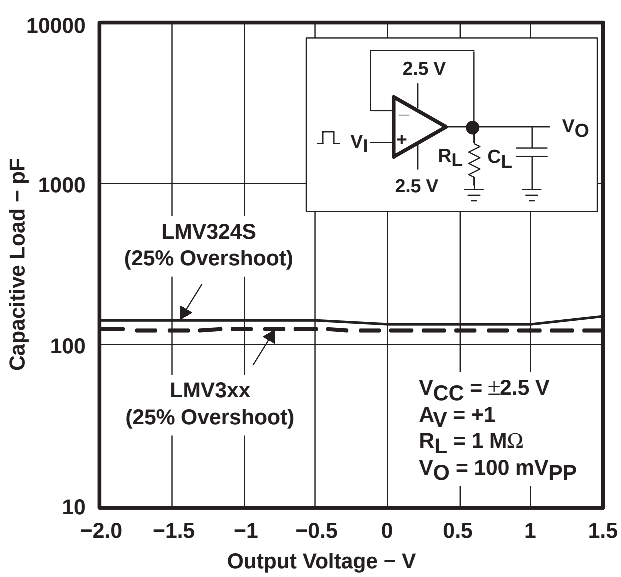


Figure 7

STABILITY vs CAPACITIVE LOAD

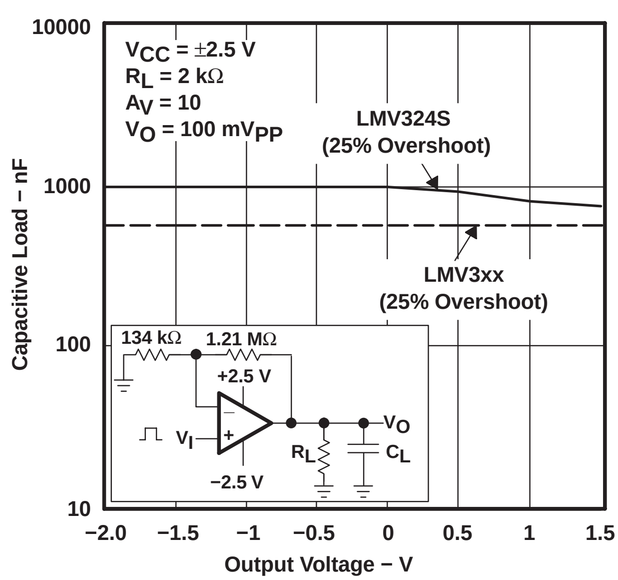


Figure 8

TYPICAL CHARACTERISTICS

STABILITY vs CAPACITIVE LOAD

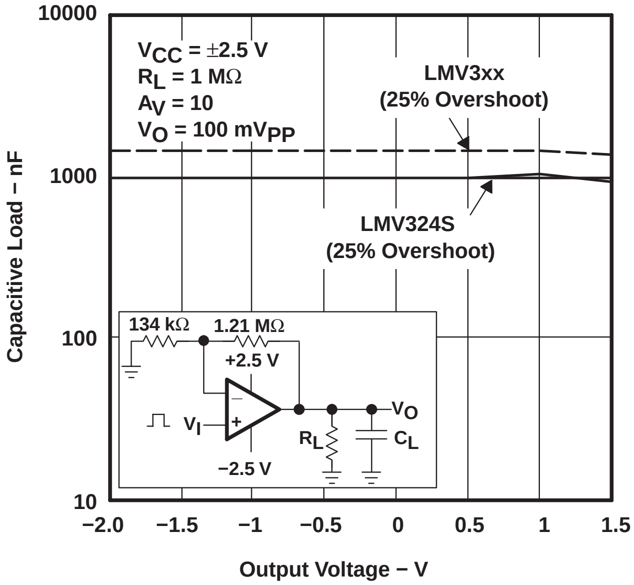


Figure 9

SLEW RATE vs SUPPLY VOLTAGE

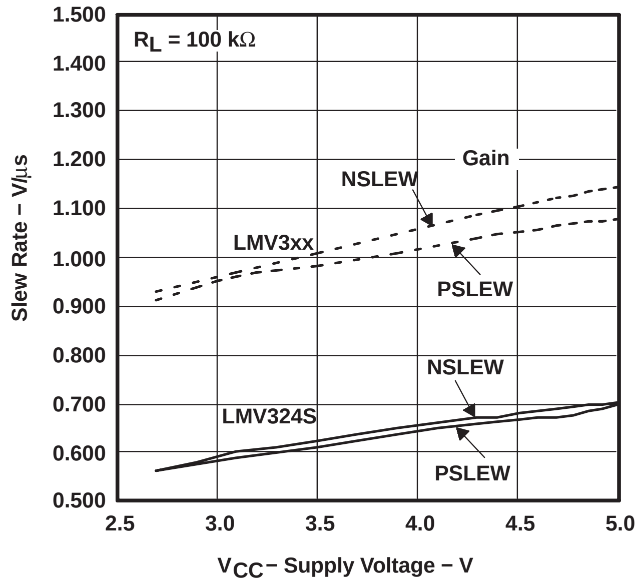


Figure 10

SUPPLY CURRENT vs SUPPLY VOLTAGE − QUAD AMPLIFIER

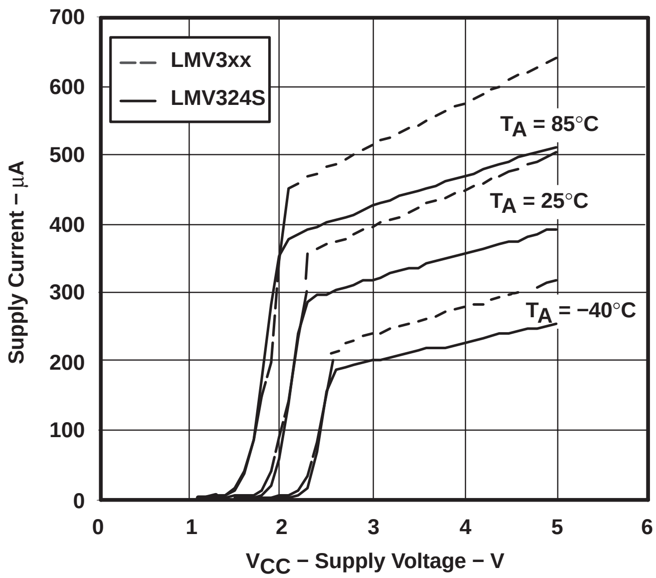


Figure 11

INPUT CURRENT vs TEMPERATURE

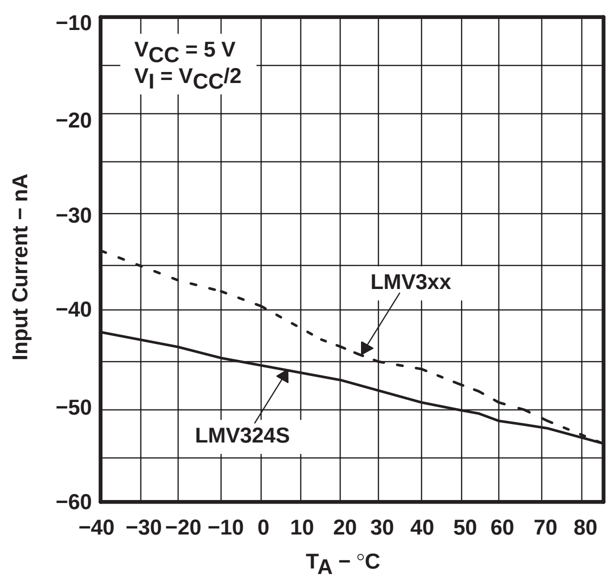


Figure 12

TYPICAL CHARACTERISTICS

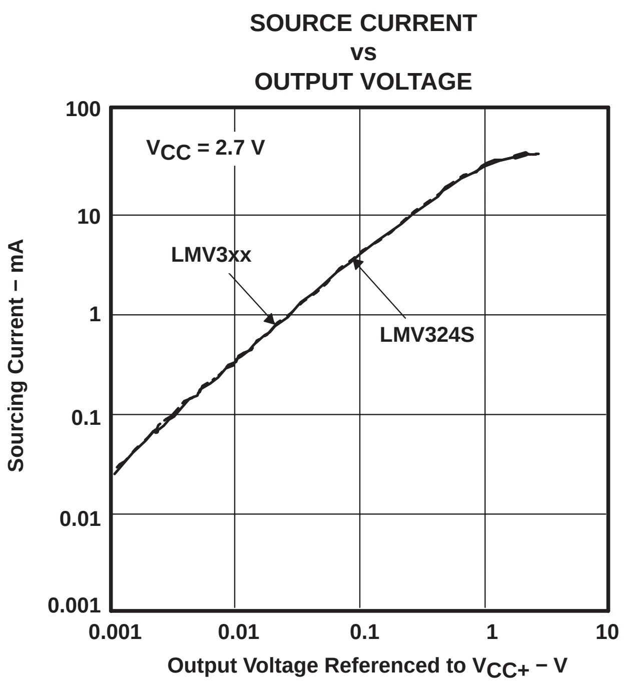


Figure 13

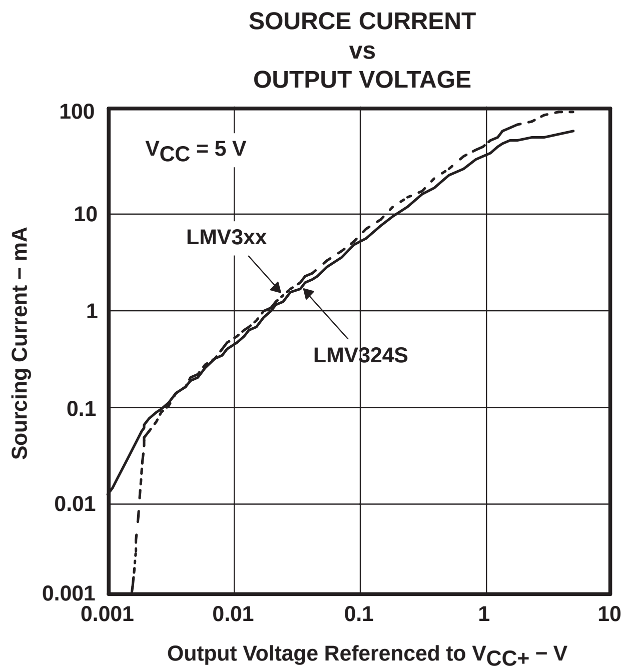


Figure 14

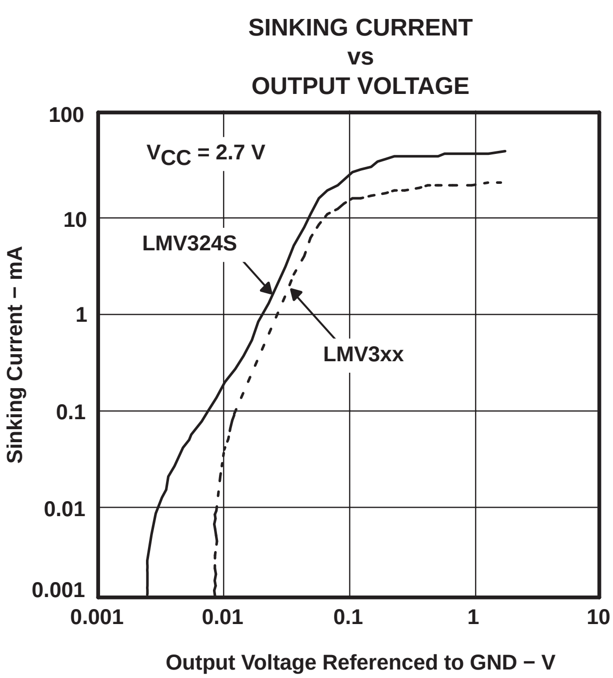


Figure 15

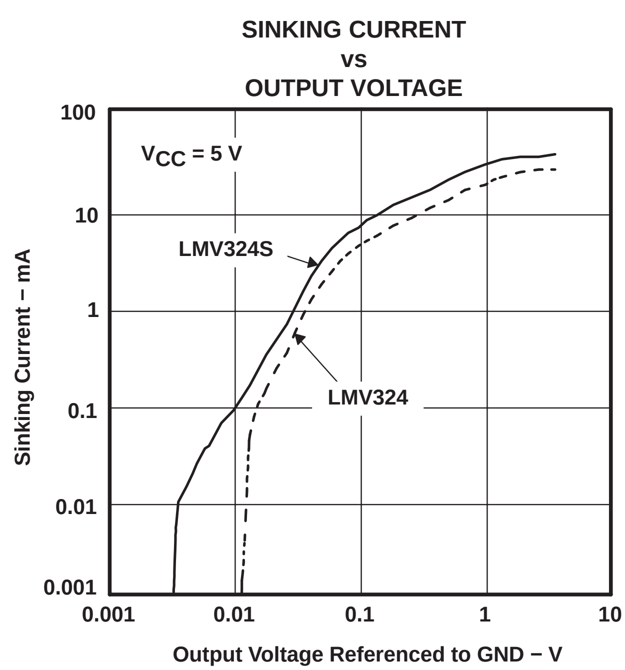


Figure 16

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT CURRENT vs TEMPERATURE

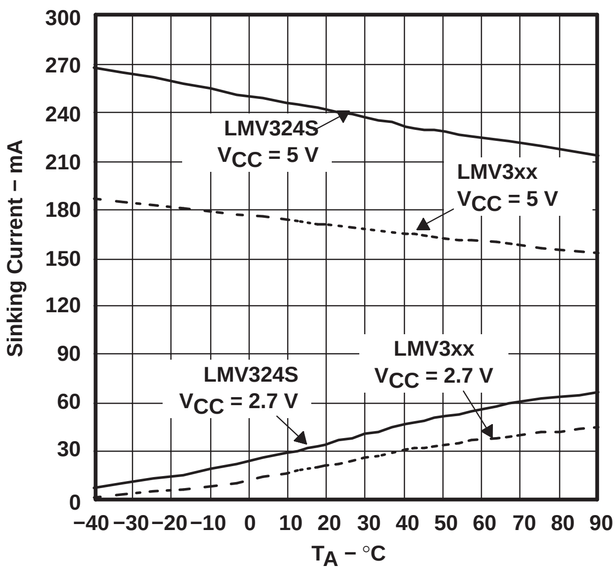


Figure 17

SHORT-CIRCUIT CURRENT vs TEMPERATURE

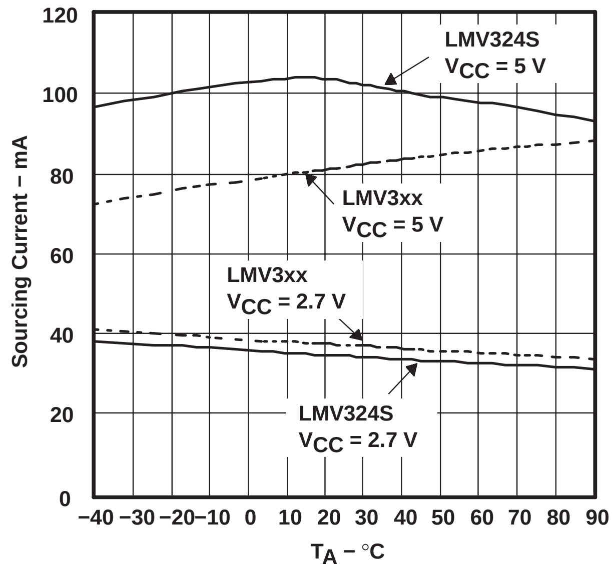


Figure 18

$-k_{SVR}$ vs FREQUENCY

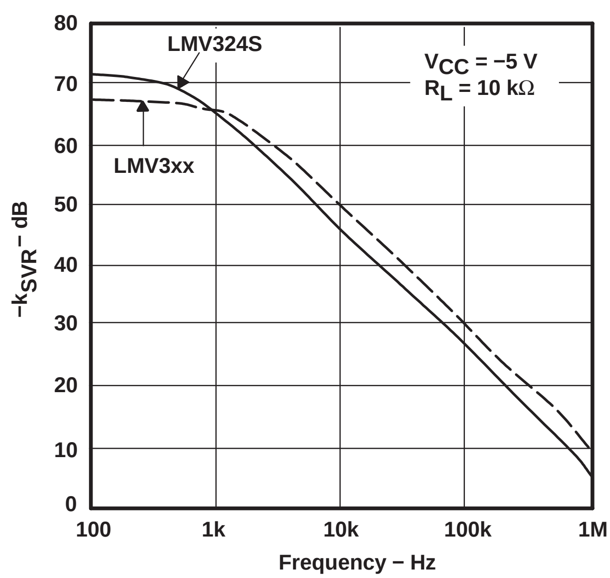


Figure 19

$+k_{SVR}$ vs FREQUENCY

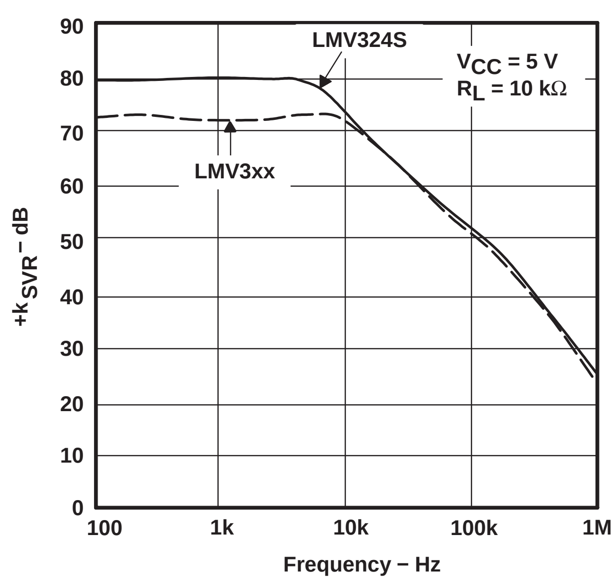


Figure 20

TYPICAL CHARACTERISTICS

$-k_{SVR}$ vs FREQUENCY

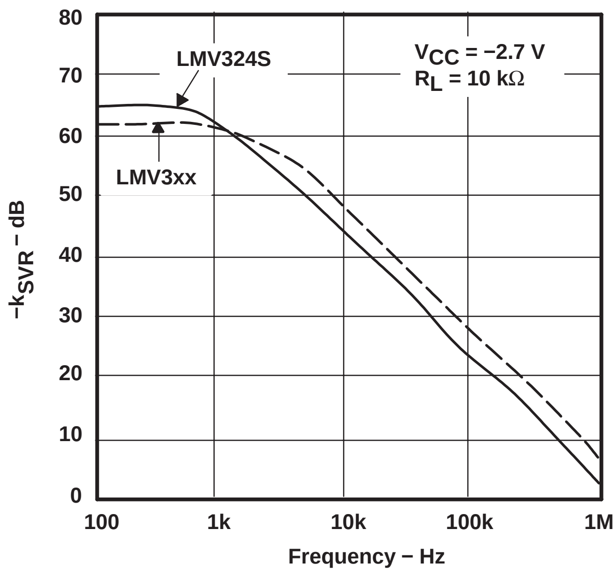


Figure 21

$+k_{SVR}$ vs FREQUENCY

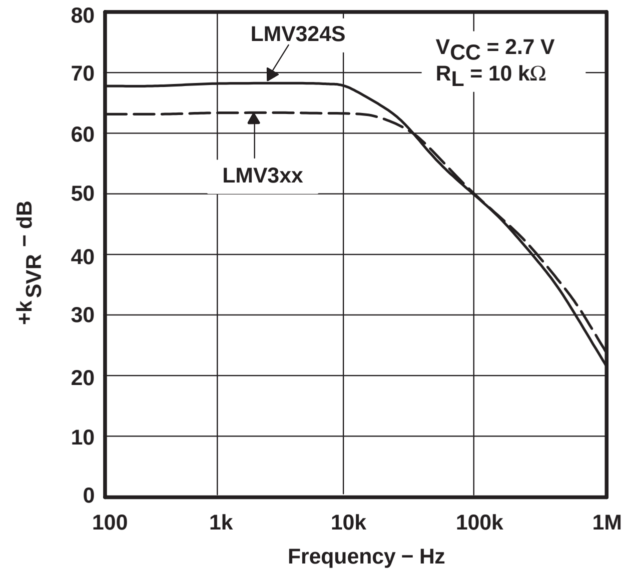


Figure 22

OUTPUT VOLTAGE SWING FROM RAILS vs SUPPLY VOLTAGE

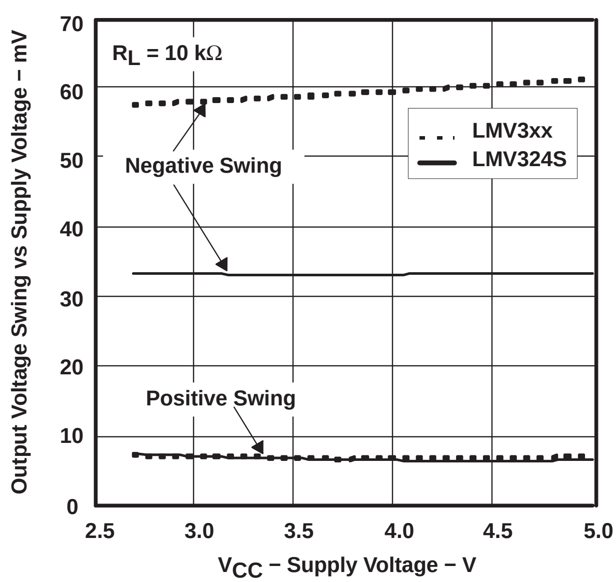


Figure 23

OUTPUT VOLTAGE vs FREQUENCY

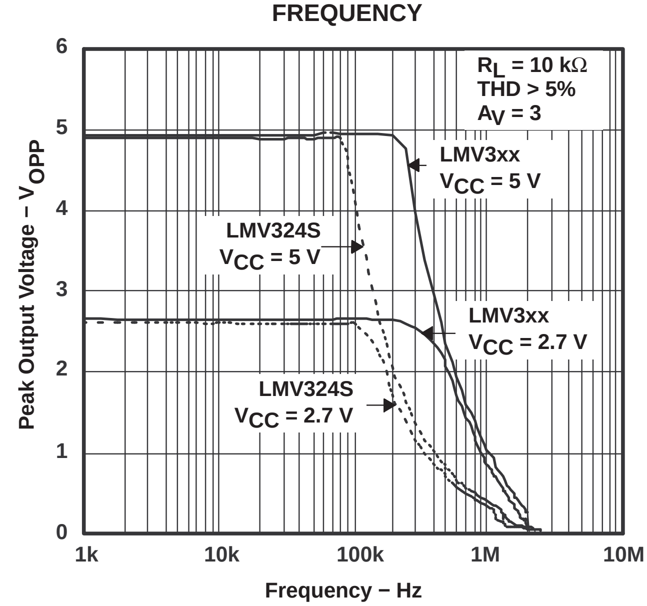


Figure 24

TYPICAL CHARACTERISTICS

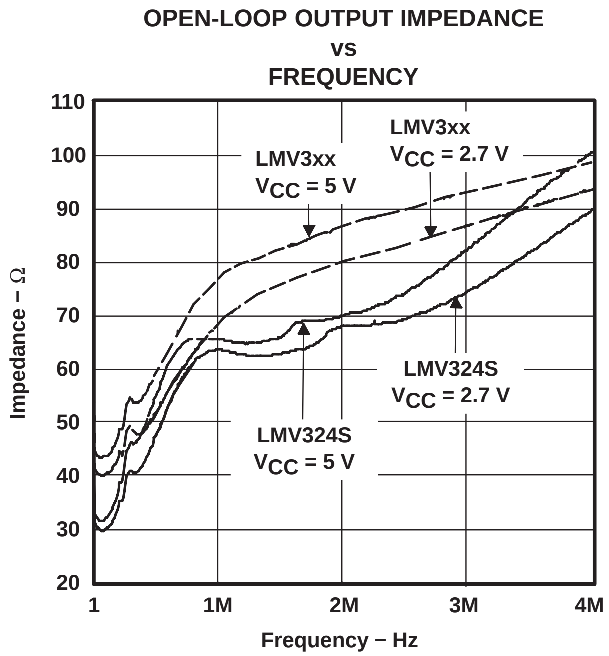


Figure 25

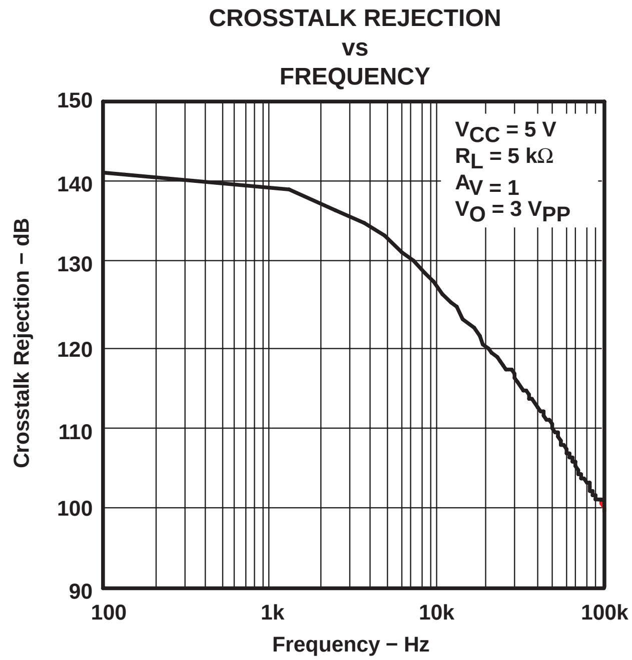


Figure 26

TYPICAL CHARACTERISTICS

NONINVERTING LARGE-SIGNAL PULSE RESPONSE

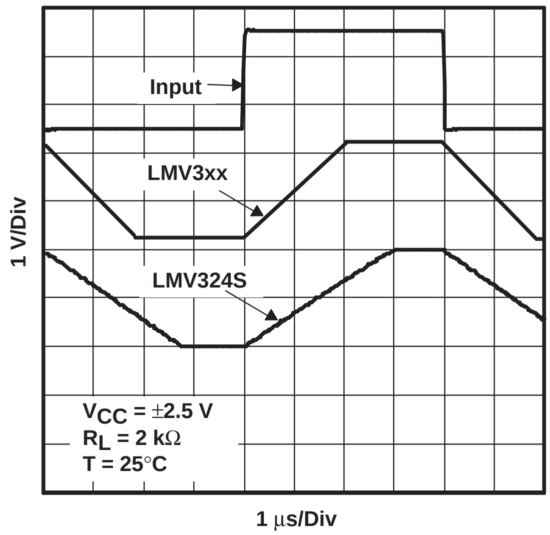


Figure 27

NONINVERTING LARGE-SIGNAL PULSE RESPONSE

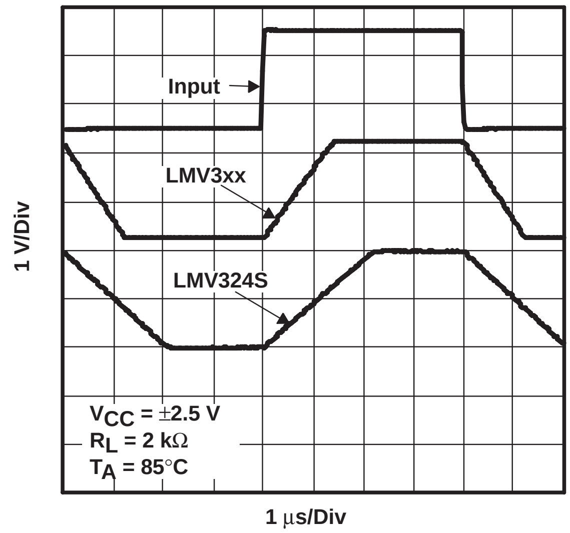


Figure 28

NONINVERTING LARGE-SIGNAL PULSE RESPONSE

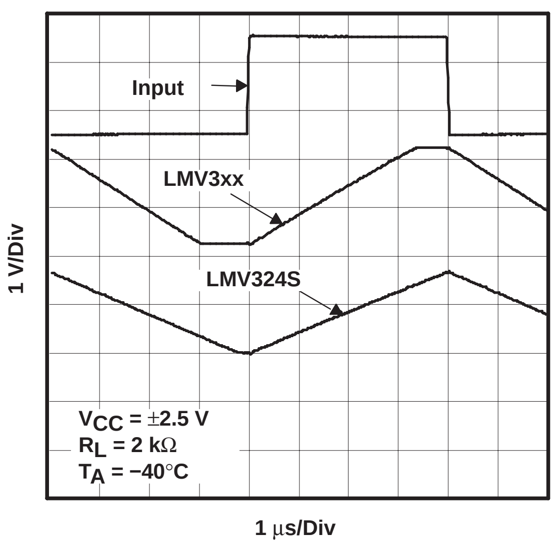


Figure 29

TYPICAL CHARACTERISTICS

NONINVERTING SMALL-SIGNAL
PULSE RESPONSE

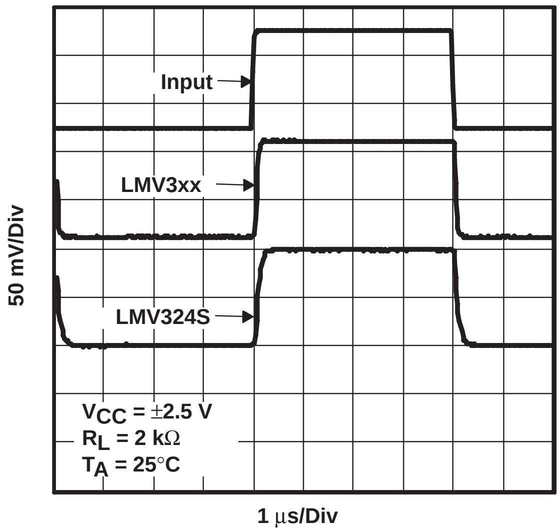


Figure 30

NONINVERTING SMALL-SIGNAL
PULSE RESPONSE

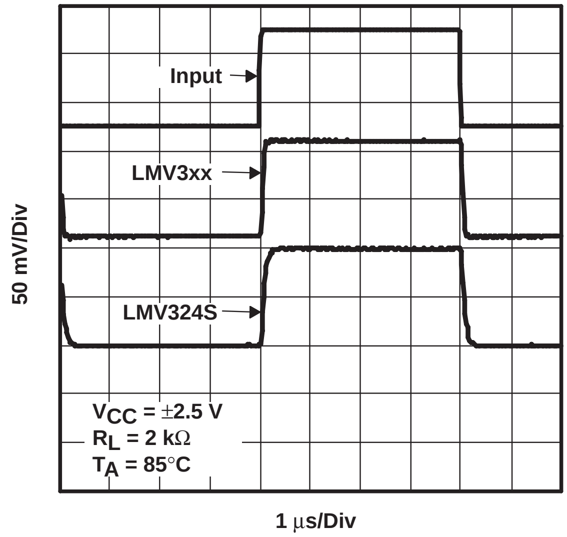


Figure 31

NONINVERTING SMALL-SIGNAL
PULSE RESPONSE

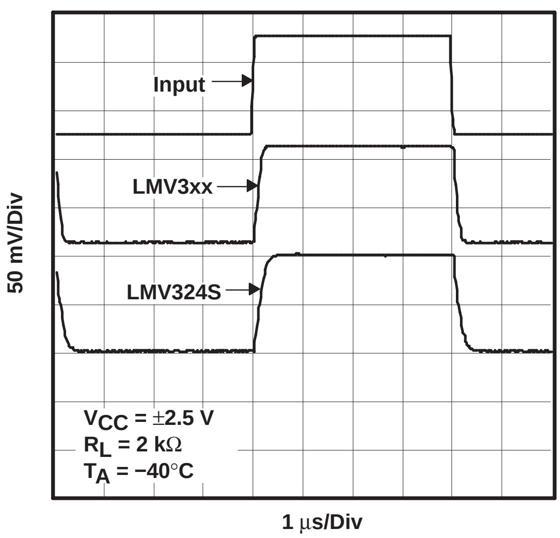


Figure 32

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE

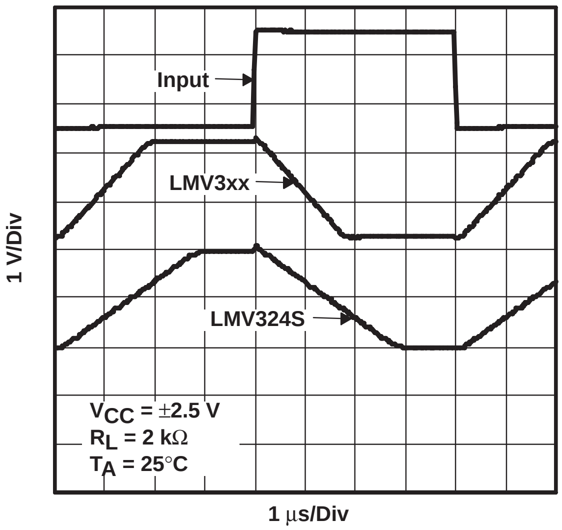


Figure 33

INVERTING LARGE-SIGNAL PULSE RESPONSE

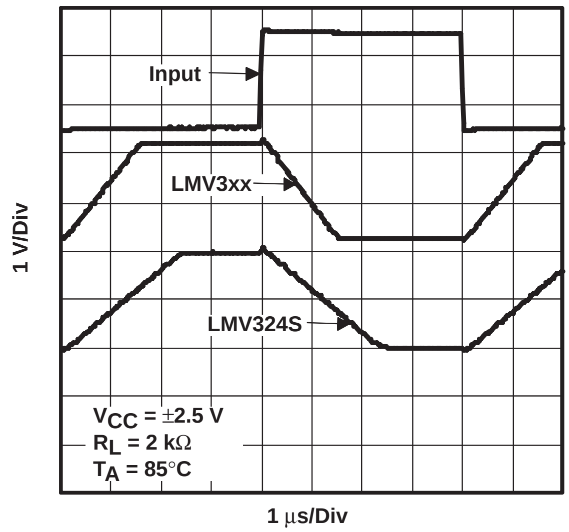


Figure 34

INVERTING LARGE-SIGNAL PULSE RESPONSE

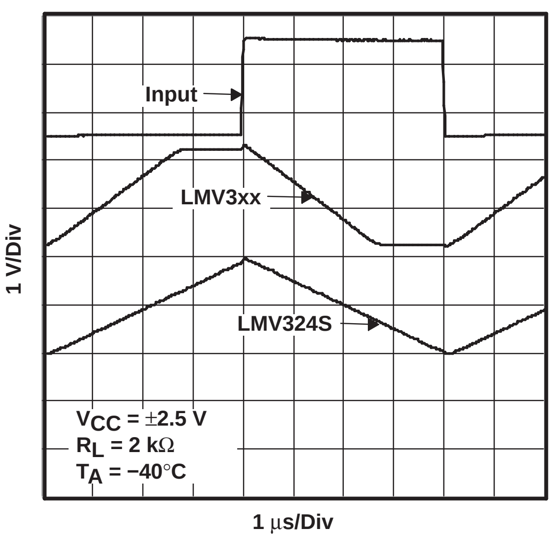


Figure 35

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE

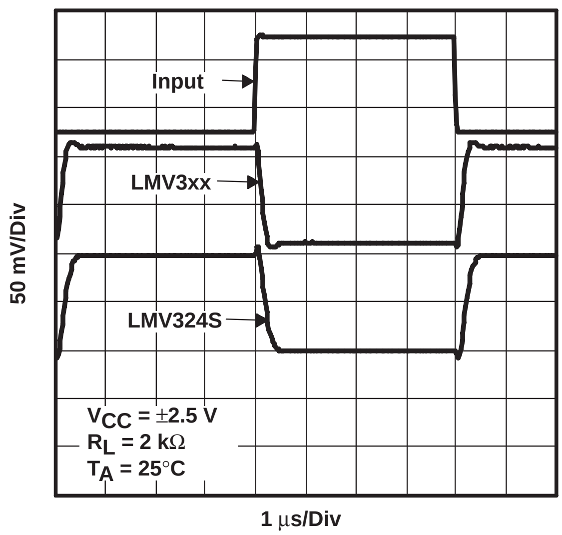


Figure 36

INVERTING SMALL-SIGNAL PULSE RESPONSE

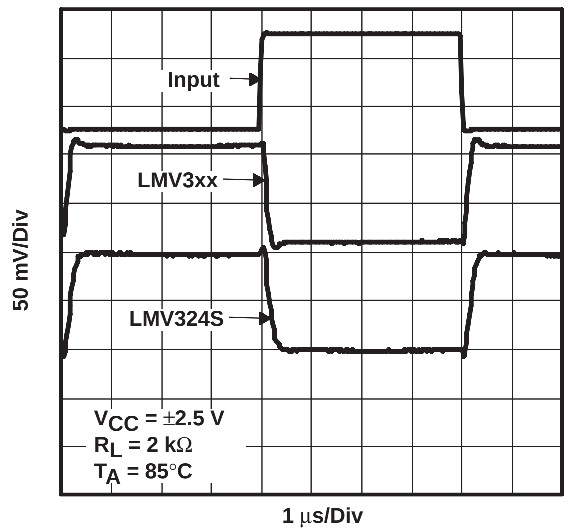


Figure 37

INVERTING SMALL-SIGNAL PULSE RESPONSE

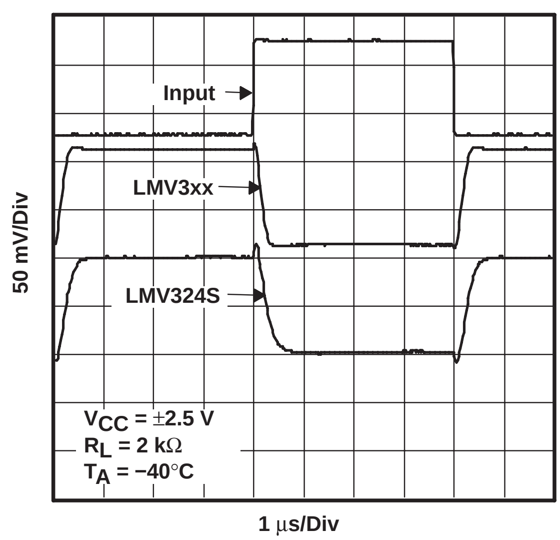


Figure 38

TYPICAL CHARACTERISTICS

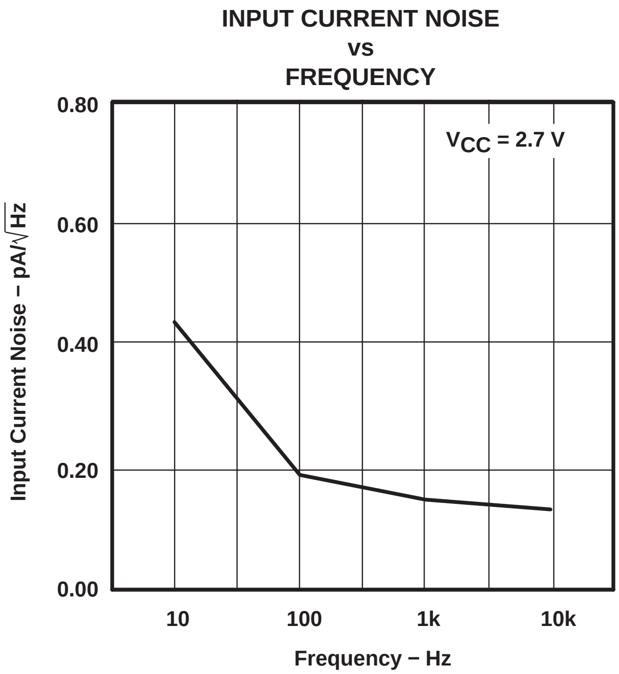


Figure 39

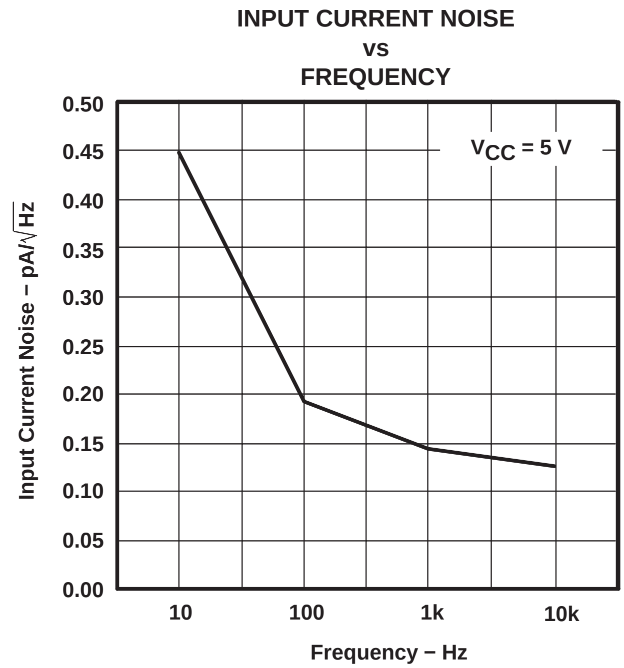


Figure 40

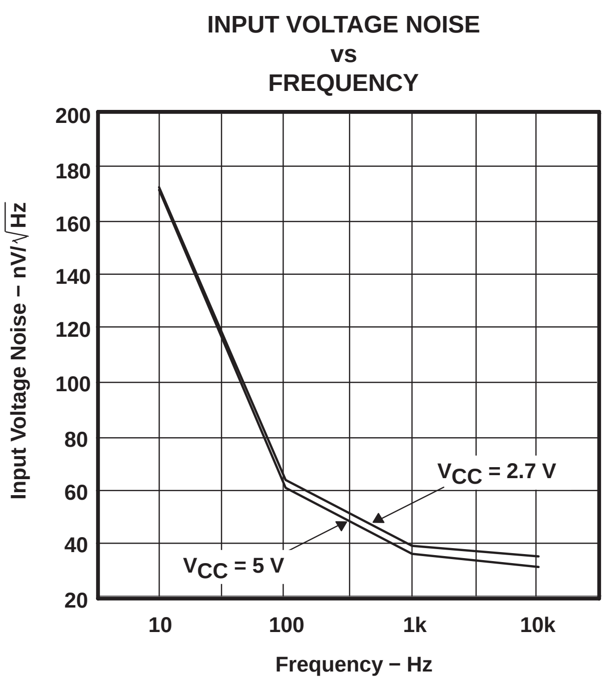


Figure 41

TYPICAL CHARACTERISTICS

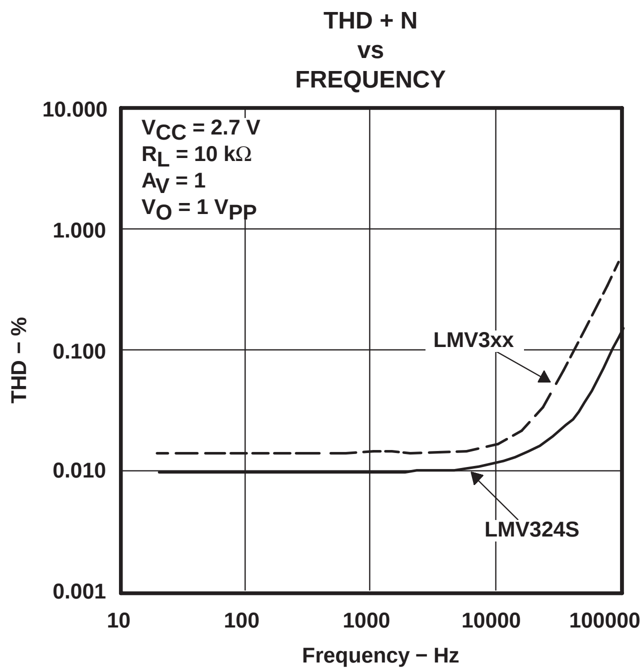


Figure 42

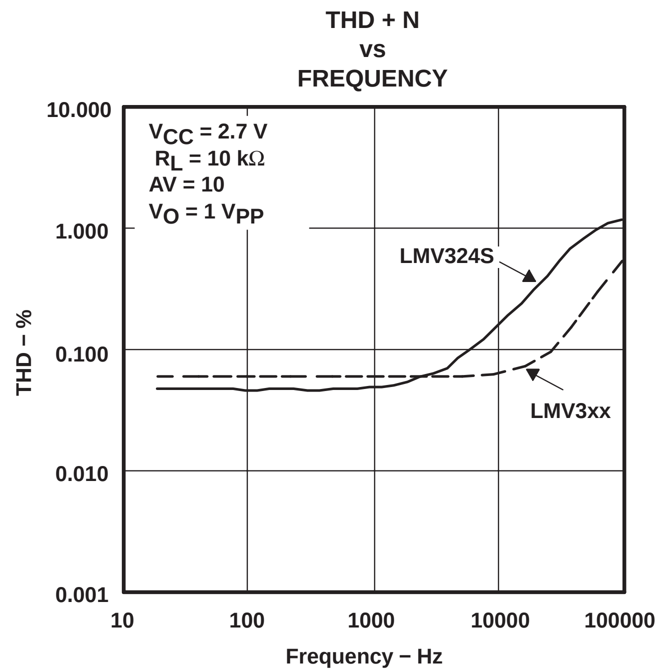


Figure 43

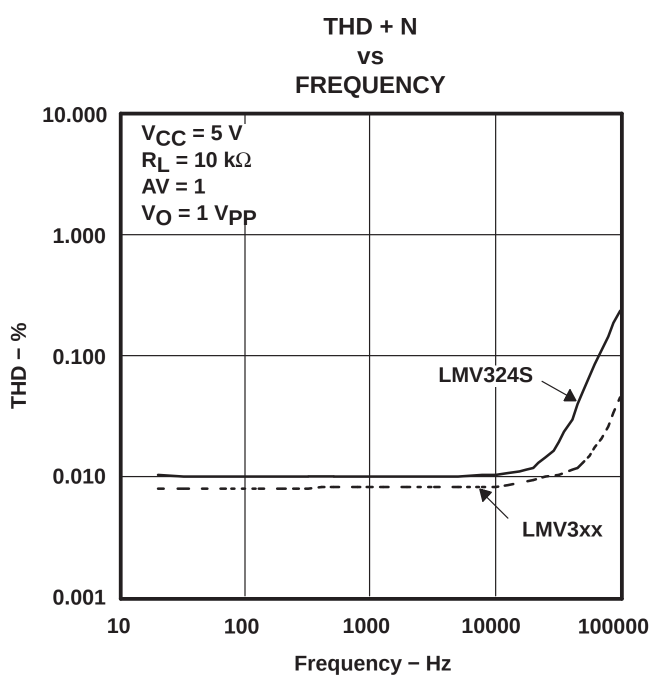


Figure 44

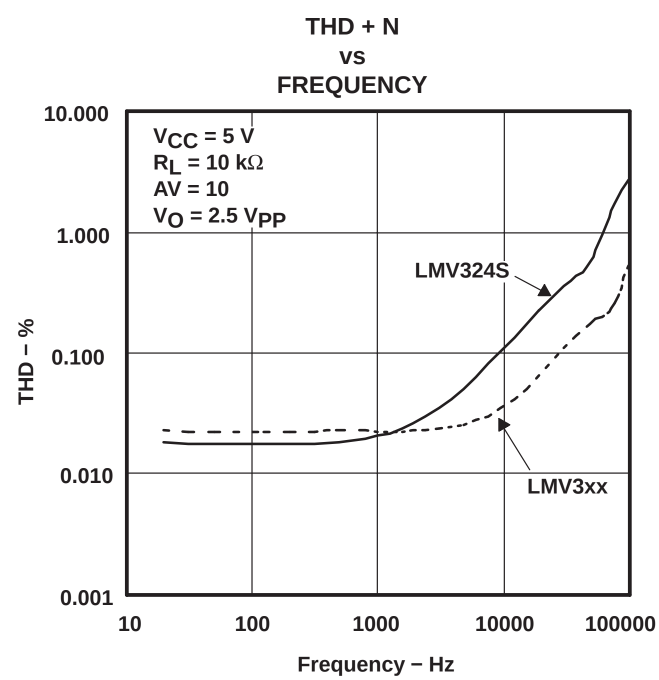


Figure 45

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
LMV321IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV321IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV321IDBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV321IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV321IDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV321IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV321IDCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324QD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324QDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324QPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324QPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324QPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324SID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324SIDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324SIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324SIDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324SIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV324SIPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358IDDUR	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358IDDURE4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
LMV358IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358IPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358IPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358QDDUR	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358QDDURE4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358QDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358QDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358QDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358QDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358QPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358QPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358QPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV358QPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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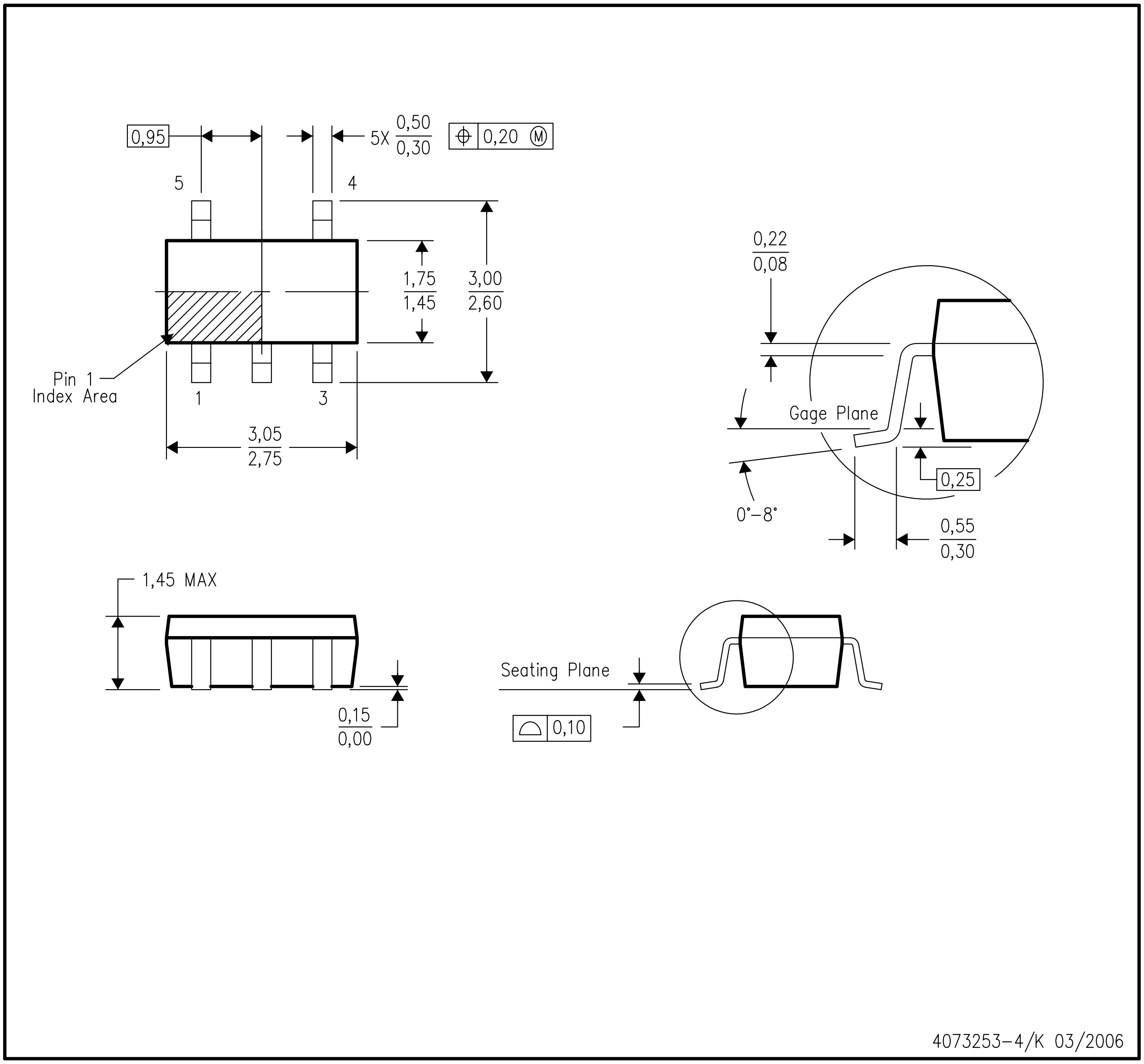
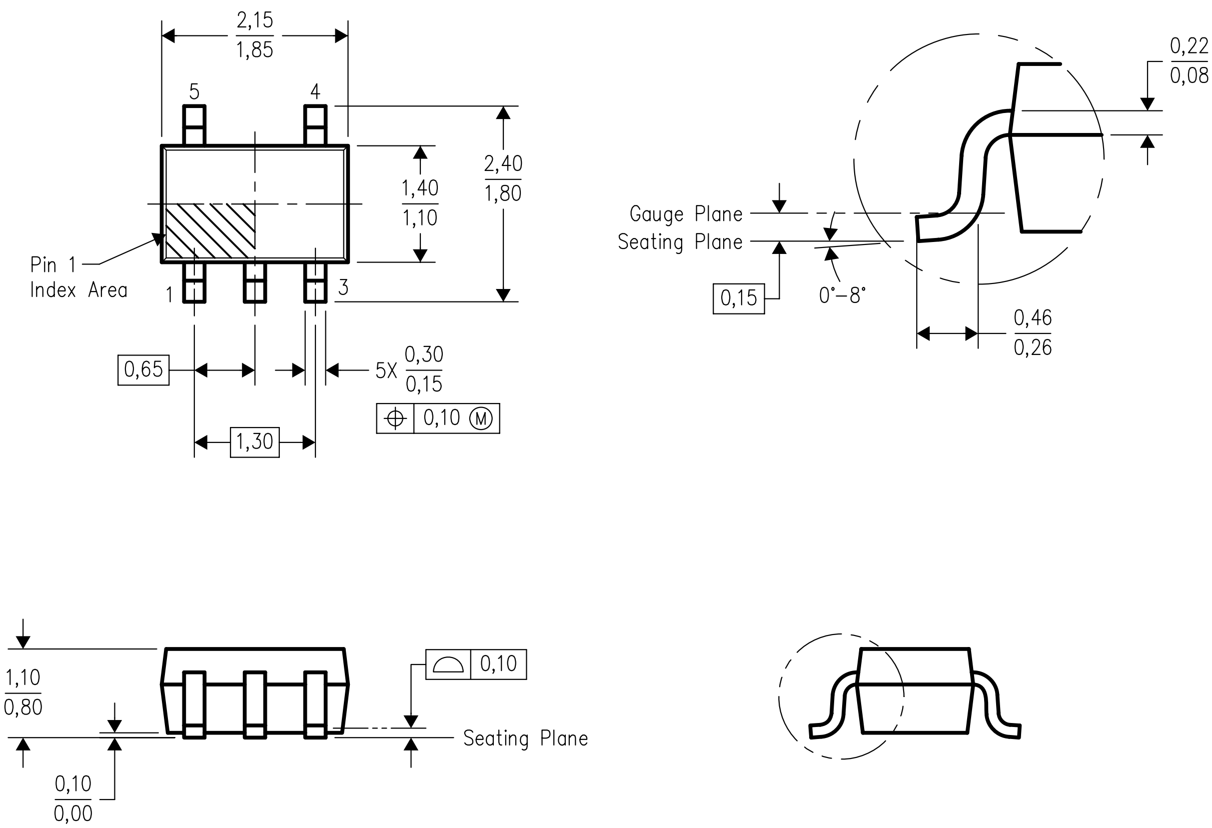
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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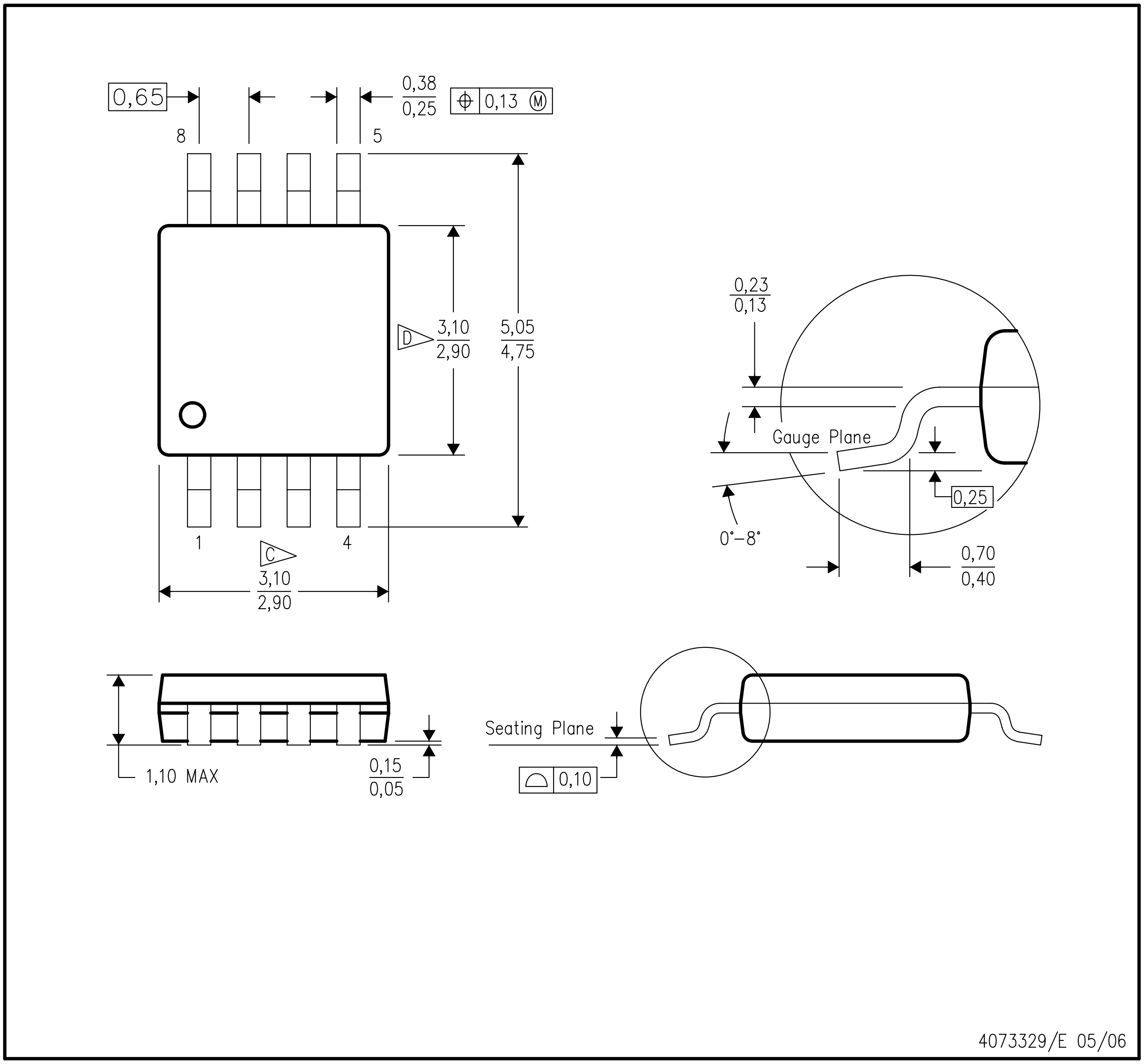
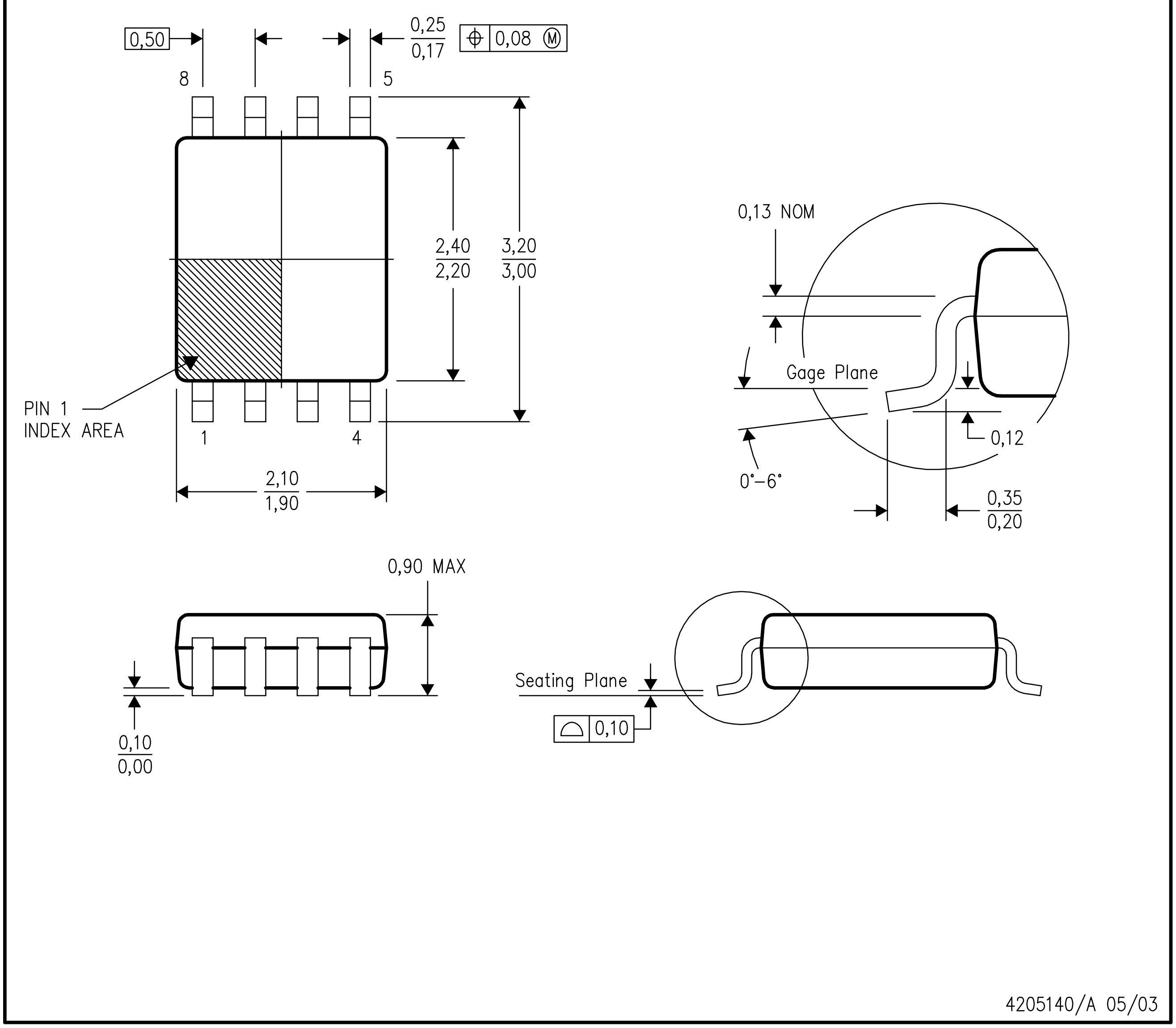
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



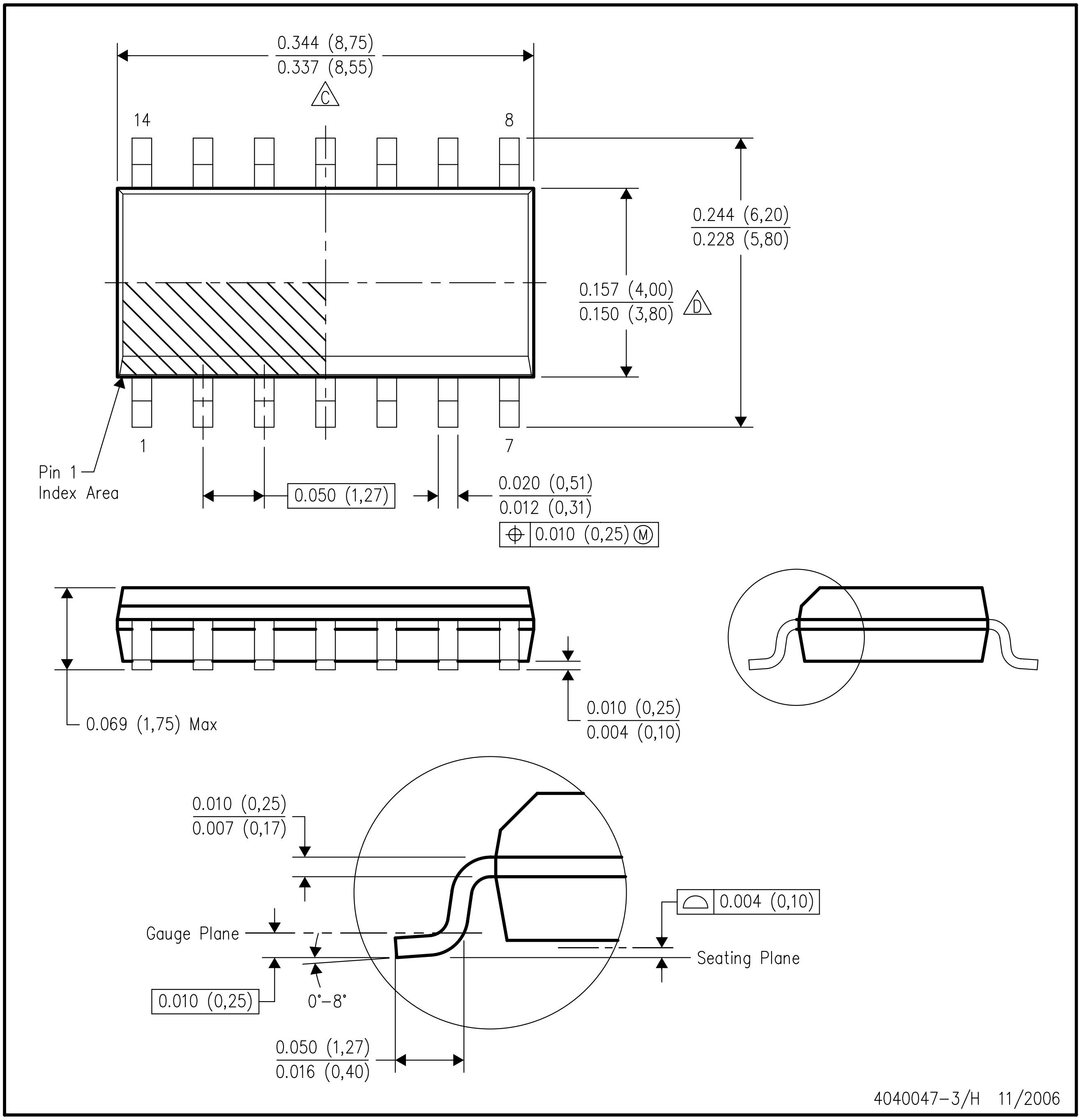
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DDU (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



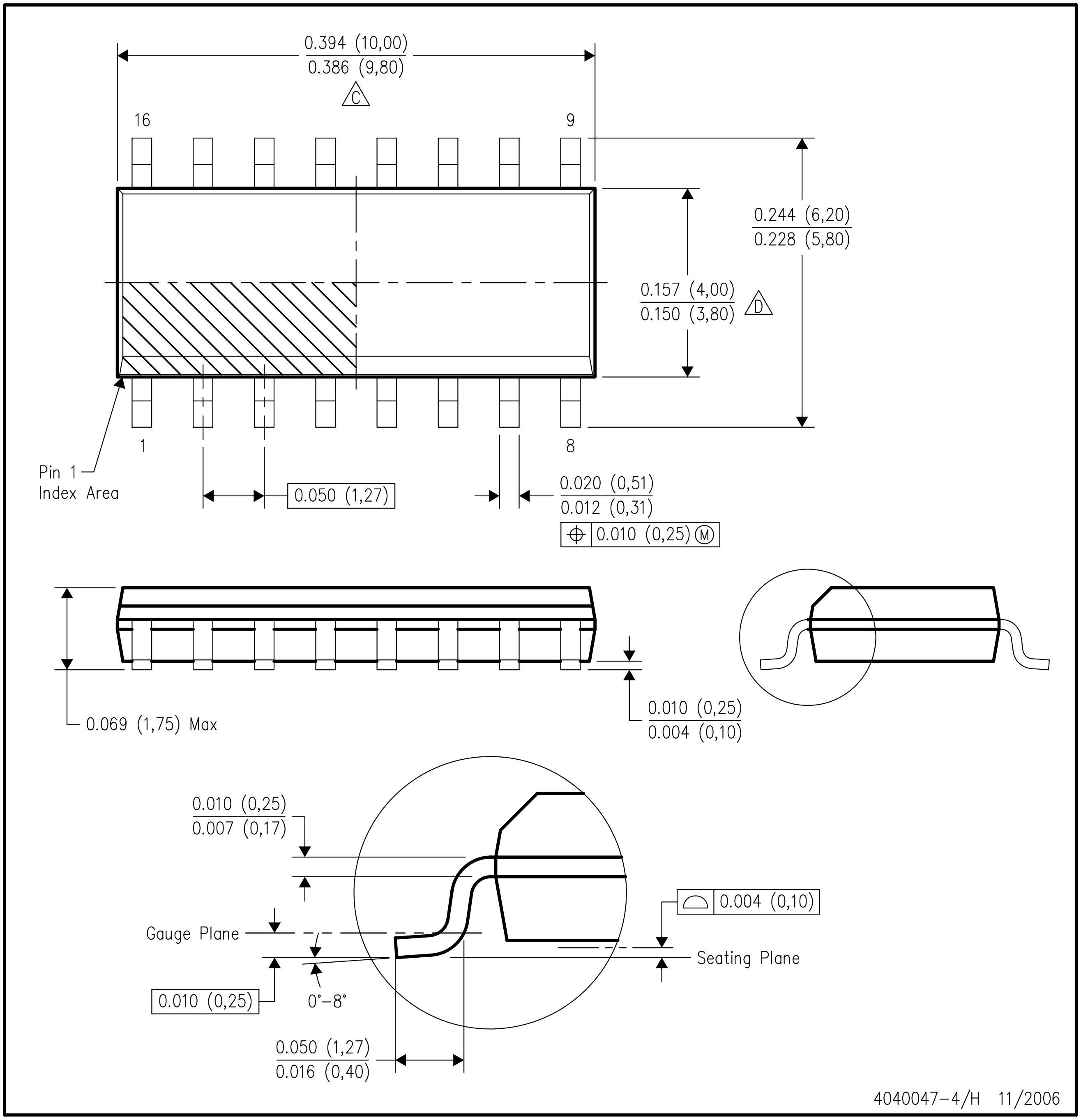
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation CA.

D (R-PDSO-G14) PLASTIC SMALL-OUTLINE PACKAGE



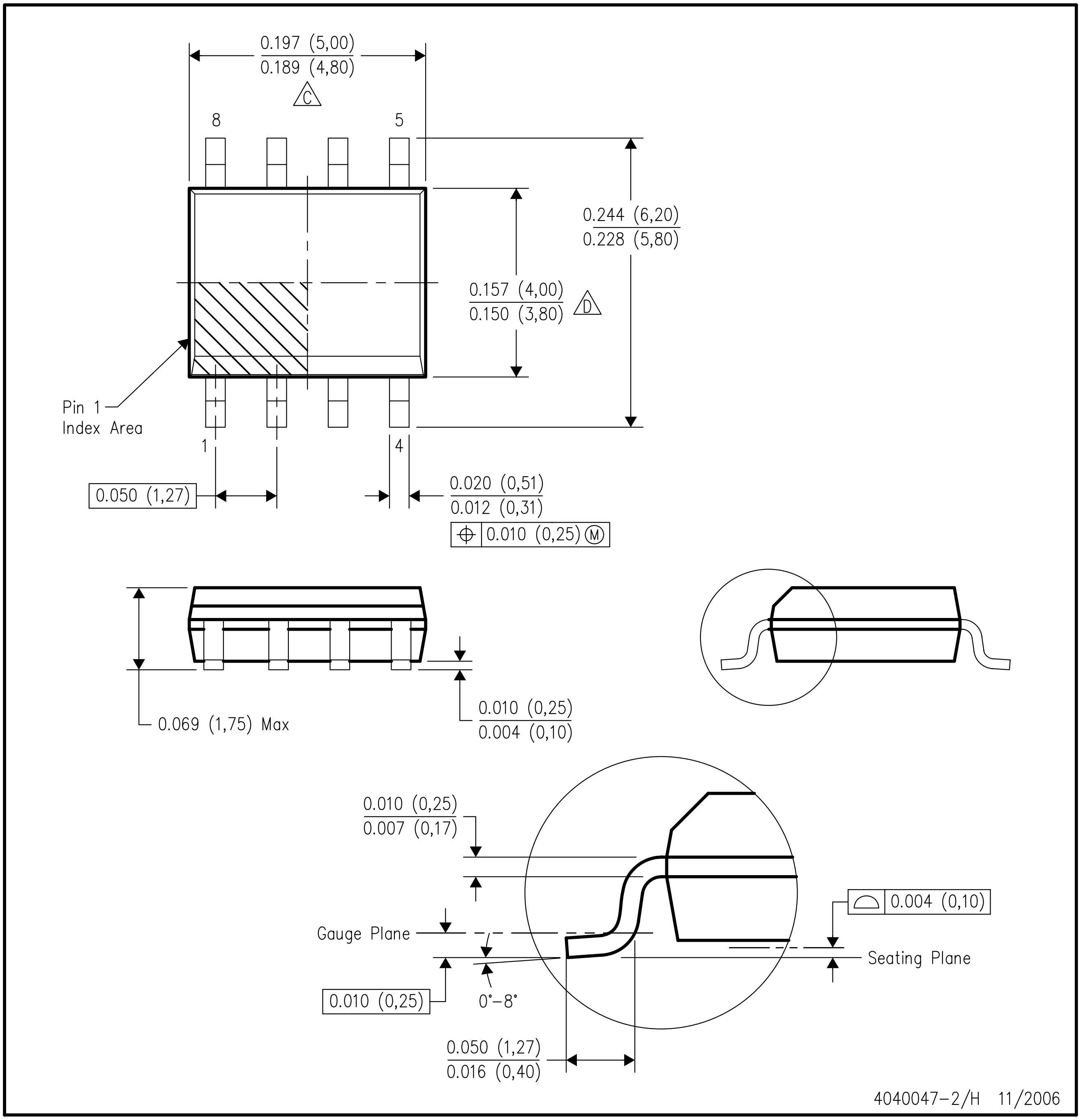
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AB.

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

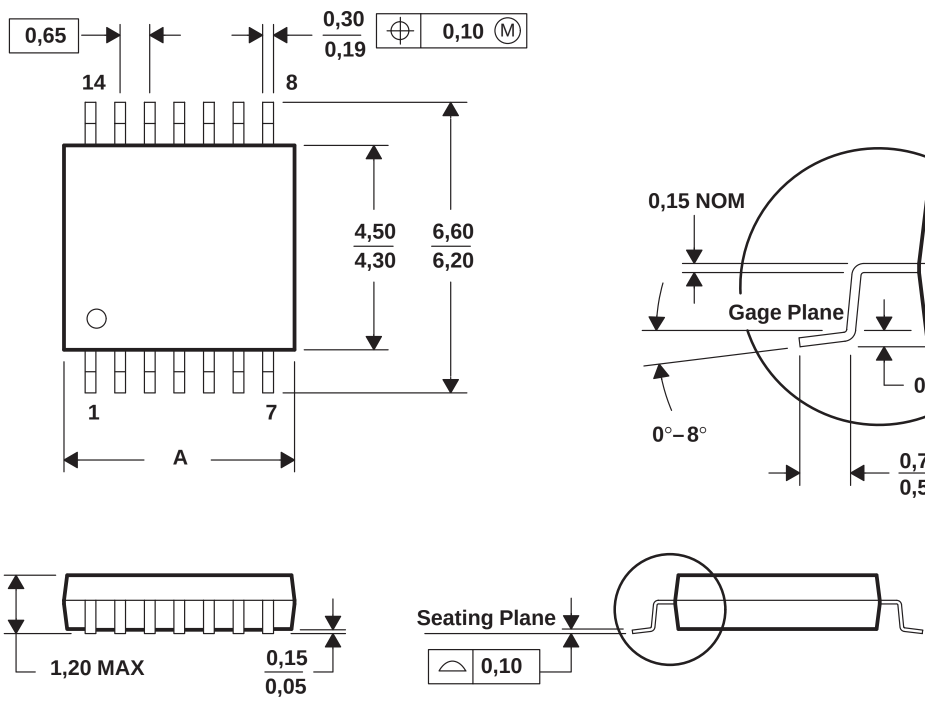
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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