# 32-Channel Vacuum-Fluorescent Display Driver

## Features

- 32 output lines
- 90V output swing
- Active pull-down
- Latches on all outputs
- Up to 6MHz @ $V_{DD}$ = 5.0V
- -40°C to +85°C operation

## Applications

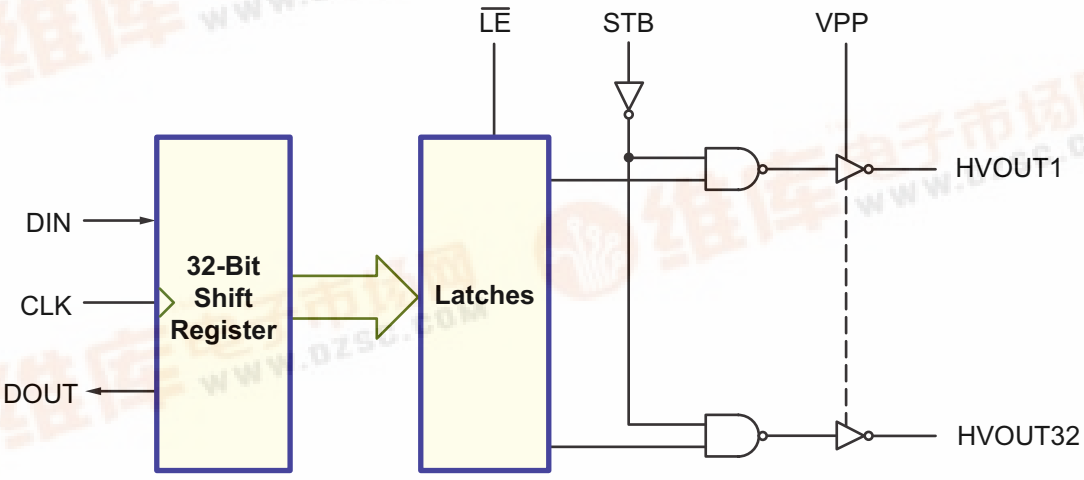
- Vacuum flourescent displays
- DC plasma displays

## General Description

The HV518 is designed for vacuum fluorescent or DC plasma applications, where it can serve as a segment, digit or matrix display driver. Each device has 32 outputs, 32 latches and a 32-bit cascadable shift register.

Serial data enters the shift register on the LOW-to-HIGH transition of the clock input. With latch enable ($\overline{LE}$) HIGH, parallel data is transferred to the output buffers through a 32-bit latch. When $\overline{LE}$ is low the data is stored in the latch. When STROBE is LOW, all outputs are enabled; if STROBE is HIGH, all outputs are LOW.

## Block Diagram



## Ordering Information

| Device | Package Options | |
|---|---|---|
| | 40-Lead PDIP | 44-Lead PLCC |
| HV518 | HV518P-G | HV518PJ-G |

*-G indicates package is RoHS compliant ('Green')*

## Absolute Maximum Ratings

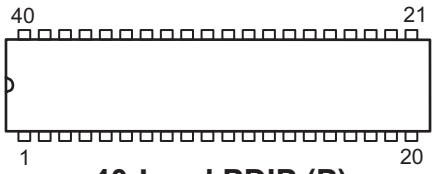
| Parameter | Value |
|---|---|
| Supply voltage, $V_{DD}$ | -0.5V to +6.0V |
| Supply voltage, $V_{PP}$ | -0.5V to +90V |
| Logic input levels | -0.5V to $V_{DD}$+0.5V |
| Continuous total power dissipation(1,2) | 1200mW |
| Operating temperature | -40°C to +85°C |
| Storage temperature | -65°C to +150°C |
| Soldering temperature(3) | 260°C |

*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to GND.*

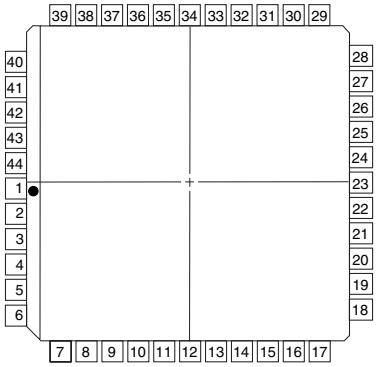
***Notes:***

*(1) Duty cycle is limited by the total power dissipated in the package.*
*(2) For operation above 25°C ambient, derate linearly to 85°C at 20mW/°C.*
*(3) Distance of 1.6mm from case for 10 seconds.*

## Pin Configurations



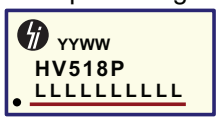

**40-Lead PDIP (P)**
***(top view)***



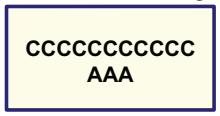

**44-Lead PLCC (PJ)**
***(top view)***

## Product Markings

Top Marking




Bottom Marking



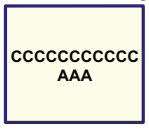

Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
_____ = "Green" Packaging

**May be part of top marking*

**40-Lead PDIP (P)**

Top Marking


Bottom Marking




YY = Year Sealed
WW = Week Sealed
L = Lot Number
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_____ = "Green" Packaging

**May be part of top marking*

**44-Lead PLCC (PJ)**

## Recommended Operating Conditions *($T_A$ = 25°C, unless otherwise noted)*

| Sym | Parameter | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| $V_{DD}$ | Logic supply voltage | 4.5 | 5.5 | V | --- |
| $V_{PP}$ | High voltage supply | 8.0 | 80 | V | --- |
| $V_{IH}$ | High-level input voltage | 3.5 | - | V | $V_{DD}$ = 4.5V, See Figure 3 |
| $V_{IL}$ | Low-level input voltage | - | 1.0 | V | $V_{DD}$ = 4.5V, See Figure 3 |
| $I_{OH}$ | High-level output current | -25 | - | mA | --- |
| $I_{OL}$ | Low-level output current | - | 2.0 | mA | --- |
| $f_{CLK}$ | Clock frequency | - | 6.0 | MHz | $V_{DD}$ = 4.5V, See Figure 3 |
| $t_{w(CKH)}$ | Pulse duration, clock high | 83 | - | ns | $V_{DD}$ = 4.5V |
| $t_{w(CKL)}$ | Pulse duration, clock low | 83 | - | ns | $V_{DD}$ = 4.5V |
| $t_{su}$ | Setup time, data before clock | 75 | - | ns | $V_{DD}$ = 4.5V |
| $t_h$ | Hold time, data after clock | 75 | - | ns | $V_{DD}$ = 4.5V |
| $T_A$ | Operating free-air temperature | -40 | 85 | °C | --- |

## Electrical Characteristics

*(over recommended ranges of operating free-air temperature and $V_{DD}$. Unless otherwise noted, $V_{PP}$ = 80V)*

| Sym | Parameter | | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | | - | - | 10 | mA | $V_{DD}$ = 5.0V, $f_{CH}$ = 6.0 MHz |
| $I_{DDQ}$ | Quiescent supply current | | - | - | 0.5 | mA | $V_{DD}$ = 5.5V, $V_{IN}$ = 0V |
| $I_{PPQ}$ | Quiescent supply current | | - | - | 100 | µA | --- |
| $V_{OH}$ | $HV_{IN}$ operating current | HV output | 70 | - | - | V | $I_{OH}$ = -25mA |
| | | Serial output | 4.5 | 4.9 | 5.0 | | $V_{DD}$ = 5.0V, $I_{OH}$ = -20µA |
| $V_{OL}$ | $LV_{IN}$ operating current | HV output | - | - | 5.0 | V | $I_{OL}$ = 1.0mA |
| | | Serial output | - | 0.06 | 0.8 | | $I_{OL}$ = 20µA |
| $I_{IH}$ | Logic input current high | | - | 0.1 | 1.0 | µA | $V_{IH}$ = $V_{DD}$ |
| $I_{IL}$ | Logic input current low | | - | -0.1 | -1.0 | µA | $V_{IL}$ = 0V |

***Note:*** *The total number of ON outputs times the duty cycle must not exceed the allowable package power disspation.*

## Switching Characteristics *($V_{PP}$ = 80V, $C_L$ = 50pF, $T_A$ = 25°C, unless otherwise noted)*

| Sym | Parameter | | Max | Unit | Conditions |
|---|---|---|---|---|---|
| $t_d$ | Delay time, clock to data output | | 600 | ns | $V_{DD}$ = 4.5V, $C_L$ = 15pF, See Figure 1 |
| $t_{DHL}$ | Turn-on time when high voltage is enabled | from latch enable | 1.5 | µs | $V_{DD}$ = 4.5V, See Figure 2 |
| | | from strobe | 1.0 | | $V_{DD}$ = 4.5V, See Figure 3 |
| $t_{DLH}$ | Delay time, high-to-low-level, HV output | from latch enable | 1.5 | µs | $V_{DD}$ = 4.5V, See Figure 2 |
| | | from strobe | 1.0 | | $V_{DD}$ = 4.5V, See Figure 3 |
| $t_{THL}$ | Transition time, high-to-low-level, HV output | | 3.0 | µs | $V_{DD}$ = 4.5V, See Figure 3 |
| $t_{TLH}$ | Transition time, low-to-high-level, HV output | | 2.5 | µs | $V_{DD}$ = 4.5V, See Figure 3 |

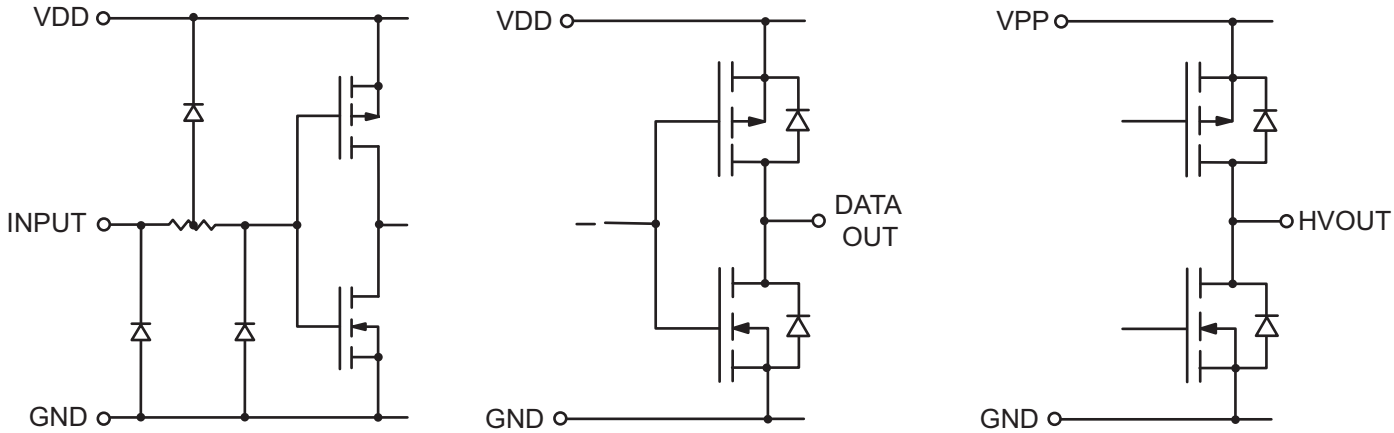
## Power-Up/ Power-Down Sequences

**Power-up sequence should be the following:**

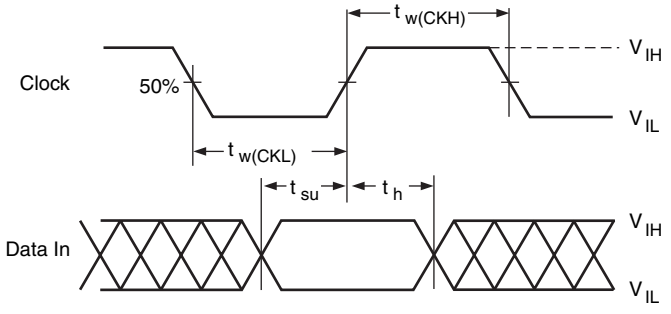
1. Connect ground.
2. Apply $V_{DD}$.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply $V_{PP}$.
5. The $V_{PP}$ should not drop below $V_{DD}$ or float during operation.

**Power-down sequence should be the reverse of the above.**

## Input and Output Equivalent Circuits




## Parameter Measurement Information




**Input Timing Voltage Waveforms**

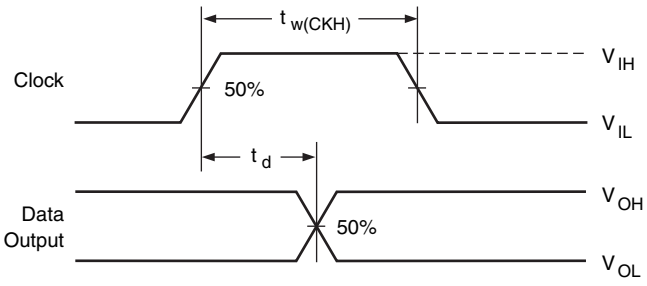



**Figure 1**

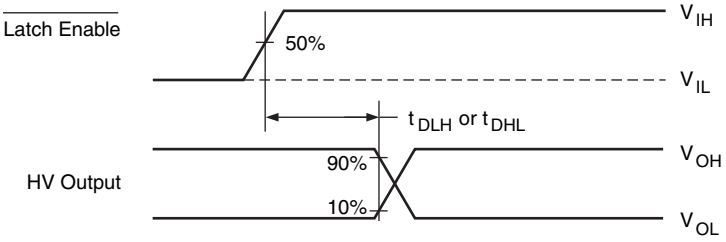



**Figure 2**

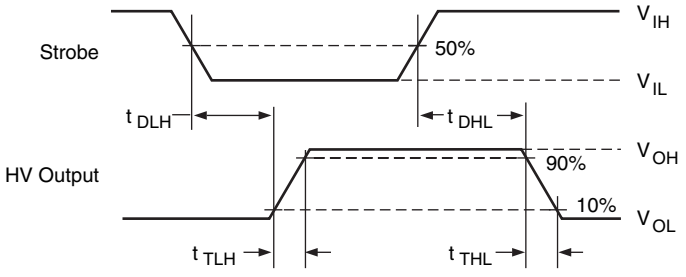



**Figure 3: Input Timing Voltage Waveforms**

***Note:*** *For testing purposes, all input pulses have maximum rise and fall times of 30 nsec.*

## Truth Tables

### Input

| Data In | CLK | Data Out |
|---|---|---|
| H | ↓ | H |
| L | ↓ | L |
| X | No Change | * |

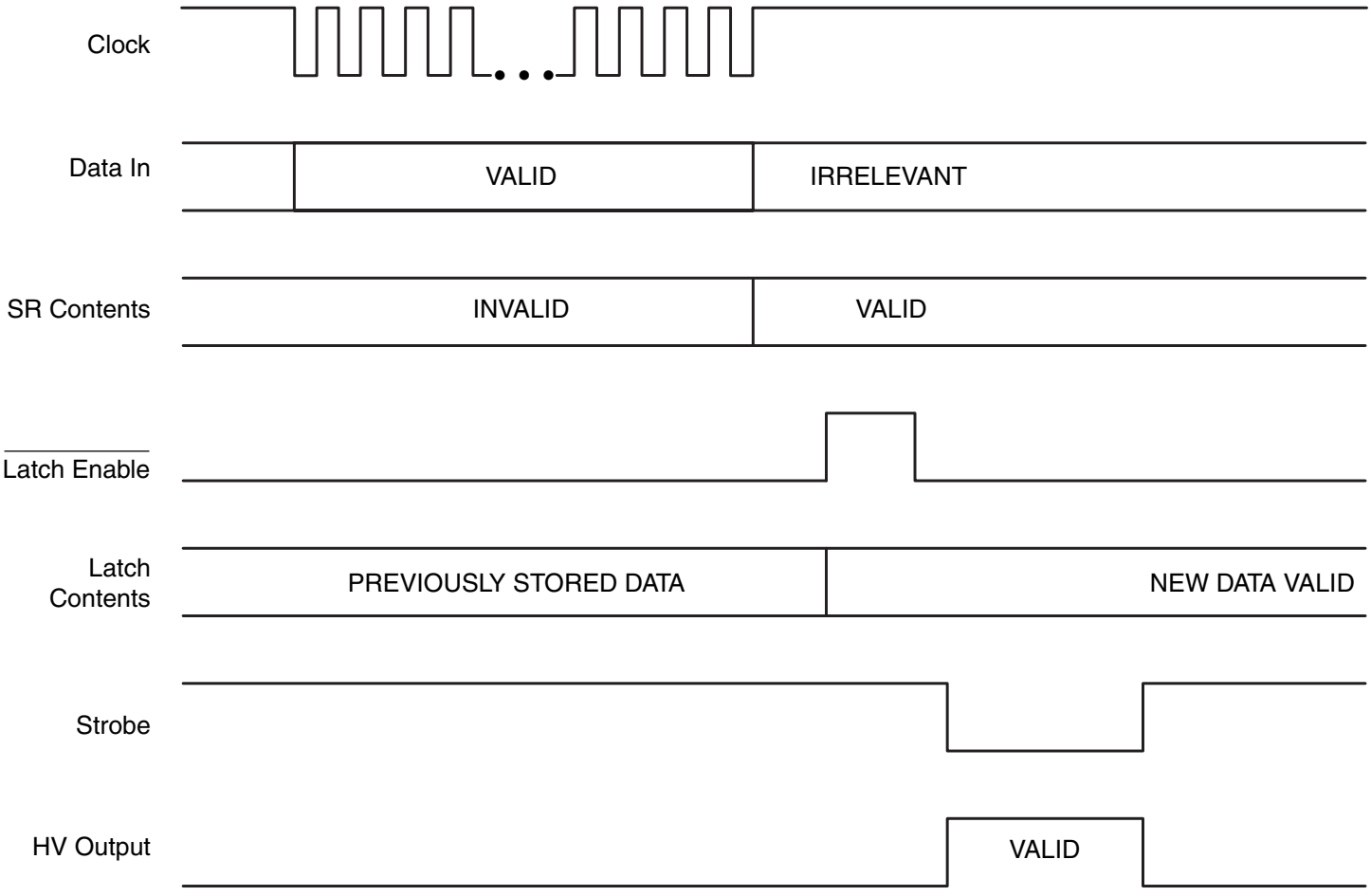
* Previous state.

### Output

| Data In | $\overline{LE}$ | STB | HV Outputs |
|---|---|---|---|
| X | X | H | All Low |
| H | H | L | High |
| L | H | L | Low |
| X | L | L | * |

* Previous state.

## Typical Operating Sequence



## Pin Descriptions

### 40-Lead PDIP (P)

| Pin | Function |
|---|---|
| 1 | VPP |
| 2 | Serial Out |
| 3 | HVOUT32 |
| 4 | HVOUT31 |
| 5 | HVOUT30 |
| 6 | HVOUT29 |
| 7 | HVOUT28 |
| 8 | HVOUT27 |
| 9 | HVOUT26 |
| 10 | HVOUT25 |
| 11 | HVOUT24 |
| 12 | HVOUT23 |
| 13 | HVOUT22 |
| 14 | HVOUT21 |

| Pin | Function |
|---|---|
| 15 | HVOUT20 |
| 16 | HVOUT19 |
| 17 | HVOUT18 |
| 18 | HVOUT17 |
| 19 | Strobe |
| 20 | GND |
| 21 | Clock |
| 22 | $\overline{LE}$ |
| 23 | HVOUT16 |
| 24 | HVOUT15 |
| 25 | HVOUT14 |
| 26 | HVOUT13 |
| 27 | HVOUT12 |
| 28 | HVOUT11 |

| Pin | Function |
|---|---|
| 29 | HVOUT10 |
| 30 | HVOUT9 |
| 31 | HVOUT8 |
| 32 | HVOUT7 |
| 33 | HVOUT6 |
| 34 | HVOUT5 |
| 35 | HVOUT4 |
| 36 | HVOUT3 |
| 37 | HVOUT2 |
| 38 | HVOUT1 |
| 39 | Data In |
| 40 | VDD |

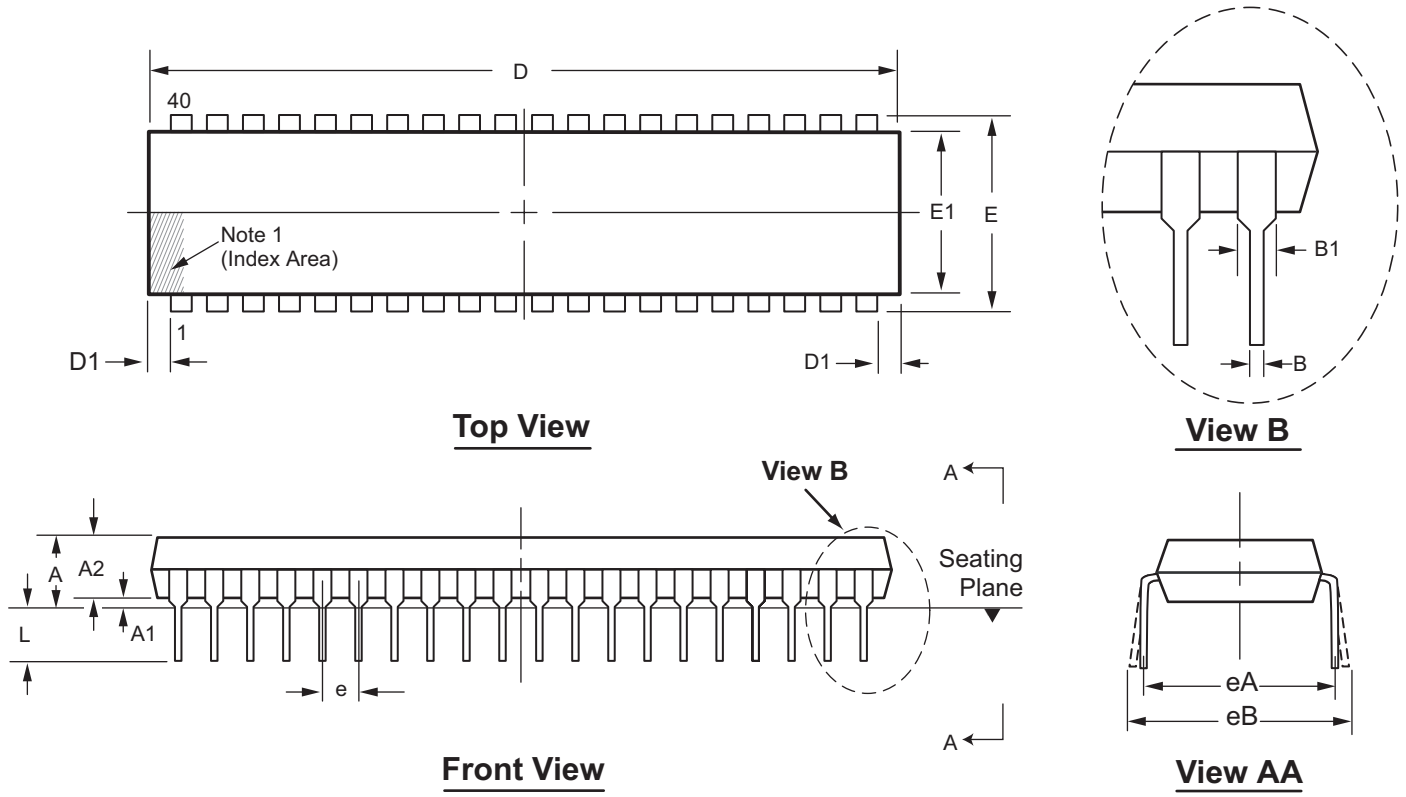
### 44-Lead PLCC (PJ)

| Pin | Function |
|---|---|
| 1 | VPP |
| 2 | Serial Out |
| 3 | HVOUT32 |
| 4 | HVOUT31 |
| 5 | HVOUT30 |
| 6 | NC |
| 7 | HVOUT29 |
| 8 | HVOUT28 |
| 9 | HVOUT27 |
| 10 | HVOUT26 |
| 11 | HVOUT25 |
| 12 | HVOUT24 |
| 13 | HVOUT23 |
| 14 | HVOUT22 |
| 15 | HVOUT21 |

| Pin | Function |
|---|---|
| 16 | HVOUT20 |
| 17 | HVOUT19 |
| 18 | N/C |
| 19 | HVOUT18 |
| 20 | HVOUT17 |
| 21 | Strobe |
| 22 | GND |
| 23 | Clock |
| 24 | $\overline{LE}$ |
| 25 | HVOUT16 |
| 26 | HVOUT15 |
| 27 | HVOUT14 |
| 28 | N/C |
| 29 | N/C |
| 30 | HVOUT13 |

| Pin | Function |
|---|---|
| 31 | HVOUT12 |
| 32 | HVOUT11 |
| 33 | HVOUT10 |
| 34 | HVOUT9 |
| 35 | HVOUT8 |
| 36 | HVOUT7 |
| 37 | HVOUT6 |
| 38 | HVOUT5 |
| 39 | HVOUT4 |
| 40 | HVOUT3 |
| 41 | HVOUT2 |
| 42 | HVOUT1 |
| 43 | Data In |
| 44 | VDD |

# 40-Lead PDIP (.600in Row Spacing) Package Outline (P)



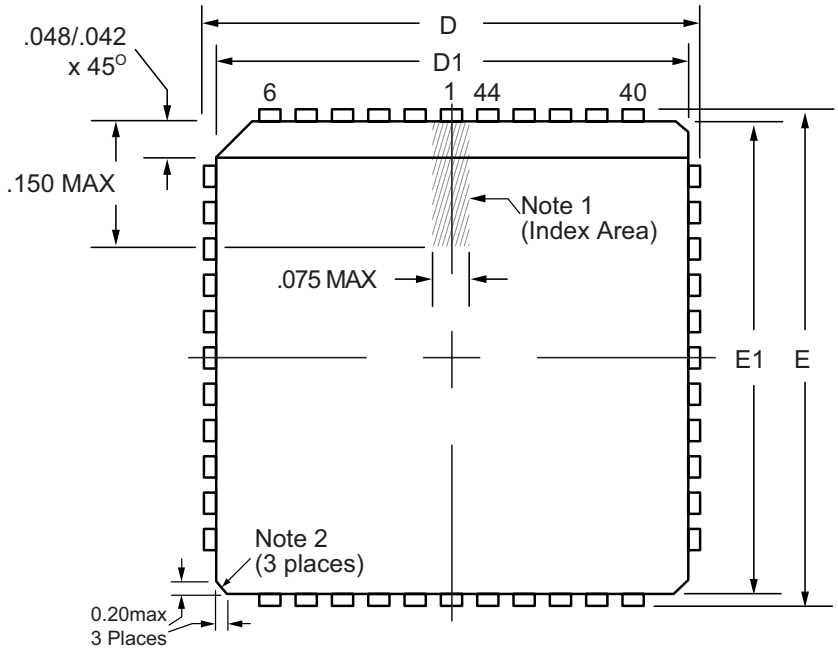

***Note 1:***
*A Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.*

| Symbol | | A | A1 | A2 | eA | B | B1 | eB | D | D1 | E | E1 | e | L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (inches) | MIN | .140 | .015 | .125 | .600 BSC | .014 | .030 | .600 | 1.980 | .005 | .600 | 0.485 | .100 BSC | .115 |
| | NOM | - | - | - | | - | - | - | - | - | - | - | | - |
| | MAX | .250 | .125 | .195 | | .022 | .070 | .700 | 2.095 | .625 | .625 | 0.580 | | .200 |

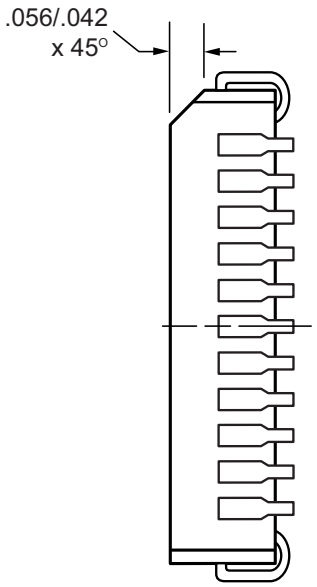
*JEDEC Registration MS-011, Variation AC, Issue B, June, 1988.*
***Drawings not to scale.***

# 44-Lead PLCC Package Outline (PJ)

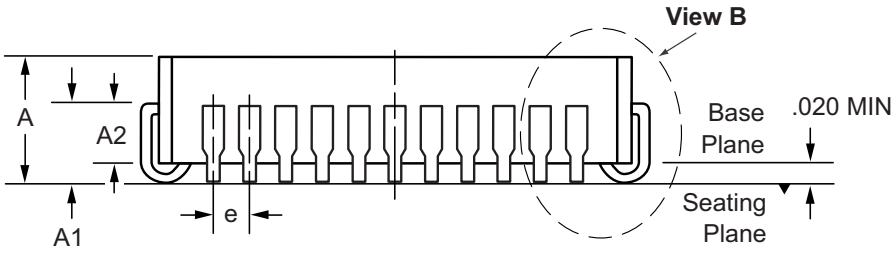
***.653x.653in body, .180in height (max.), .050in pitch***



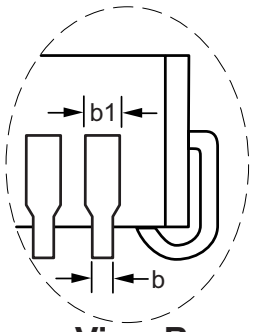

**Top View**




**Side View**




**Side View**




**View B**

***Note:***

*1. A Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.*

*2. Exact shape of this feature is optional.*

| Symbol | | A | A1 | A2 | b | b1 | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (inches) | MIN | .165 | .090 | .062 | .013 | .026 | .685 | .650 | .685 | .650 | .050 BSC |
| | NOM | .172 | .105 | - | - | - | .690 | .653 | .690 | .653 | |
| | MAX | .180 | .120 | .083 | .021 | .036 | .695 | .656 | .695 | .656 | |

*JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.*

***Drawings are not to scale.***

*(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [http://www.supertex.com/packaging.html](http://www.supertex.com/packaging.html).)*



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