TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

2 GBIT (256M × 8 BIT/128M × 16 BIT) CMOS NAND E^{2}PROM

DESCRIPTION

The TC58NVG1SxB is a single 3.3 V 2 Gbit (2,214,592,512 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E^{2}PROM) organized as (2048 + 64) bytes/(1024 + 32) words × 64 pages × 2048 blocks. The device has a 2112-byte/1056-word static register which allow program and read data to be transferred between the register and the memory cell array in 2112-byte increments. The Erase operation is implemented in a single block unit (128 Kbytes + 4 Kbytes: 2112 bytes × 64 pages).

The TC58NVG1SxB is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

FEATURES

- Organization

	TC58NVG1S3B	TC58NVG1S8B
Memory cell array	2112 × 128K × 8	1056 × 128K × 16
Register	2112 × 8	1056 × 16
Page size	2112 bytes	1056 words
Block size	(128K + 4K) bytes	(64K + 2K) words

- Modes
  Read, Reset, Auto Page Program, Auto Block Erase, Status Read
- Mode control
  Serial input/output
  Command control
- Number of valid blocks
  Max 2048 blocks
  Min 2008 blocks
- Power supply
  V_{CC} = 2.7 V to 3.6 V
- Program/Erase Cycles
  100000 Cycles (With ECC)
- Access time

Cell array to register	25 µs max
Serial Read Cycle	50 ns min

- Program/Erase time

Auto Page Program	200 µs/page typ.
Auto Block Erase	1.5 ms/block typ.

- Operating current

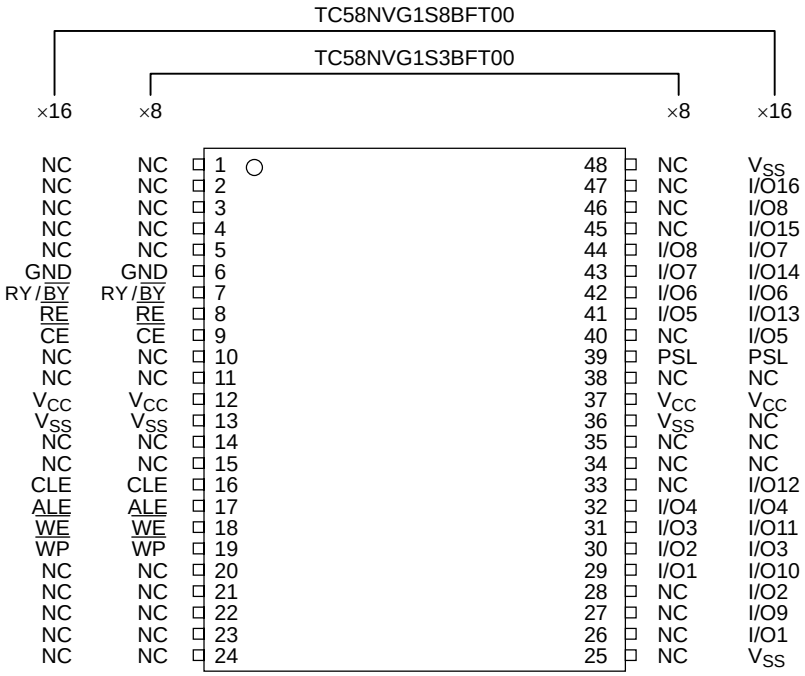
Read (50 ns cycle)	10 mA typ.
Program (avg.)	10 mA typ.
Erase (avg.)	10 mA typ.
Standby	50 µA max

- Package

TC58NVG1S3BFT00	TSOP I 48-P-1220-0.50
TC58NVG1S8BFT00	TSOP I 48-P-1220-0.50

(Weight: 0.53 g typ.)

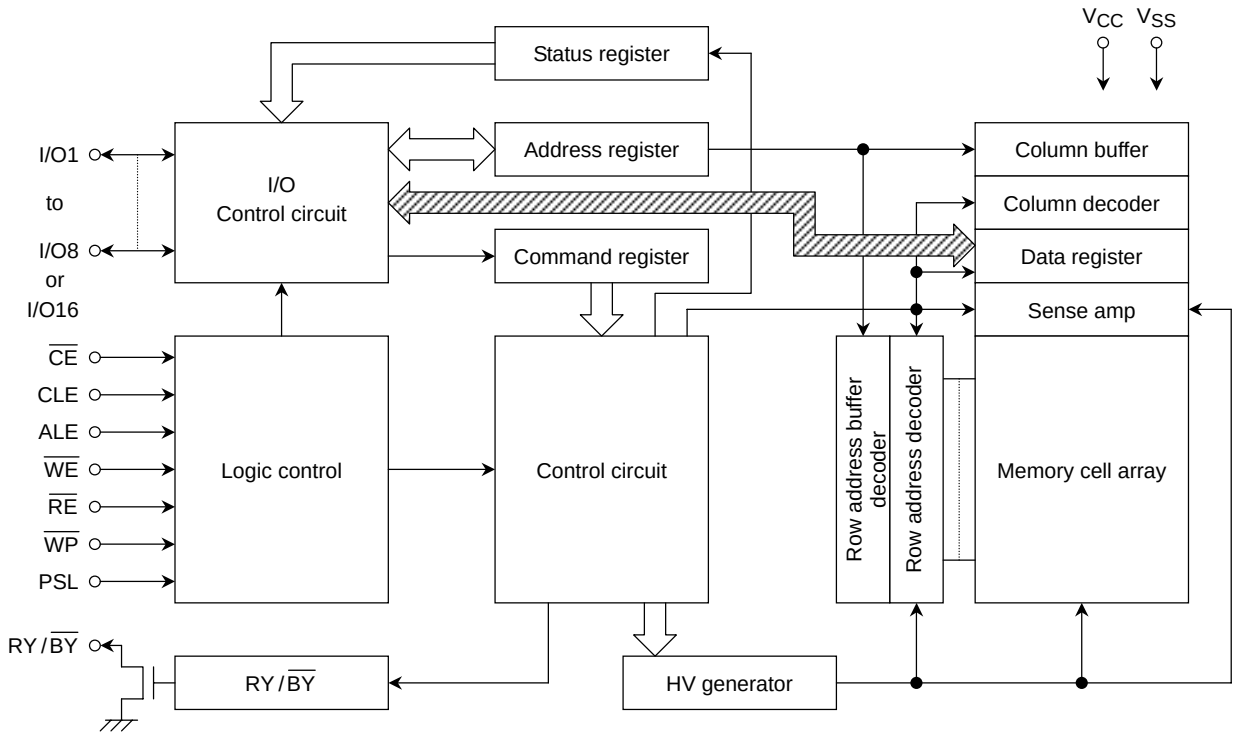
PIN ASSIGNMENT (TOP VIEW)



PINNAMES

I/O1 to I/O8	I/O port
I/O9 to I/O16	I/O port (×16)
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
PSL	Power on select
$\overline{WP}$	Write protect
RY/$\overline{BY}$	Ready/Busy
GND	Ground
V_{CC}	Power supply
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 4.6	V
V_{IN}	Input Voltage	−0.6 to 4.6	V
$V_{I/O}$	Input /Output Voltage	−0.6 V to V_{CC} + 0.3 V (≤ 4.6 V)	V
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	−55 to 150	°C
T_{OPR}	Operating Temperature	0 to 70	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMB0L	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	10	pF

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	2008	—	2048	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The minimum number of valid blocks is guaranteed over the lifetime.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER		MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage		2.7 V	—	3.6 V	V
V_{IH}	High Level input Voltage	2.7 V ≤ V_{CC} ≤ 3.6 V	2.0	—	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	2.7 V ≤ V_{CC} ≤ 3.6 V	−0.3*	—	0.8	V

* −2 V (pulse width lower than 20 ns)

DC CHARACTERISTICS (Ta = 0 to 70℃, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	±10	μA
I_{CCO0}*	Power On Reset Current	PSL = GND or NC	—	10	30	mA
		PSL = V_{CC}, FFh command input after Power On	—	10	30	
I_{CCO1}	Serial Read Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, tcycle = 50 ns	—	10	30	mA
I_{CCO2}	Programming Current	—	—	10	30	mA
I_{CCO3}	Erasing Current	—	—	10	30	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}, $\overline{WP}$ = 0 V/V_{CC}	—	—	1	mA
I_{CCS2}	Standby Current	$\overline{CE}$ = V_{CC} − 0.2 V, $\overline{WP}$ = 0 V/V_{CC}	—	10	50	μA
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	2.4	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA (2.7 V ≤ V_{CC} ≤ 3.6 V)	—	—	0.4	V
I_{OL} (RY/$\overline{BY}$)	Output current of RY/$\overline{BY}$ pin	V_{OL} = 0.4 V (2.7 V ≤ V_{CC} ≤ 3.6 V)	—	8	—	mA

* Refer to application note (2) for detail

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t_{CLS}	CLE Setup Time	0	—	ns	
t_{CLH}	CLE Hold Time	10	—	ns	
t_{CS}	$\overline{CE}$ Setup Time	0	—	ns	
t_{CH}	$\overline{CE}$ Hold Time	10	—	ns	
t_{WP}	Write Pulse Width	25	—	ns	
t_{ALS}	ALE Setup Time	0	—	ns	
t_{ALH}	ALE Hold Time	10	—	ns	
t_{DS}	Data Setup Time	20	—	ns	
t_{DH}	Data Hold Time	10	—	ns	
t_{WC}	Write Cycle Time	50	—	ns	
t_{WH}	$\overline{WE}$ High Hold Time	15	—	ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	—	ns	
t_{RW}	Ready to $\overline{WE}$ Falling Edge	20	—	ns	
t_{RP}	Read Pulse Width	35	—	ns	
t_{RC}	Read Cycle Time	50	—	ns	
t_{REA}	$\overline{RE}$ Access Time	—	35	ns	
t_{CEA}	$\overline{CE}$ Access Time	—	45	ns	
t_{CLEA}	CLE Access Time	—	45	ns	
t_{ALEA}	ALE Access Time	—	45	ns	
t_{OH}	Data Output Hold Time	10	—	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	—	30	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	—	20	ns	
t_{REH}	$\overline{RE}$ High Hold Time	15	—	ns	
t_{IR}	Output-High-impedance-to-$\overline{RE}$ Falling Edge	0	—	ns	
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	30	—	ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	30	—	ns	
t_{R}	Memory Cell Array to Starting Address	—	25	μs	
t_{WB}	$\overline{WE}$ High to Busy	—	200	ns	
t_{RST}	Device Reset Time (Ready/Read/Program/Erase)	—	6/6/10/500	μs	

AC TEST CONDITIONS

PARAMETER	CONDITION
	$2.7\ V \leq V_{CC} \leq 3.6\ V$
Input level	2.4 V, 0.4 V
Input pulse rise and fall time	3ns
Input comparison level	1.5 V, 1.5 V
Output data comparison level	1.5 V, 1.5 V
Output load	C_L (100 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the $RY/\overline{BY}$ pin.
(Refer to Application Note (9) toward the end of this document.)

PROGRAMMING AND ERASING CHARACTERISTICS

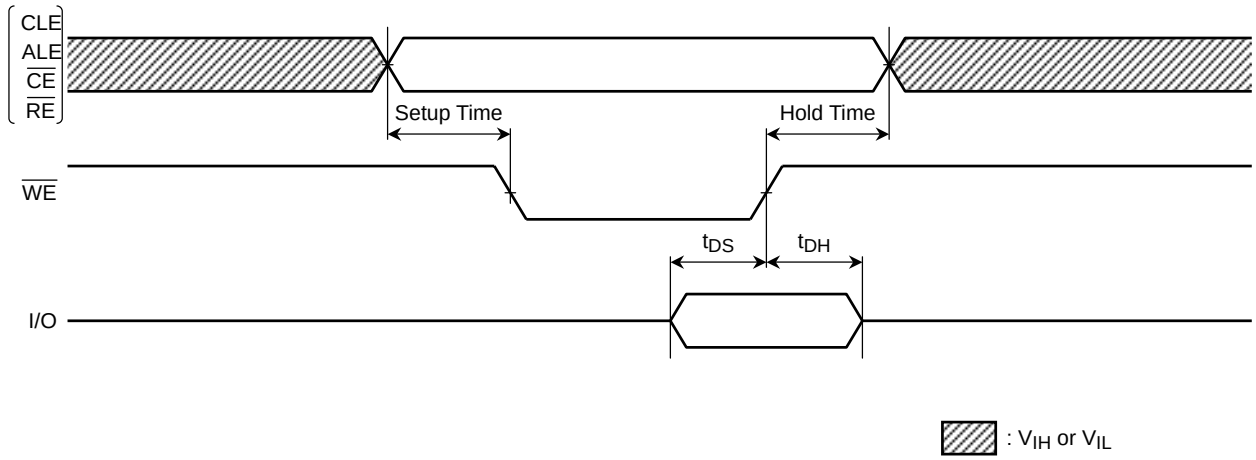
(Ta = 0 to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Average Programming Time	—	200	500	μs	
N	Number of Partial Program Cycles in the Same Page	—	—	8		(1)
t_{BERASE}	Block Erasing Time	—	1.5	3	ms	

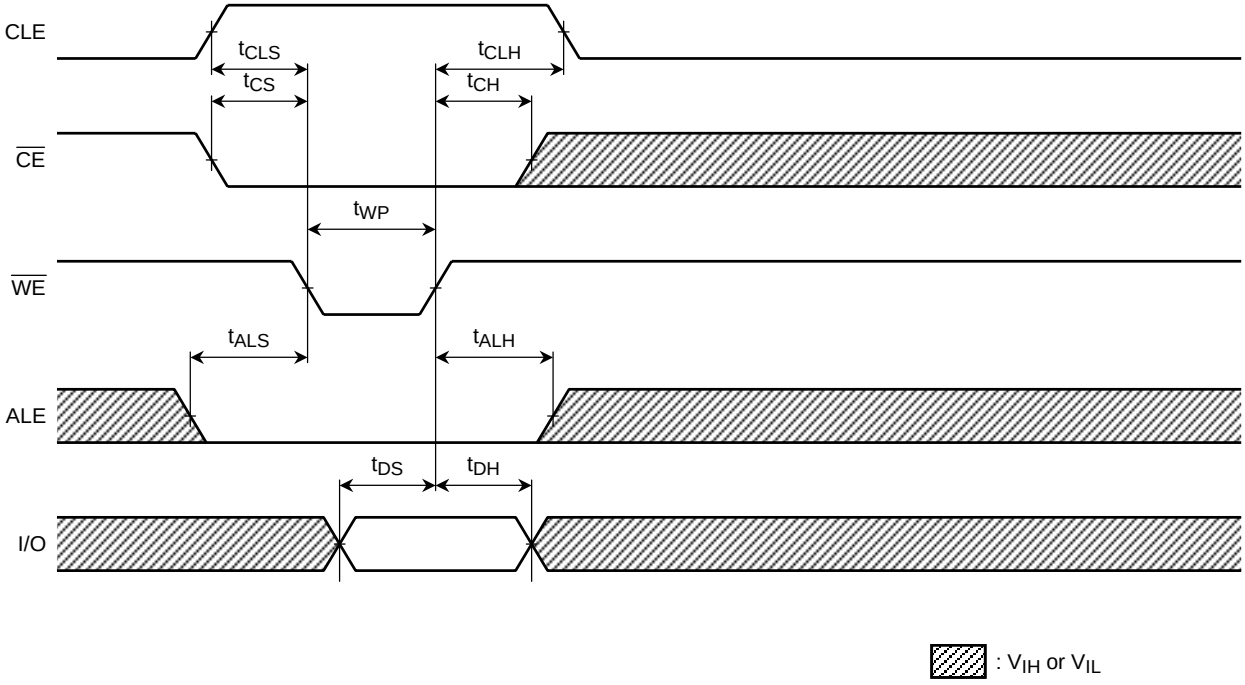
(1) Refer to Application Note (12) toward the end of this document.

TIMING DIAGRAMS

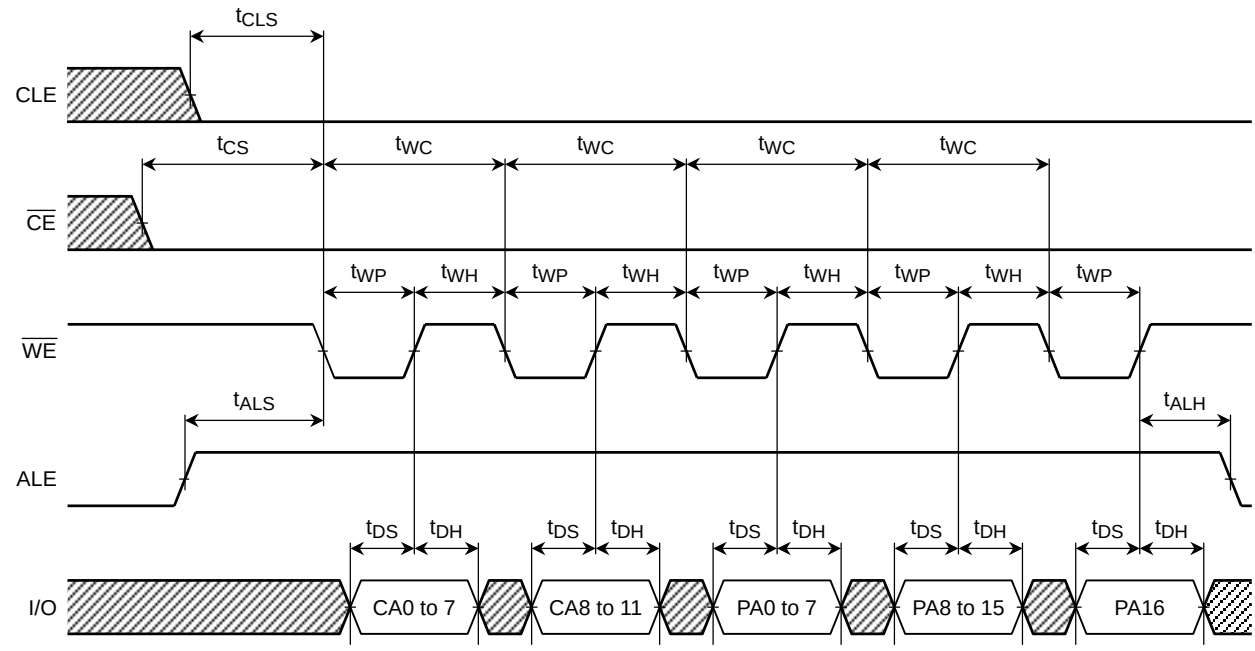
Latch Timing Diagram for Command/Address/Data



Command Input Cycle Timing Diagram

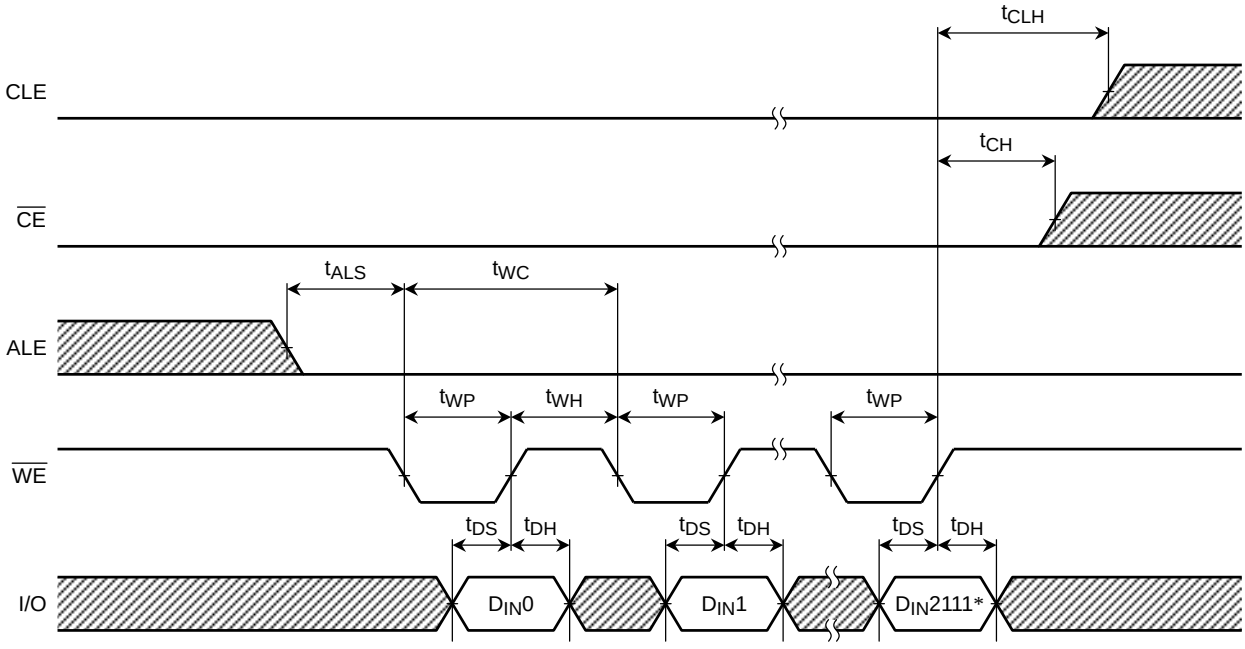


Address Input Cycle Timing Diagram



: V_{IH} or V_{IL}

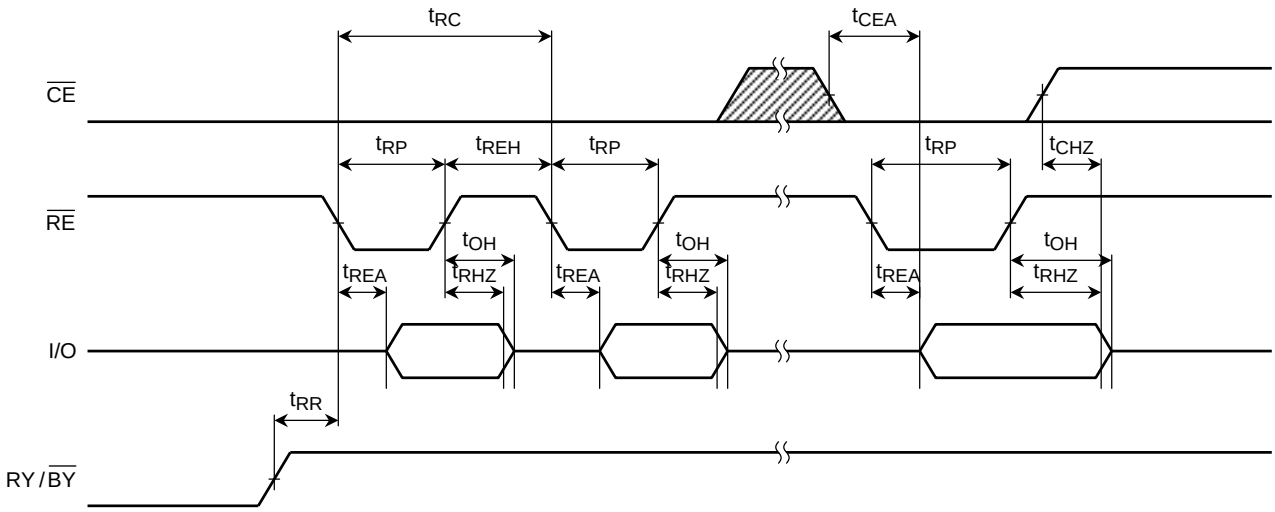
Data Input Cycle Timing Diagram



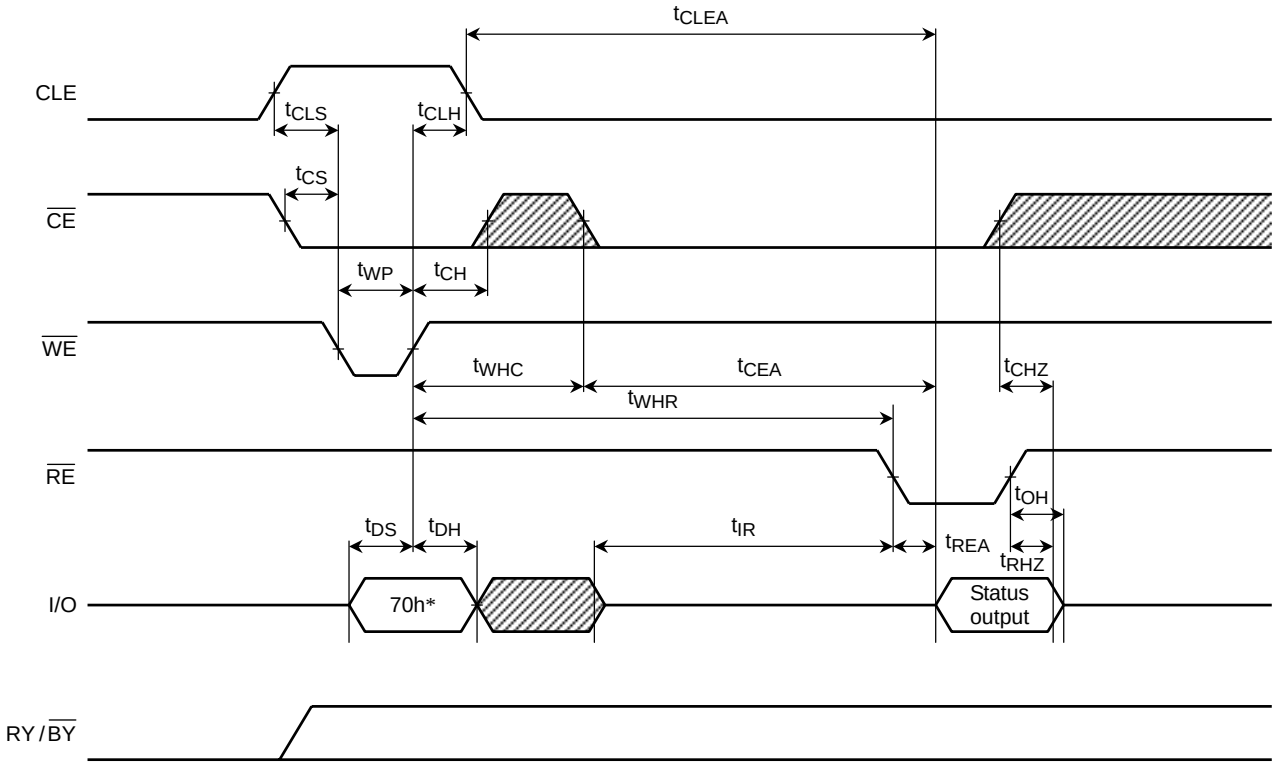
*) ×16: 1055

: V_{IH} or V_{IL}

Serial Read Cycle Timing Diagram



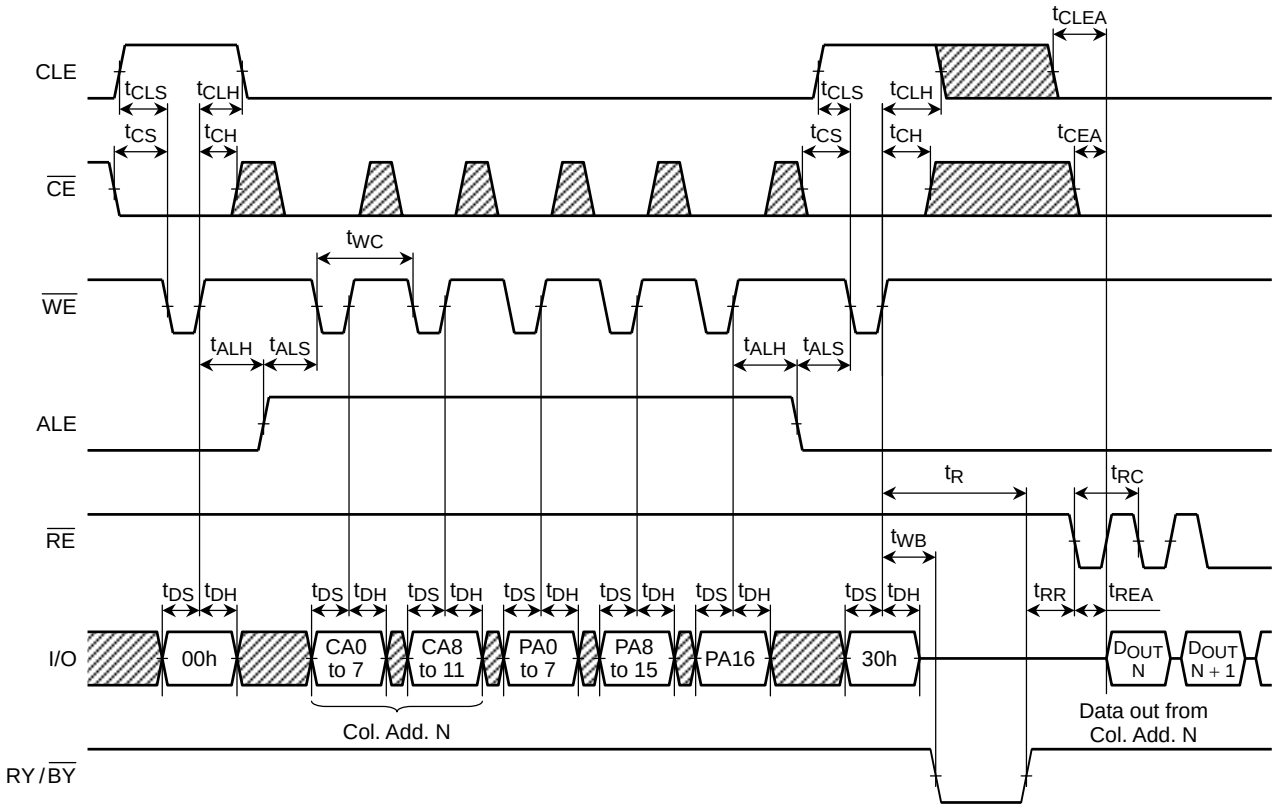
Status Read Cycle Timing Diagram



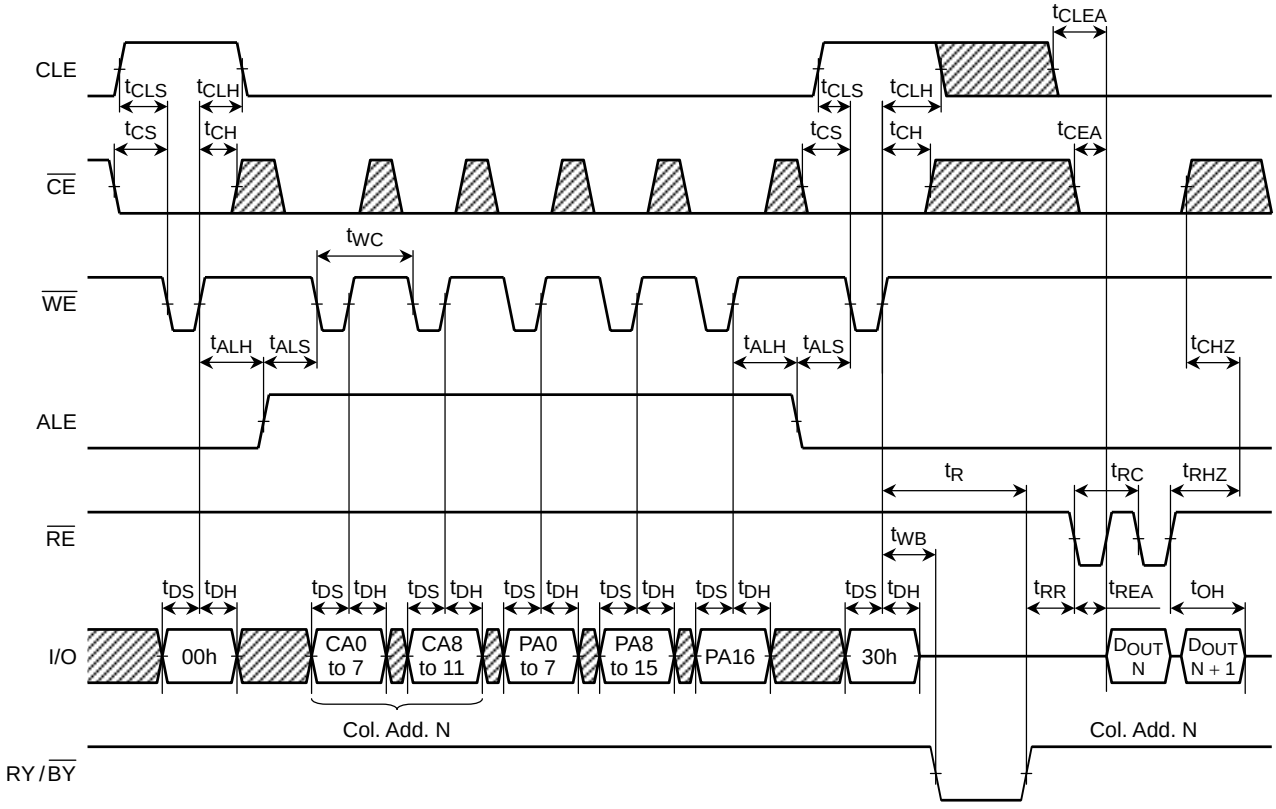
*: 70h represents the hexadecimal number

: V_{IH} or V_{IL}

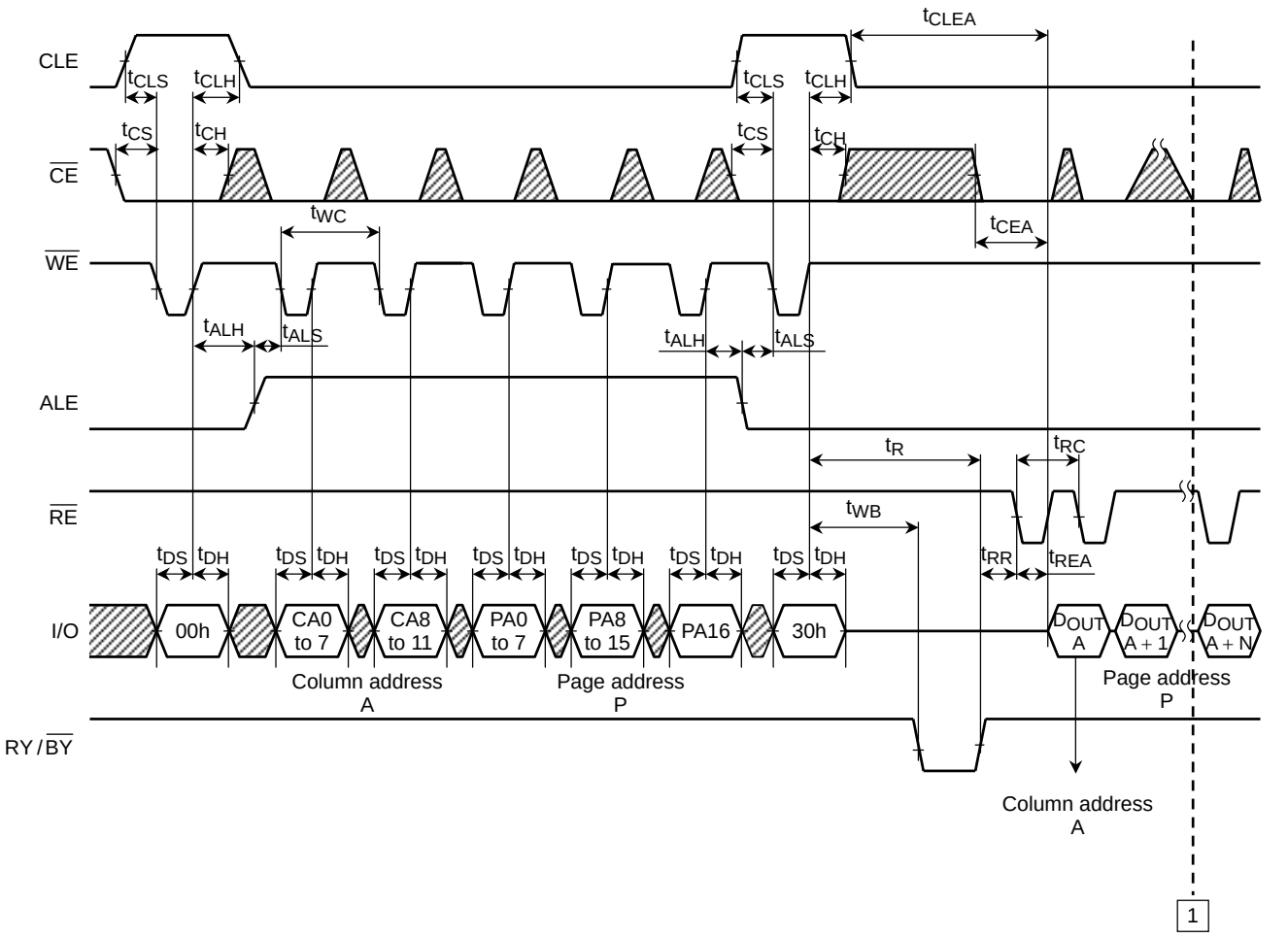
Read Cycle Timing Diagram



Read Cycle Timing Diagram: When Interrupted by $\overline{CE}$



Column Address Change in Read Cycle Timing Diagram (1/2)



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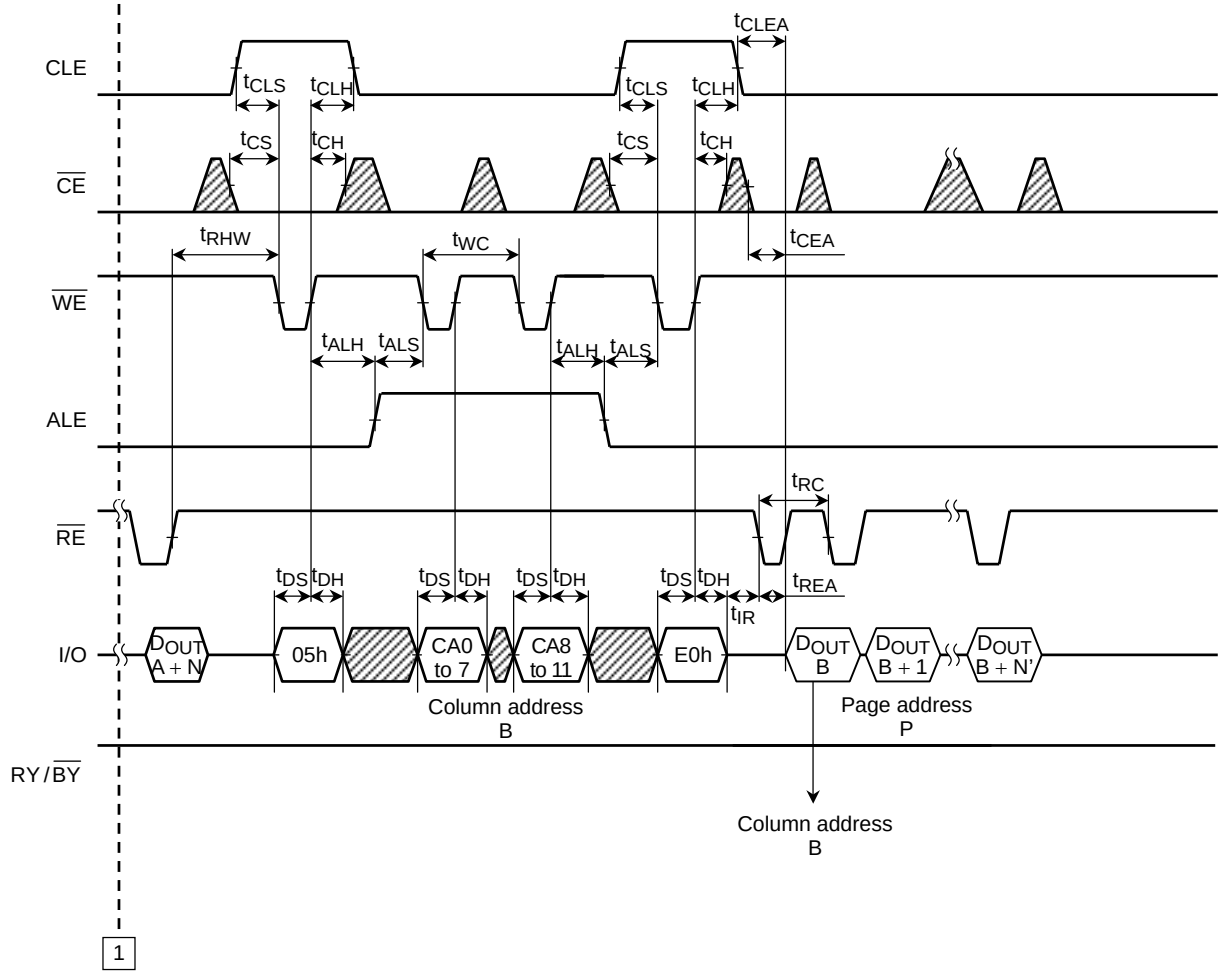
Column Address Change in Read Cycle Timing Diagram (2/2)



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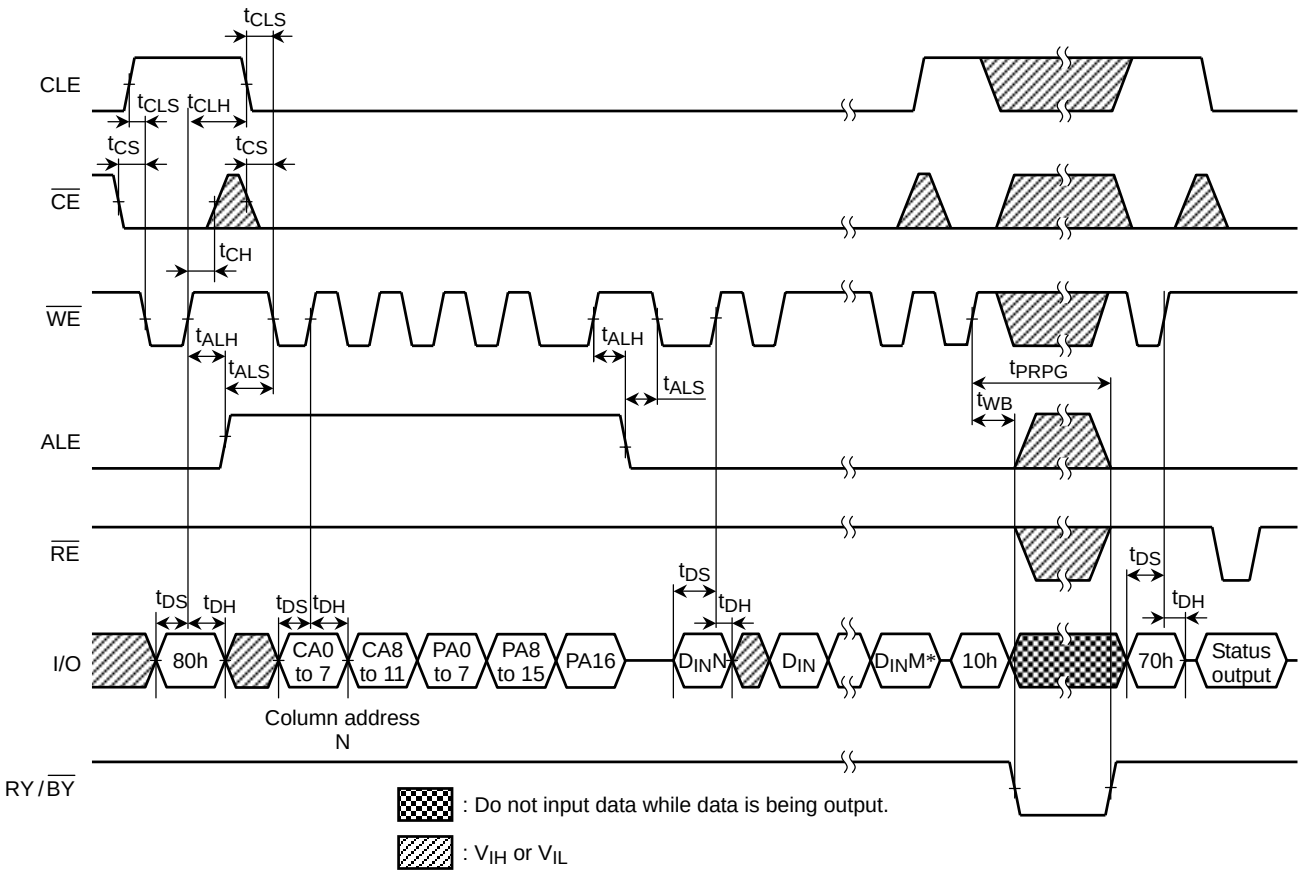
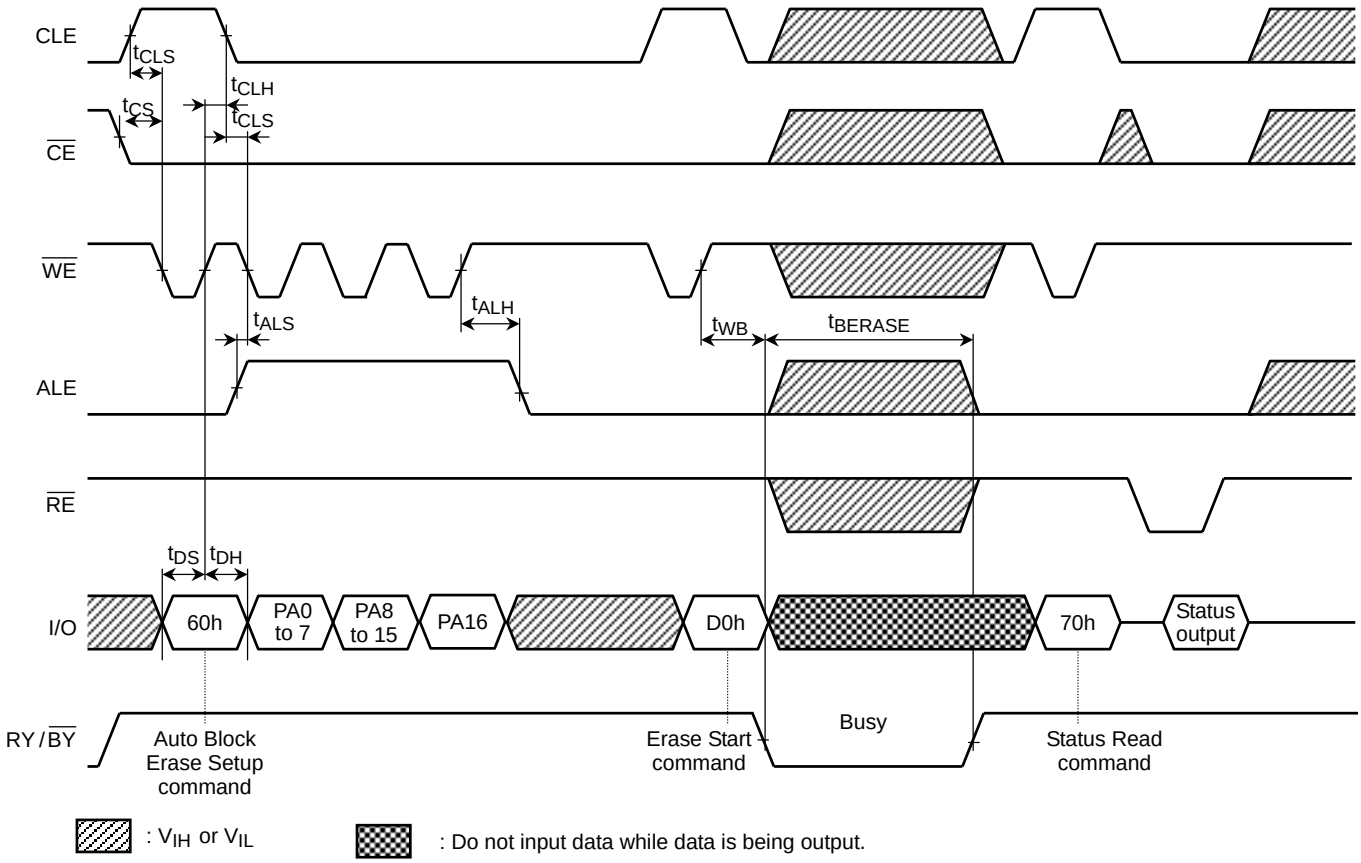
Auto-Program Operation Timing Diagram

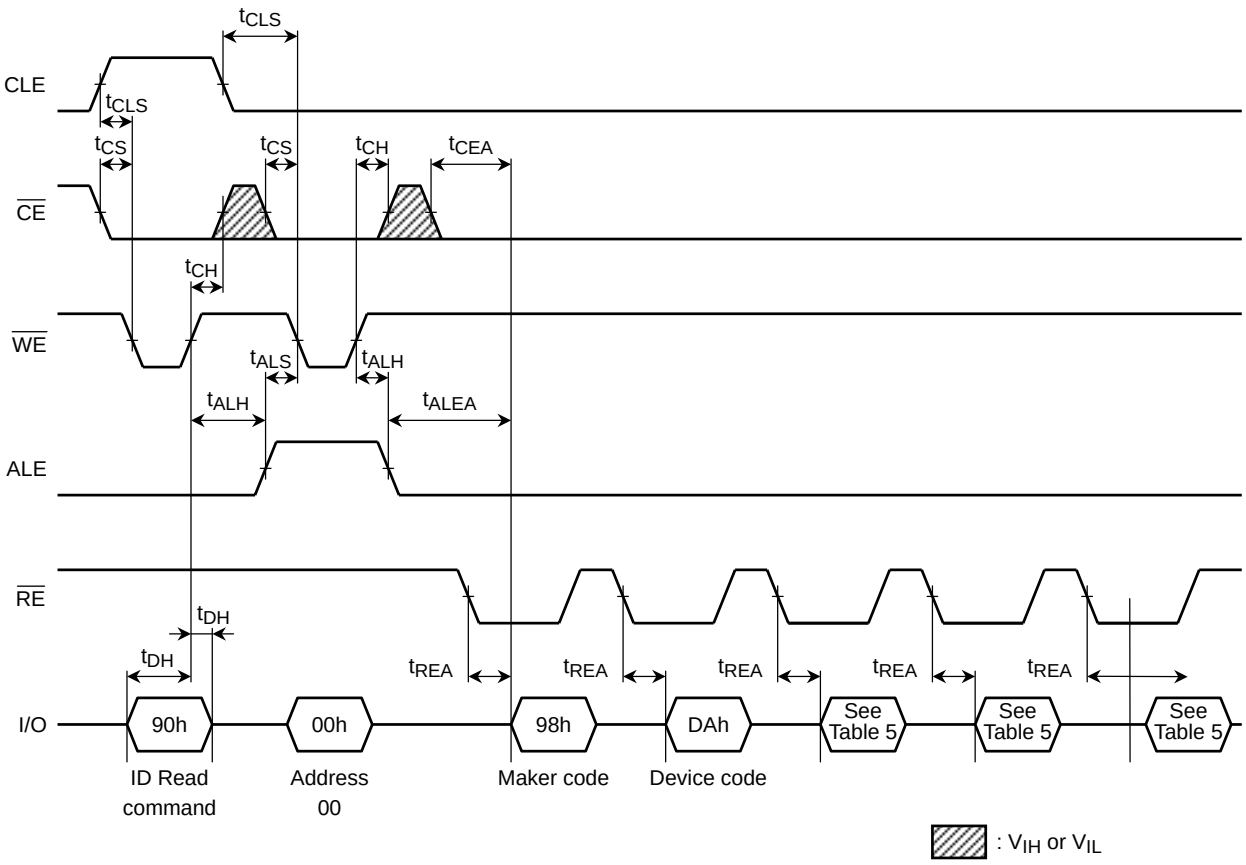


*) M: up to 2112 (byte input data for ×8 device).
M: up to 1056 (word input data for ×16 device).

Auto Block Erase Timing Diagram



ID Read Operation Timing Diagram



PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O port on the rising edge of $\overline{WE}$ while ALE is High.

Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when $\overline{CE}$ goes High during the device is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state ($RY/\overline{BY}$ = L), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address = Address + l) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

I/O Port: I/O9 to 16 (×16 device)

The I/O9 to 16 pins are used as a port for transferring input/output data to and from the device. I/O9 to 16 pins must be low level (VIL) when address and command are input.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: $RY/\overline{BY}$

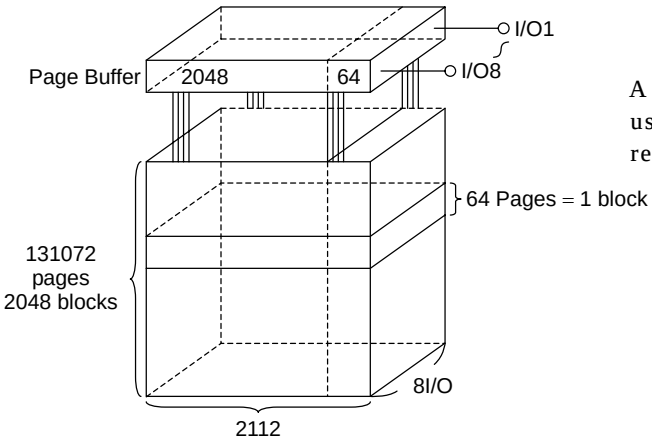
The $RY/\overline{BY}$ output signal is used to indicate the operating condition of the device. The $RY/\overline{BY}$ signal is in Busy state ($RY/\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state ($RY/\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain and has to be pulled-up to Vccq with an appropriate resister.

Power on Select: PSL

The PSL signal is used to select whether the device initialization should take place during the device power on or during the first Reset. Please refer to the application note (2) for details.

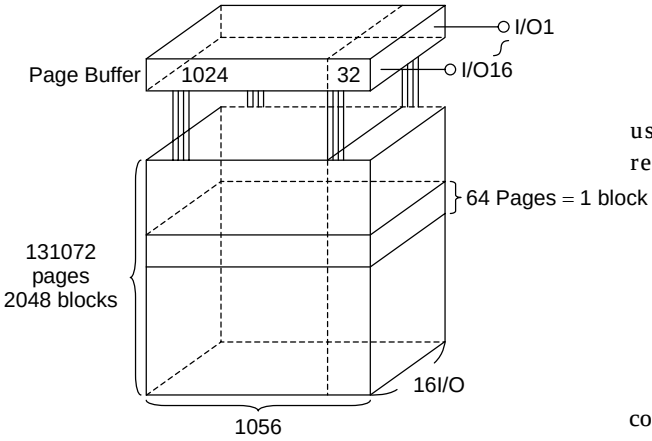
Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.



A page consists of 2112 bytes in which 2048 bytes are used for main memory storage and 64 bytes are for redundancy or for other uses.

1 page = 2112 bytes
1 block = 2112 bytes × 64 pages = (128K + 4K) bytes
Capacity = 2112 bytes × 64pages x 2048blocks



A page consists of 1056 words in which 1024 words are used for main memory storage and 32 words are for redundancy or for other uses.

1 page = 1056 words
1 block = 1056 words × 64 pages = (64K + 2K) words
Capacity = 1056 words × 64 pages × 2048 blocks

An address is read in via the I/O port over three consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	L	L	L	L	CA11	CA10	CA9	CA8
Third cycle	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth cycle	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8
Fifth cycle	L	L	L	L	L	L	L	PA16

CA0 to CA11: Column address
PA0 to PA16: Page address

PA6 to PA16: Block address
PA0 to PA5: NAND address in block

Note) I/O9 − 16 must be held low when address is input (×16 device).

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L		H	*
Data Input	L	L	L		H	H
Address input	L	H	L		H	*
Serial Data Output	L	L	L	H		*
During Program (Busy)	*	*	*	*	*	H
During Erase (Busy)	*	*	*	*	*	H
During Read (Busy)	*	*	H	*	*	*
	*	*	L	H (*2)	H (*2)	*
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V/V_{CC}

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: Refer to Application Note (10) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit

*2: If $\overline{CE}$ is low during read busy, $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to the device or read to device. Reset or Status Read command can be input during Read Busy.

Table 3. Command table (HEX)

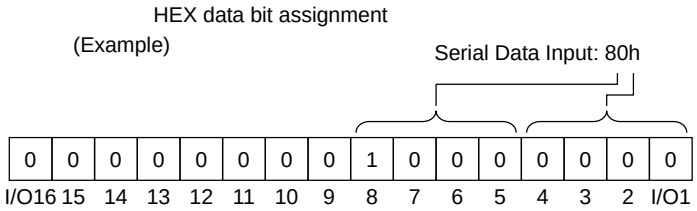
	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read	00	30	
Column Address Change in Serial Data Output	05	E0	
Auto Page Program	80	10	
Column Address Change in Serial Data Input	85	—	
Auto Block Erase	60	D0	
ID Read	90	—	
Status Read	70	—	O
Reset	FF	—	O

Table 4 shows the operation states for Read mode.

Table 4. Read mode operation states

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 to I/O8 (I/O16)	Power
Output select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

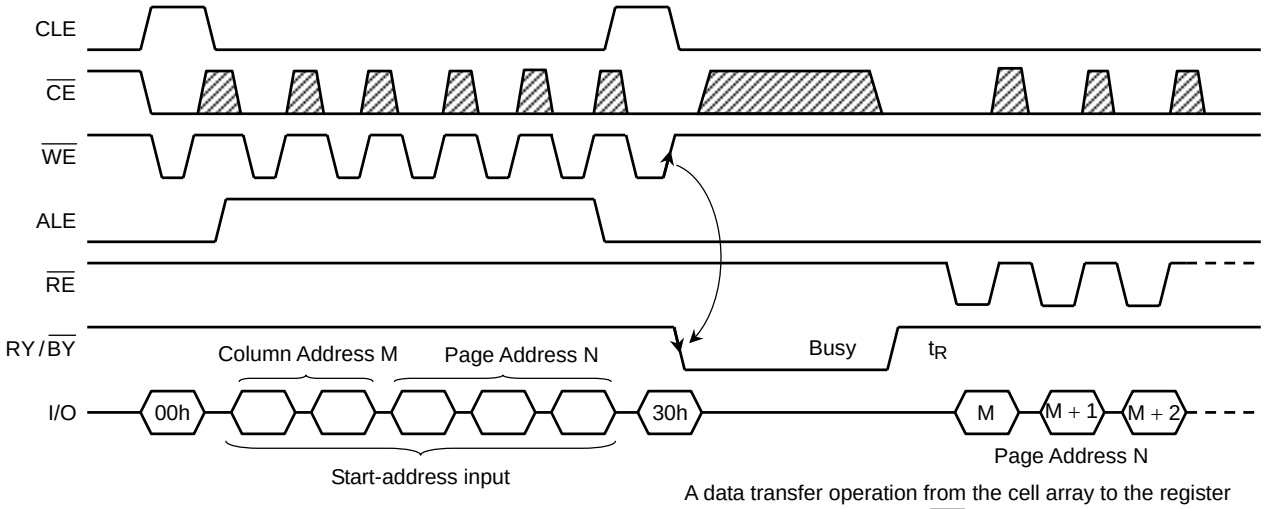
H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}



DEVICE OPERATION

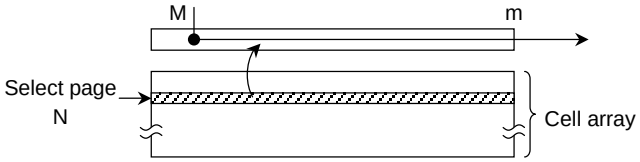
Read Mode

Read mode is set when the "00h" and “30h” commands are issued to the Command register. Between the two commands, a start address for the Read mode needs to be issued. Refer to the figures below for the sequence and the block diagram (Refer to the detailed timing chart.).



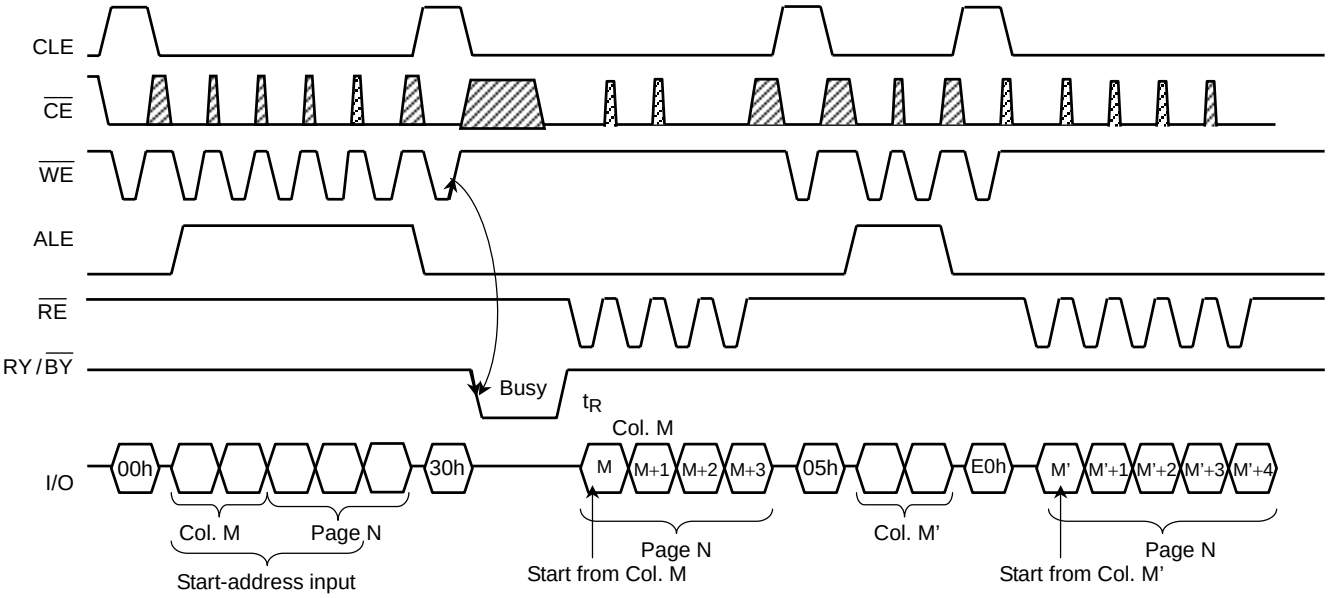
A data transfer operation from the cell array to the register starts on the rising edge of $\overline{WE}$ in the 30h command input cycle (after the address information has been latched). The device will be in the Busy state during this transfer period.

After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start address designated in the address input cycle.

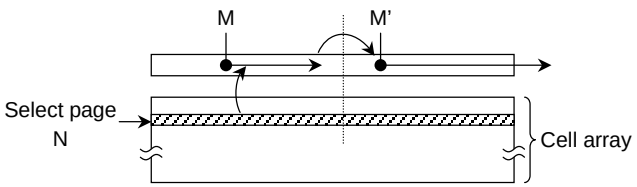


I/O1 to 8: m = 2111
I/O1 to 16: m = 1055

Random Column Address Change in Read Cycle

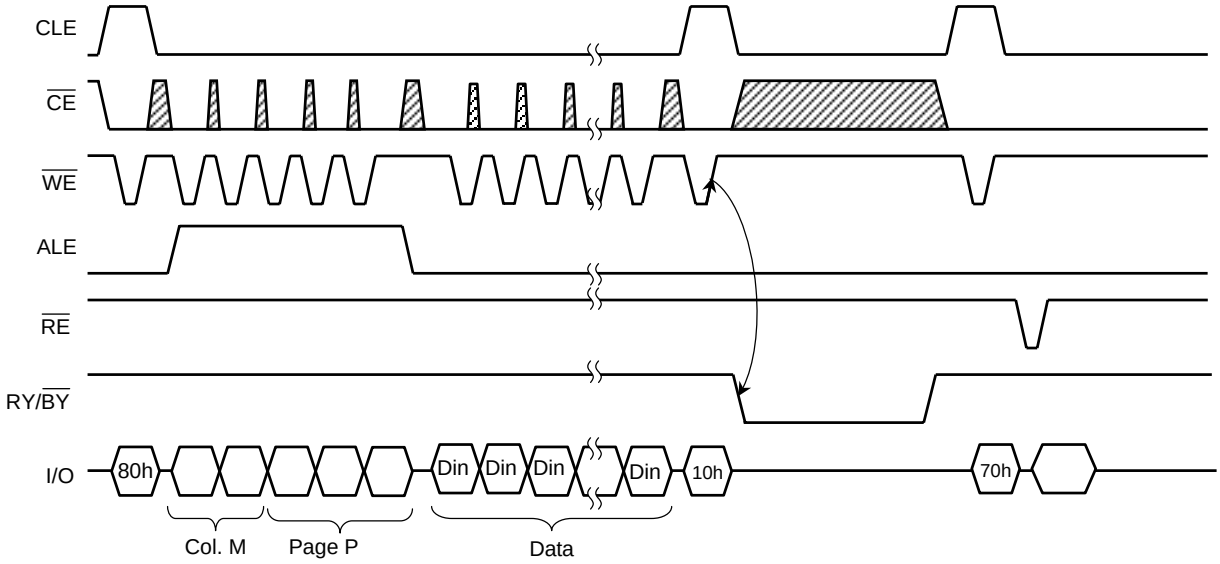


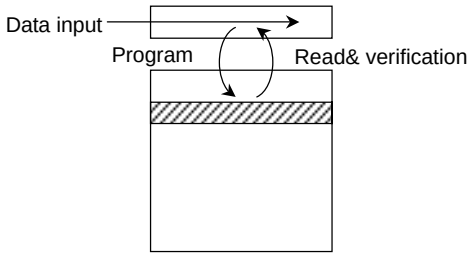
During the serial data output from the register the column address can be changed by inputting a new column address using the 05h and E0h commands. The data is read out in serial starting at the new column address. Random Column Address Change operation can be done multiple times within the same page.



Auto Page Program Operation

The device carries out an Automatic Page Program operation when it receives a "10h" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)



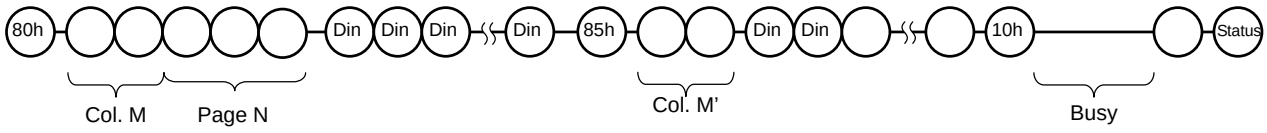


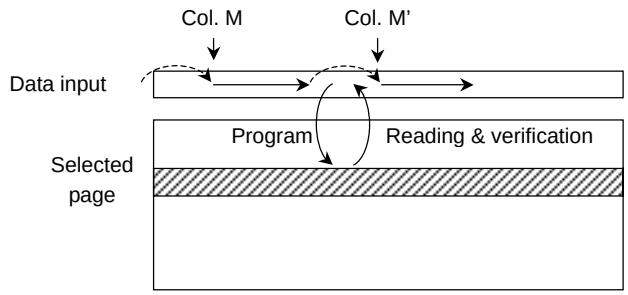
The data is transferred (programmed) from the register to the selected page on the rising edge of $\overline{WE}$ following input of the “10h” command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Random Column Address Change in Auto Page Program Operation

The column address can be changed by the 85h command during the data input sequence of the Auto Page Program operation.

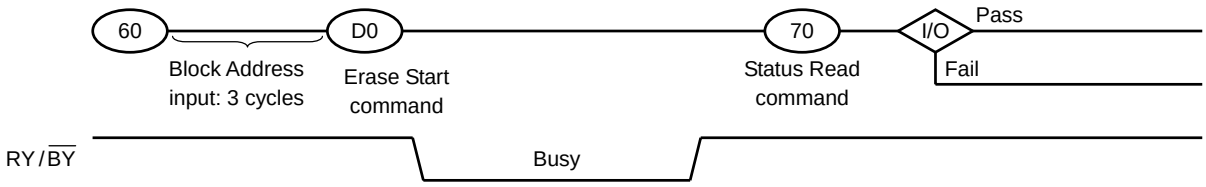
Two address input cycles after the 85h command are recognized as a new column address for the data input. After the new data is input to the new column address, the 10h command initiates the actual data program into the selected page automatically. The Random Column Address Change operation can be repeated multiple times within the same page.





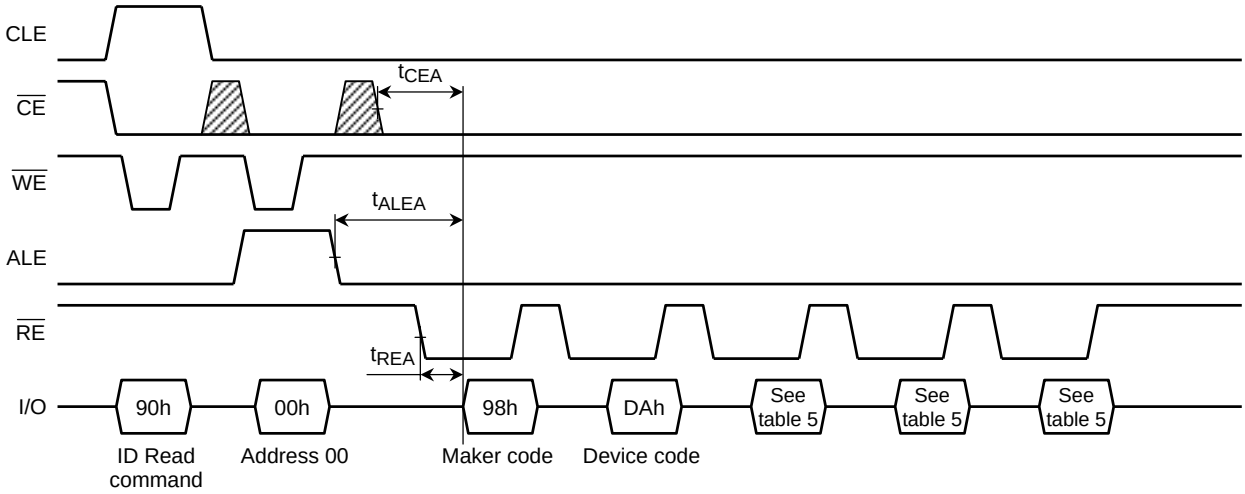
Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Start command "D0h" which follows the Erase Setup command "60h". This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:



For the specifications of the access times t_{REAI}, t_{CEA} and t_{ALEA} refer to the AC Characteristics.

Table 5. Code table

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98h
2nd Data	Device Code	1	1	0	1	1	0	1	0	DAh
3rd Data	Chip Number, Cell Type, PGM Page	0 or 1	0	0	0	0	0	0	0	00h or 80h
4th Data	Page Size, Block Size, Redundant Size, Organization	0 or 1	0 or 1	0	1	0	1	0	1	×8) 15h or 95h ×16) 55h or D5h
5th Data	Plane Number, Plane Size	0 or 1	1	0	0	0	1	0	0	44h or C4h

3rd Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 level cell 4 level cell 8 level cell 16 level cell					0 0 1 1	0 1 0 1		
Number of simultaneously programmed pages	1 2 4 8			0 0 1 1	0 1 0 1				
Reserved		0 or 1	0						

4th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Page Size (without redundant area)	1 KB 2 KB 4K KB 8 KB							0 0 1 1	0 1 0 1
Block Size (without redundant area)	64 KB 128 KB 256 KB 512 KB			0 0 1 1	0 1 0 1				
Redundant area size (byte/512byte)	8 16 Reserved Reserved					0 0 1 1	0 1 0 1		
Organization	×8 ×16		0 1						
Reserved		0 or 1							

5th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Plane Number	1 2 4 8					0 0 1 1	0 1 0 1		
Plane Size	64 Mbit 128 Mbit 256 Mbit 512 Mbit 1 Gbit 2 Gbit 4 Gbit 8 Gbit		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1				
Power Supply	3 V only 1.8 V & 3.3 V dual								0 1
Reserved		0 or 1						0	

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass /fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using $\overline{RE}$ after a "70h" command input. The Status Read can also be used during a Read operation to find out the Ready/Busy status.

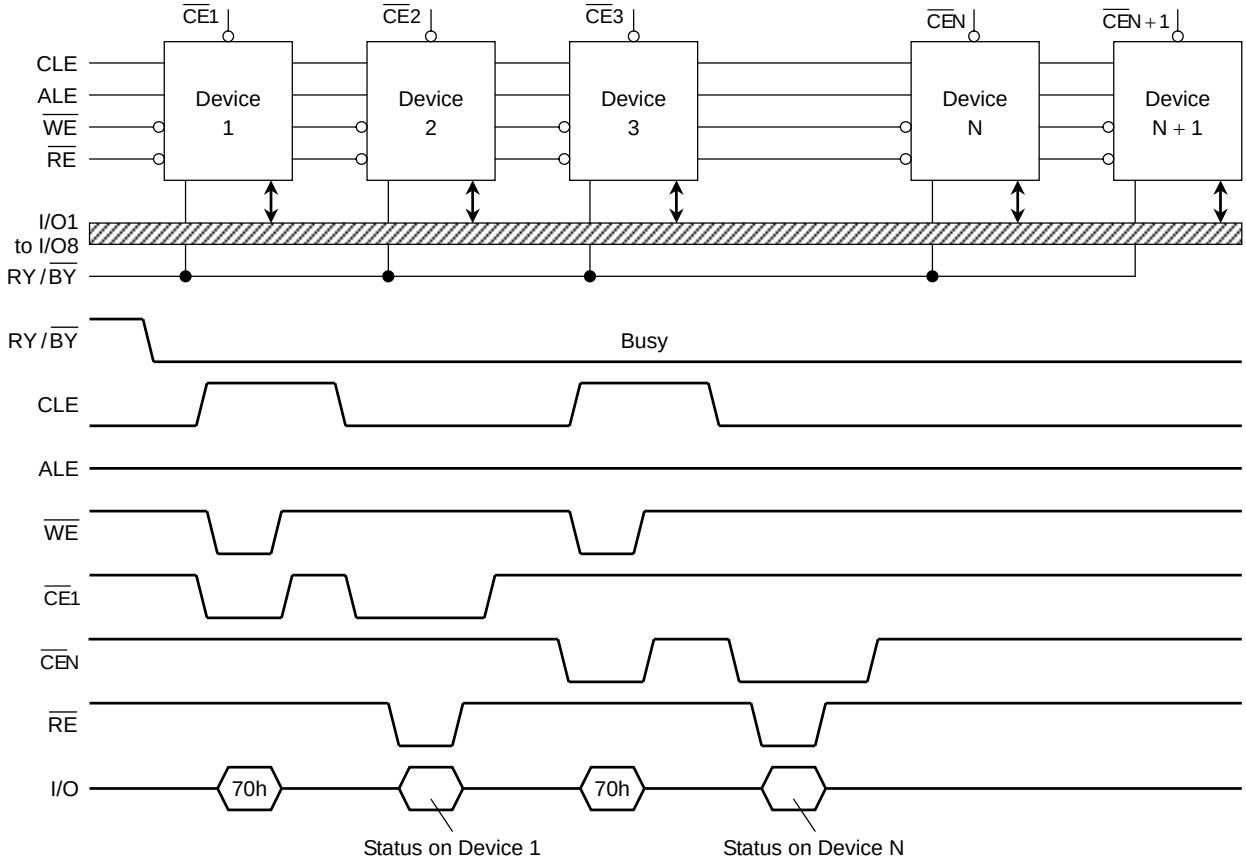
The resulting information is outlined in Table 6.

Table 6. Status output table

	Definition	Page Program Block Erase	Read
I/O1	Chip Status1 Pass: 0 Fail: 1	Pass/Fail	Invalid
I/O2	Not Used	Invalid	Invalid
I/O3	Not Used	0	0
I/O4	Not Used	0	0
I/O5	Not Used	0	0
I/O6	Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy
I/O7	Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy
I/O8	Write Protect Not Protected :0 Protected: 1	Write Protect	Write Protect
I/O9 to 16	Not used	Not used	Not used

The Pass/Fail status on I/O1 is only valid during a Program/Erase operation when the device is in the Ready state.

An application example with multiple devices is shown in the figure below.



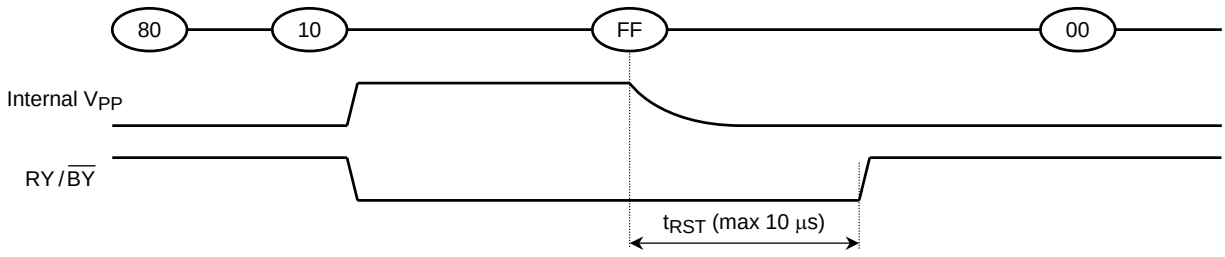
System Design Note: If the RY / $\overline{BY}$ pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Reset

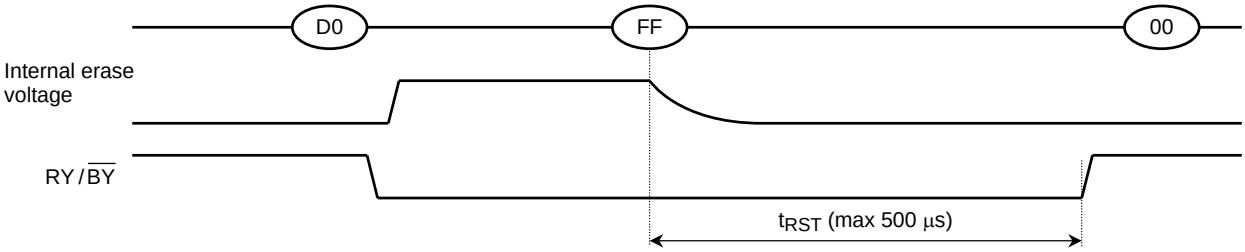
The Reset mode stops all operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged to 0 volt and the device enters the Wait state.

The response to a "FFh" Reset command input during the various device operations is as follows:

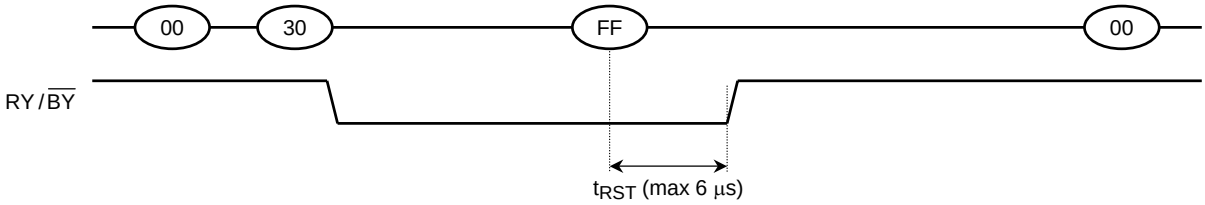
When a Reset (FFh) command is input during programming



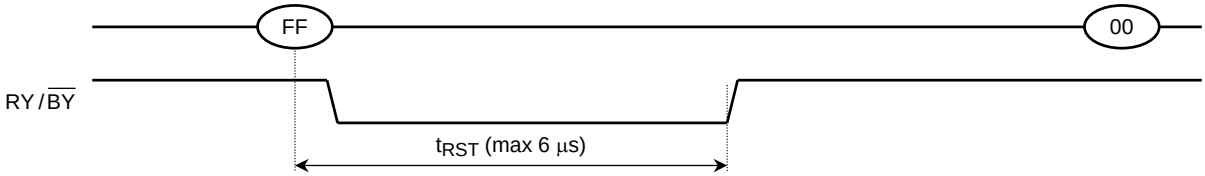
When a Reset (FFh) command is input during erasing



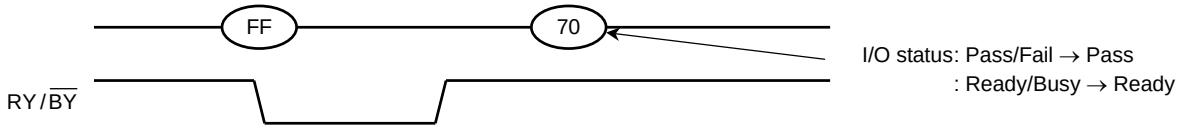
When a Reset (FFh) command is input during Read operation



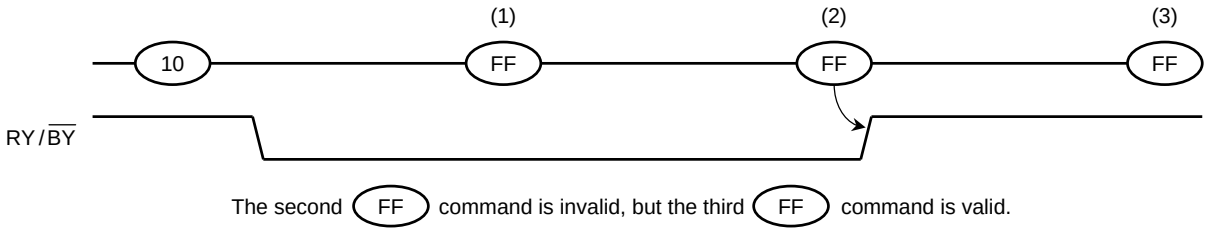
When a Reset (FFh) command is input during Ready



When a Status Read command (70h) is input after a Reset



When two or more Reset commands are input in succession



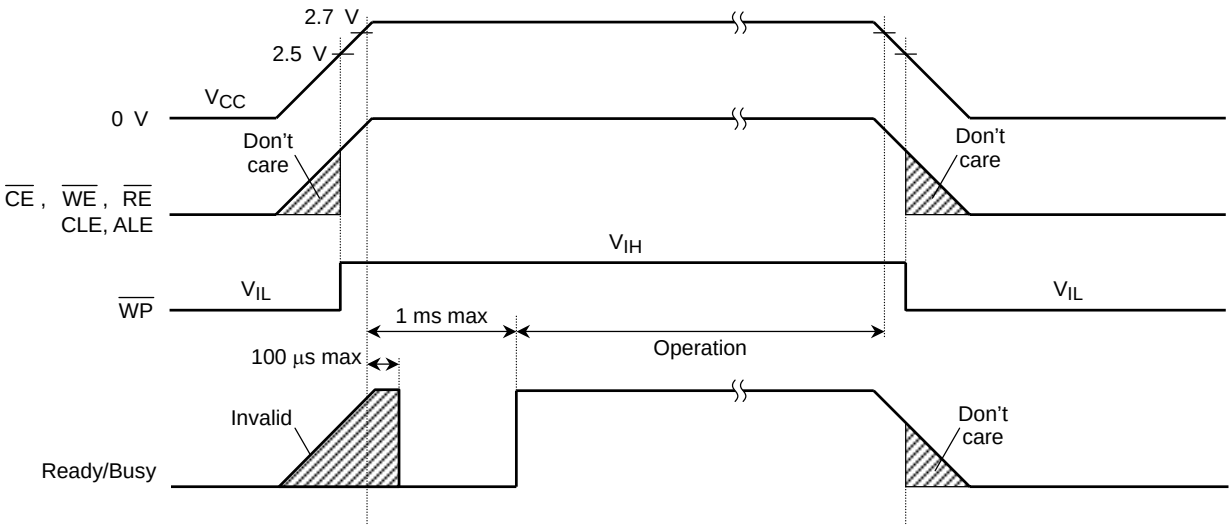
APPLICATION NOTES AND COMMENTS

(1) Power-on/off sequence:

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

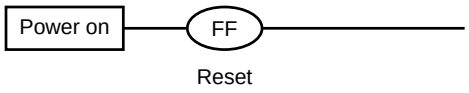
The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device Ready/Busy signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are FFh or 70h.

The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off.



(2) Power-on Reset

The device goes into automatic self initialization during power on if PSL is tied either to GND or NC. During the initialization process, the device consumes a maximum current of 30 mA (I_{CCO0}). If PSL is tied to VCC, the device will not complete its self initialization during power on and will not consume I_{CCO0}, and completes the initialization process with the first Reset command input after power on. During the first FFh reset Busy period, the device consumes a maximum current of 30 mA (I_{CCO0}). In either case (PSL = GND/ NC or V_{CC}), the following sequence is necessary because some input signals may not be stable at power-on.



(3) Prohibition of unspecified commands

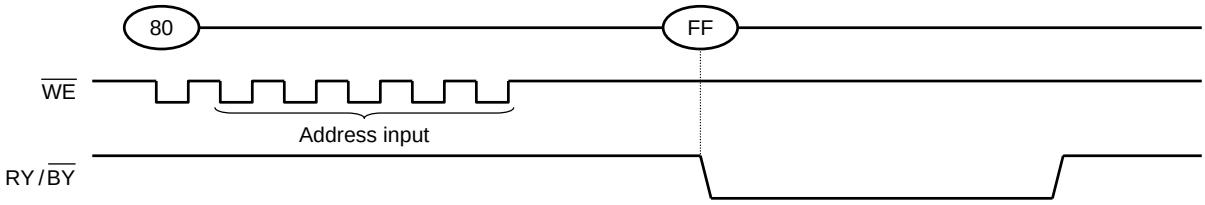
The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(4) Restriction of commands while in the Busy state

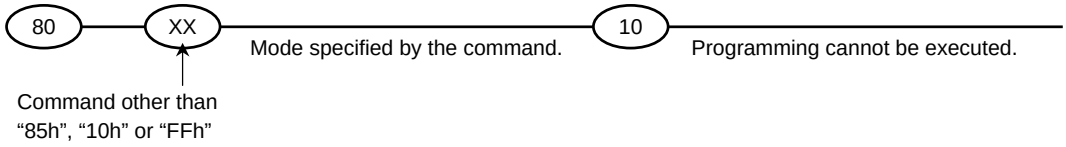
During the Busy state, do not input any command except 70h and FFh.

(5) Acceptable commands after Serial Input command “80h”

Once the Serial Input command “80h” has been input, do not input any command other than the Column Address Change in Serial Data Input command “85h”, Auto Program command “10h”, or the Reset command “FFh”.

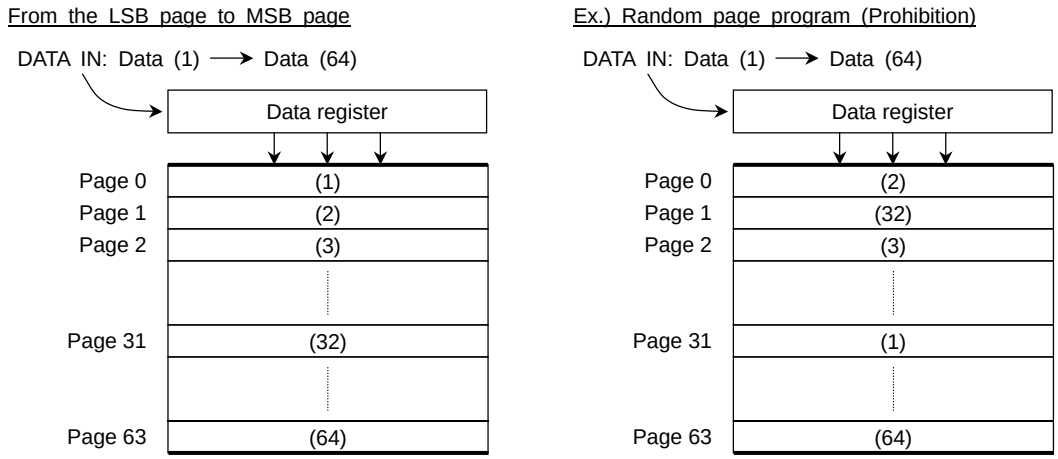


If a command other than “85h”, “10h” or “FFh” is input, the Program operation is not performed and the device operation is set to the mode which the input command specifies.

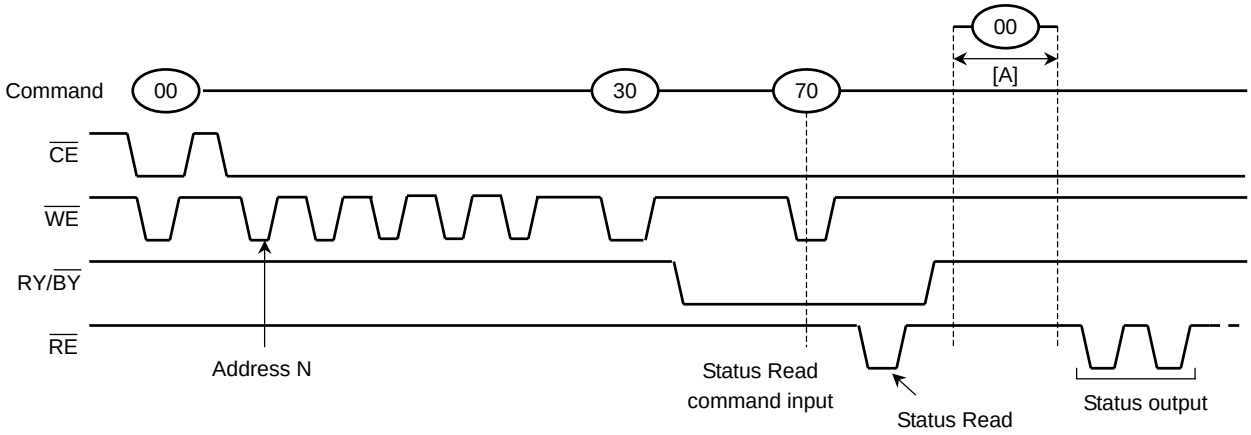


(6) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.

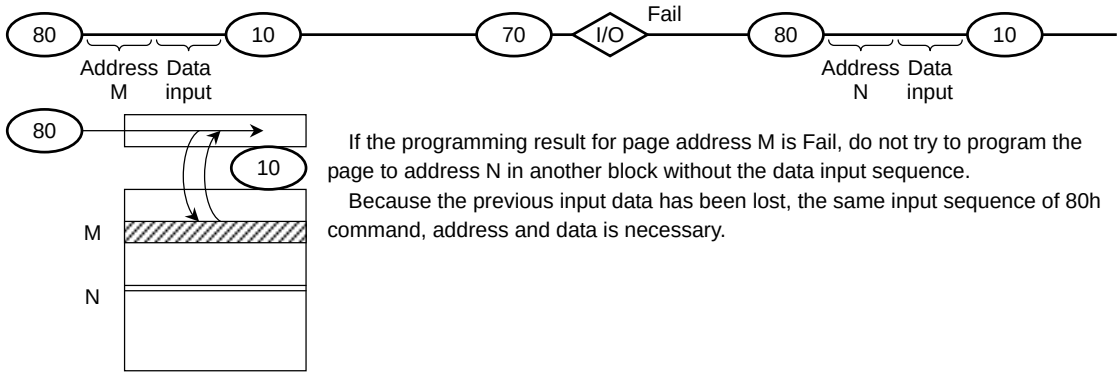


(7) Status Read during a Read operation



The device status can be read out by inputting the Status Read command "70h" in Read mode. Once the device has been set to Status Read mode by a "70h" command, the device will not return to Read mode unless the Read command "00h" is input during [A]. In this case, data output starts automatically from address N and address input is unnecessary

(8) Auto programming failure

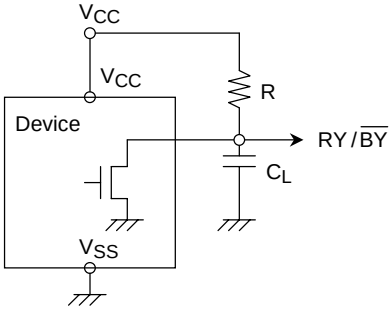


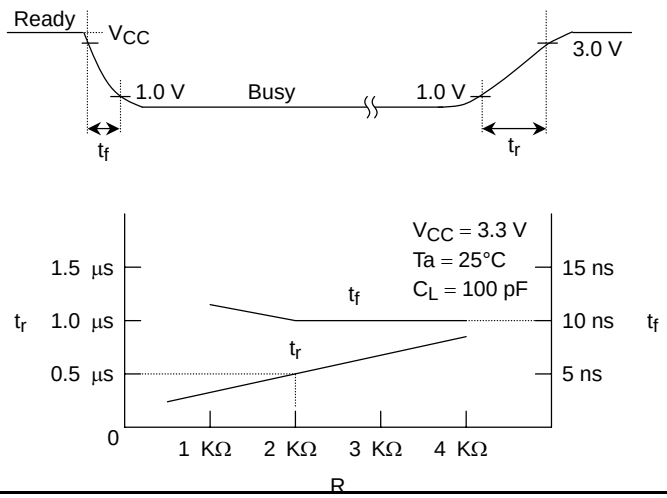
If the programming result for page address M is Fail, do not try to program the page to address N in another block without the data input sequence.

Because the previous input data has been lost, the same input sequence of 80h command, address and data is necessary.

(9) RY / $\overline{BY}$: termination for the Ready/Busy pin (RY / $\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY / $\overline{BY}$ buffer consists of an open drain circuit.



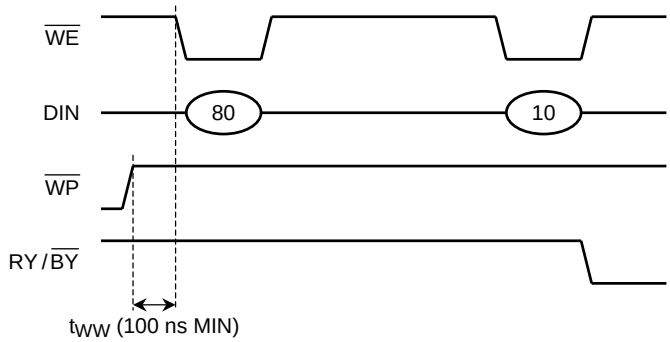


This data may vary from device to device.
We recommend that you use this data as a reference when selecting a resistor value.

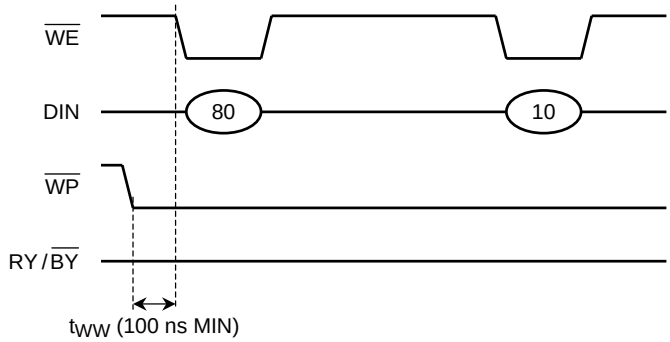
(10) Note regarding the $\overline{WP}$ signal

The Erase and Program operations are automatically reset when $\overline{WP}$ goes Low. The operations are enabled and disabled as follows:

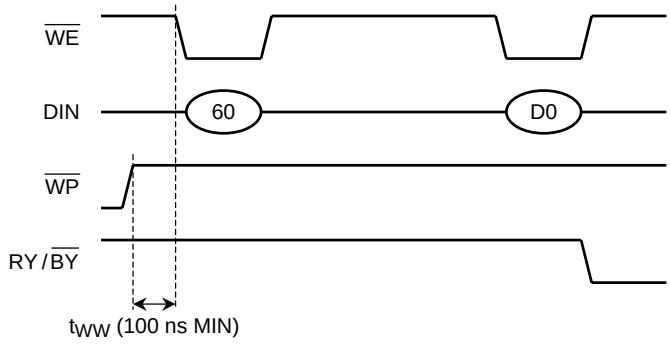
Enable Programming



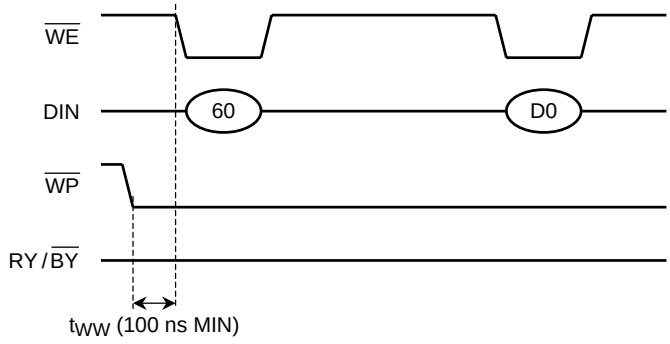
Disable Programming



Enable Erasing

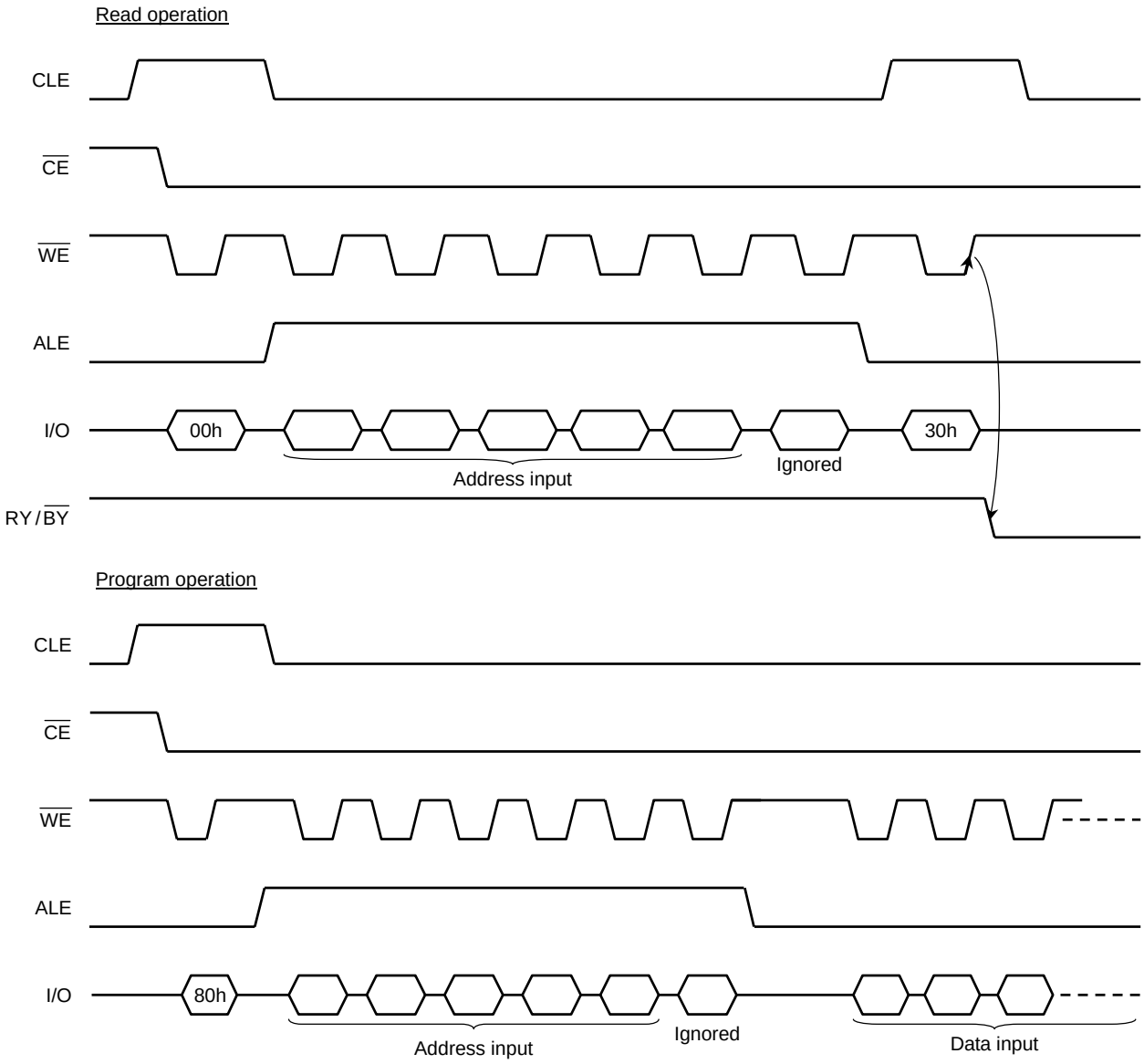


Disable Erasing



(11) When six address cycles are input

Although the device may read in a sixth address, it is ignored inside the chip.



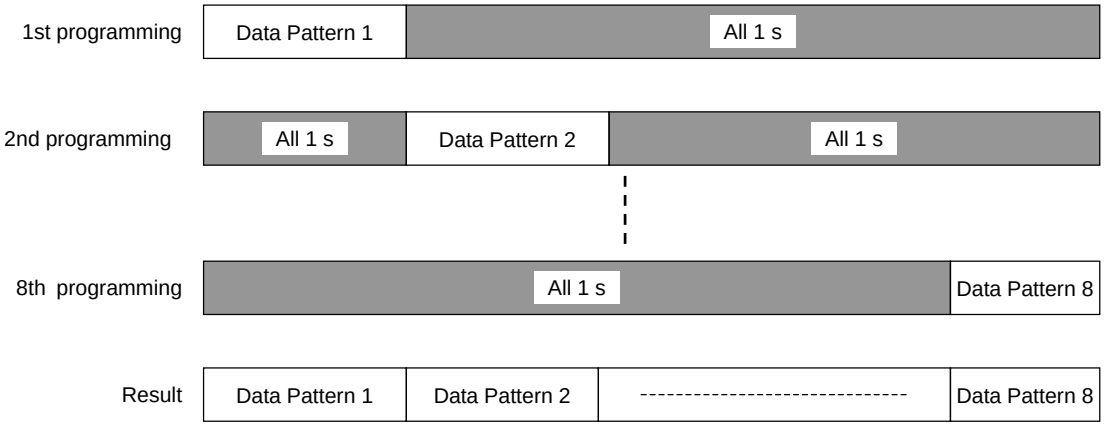
(12) Several programming cycles on the same page (Partial Page Program)

A page can be divided into up to 8 segments as follows:

Data area (column address 0 to 2047) : 512 bytes × 4 segments
- 1st segment: column address 0 to 511
- 2nd segment: column address 512 to 1023
- 3rd segment: column address 1024 to 1535
- 4th segment: column address 1536 to 2047

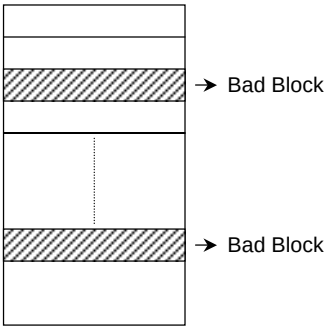
Redundant area (column address 2048 to 2111) : 16 bytes × 4 segments
- 1st segment: column address 2048 to 2063
- 2nd segment: column address 2064 to 2079
- 3rd segment: column address 2080 to 2095
- 4th segment: column address 2096 to 2111

Each segment can be programmed individually as follows:



(13) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



At the time of shipment, all data bytes in a valid block are FFh. For bad blocks, all bytes are not in the FFh state. Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block information if the information is erased.

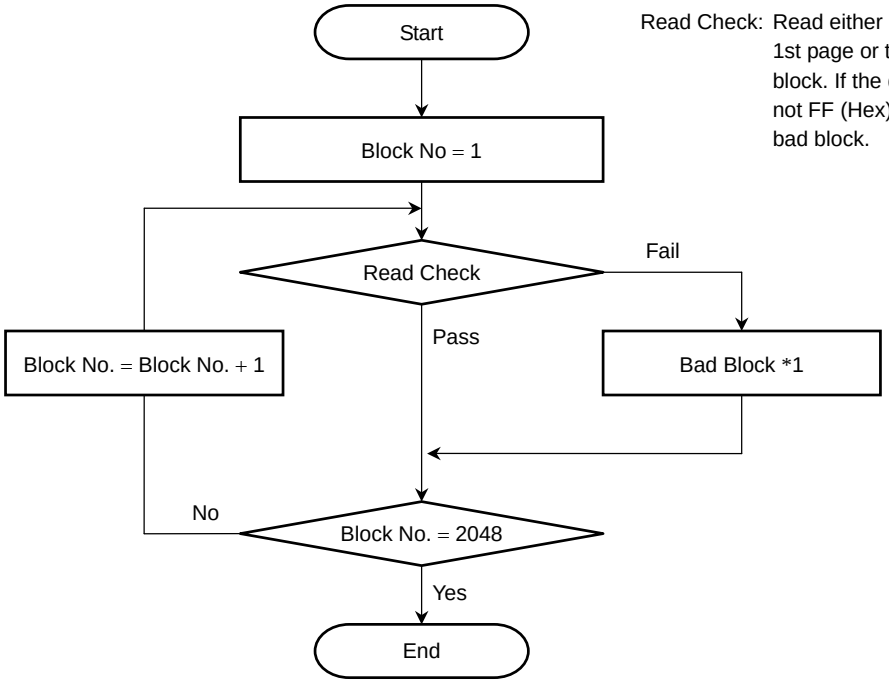
Check if the device has any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates.

The number of valid blocks at the time of shipment is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	2008	—	2048	Block

Bad Block Test Flow



Read Check: Read either column 0 or 2048 of the 1st page or the 2nd page of each block. If the data of the column is not FF (Hex), define the block as a bad block.

*1: No erase operation is allowed to detected bad blocks

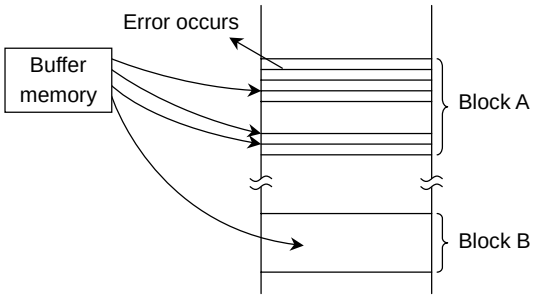
(14) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Single Bit	Programming Failure "1 to 0"	ECC

- ECC: Error Correction Code. 2 bits per page is necessary.
  In case the 2 Kbyte page is divided into segments of 512 bytes, 1 bit correction per segment is necessary.
- Block Replacement

Program



When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

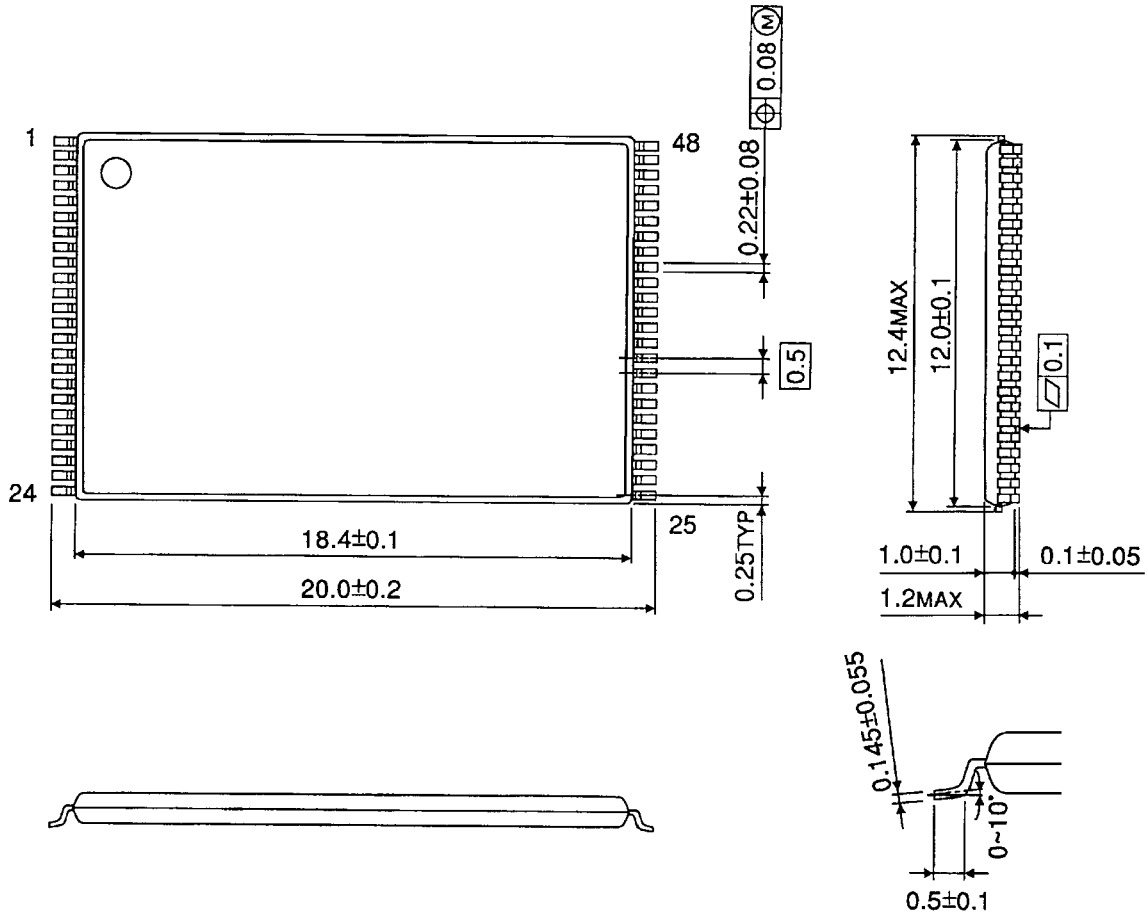
Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(15) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

Package Dimensions

TSOP I 48-P-1220-0.50 Unit : mm



Weight: 0.53 g (typ.)

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030619EBA

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