4V Drive Nch+Nch MOSFET

SP8K64

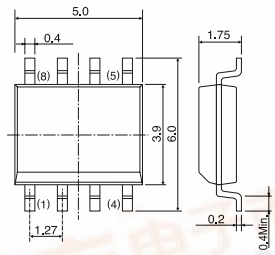
●Structure
Silicon N-channel MOSFET

●Features
1) Low on-resistance.
2) Built-in G-S Protection Diode.
3) Small surface Mount Package (SOP8).

●Application
Switching

●Dimensions (Unit : mm)

SOP8

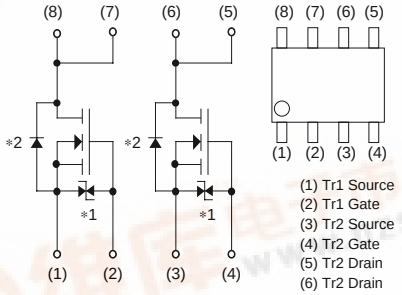


Each lead has same dimensions

●Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SP8K64		○

●Equivalent circuit



(1) Tr1 Source
(2) Tr1 Gate
(3) Tr2 Source
(4) Tr2 Gate
(5) Tr2 Drain
(6) Tr2 Drain
(7) Tr1 Drain
(8) Tr1 Drain

*1 ESD PROTECTION DIODE
*2 BODY DIODE

*A protection diode is included between the gate and the source terminals to protect the diode against static electricity when the product is in use. Use the protection circuit when the fixed voltages are exceeded.

●Absolute maximum ratings (Ta=25°C)
<It is the same ratings for the Tr1 and Tr2.>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D	±9	A
	Pulsed	I_{DP} *1	±36	A
Source current (Body diode)	Continuous	I_S	1.6	A
	Pulsed	I_{SP} *1	36	A
Total power dissipation		P_D *2	2.0	W/TOTAL
			1.4	W/ELEMENT
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	−55 to +150	°C

*1 Pw≤10μs, Duty cycle≤1%
*2 Mounted on a ceramic board.

●**Electrical characteristics** (Ta=25°C)
<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	30	–	–	V	I_D=1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	1	μA	V_{DS}=30V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	1.0	–	2.5	V	V_{DS}=10V, I_D=1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$*	–	14	19	mΩ	I_D=9A, V_{GS}=10V
		–	17	23		I_D=9A, V_{GS}=4.5V
		–	18	24.5		I_D=9A, V_{GS}=4.0V
Forward transfer admittance	$\|Y_{fs}\|$*	6.5	–	–	S	I_D=9A, V_{DS}=10V
Input capacitance	C_{iss}	–	1600	–	pF	V_{DS}=10V
Output capacitance	C_{oss}	–	230	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	190	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$*	–	15	–	ns	I_D=4.5A, V_{DD}≒15V
Rise time	t_r*	–	40	–	ns	V_{GS}=10V
Turn-off delay time	$t_{d\ (off)}$*	–	60	–	ns	R_L=3.33Ω
Fall time	t_f*	–	75	–	ns	R_G=10Ω
Total gate charge	Q_g*	–	15.0	22.5	nC	I_D=9A, V_{DD}≒15V
Gate-source charge	Q_{gs}*	–	4.0	–	nC	V_{GS}=5V
Gate-drain charge	Q_{gd}*	–	4.4	–	nC	R_L=1.67Ω, R_G=10Ω

*Pulsed

●**Body diode characteristics** (Source-Drain) (Ta=25°C)
<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}*	–	–	1.2	V	I_S=9A, V_{GS}=0V

*Pulsed

●**Electrical characteristic curves**

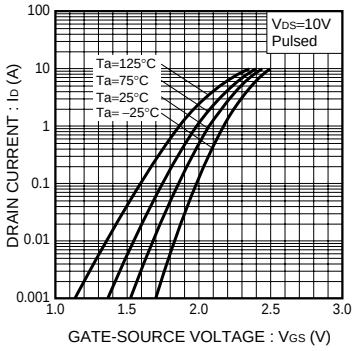


Fig.1 Typical Transfer Characteristics

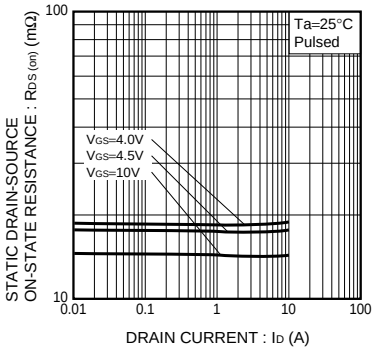


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current(Ⅰ)

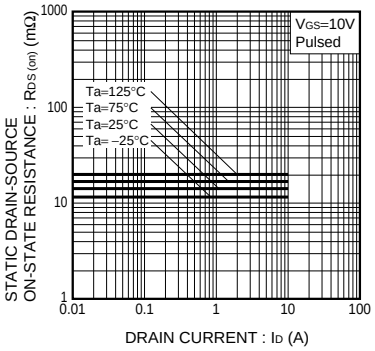


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current(II)

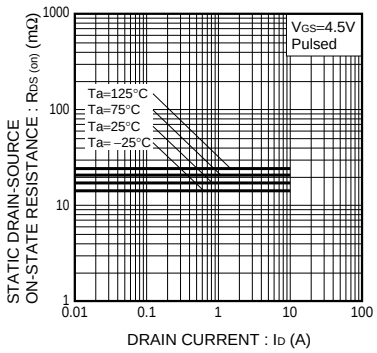


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(III)

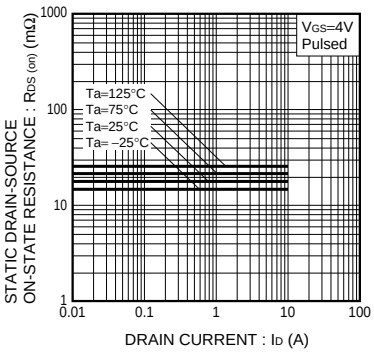


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(Ⅳ)

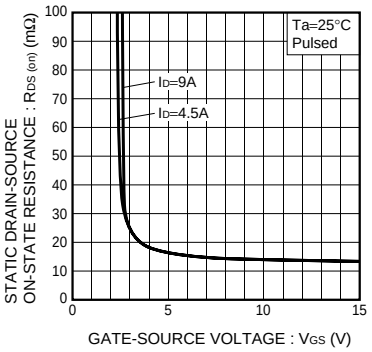


Fig.6 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

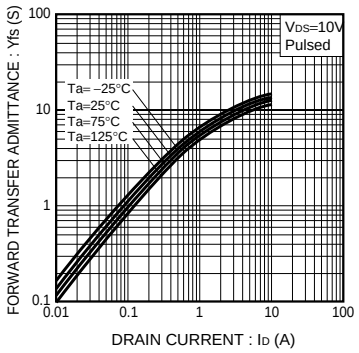


Fig.7 Forward Transfer Admittance vs. Drain Current

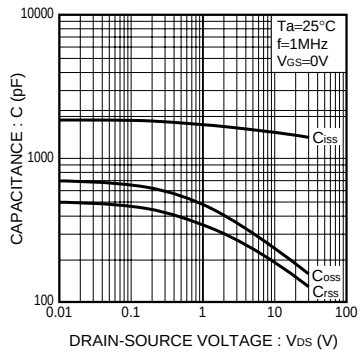


Fig.8 Typical Capacitance vs. Drain-Source Voltage

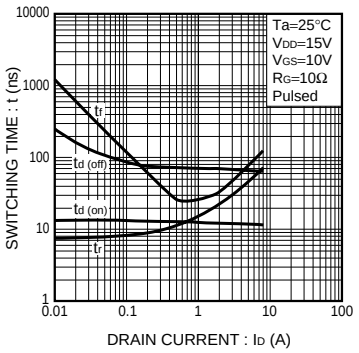


Fig.9 Switching Characteristics

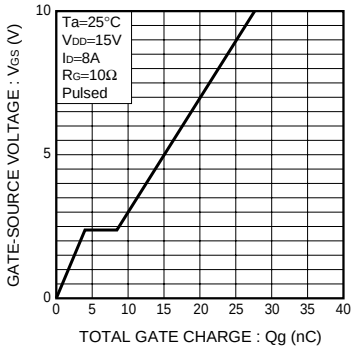


Fig.10 Dynamic Input Characteristics

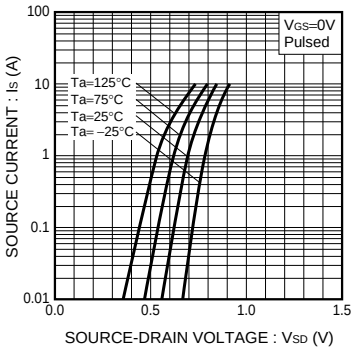


Fig.11 Source Current vs. Source-Drain Voltage

●Measurement circuit

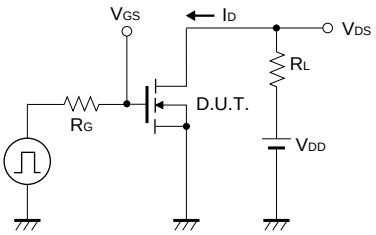


Fig.12 Switching Time Test Circuit

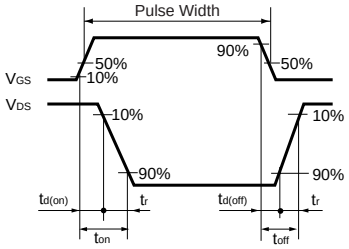


Fig.13 Switching Time Waveforms

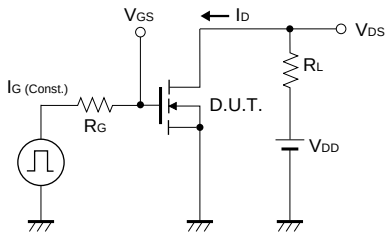


Fig.14 Gate Charge Test Circuit

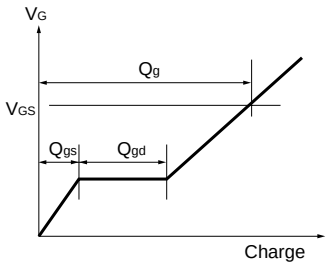


Fig.15 Gate Charge Waveform

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Contact us : webmaster@rohm.co.jp

ROHM CO., LTD. 21 Saiin Mizosaki-cho, Ukyo-ku, Kyoto 615-8585, Japan
TEL : +81-75-311-2121
FAX : +81-75-315-0172