S71WS-J Based MCPs

Stacked Multi-Chip Product (MCP)
I28/64 Megabit (8M/4M x I6-bit) CMOS I.8 Volt-only, Simultaneous Read/Write, Burst Mode Flash Memory with CosmoRAM

Data Sheet

PRELIMINARY

Notice to Readers: This document indicates states the current technical specifications regarding the Spansion product(s) described herein. The Preliminary status of this document indicates that a product qualification has been completed, and that initial production has begun. Due to the phases of the manufacturing process that require maintaining efficiency and quality, this document may be revised by subsequent versions or modifications due to changes in technical specifications.

Publication Number S71WS-J_04 **Revision** A **Amendment** 2 **Issue Date** August 19, 2005

Notice On Data Sheet Designations

Spansion LLC issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion LLC is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion LLC therefore places the following conditions upon Advance Information content:

> "This document contains information on one or more products under development at Spansion LLC. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion LLC reserves the right to change or discontinue work on this proposed product without notice."

Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. The Preliminary status of this document indicates that product qualification has been completed, and that initial production has begun. Due to the phases of the manufacturing process that require maintaining efficiency and quality, this document may be revised by subsequent versions or modifications due to changes in technical specifications."

Combination

Some data sheets will contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document will distinguish these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with DC Characteristics table and AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion LLC deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local AMD or Fujitsu sales office.

S71WS-J Based MCPs

Stacked Multi-Chip Product (MCP)
I28/64 Megabit (8M/4M x I6-bit) CMOS I.8 Volt-only, Simultaneous Read/Write, Burst Mode Flash Memory with CosmoRAM

Data Sheet

PRELIMINARY

Distinctive Characteristics

MCP Features

- **Power supply voltage of 1.7 to 1.95V**
- **Speed: 66MHz**
- **Packages:**
  - 8 x 11.6mm, 84 ball FBGA
  - 7 x 9mm, 80-ball FBGA
- **Operating Temperature**
  - –25°C to +85°C

General Description

The S71WS series is a product line of stacked Multi-Chip Product (MCP) packages and consists of:

- One or more flash memory die
- pSRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to the individual constituent datasheets for further details:

		Flash Memory Density		
		256Mb	I28Mb	64Mb
pSRAM Density	64Mb	S71WS256JC0	S71WS128JC0	
	32Mb		S71WS128JB0	S71WS064JB0
	16Mb		S71WS128JA0	S71WS064JA0

Product Selector Guide

Device-Model#	Flash Density	pSRAM Density	Flash Speed (MHz)	pSRAM Speed (MHz/ns)	Supplier	Package	Availability Status
S71WS064JA0-2Y	64Mb	16Mb	66	66/70	Cosmo RAM	7x9x1.2mm 80-ball	Preliminary
S71WS064JB0-2Y		32Mb			Cosmo RAM		Preliminary
S71WS128JA0-AY	128Mb				Cosmo RAM	8x11.6x1.2 mm 84-ball	Preliminary
S71WS128JB0-AY					Cosmo RAM		Preliminary
S71WS128JC0-AY		64Mb			Cosmo RAM		Preliminary
S71WS256JC0-TY	256Mb				Cosmo RAM	8x11.6x1.4 mm 84-ball	Preliminary

S71WS-J Based MCPs

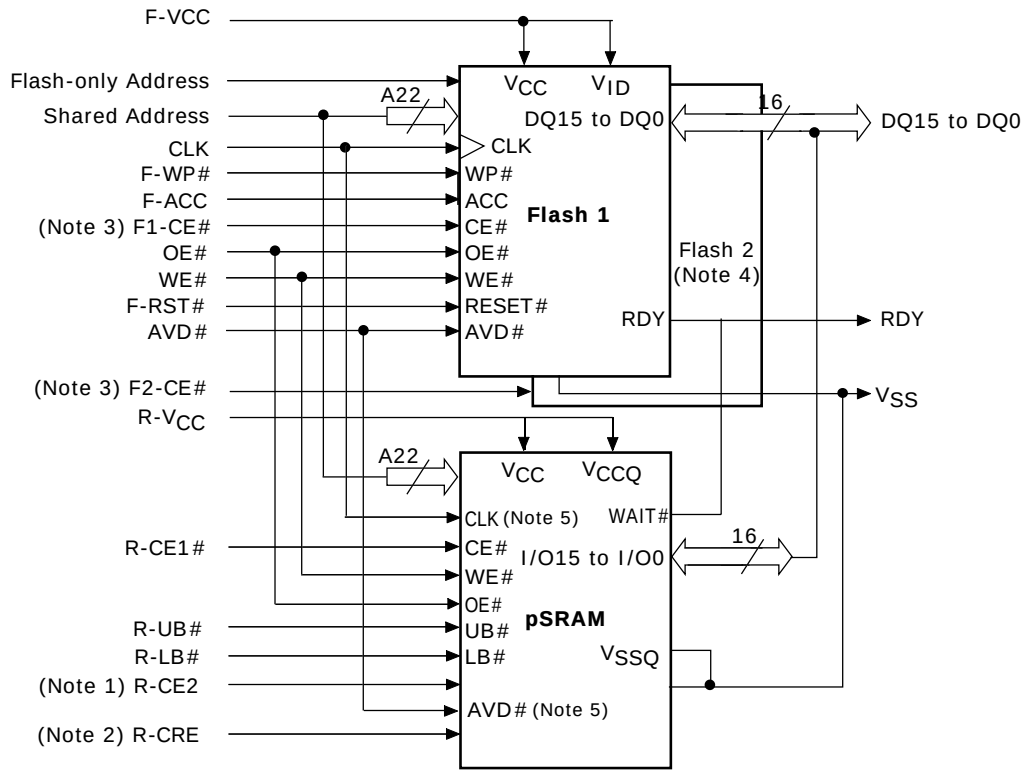
S29WS128/064J

CosmoRAM

COSMORAM Type I – 1.8 V, 16 Mb

Revision Summary

MCP Block Diagram



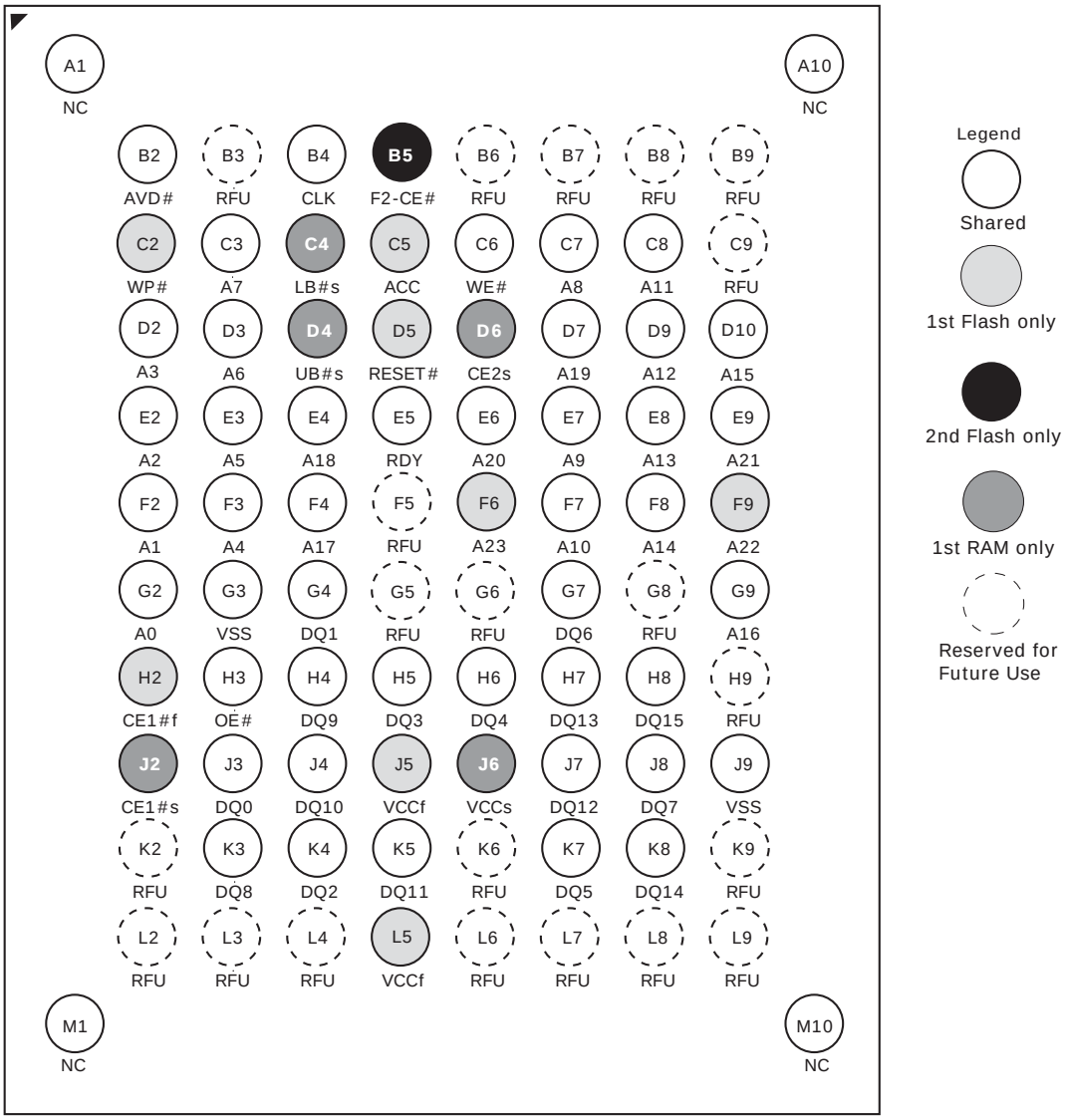
Notes:

1. *R-CRE is only present in CellularRAM-compatible pSRAM.*
2. *R-CE2 is only present in CosmoRAM-compatible pSRAM.*
3. *For 1 Flash = pSRAM, F1-CE# = CE#. For 2 Flash + pSRAM, CE# = F1-CE# and F2-CE# is the chip-enable pin for the second Flash.*
4. *Only needed for S71WS256JC0, and S70WS256J00.*
5. *CLK and AVD# not applicable for 16Mb pSRAM.*

Connection Diagrams

(CosmoRAM Type-based)

84-ball Fine-Pitch Ball Grid Array
CosmoRAM-based Pinout (Top View, Balls Facing Down)



Notes:

1. *In MCP's based on a single S29WSxxxJ (S71WSxxxJ), ball B5 is RFU. In MCP's based on two S29WSxxxJ (S71WS256J), ball B5 is CE#f2 or F2-CE#.*
2. *Addresses are shared btween Flash and RAM depending on the density of the pSRAM.*

MCP	Flash-only Addresses	Shared Addresses
S71WS064JA0	A21-A20	A19-A0
S71WS064JB0	A21	A20-A0
S71WS128JA0	A22-A20	A19-A0
S71WS128JB0	A22-A21	A19-A0
S71WS128JC0	A22	A21-A0

MCP	Flash-only Addresses	Shared Addresses
S71WS256JC0	A22	A21-A0

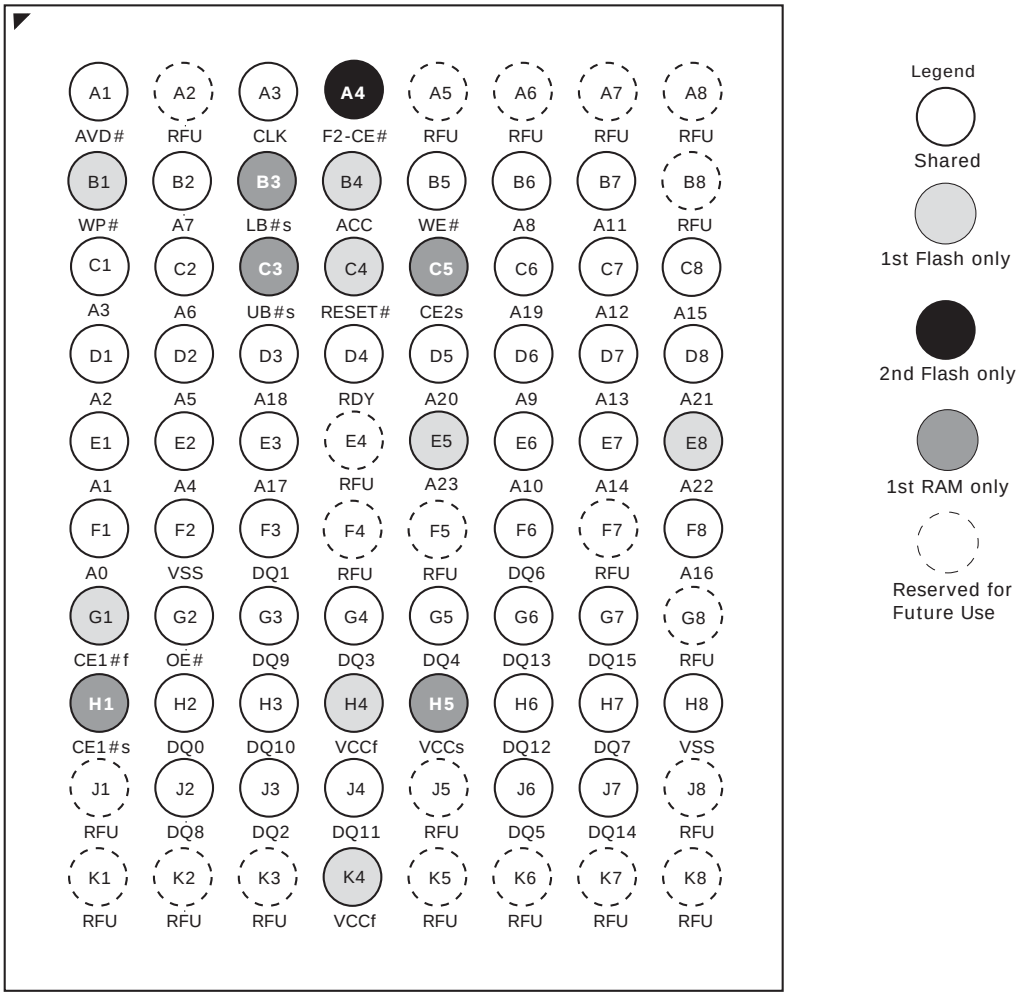
Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

(CosmoRAM Type-based)

80-ball Fine-Pitch Ball Grid Array
CosmoRAM-based Pinout (Top View, Balls



Notes:

1. *In MCP's based on a single S29WSxxxJ (S71WSxxxJ), ball B5 is RFU. In MCP's based on two S29WSxxxJ (S71WS256J), ball B5 is CE#f2 or F2-CE#.*
2. *Addresses are shared btween Flash and RAM depending on the density of the pSRAM.*
3. *The 80-ball pinout is applicable only to those MCPs with Flash density of 64Mb or 32Mb. For all the other MCPs included in this datasheet, please use the 84-ball pinout for design.*

MCP	Flash-only Addresses	Shared Addresses
S71WS064JA0	A21-A20	A19-A0
S71WS064JB0	A21	A20-A0

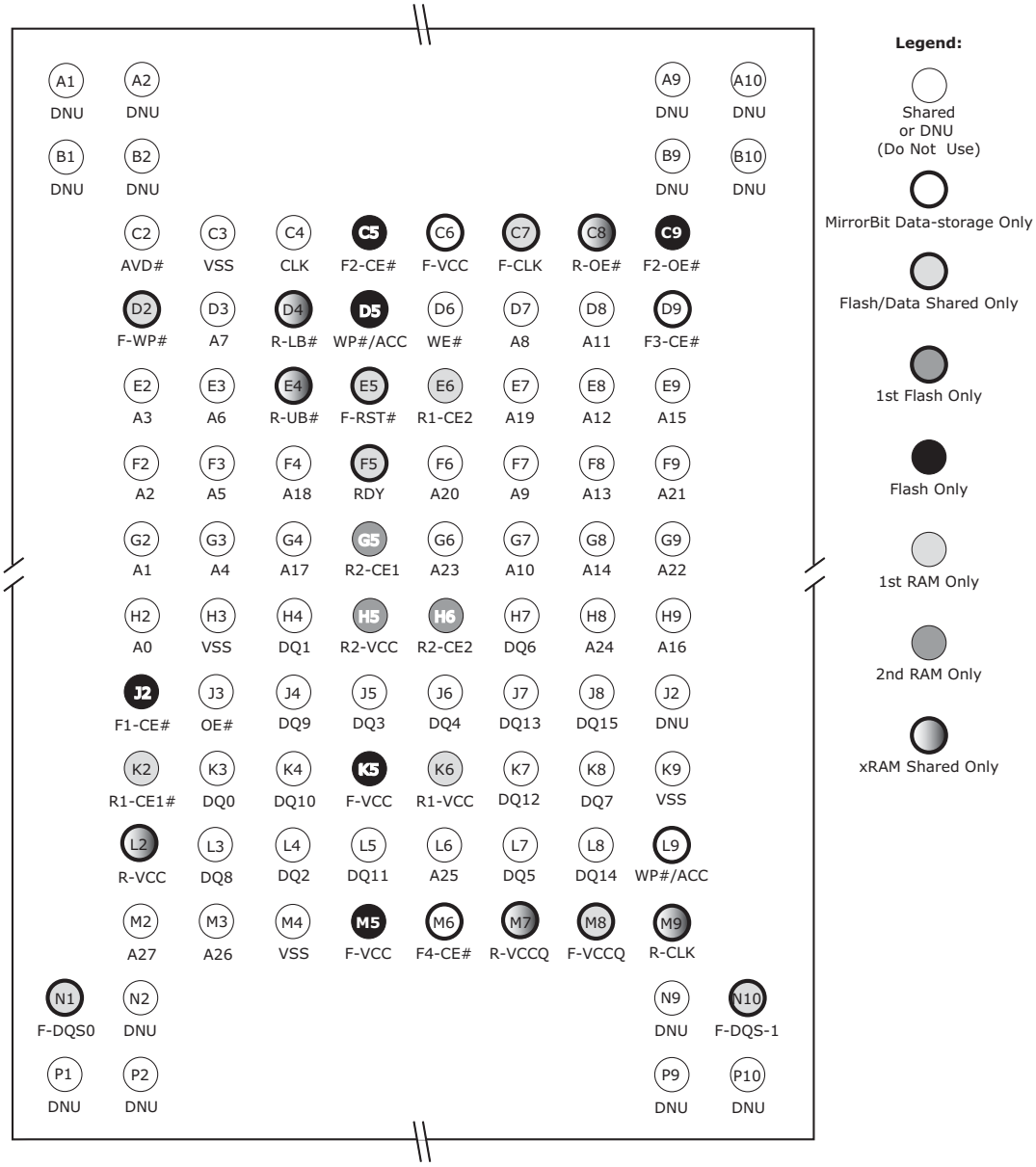
MCP	Flash-only Addresses	Shared Addresses
S71WS128JA0	A22-A20	A19-A0
S71WS128JB0	A22-A21	A19-A0
S71WS128JC0	A22	A21-A0
S71WS256JC0	A22	A21-A0

Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Lookahead Connection Diagram



Notes:

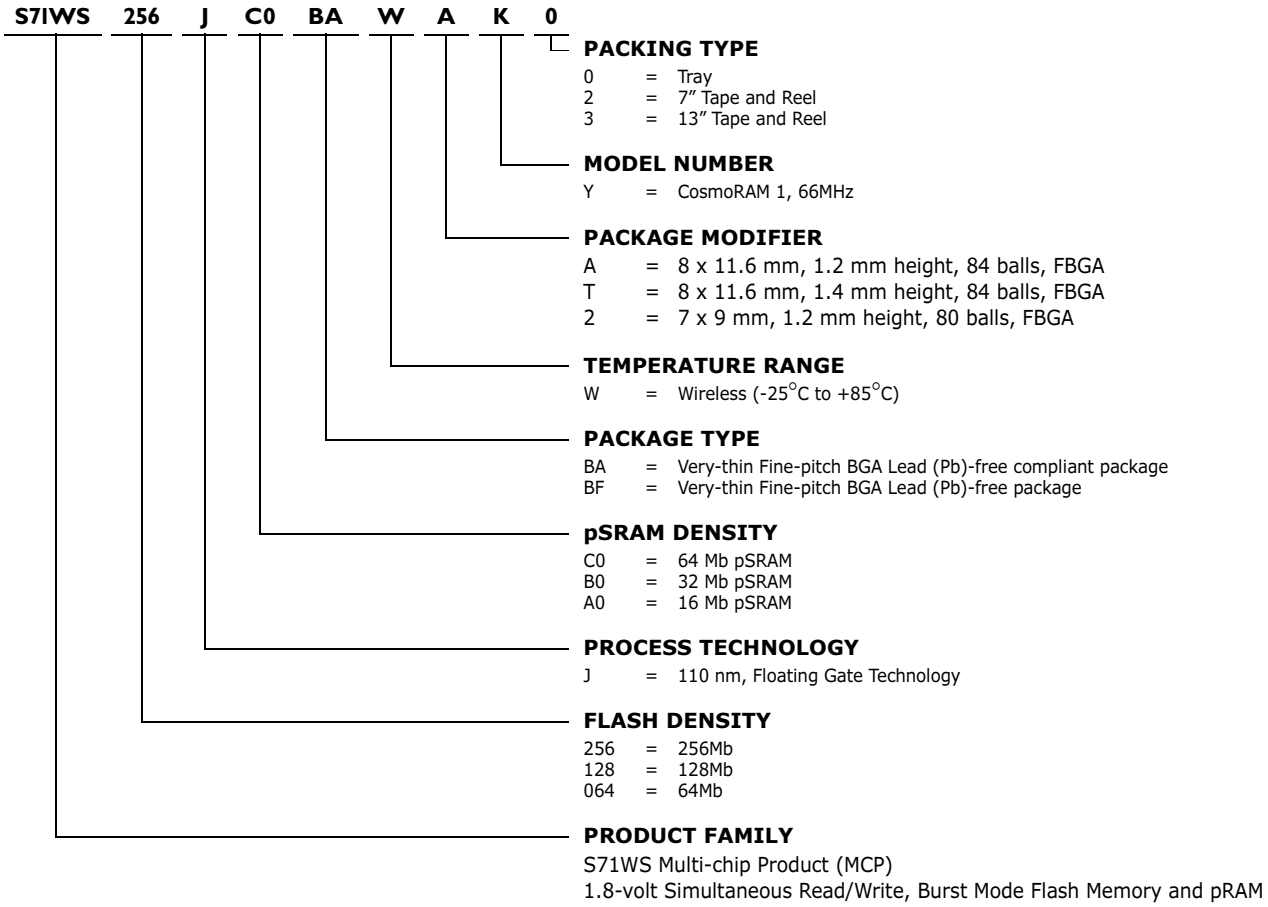
1. *F1 and F2 denote XIP/Code Flash, while F3 and F4 denote Data/Companion Flash.*
2. *In addition to being defined as F2-CE#, Ball C5 can also be assigned as F1-CE2# for code flash that has two chip enable signals.*
3. *For MCPs requiring 3.0V Vcc and 1.8V Vio, use the 1.8V Look-ahead Pinout in order to accommodate extra AVD, MRS and CLK pins for the pSRAM (if needed).*
4. *Refer to Application Note on pinout subsets to match the package size offerings.*
5. *Ball B5 is shared between Flash RDY and RAM WAIT# signals.*

Input/Output Descriptions

A22-A0	=	Address inputs
DQ15-DQ0	=	Data input/output
OE#	=	Output Enable input. Asynchronous relative to CLK for the Burst mode.
WE#	=	Write Enable input.
V_{SS}	=	Ground
NC	=	No Connect; not connected internally
RDY	=	Ready output. Indicates the status of the Burst read (shared with WAIT# pin of RAM).
CLK	=	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at V_{IL} or V_{IH} while in asynchronous mode
AVD#	=	Address Valid input. Indicates to device that the valid address is present on the address inputs. Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched. High = device ignores address inputs
F-RST#	=	Hardware reset input. Low = device resets and returns to reading array data
F-WP#	=	Hardware write protect input. At V_{IL}, disables program and erase functions in the four outermost sectors. Should be at V_{IH} for all other conditions.
F-ACC	=	Accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.
R-CE1#	=	Chip-enable input for pSRAM.
F1-CE#	=	Chip-enable input for Flash 1. Asynchronous relative to CLK for Burst Mode.
R-CRE	=	Control Register Enable (Only for MCPs with CellularRAM pSRAM).
F-V_{CC}	=	Flash 1.8 Volt-only single power supply.
R-V_{CC}	=	pSRAM Power Supply.
R-UB#	=	Upper Byte Control (pSRAM).
R-LB#	=	Lower Byte Control (pSRAM).
F2-CE#	=	Chip-enable input for Flash 2. Asynchronous relative to CLK for burst mode (needed only for S71WS256J).
DNU	=	Do not use. Reserved for future Spansion products.
R-CE2	=	Chip-enable input for pSRAM

Ordering Information

The order number is formed by a valid combinations of the following:



S71WS064JA0 Valid Combinations (WS064J Flash + I6Mb pSRAM)					
Base Ordering Part Number	**Package Marking**	**Temperature Range**	**Burst Speed**	**Material Set**	**Supplier**
S71WS064JA0BAW2Y	71WS064JA0BAW2Y	-25°C to +85°C	66 MHz	Pb-free compliant	CosmoRAM
S71WS064JA0BFW2Y	71WS064JA0BFW2Y	-25°C to +85°C		Pb-free	

Notes:

1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S71WS064JB0 Valid Combinations (WS064J Flash + 32Mb pSRAM)					
Base Ordering Part Number	Package Marking	Temperature Range	Burst Speed	Material Set	Supplier
S71WS064JB0BAW2Y	71WS064JB0BAW2Y	-25°C to +85°C	66 MHz	Pb-free compliant	CosmoRAM
S71WS064JB0BFW2Y	71WS064JB0BFW2Y	-25°C to +85°C		Pb-free	

Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S71WSI28JA0 Valid Combinations (WSI28J Flash + 16Mb pSRAM)					
Base Ordering Part Number	Package Marking	Temperature Range	Burst Speed	Material Set	Supplier
S71WS128JA0BAWAY	71WS128JA0BAWAY	-25°C to +85°C	66 MHz	Pb-free compliant	CosmoRAM
S71WS128JA0BFWAY	71WS128JA0BFWAY	-25°C to +85°C		Pb-free	

Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S71WSI28JB0 Valid Combinations (WSI28J Flash + 32Mb pSRAM)					
Base Ordering Part Number	Package Marking	Temperature Range	Burst Speed	Material Set	Supplier
S71WS128JB0BAWAY	71WS128JB0BAWAY	-25°C to +85°C	66 MHz	Pb-free compliant	CosmoRAM
S71WS128JB0BFWAY	71WS128JB0BFWAY	-25°C to +85°C		Pb-free	

Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S71WSI28JC0 Valid Combinations (WSI28J Flash + 64Mb pSRAM)					
Base Ordering Part Number	Package Marking	Temperature Range	Burst Speed	Material Set	Supplier
S71WS128JC0BAWAY	71WS128JC0BAWAY	-25°C to +85°C	66 MHz	Pb-free compliant	CosmoRAM
S71WS128JC0BFWAY	71WS128JC0BFWAY	-25°C to +85°C		Pb-free	

Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S71WS256JC0 Valid Combinations (2 x WSI28J Flash + 64Mb pSRAM)					
Base Ordering Part Number	Package Marking	Temperature Range	Burst Speed	Material Set	Supplier
S71WS256JC0BAWTY	71WS256JC0BAWTY	-25°C to +85°C	66 MHz	Pb-free compliant	CosmoRAM
S71WS256JC0BFWTY	71WS256JC0BFWTY	-25°C to +85°C		Pb-free	

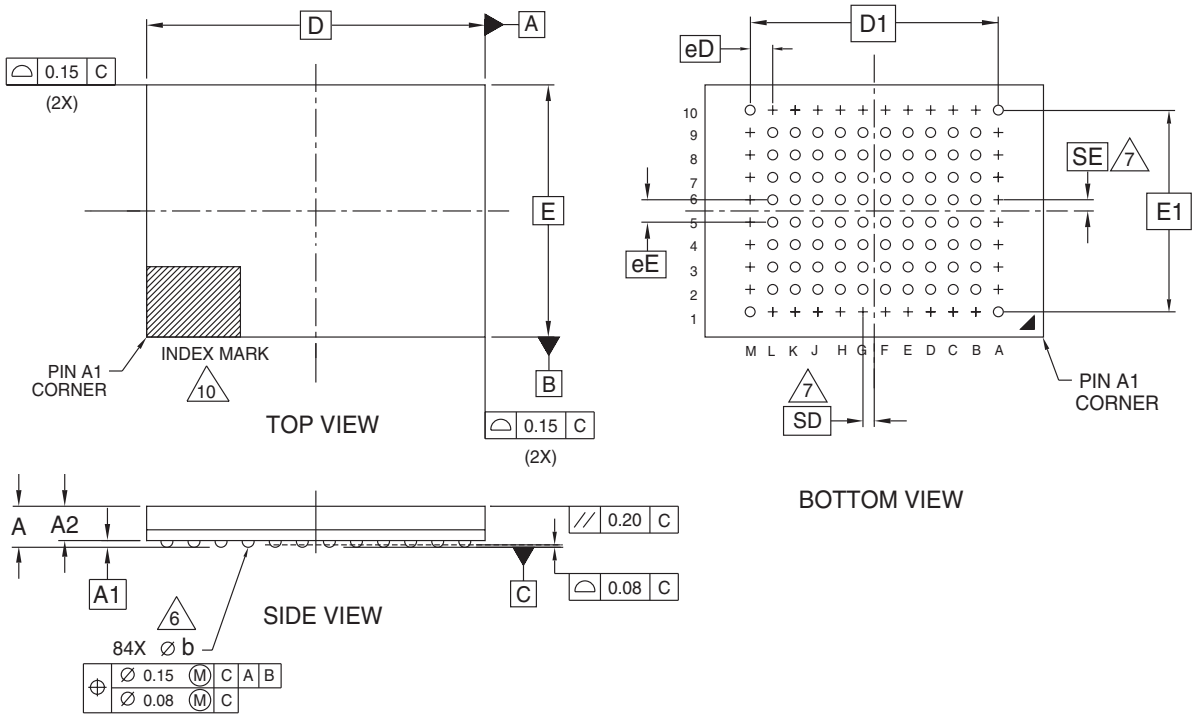
Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Physical Dimensions

TLA084—84-ball Fine-Pitch Ball Grid Array (FBGA) 8 x 11.6 mm Package



PACKAGE	TLA 084			
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	11.60 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	84			BALL COUNT
Ø b	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10, E1,E10,F1,F10,G1,G10, H1,H10,J1,J10,K1,K10,L1,L10, M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

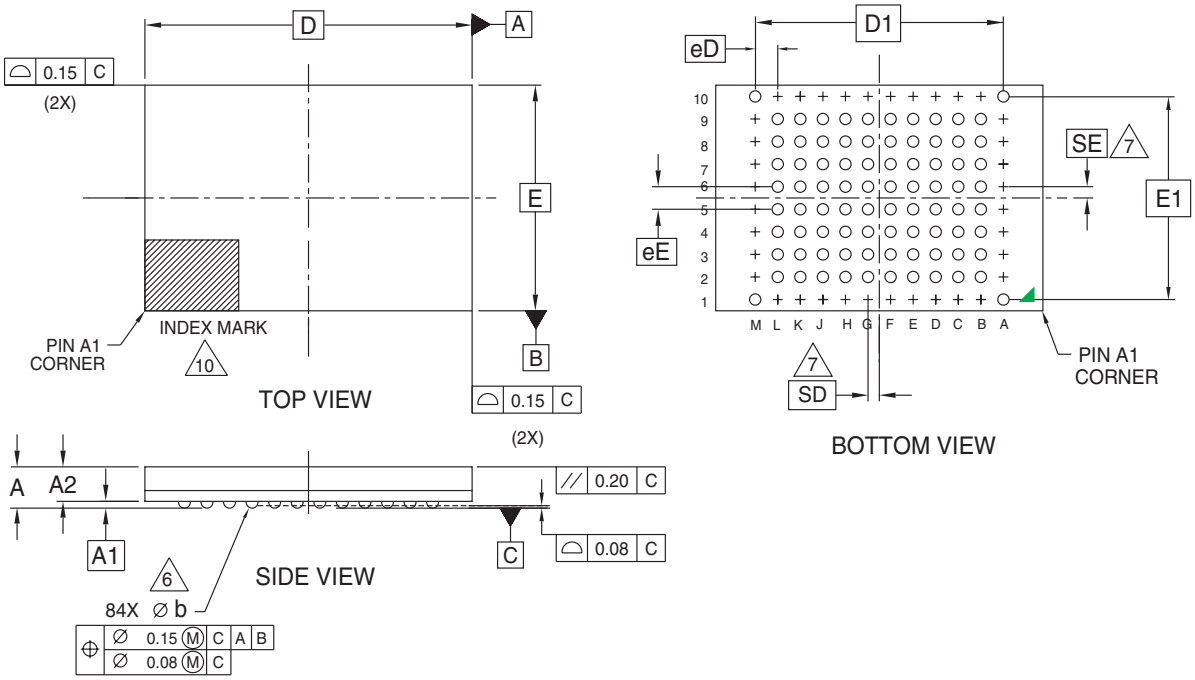
   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3372-2 \ 16-038.22a

FTA084—84-ball Fine-Pitch Ball Grid Array (FBGA) 8 x 11.6 mm Package



PACKAGE	FTA 084			NOTE
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.40	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	1.02	---	1.17	BODY THICKNESS
D	11.60 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	84			BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10,E1,E10 F1,F10,G1,G10,H1,H10 J1,J10,K1,K10,L1,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

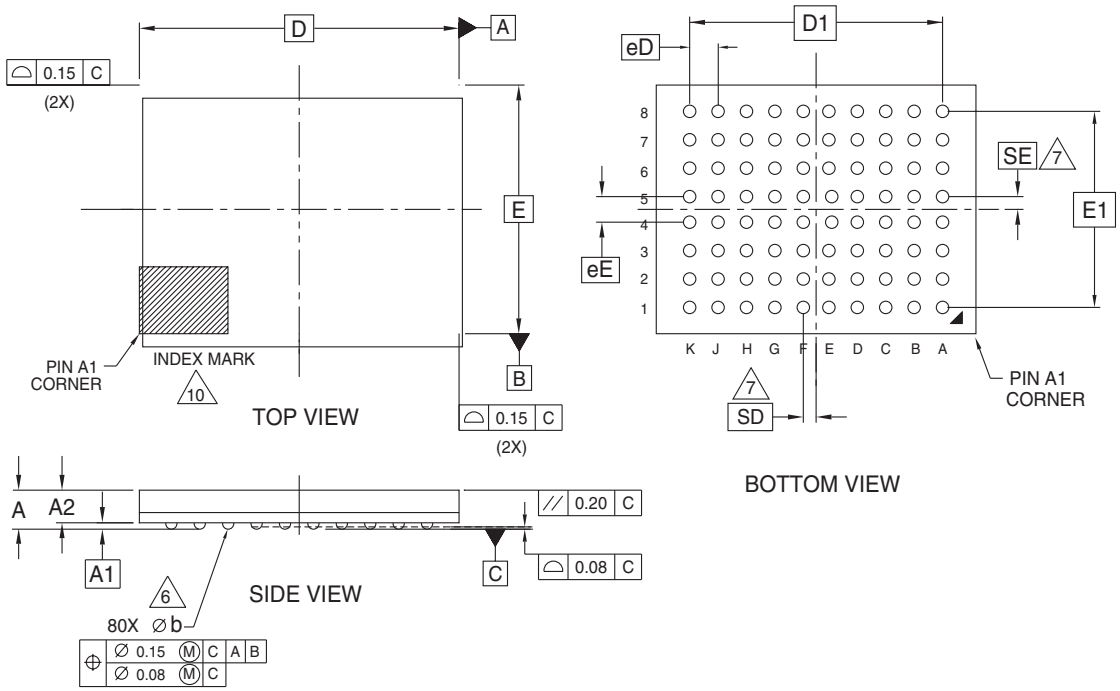
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3388 \ 16-038.21a

TLC080—80-ball Fine-Pitch Ball Grid Array (FBGA) 7 x 9 mm Package



PACKAGE	TLC 080			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		9.00 BSC.		BODY SIZE
E		7.00 BSC.		BODY SIZE
D1		7.20 BSC.		MATRIX FOOTPRINT
E1		5.60 BSC.		MATRIX FOOTPRINT
MD		10		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
n		80		BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
				DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

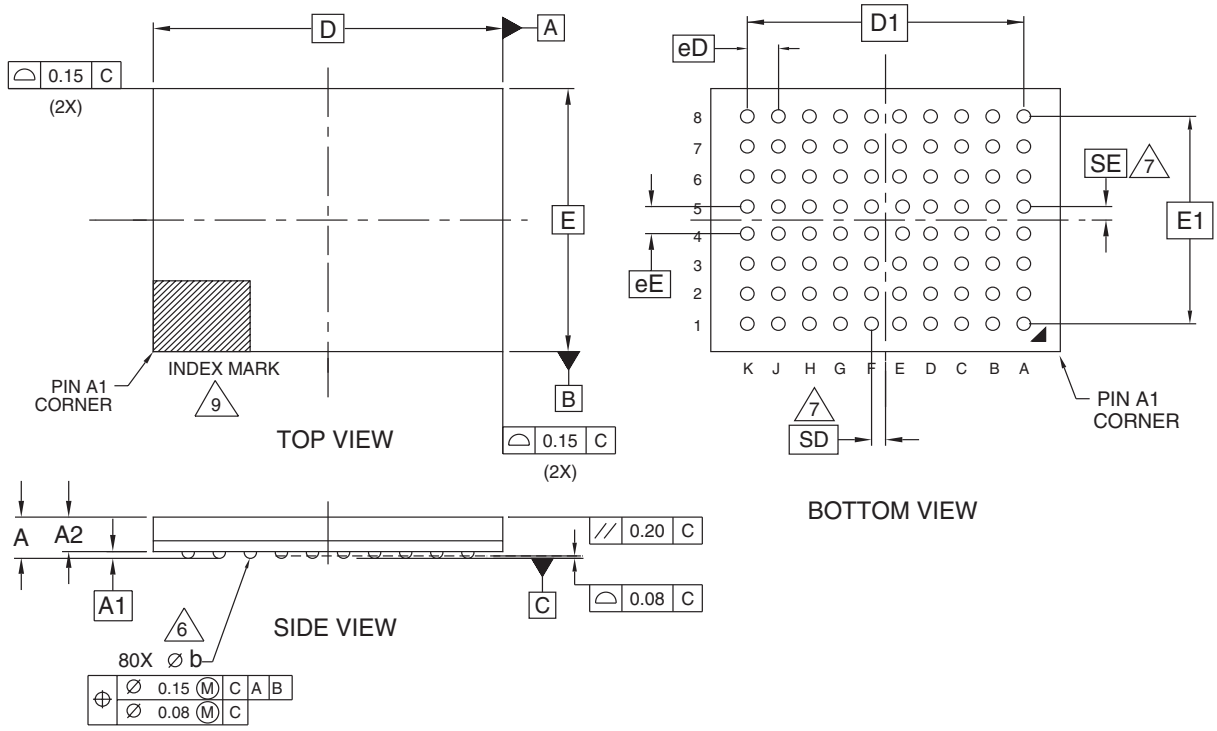
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3430 \ 16-038.22 \ 10.15.04

TSC080 - Fine-Pitch Ball Grid Array (FBGA) 7 x 9 mm Package



PACKAGE	TSC 080			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		9.00 BSC.		BODY SIZE
E		7.00 BSC.		BODY SIZE
D1		7.20 BSC.		MATRIX FOOTPRINT
E1		5.60 BSC.		MATRIX FOOTPRINT
MD		10		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
n		80		BALL COUNT
Øb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
				DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3496 \ 16-038.22 \ 5.20.05

S29WSI28/064J

Flash Family for Multi-Chip Products (MCP)
I28/64 Megabit (8/4 M x I6-Bit) CMOS I.8 Volt-only Simultaneous Read/Write, Burst Mode Flash Memory

PRELIMINARY

Distinctive Characteristics

Architectural Advantages

- **Single 1.8 volt read, program and erase (1.65 to 1.95 volt)**
- **Manufactured on 0.11 µm process technology**
- **VersatileIO™ (V_{IO}) Feature**
  - — Device generates data output voltages and tolerates data input voltages as determined by the voltage on the V_{IO} pin
  - — 1.8V compatible I/O signals (1.65-1.95 V)
- **Simultaneous Read/Write operation**
  - — Data can be continuously read from one bank while executing erase/program functions in other bank
  - — Zero latency between read and write operations
  - — Four bank architecture: WS128J: 16Mb/48Mb/48Mb/16Mb, WS064J: 8Mb/24Mb/24Mb/8Mb
- **Programable Burst Interface**
  - — 2 Modes of Burst Read Operation
  - — Linear Burst: 8, 16, and 32 words with wrap-around
  - — Continuous Sequential Burst
- **Secured Silicon Sector region**
  - — 128 words accessible through a command sequence, 64words for the Factory Secured Silicon Sector and 64words for the Customer Secured Silicon Sector.
- **Sector Architecture**

  4 Kword x 16 boot sectors, eight at the top of the address range, and eight at the bottom of the address range
  - — **WS128J:** 4 Kword X 16, 32 Kword x 254 sectors

    Bank A: 4 Kword x 8, 32 Kword x 31 sectors

    Bank B: 32 Kword x 96 sectors

    Bank C: 32 Kword x 96 sectors

    Bank D: 4 Kword x 8, 32 Kword x 31 sectors
  - — **WS064J:** 4 Kword x 16, 32 Kword x 126 sectors.

    Bank A: 4 Kword x 8, 32 Kword x 15 sectors

    Bank B: 32 Kword x 48 sectors

    Bank C: 32 Kword x 48 sectors

    Bank D: 4 Kword x 8, 32 Kword x 15 sectors
- **Cycling Endurance: 100,000 cycles per sector typical**
- **Data retention: 20-years typical**

Performance Characteristics

- **Read access times at 80/66 MHz**
  - — Burst access times of 9.1/11.2 ns @ 30 pF at industrial temperature range
  - — Synchronous latency of 46/56 ns (at 30 pF)
  - — Asynchronous random access times of 45/55 ns (at 30 pF)
- **Power dissipation (typical values, C_L = 30 pF)**
  - — Burst Mode Read: 10 mA @ 80Mhz
  - — Simultaneous Operation: 25 mA @ 80Mhz
  - — Program/Erase: 15 mA
  - — Standby mode: 0.2 µA

Hardware Features

- **Handshaking feature available**
  - — Provides host system with minimum possible latency by monitoring RDY
- **Hardware reset input (RESET#)**
  - — Hardware method to reset the device for reading array data
- **WP# input**
  - — Write protect (WP#) function allows protection of four outermost boot sectors, regardless of sector protect status
- **Persistent Sector Protection**
  - — A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector
  - — Sectors can be locked and unlocked in-system at V_{CC} level
- **Password Sector Protection**
  - — A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-defined 64-bit password
- **ACC input: Acceleration function reduces programming time; all sectors locked when ACC = V_{IL}**
- **CMOS compatible inputs, CMOS compatible outputs**
- **Low V_{CC} write inhibit**

Software Features

- **Supports Common Flash Memory Interface (CFI)**
- **Software command set compatible with JEDEC 42.4 standards**
  - — Backwards compatible with AMD Am29BDS, AMD Am29BDD, AMD Am29BL, and Fujitsu MBM29BS families
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program and erase operation completion

- **Erase Suspend/Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

General Description

The S29WS128/064J_MCP/S29WS064J is a 128/64 Mbit, 1.8 Volt-only, simultaneous Read/Write, Burst Mode Flash memory device, organized as 8,388,608/4,194,304 words of 16 bits each. This device uses a single V_{CC} of 1.65 to 1.95 V to read, program, and erase the memory array. A 12.0-volt V_{HH} on ACC may be used for faster program performance if desired. The device can also be programmed in standard EPROM programmers.

At 80 MHz, the device provides a burst access of 9.1 ns at 30 pF with a latency of 46 ns at 30 pF. At 66 MHz, the device provides a burst access of 11.2 ns at 30 pF with a latency of 56 ns at 30 pF. The device operates within the industrial temperature range of -40°C to +85°C and the wireless temperature range of -25°C to +85°C. The device is offered in Various FBGA packages.

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into four banks. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The device is divided as shown in the following table:

Bank	Quantity		Size
	128Mb	64 Mb	
A	8	8	4 Kwords
	31	15	32 Kwords
B	96	48	32 Kwords
C	96	48	32 Kwords
D	31	15	32 Kwords
	8	8	4 Kwords

The VersatileIO™ (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{IO} pin.

The device uses Chip Enable (CE#), Write Enable (WE#), Address Valid (AVD#) and Output Enable (OE#) to control asynchronous read and write operations. For burst operations, the device additionally requires Ready (RDY), and Clock (CLK). This implementation allows easy interface with minimal glue logic to a wide range of microprocessors/microcontrollers for high performance read operations.

The burst read mode feature gives system designers flexibility in the interface to the device. The user can preset the burst length and wrap through the same memory space, or read the flash array in continuous mode.

The clock polarity feature provides system designers a choice of active clock edges, either rising or falling. The active clock edge initiates burst accesses and determines when data will be output.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The **Erase Suspend/Erase Resume** feature enables the user to put erase or program on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the Secured Silicon Sector area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region. Program suspend is also offered.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset cir-

cuitry. A system reset would thus also reset the device, enabling the system microprocessor to read boot-up firmware from the Flash memory device.

The host system can detect whether a program or erase operation is complete by using the device status bit DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The device also offers two types of data protection at the sector level. When at V_{IL}, **WP#** locks the four outermost boot sectors.

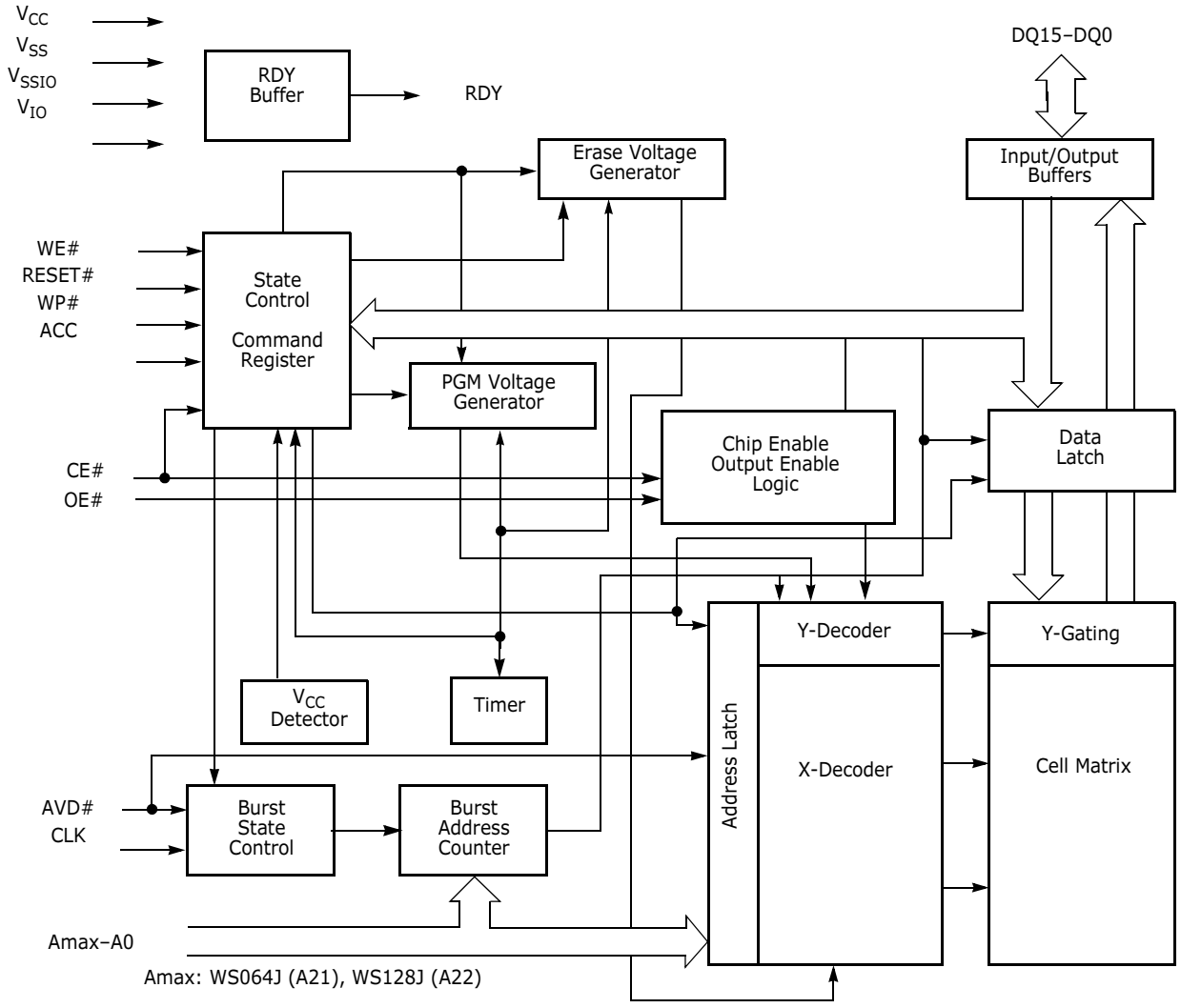
The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

Spansion™ Flash memory products combine years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunnelling. The data is programmed using hot electron injection.

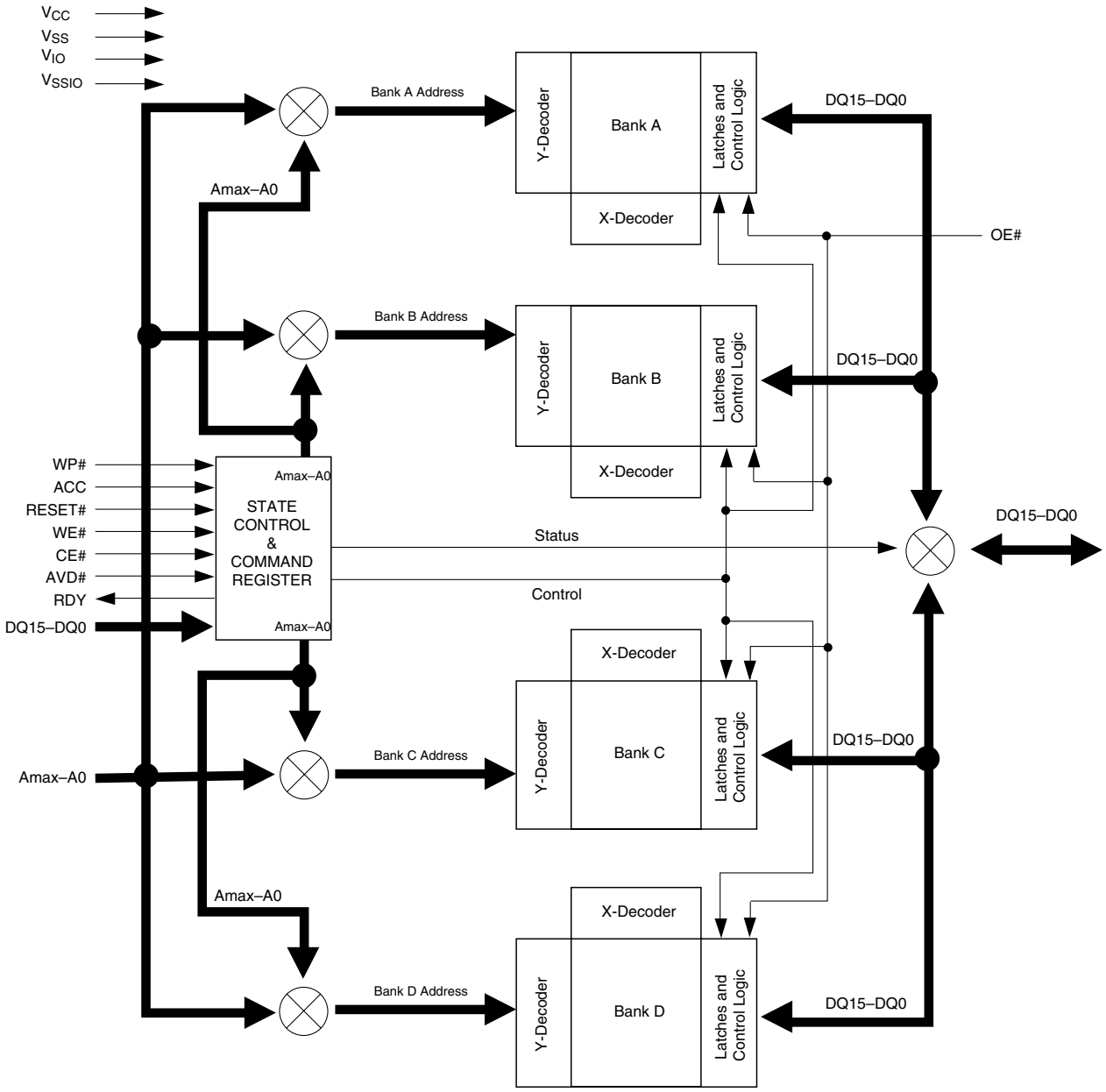
Product Selector Guide

Part Number	S29WS128/064J_MCP/S29WS064J					
	Synchronous/Burst			Asynchronous		
	Speed Option	66 MHz	80*[2] MHz	Speed Option	66 MHz	80*[2] MHz
V_{IO} = 1.65 – 1.95 V	Max Latency, ns (t_{IACC})	56	46	Max Access Time, ns (t_{ACC})	55	45
	Max Burst Access Time, ns (t_{BACC})	11.2	9.1	Max CE# Access, ns (t_{CE})	55	45
	Max OE# Access, ns (t_{OE})	11.2	9.1	Max OE# Access, ns (t_{OE})	11.2	9.1

Block Diagram



Block Diagram of Simultaneous Operation Circuit



Amax: WS064J (A21), WS128J (A22)

Input/Output Descriptions

Amax-A0	=	Address inputs
DQ15-DQ0	=	Data input/output
CE#	=	Chip Enable input. Asynchronous relative to CLK for the Burst mode.
OE#	=	Output Enable input. Asynchronous relative to CLK for the Burst mode.
WE#	=	Write Enable input.
V_{CC}	=	Device Power Supply (1.65 – 1.95 V).
V_{IO}	=	Input & Output Buffer Power Supply (1.65 – 1.95 V).
V_{SS}	=	Ground
NC	=	No Connect; not connected internally
RDY	=	Ready output; In Synchronous Mode, indicates the status of the Burst read. Low = data not valid at expected time. High = data valid. In Asynchronous Mode, indicates the status of the internal program and erase function. Low = program/erase in progress. High Impedance = program/erase completed.
CLK	=	CLK is not required in asynchronous mode. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter.
AVD#	=	Address Valid input. Indicates to device that the valid address is present on the address inputs (Amax-A0). Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched. High = device ignores address inputs
RESET#	=	Hardware reset input. Low = device resets and returns to reading array data
WP#	=	Hardware write protect input. At V_{IL}, disables program and erase functions in the four outermost sectors. Should be at V_{IH} for all other conditions.
ACC	=	At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, locks all sectors. Should be at V_{IH} for all other conditions.

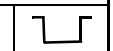
Note:

1. Amax = A22 (WS128J), A21 (WS064J)

Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table I. Device Bus Operations

Operation	CE#	OE#	WE#	A22–0	DQ15–0	RESET#	CLK (See Note)	AVD#
Asynchronous Read - Addresses Latched	L	L	H	Addr In	I/O	H	X	
Asynchronous Read - Addresses Steady State	L	L	H	Addr In	I/O	H	X	L
Asynchronous Write	L	H	L	Addr In	I/O	H	X	L
Synchronous Write	L	H	L	Addr In	I/O	H		
Standby (CE#)	H	X	X	HIGH Z	HIGH Z	H	X	X
Hardware Reset	X	X	X	HIGH Z	HIGH Z	L	X	X
Burst Read Operations								
Load Starting Burst Address	L	X	H	Addr In	X	H		
Advance Burst to next address with appropriate Data presented on the Data Bus	L	L	H	HIGH Z	Burst Data Out	H		H
Terminate current Burst read cycle	H	X	H	HIGH Z	HIGH Z	H		X
Terminate current Burst read cycle via RESET#	X	X	H	HIGH Z	HIGH Z	L	X	X
Terminate current Burst read cycle and start new Burst read cycle	L	X	H	HIGH Z	I/O	H		

Legend: *L = Logic 0, H = Logic 1, X = Don't Care*

Note: *Default active edge of CLK is the rising edge.*

VersatileIO™ (V_{IO}) Control

The VersatileIO (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{IO} pin.

Requirements for Asynchronous Read Operation (Non-Burst)

To read data from the memory array, the system must first assert a valid address on Amax–A0(A22-A0 for WS128J and A21-A0 for WS064J), while driving AVD# and CE# to V_{IL}. WE# should remain at V_{IH}. The rising edge of AVD# latches the address. The data will appear on DQ15–DQ0. Since the memory array is divided into four banks, each bank remains enabled for read access until the command register contents are altered.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable ad-

dresses and stable CE# to valid data at the outputs. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output.

The internal state machine is set for reading array data in asynchronous mode upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

Requirements for Synchronous (Burst) Read Operation

The device is capable of continuous sequential burst operation and linear burst operation of a preset length. When the device first powers up, it is enabled for asynchronous read operation.

Prior to entering burst mode, the system should determine how many wait states are desired for the initial word (t_{IACC}) of each burst access, what mode of burst operation is desired, which edge of the clock will be the active clock edge, and how the RDY signal will transition with valid data. The system would then write the configuration register command sequence. See "Set Configuration Register Command Sequence" section on page 62 and "Command Definitions" section on page 62 for further details.

Once the system has written the "Set Configuration Register" command sequence, the device is enabled for synchronous reads only.

The initial word is output t_{IACC} after the active edge of the first CLK cycle. Subsequent words are output t_{BACC} after the active edge of each successive clock cycle, which automatically increments the internal address counter. Note that the device has a fixed internal address boundary that occurs every 64 words, starting at address 00003Fh.

During the time the device is outputting data at this fixed internal address boundary (address 00003Fh, 00007Fh, 0000BFh, etc.), a two cycle latency occurs before data appears for the next address (address 000040h, 000080h, 0000C0h, etc.).

Additionally, when the device is read from an odd address, 1 wait state is inserted when the address pointer crosses the first boundary that occurs every 16 words. For instance, if the device is read from 00001Ah (odd), 1 wait state is inserted before the data of 000020h is output. This wait states is inserted at only the first 16 words boundary. Then, if the device is read from the odd address within the last 16 words of 64 word boundary (address 000031h, 000033h,..., 00003Eh), a three cycle latency occurs before data appears for the next address (address 000040h).

The RDY output indicates this condition to the system by pulsing deactive (low). See Figure 34, "Latency with Boundary Crossing," on page 109.

The device will continue to output sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location, until the system drives CE# high, RESET# low, or AVD# low in conjunction with a new address. See Table 1, "Device Bus Operations," on page 25.

If the host system crosses the bank boundary while reading in burst mode, and the device is not programming or erasing, a two-cycle latency will occur as described above in the subsequent bank. If the host system crosses the bank boundary while the device is programming or erasing, the device will provide read status information. The clock will be ignored. After the host has completed status reads, or the device has completed the program or erase operation, the host can restart a burst operation using a new address and AVD# pulse.

8-, 16-, and 32-Word Linear Burst with Wrap Around

The remaining three burst read modes are of the linear wrap around design, in which a fixed number of words are read from consecutive addresses. In each of these modes, the burst addresses read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode (see Table 2.)

Table 2. Burst Address Groups

Mode	Group Size	Group Address Ranges
8-word	8 words	0-7h, 8-Fh, 10-17h,...
16-word	16 words	0-Fh, 10-1Fh, 20-2Fh,...
32-word	32 words	00-1Fh, 20-3Fh, 40-5Fh,...

As an example: if the starting address in the 8-word mode is 39h, the address range to be read would be 38-3Fh, and the burst sequence would be 39-3A-3B-3C-3D-3E-3F-38h-etc. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group. In a similar fashion, the 16-word and 32-word Linear Wrap modes begin their burst sequence on the starting address written to the device, and then wrap back to the first address in the selected address group. **Note that in these three burst read modes the address pointer does not cross the boundary that occurs every 128 or 64 words; thus, no wait states are inserted (except during the initial access).**

The RDY pin indicates when data is valid on the bus.

Configuration Register

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, active clock edge, RDY configuration, and synchronous mode active.

Handshaking

The device is equipped with a handshaking feature that allows the host system to simply monitor the RDY signal from the device to determine when the initial word of burst data is ready to be read. The host system should use the programmable wait state configuration to set the number of wait states for optimal burst mode operation. The initial word of burst data is indicated by the active edge of RDY after OE# goes low.

For optimal burst mode performance, the host system must set the appropriate number of wait states in the flash device depending on clock frequency. See "Set Configuration Register Command Sequence" section on page 62 for more information.

Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in another bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 37, "Back-to-Back Read/Write Cycle Timings," on page 112 shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the DC Characteristics table for read-while-program and read-while-erase current specifications.

Writing Commands/Command Sequences

The device has the capability of performing an asynchronous or synchronous write operation. While the device is configured in Asynchronous read mode, it is able to perform Asynchronous write operations only. CLK is ignored in the Asynchronous programming mode. When in the Synchronous read mode configuration, the device is able to perform both Asynchronous and Synchronous write operations. CLK and WE# address latch is supported in the Synchronous programming mode. During a synchronous write operation, to write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive AVD# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive WE# and CE# to V_{IL}, and OE# to V_{IH}. when writing commands or data. During an asynchronous write operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when providing an address, command, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE#. The asynchronous and synchronous programing operation is independent of the Set Device Read Mode bit in the Configuration Register (see Table 17, "Configuration Register," on page 66).

The device features an Unlock Bypass mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 12, "WS128J Sector Address Table," on page 48 and Table 13, "WS064J Sector Address Table," on page 56 indicate the address space that each sector occupies. The device address space is divided into four banks. A "bank address" is the address bits required to uniquely select a bank. Similarly, a "sector address" is the address bits required to uniquely select a sector.

I_{CC2} in the "DC Characteristics" section on page 87 represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. ACC is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this input, the device automatically enters the aforementioned Unlock Bypass mode and uses the higher voltage on the input to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the ACC input returns the device to normal operation. Note that sectors must be unlocked prior to raising ACC to V_{HH}. *Note that the ACC pin must not be at V_{HH} for operations other than accelerated programming, or device dam-*

age may result. In addition, the ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

When at V_{IL}, ACC locks all sectors. ACC should be at V_{IH} for all other conditions.

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output from the internal register (which is separate from the memory array) on DQ15–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins must be as shown in Table 3, "Autoselect Codes (High Voltage Method)," on page 30. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 4, "S29WS128/064J_MCP Boot Sector/Sector Block Addresses for Protection/Unprotection," on page 30 and Table 5, "S29WS064J Boot Sector/Sector Block Addresses for Protection/Unprotection," on page 32). Table 3 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15–DQ0. However, the autoselect codes can also be accessed in-system through the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 18, "Command Definitions," on page 76. *Note that if a Bank Address (BA) on address bits A22, A21, and A20 for the WS128J (A21:A19 for the WS064J) is asserted during the third write cycle of the autoselect command, the host system can read autoselect data that bank and then immediately read array data from the other bank, without exiting the autoselect mode.*

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 18, "Command Definitions," on page 76. This method does not require V_{ID}. Autoselect mode may only be entered and used when in the asynchronous read mode. Refer to the "Autoselect Command Sequence" section on page 67 for more information.

Table 3. Autoselect Codes (High Voltage Method)

Description		CE#	OE#	WE #	RESET#	Amax to A12	A11 to A10	A9	A8	A7	A6	A5 to A4	A3	A2	A1	A0	DQ15 to DQ0
Manufacturer ID: FASL		L	L	H	H	X	X	V_{ID}	X	X	L	X	L	L	L	L	0001h
Device ID	Read Cycle 1	L	L	H	H	X	X	V_{ID}	X	L	L	L	L	L	L	H	227Eh
	Read Cycle 2												H	H	H	L	2218h (WS128J) 221Eh (WS064J)
	Read Cycle 3												H	H	H	H	2200h (WS128J) 2201h (WS064J)
Sector Protection Verification		L	L	H	H	SA	X	V_{ID}	X	L	L	L	L	L	H	L	0001h (protected), 0000h (unprotected)
Indicator Bits		L	L	H	H	X	X	V_{ID}	X	X	L	X	L	L	H	H	DQ15 - DQ8 = 0 DQ7 - Factory Lock Bit 1 = Locked, 0 = Not Locked DQ6 -Customer Lock Bit 1 = Locked, 0 = Not Locked DQ5 = Handshake Bit 1 = Reserved, 0 = Standard Handshake DQ4 & DQ3 - Boot Code DQ2 - DQ0 = 001
Hardware Sector Group Protection		L	L	H	H	SA	X	V_{ID}	X	X	X	L	L	L	H	L	0001h (protected), 0000h (unprotected)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, BA = Bank Address, SA = Sector Address, X = Don't care.*

Notes:

1. *The autoselect codes may also be accessed in-system via command sequences.*
2. *PPB Protection Status is shown on the data bus*

Sector/Sector Block Protection and Unprotection

The hardware sector protection feature disables both programming and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented via two methods.

(Note: For the following discussion, the term "sector" applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table 4, "S29WS128/064J_MCP Boot Sector/Sector Block Addresses for Protection/Unprotection," on page 30 and Table 5, "S29WS064J Boot Sector/Sector Block Addresses for Protection/Unprotection," on page 32).)

Table 4. S29WSI28/064J_MCP Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector	A22–A12	Sector/ Sector Block Size
SA0	00000000000	4 Kwords
SA1	00000000001	4 Kwords
SA2	00000000010	4 Kwords
SA3	00000000011	4 Kwords
SA4	00000000100	4 Kwords
SA5	00000000101	4 Kwords

Sector	A22–A12	Sector/ Sector Block Size
SA6	00000000110	4 Kwords
SA7	00000000111	4 Kwords
SA8	00000001XXX,	32 Kwords
SA9	00000010XXX,	32 Kwords
SA10	00000011XXX,	32 Kwords
SA11–SA14	000001XXXXX	128 (4x32) Kwords
SA15–SA18	000010XXXXX	128 (4x32) Kwords
SA19–SA22	000011XXXXX	128 (4x32) Kwords
SA23-SA26	000100XXXXX	128 (4x32) Kwords
SA27-SA30	000101XXXXX	128 (4x32) Kwords
SA31-SA34	000110XXXXX	128 (4x32) Kwords
SA35-SA38	000111XXXXX	128 (4x32) Kwords
SA39-SA42	001000XXXXX	128 (4x32) Kwords
SA43-SA46	001001XXXXX	128 (4x32) Kwords
SA47-SA50	001010XXXXX	128 (4x32) Kwords
SA51–SA54	001011XXXXX	128 (4x32) Kwords
SA55–SA58	001100XXXXX	128 (4x32) Kwords
SA59–SA62	001101XXXXX	128 (4x32) Kwords
SA63–SA66	001110XXXXX	128 (4x32) Kwords
SA67–SA70	001111XXXXX	128 (4x32) Kwords
SA71–SA74	010000XXXXX	128 (4x32) Kwords
SA75–SA78	010001XXXXX	128 (4x32) Kwords
SA79–SA82	010010XXXXX	128 (4x32) Kwords
SA83–SA86	010011XXXXX	128 (4x32) Kwords
SA87–SA90	010100XXXXX	128 (4x32) Kwords
SA91–SA94	010101XXXXX	128 (4x32) Kwords
SA95–SA98	010110XXXXX	128 (4x32) Kwords
SA99–SA102	010111XXXXX	128 (4x32) Kwords
SA103–SA106	011000XXXXX	128 (4x32) Kwords
SA107–SA110	011001XXXXX	128 (4x32) Kwords
SA111–SA114	011010XXXXX	128 (4x32) Kwords
SA115–SA118	011011XXXXX	128 (4x32) Kwords
SA119–SA122	011100XXXXX	128 (4x32) Kwords
SA123–SA126	011101XXXXX	128 (4x32) Kwords
SA127–SA130	011110XXXXX	128 (4x32) Kwords
SA131-SA134	011111XXXXX	128 (4x32) Kwords
SA135-SA138	100000XXXXX	128 (4x32) Kwords
SA139-SA142	100001XXXXX	128 (4x32) Kwords
SA143-SA146	100010XXXXX	128 (4x32) Kwords
SA147-SA150	100011XXXXX	128 (4x32) Kwords
SA151–SA154	100100XXXXX	128 (4x32) Kwords
SA155–SA158	100101XXXXX	128 (4x32) Kwords
SA159–SA162	100110XXXXX	128 (4x32) Kwords
SA163–SA166	100111XXXXX	128 (4x32) Kwords
SA167–SA170	101000XXXXX	128 (4x32) Kwords

Sector	A22–A12	Sector/ Sector Block Size
SA171–SA174	101001XXXXX	128 (4x32) Kwords
SA175–SA178	101010XXXXX	128 (4x32) Kwords
SA179–SA182	101011XXXXX	128 (4x32) Kwords
SA183–SA186	101100XXXXX	128 (4x32) Kwords
SA187–SA190	101101XXXXX	128 (4x32) Kwords
SA191–SA194	101110XXXXX	128 (4x32) Kwords
SA195–SA198	101111XXXXX	128 (4x32) Kwords
SA199–SA202	110000XXXXX	128 (4x32) Kwords
SA203–SA206	110001XXXXX	128 (4x32) Kwords
SA207–SA210	110010XXXXX	128 (4x32) Kwords
SA211–SA214	110011XXXXX	128 (4x32) Kwords
SA215–SA218	110100XXXXX	128 (4x32) Kwords
SA219–SA222	110101XXXXX	128 (4x32) Kwords
SA223–SA226	110110XXXXX	128 (4x32) Kwords
SA227–SA230	110111XXXXX	128 (4x32) Kwords
SA231–SA234	111000XXXXX	128 (4x32) Kwords
SA235–SA238	111001XXXXX	128 (4x32) Kwords
SA239–SA242	111010XXXXX	128 (4x32) Kwords
SA243–SA246	111011XXXXX	128 (4x32) Kwords
SA247–SA250	111100XXXXX	128 (4x32) Kwords
SA251–SA254	111101XXXXX	128 (4x32) Kwords
SA255–SA258	111110XXXXX	128 (4x32) Kwords
SA259	11111100XXX	32 Kwords
SA260	11111101XXX	32 Kwords
SA261	11111110XXX	32 Kwords
SA262	11111111000	4 Kwords
SA263	11111111001	4 Kwords
SA264	11111111010	4 Kwords
SA265	11111111011	4 Kwords
SA266	11111111100	4 Kwords
SA267	11111111101	4 Kwords
SA268	11111111110	4 Kwords
SA269	11111111111	4 Kwords

Table 5. S29WS064J Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector	A21–A12	Sector/ Sector Block Size
SA0	0000000000	4 Kwords
SA1	0000000001	4 Kwords
SA2	0000000010	4 Kwords
SA3	0000000011	4 Kwords
SA4	0000000100	4 Kwords
SA5	0000000101	4 Kwords
SA6	0000000110	4 Kwords
SA7	0000000111	4 Kwords
SA8	0000001XXX	32 Kwords

Sector	A21–A12	Sector/ Sector Block Size
SA9	0000010XXX	32 Kwords
SA10	0000011XXX	32 Kwords
SA11–SA14	00001XXXXX	128 (4x32) Kwords
SA15–SA18	00010XXXXX	128 (4x32) Kwords
SA19–SA22	00011XXXXX	128 (4x32) Kwords
SA23-SA26	00100XXXXX	128 (4x32) Kwords
SA27-SA30	00101XXXXX	128 (4x32) Kwords
SA31-SA34	00110XXXXX	128 (4x32) Kwords
SA35-SA38	00111XXXXX	128 (4x32) Kwords
SA39-SA42	01000XXXXX	128 (4x32) Kwords
SA43-SA46	01001XXXXX	128 (4x32) Kwords
SA47-SA50	01010XXXXX	128 (4x32) Kwords
SA51–SA54	01011XXXXX	128 (4x32) Kwords
SA55–SA58	01100XXXXX	128 (4x32) Kwords
SA59–SA62	01101XXXXX	128 (4x32) Kwords
SA63–SA66	01110XXXXX	128 (4x32) Kwords
SA67–SA70	01111XXXXX	128 (4x32) Kwords
SA71–SA74	10000XXXXX	128 (4x32) Kwords
SA75–SA78	10001XXXXX	128 (4x32) Kwords
SA79–SA82	10010XXXXX	128 (4x32) Kwords
SA83–SA86	10011XXXXX	128 (4x32) Kwords
SA87–SA90	10100XXXXX	128 (4x32) Kwords
SA91–SA94	10101XXXXX	128 (4x32) Kwords
SA95–SA98	10110XXXXX	128 (4x32) Kwords
SA99–SA102	10111XXXXX	128 (4x32) Kwords
SA103–SA106	11000XXXXX	128 (4x32) Kwords
SA107–SA110	11001XXXXX	128 (4x32) Kwords
SA111–SA114	11010XXXXX	128 (4x32) Kwords
SA115–SA118	11011XXXXX	128 (4x32) Kwords
SA119–SA122	11100XXXXX	128 (4x32) Kwords
SA123–SA126	11101XXXXX	128 (4x32) Kwords
SA127–SA130	11110XXXXX	128 (4x32) Kwords
SA131	1111100XXX	32 Kwords
SA132	1111101XXX	32 Kwords
SA133	1111110XXX	32 Kwords
SA134	1111111000	4 Kwords
SA135	1111111001	4 Kwords
SA136	1111111010	4 Kwords
SA137	1111111011	4 Kwords
SA138	1111111100	4 Kwords
SA139	1111111101	4 Kwords
SA140	1111111110	4 Kwords
SA141	1111111111	4 Kwords

Sector Protection

The device features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

Persistent Sector Protection

A command sector protection method that replaces the old 12 V controlled protection method.

Password Sector Protection

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted

WP# Hardware Protection

A write protect pin that can prevent program or erase operations in the outermost sectors.

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used. If the customer decides to continue using the Persistent Sector Protection method, they must set the **Persistent Sector Protection Mode Locking Bit**. This will permanently set the part to operate only using Persistent Sector Protection. If the customer decides to use the password method, they must set the **Password Mode Locking Bit**. This will permanently set the part to operate only using password sector protection.

It is important to remember that setting either the **Persistent Sector Protection Mode Locking Bit** or the **Password Mode Locking Bit** permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit has been set. **It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone.** This is so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

The device is shipped with all sectors unprotected. Optional Spansion™ programming services enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for Details.

It is possible to determine whether a sector is protected or unprotected. See "Autoselect Command Sequence" section on page 67 for details.

Persistent Sector Protection

The Persistent Sector Protection method replaces the old 12 V controlled protection method while at the same time enhancing flexibility by providing three different sector protection states:

- **Persistently Locked**—A sector is protected and cannot be changed.
- **Dynamically Locked**—The sector is protected and can be changed by a simple command
- **Unlocked**—The sector is unprotected and can be changed by a simple command

In order to achieve these states, three types of "bits" are going to be used:

Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to a maximum of four sectors ("S29WS128/064J_MCP Boot Sector/Sector Block Addresses for Protection/Unprotection" section on page 30, "S29WS064J Boot Sector/Sector Block Addresses for Protection/Unprotection" section on page 32). All 4 Kbyte boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the **PPB Program Command**.

Note: If a PPB requires erasure, all of the sector PPBs must first be preprogrammed prior to PPB erasing. All PPBs erase in parallel, unlike programming where individual PPBs are programmable. It is the responsibility of the user to perform the preprogramming operation. Otherwise, an already erased sector PPBs has the potential of being over-erased. There is no hardware mechanism to prevent sector PPBs over-erasure.

Persistent Protection Bit Lock (PPB Lock)

A global volatile bit. When set to "1", the PPBs cannot be changed. When cleared ("0"), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYBs is "0". Each DYB is individually modifiable through the DPB Write Command.

When the parts are first shipped, the PPBs are cleared ("0"). The DPBs and PPB Lock are defaulted to power up in the cleared state – meaning the PPBs are changeable.

When the device is first powered on, the DYBs power up in the cleared state (sectors not protected). The Protection State for each sector is determined by the logical OR of the PPB and the DPB related to that sector. For the sectors that have the PPBs cleared, the DPBs control whether or not the sector is protected or unprotected. By issuing the DPB Write command sequences, the DPBs will be set or cleared, thus placing each sector in the protected or unprotected state. These are the so-called **Dynamic Locked or Unlocked** states. They are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DPBs maybe set or cleared as often as needed.

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because they are Non-Volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are also limited to 100 erase cycles.

The PBB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to "1". Setting the PPB Lock disables all program and erase commands to the Non-Volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the PPB are needed e.g. to allow new system code to be

downloaded. If no changes are needed then the boot code can set the PPB Lock to disable any further changes to the PPBs during system operation.

The WP# write protect pin adds a final level of hardware protection to the four outermost 4 Kbytes sectors (SA0 - SA3 for a bottom boot, WS128J: SA266 - SA269, WS064J: SA138 - SA141, or SA0 - SA3 & WS128J: SA266 - SA269, WS064J: SA138 - SA141 for a dual boot). When this pin is low it is not possible to change the contents of these four sectors. These sectors generally hold system boot code. So, the WP# pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DPB Write command sequence is all that is necessary. The DPB write command for the dynamic sectors switch the DPBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB lock bit once again will lock the PPBs, and the device operates normally again.

Note: to achieve the best protection, it's recommended to execute the PPB lock bit set command early in the boot code, and protect the boot code by holding WP# = V_{IL}.

Table 6. Sector Protection Schemes

DPB	PPB	PPB Lock	Sector State
0	0	0	Unprotected—PPB and DPB are changeable
1	0	0	Protected—PPB and DPB are changeable
0	1	0	Protected—PPB and DPB are changeable
1	1	0	Protected—PPB and DPB are changeable
0	0	1	Unprotected—PPB not changeable, DPB is changeable
1	0	1	Protected—PPB not changeable, DPB is changeable
0	1	1	Protected—PPB not changeable, DPB is changeable
1	1	1	Protected—PPB not changeable, DPB is changeable

Table 6 contains all possible combinations of the DPB, PPB, and PPB lock relating to the status of the sector.

In summary, if the PPB is set, and the PPB lock is set, the sector is protected and the protection can not be removed until the next power cycle clears the PPB lock. If the PPB is cleared, the sector can be dynamically locked or unlocked. The DPB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector.

The programming of the DPB, PPB, and PPB lock for a given sector can be verified by writing a DPB/PPB/PPB lock verify command to the device.

Persistent Sector Protection Mode Locking Bit

Like the password mode locking bit, a Persistent Sector Protection mode locking bit exists to guarantee that the device remain in software sector protection. Once set, the Persistent Sector Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that a hacker could not place the device in password protection mode.

Password Protection Mode

The Password Sector Protection Mode method allows an even higher level of security than the Persistent Sector Protection Mode. There are two main differences between the Persistent Sector Protection and the Password Sector Protection Mode:

- When the device is first powered on, or comes out of a reset cycle, the PPB Lock bit is set to the **locked state**, rather than cleared to the unlocked state.
- The only means to clear the PPB Lock bit is by writing a unique **64-bit Password** to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

The password is stored in a the Secured Silicon region of the flash memory. Once the Password Mode Locking Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 2 µs delay for each "password check." This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

Password and Password Mode Locking Bit

In order to select the Password sector protection scheme, the customer must first program the password. FASL recommends that the password be somehow correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

1. It permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
2. It also disables *all further commands* to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there will be no way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see "Password Program Command" section on page 72 and "Password Verify Command" section on page 73). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

Persistent Protection Bit Lock

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Lock Bit is also set, after a hardware reset (RESET# asserted) or a power-up reset the ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a "1".

If the Password Mode Locking Bit is not set, including Persistent Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is setable by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

High Voltage Sector Protection

Sector protection and unprotection may also be implemented using programming equipment. The procedure requires high voltage (VID) to be placed on the RESET# pin. Refer to Figure 2, "In-System Sector Protection/Sector Unprotection Algorithms," on page 41 for details on this procedure. Note that for sector unprotect, all unprotected sectors must be first protected prior to the first sector write cycle. Once the Password Mode Locking bit or Persistent Protection Locking bit are set, the high voltage sector protect/unprotect capability is disabled.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# inputs are both held at V_{CC} ± 0.2 V. The device requires standard access time (t_{CE}) for read access, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the "DC Characteristics" section on page 87 represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. While in asynchronous mode, the device automatically enables this mode when addresses remain stable for t_{ACC} + 60 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. **Based on the implementation by design, the Auto Power Down feature is disabled in synchronous mode and enabled in asynchronous mode. As a result, in synchronous mode, the device can be in Auto Power Down Mode only by deselecting the CE#.** Note that a new burst operation is required to provide new data.

I_{CC6} in the "DC Characteristics" section on page 87 represents the automatic sleep mode current specification.

RESET#: Hardware Reset Input

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, resets the configuration register, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS} ± 0.2 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS} ± 0.2 V, the standby current will be greater.

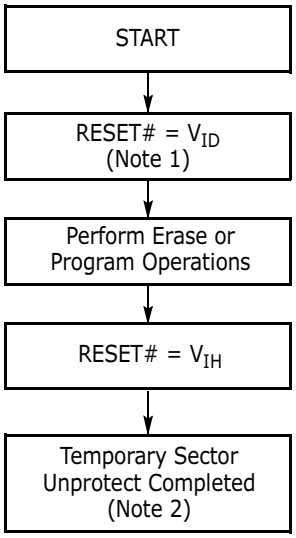
RESET# may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the device requires a time of t_{READY} (during Embedded Algorithms) before the device is ready to read data again. If RESET# is asserted when a program or erase operation is not executing, the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after RESET# returns to V_{IH}.

Refer to the "AC Characteristics" section on page 97 for RESET# parameters and to Figure 21, "Reset Timings," on page 97 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.



Notes:

1. *All protected sectors unprotected (If WP# = V_{IL}, outermost boot sectors will remain protected).*
2. *All previously protected sectors are protected once again.*

Figure I. Temporary Sector Unprotect Operation

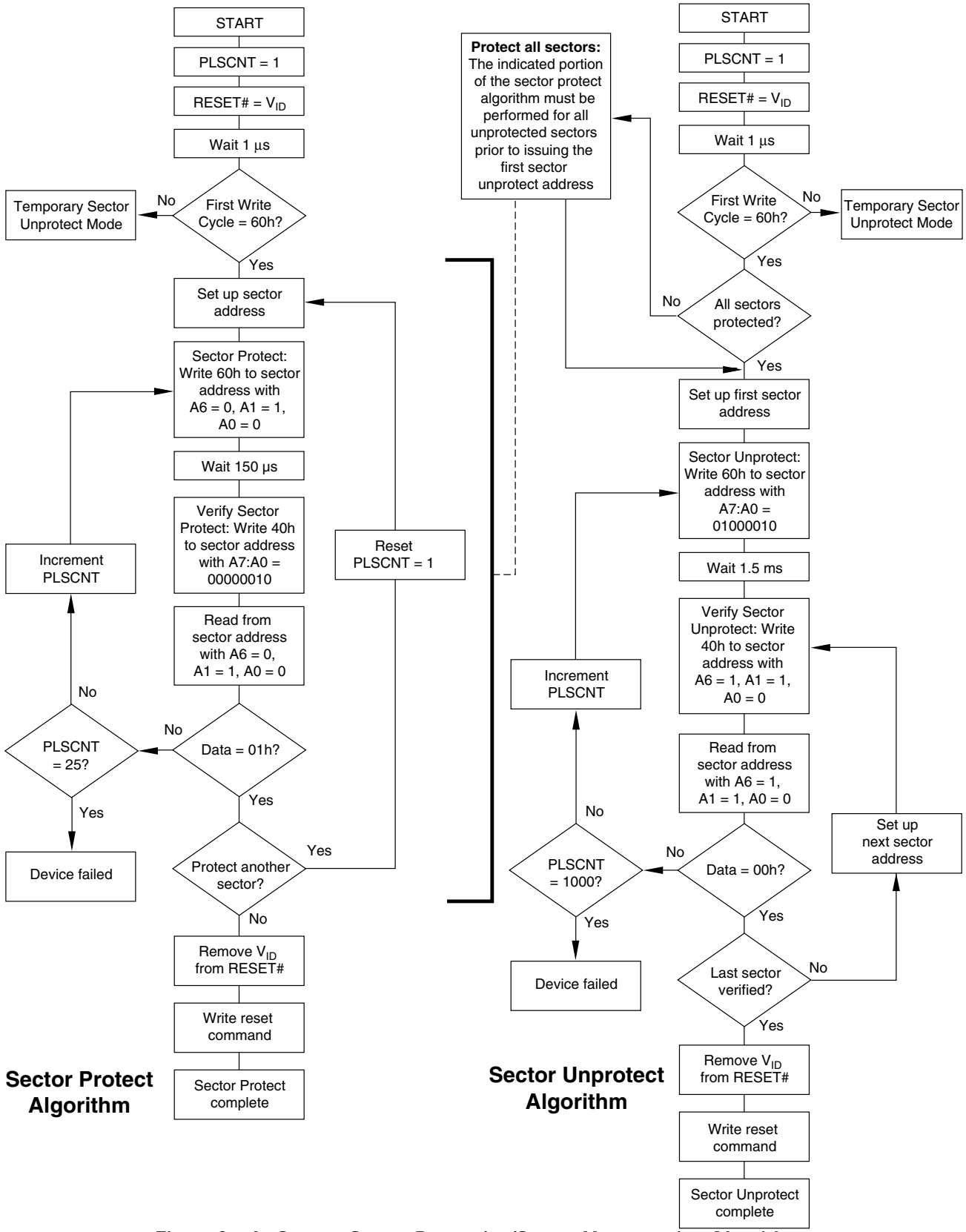


Figure 2. In-System Sector Protection/Sector Unprotection Algorithms

Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector is 128 words in length and located at addresses 000000h-000007h. The Factory Indicator Bit (DQ7) is used to indicate whether or not the Factory Secured Silicon Sector is locked when shipped from the factory. The Customer Indicator Bit (DQ6) is used to indicate whether or not the Customer Secured Silicon Sector is locked when shipped from the factory. These bits are permanently set at the factory and cannot be changed, in order to prevent cloning of a factory locked part. This ensures the security of the ESN and customer code once the product is shipped to the field.

FASL™ offers the device with a 64 word Factory Secured Silicon Sector that is locked when the part is shipped and a 64 words Customer Secured Silicon Sector that is either locked or is lockable. The Factory Secured Silicon Sector is always protected when shipped from the factory, and has the Factory Indicator Bit (DQ7) permanently set to a "1". The Customer Secured Silicon Sector is shipped unprotected with the Customer Indicator Bit (DQ6) set to "0", allowing customers to utilize that sector in any manner they choose. Once the Customer Secured Silicon Sector area is protected, the Customer Indicator Bit will be permanently set to "1."

The system accesses the Secured Silicon Sector through a command sequence (see "Enter/Exit Secured Silicon Sector Command Sequence"). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by the memory array. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. While Secured Silicon Sector access is enabled, Memory Array read access, program operations, and erase operations to all sectors other than SA0 are also available. On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space.

Factory Locked: Factor Secured Silicon Sector Programmed and Protected At the Factory

In a factory sector locked device, the Factory Secured Silicon Sector is protected when the device is shipped from the factory whether or not the area was programmed at the factory. The Factory Secured Silicon Sector cannot be modified in any way. Optional Spansion™ programming service can preprogram a random ESN, a customer-defined code, or any combination of the two. The Factory Secured Silicon Sector is located at addresses 000000h–00003Fh.

The device is available preprogrammed with one of the following:

- A random, secure ESN only within the Factor Secured Silicon Sector
- Customer code within the Customer Secured Silicon Sector through the Spansion programming service
- Both a random, secure ESN and customer code through the Spansion programming service.

Table 7. Secured Silicon Sector Addresses

Sector	Sector Size	Address Range
Customer	64 words	000040h-00007Fh
Factory	64 words	000000h-00003Fh

Customers may opt to have their code programmed by FASL through the Spansion programming service. FASL programs the customer's code, with or without the random ESN. The devices are then shipped from FASL's factory with the Factory Secured Silicon Sector and Customer Secured Silicon Sector permanently locked. Contact the local sales office for details on using Spansion programming services.

Customer Secured Silicon Sector

The customer lockable area is shipped unprotected, which allows the customer to program and optionally lock the area as appropriate for the application. security feature is not required, the Customer Secured Silicon Sector can be treated as an additional Flash memory space. The Customer Secured Silicon Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the Customer Secured Silicon Sector, but reading in Banks A, B, and C is available. The Customer Secured Silicon Sector is located at addresses 000040h–00007Fh.

The Customer Secured Silicon Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, "In-System Sector Protection/Sector Unprotection Algorithms," on page 41 except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the Customer Secured Silicon Sector Region without raising any device pin to a high voltage. Note that this method is only applicable to the Secured Silicon Sector.
- Write the Secured Silicon Sector Protection Bit Lock command sequence.

Once the Customer Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing the remainder of the array.

The Customer Secured Silicon Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the Customer Secured Silicon Sector area and none of the bits in the Customer Secured Silicon Sector memory space can be modified in any way.

Secured Silicon Sector Protection Bit

The Customer Secured Silicon Sector Protection Bit prevents programming of the Customer Secured Silicon Sector memory area. Once set, the Customer Secured Silicon Sector memory area contents are non-modifiable.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 18, "Command Definitions," on page 76 for command definitions).

The device offers two types of data protection at the sector level:

- The PPB and DPB associated command sequences disables or re-enables both program and erase operations in any sector or sector group.
- When WP# is at V_{IL}, the four outermost sectors are locked.
- When ACC is at V_{IL}, all sectors are locked.

The following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting the four outermost sectors. This function is provided by the WP# pin and overrides the previously discussed Sector Protection/Unprotection method.

If the system asserts V_{IL} on the WP# pin, the device disables program and erase functions in the four "outermost" 4 Kword boot sectors. The four outermost 4 Kword boot sectors are the four sectors containing the lowest addresses (SA0 - SA3), or the four sectors containing the highest addresses (WS128J: SA266 - SA269, WS064J: SA138 - SA141) or both the lower four (SA0 - SA3) and upper four sectors (WS128J: SA266 - SA269, WS064J: SA138 - SA141) in a dual-boot-configured device.

If the system asserts V_{IH} on the WP# pin, the device reverts to whether the upper and/or lower four sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected using the method described in "PPB Program Command" section on page 75.

Note that the WP# pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = RESET# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 8-11. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 8-11. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the FASL site at the following URL: http://www.amd.com/us-en/FlashMemory/TechnicalResources/0,,37_1693_1780_1834^1955,00.html. Alternatively, contact an FASL representative for copies of these documents.

Table 8. CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string "QRY"
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 9. System Interface String

Addresses	Data	Description
1Bh	0017h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0019h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0003h	Typical timeout per single byte/word write 2^N µs
20h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	0009h	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0004h	Max. timeout for byte/word write 2^N times typical
24h	0000h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table I0. Device Geometry Definition

Addresses	Data	Description
27h	0018h (WS128J) 0017h (WS064J)	Device Size = 2^N byte
28h 29h	0001h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0000h 0000h	Max. number of bytes in multi-byte write = 2^N (00h = not supported)
2Ch	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h	00FDh (WS128J) 007Dh (WS064J)	Erase Block Region 2 Information
32h 33h 34h	0000h 0000h 0001h	
35h 36h 37h 38h	0007h 0000h 0020h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

Table II. Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string "PRI"
43h	0031h	Major version number, ASCII
44h	0033h	Minor version number, ASCII
45h	000Ch	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Technology (Bits 5-2) 0011 = 0.13 µm
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0007h	Sector Protect/Unprotect scheme 07 = Advanced Sector Protection
4Ah	00E7h (WS128J) 0077h (WS064J)	Simultaneous Operation Number of Sectors in all banks except boot block
4Bh	0001h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page, 04 = 16 Word Page
4Dh	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0001h	Top/Bottom Boot Sector Flag 01h = Dual Boot Device, 02h = Bottom Boot Device, 03h = Top Boot Device
50h	0000h	Program Suspend. 00h = not supported
57h	0004h	Bank Organization: X = Number of banks
58h	0027h (WS128J) 0017h (WS064J)	Bank A Region Information. X = Number of sectors in bank
59h	0060h (WS128J) 0030h (WS064J)	Bank B Region Information. X = Number of sectors in bank
5Ah	0060h (WS128J) 0030h (WS064J)	Bank C Region Information. X = Number of sectors in bank
5Bh	0027h (WS128J) 0017h (WS064J)	Bank D Region Information. X = Number of sectors in bank

Table I2. WSI28J Sector Address Table

Bank	Sector	Sector Size	(x16) Address Range
Bank D	SA0	4 Kwords	000000h-000FFFh
	SA1	4 Kwords	001000h-001FFFh
	SA2	4 Kwords	002000h-002FFFh
	SA3	4 Kwords	003000h-003FFFh
	SA4	4 Kwords	004000h-004FFFh
	SA5	4 Kwords	005000h-005FFFh
	SA6	4 Kwords	006000h-006FFFh
	SA7	4 Kwords	007000h-007FFFh
	SA8	32 Kwords	008000h-00FFFFh
	SA9	32 Kwords	010000h-017FFFh
	SA10	32 Kwords	018000h-01FFFFh
	SA11	32 Kwords	020000h-027FFFh
	SA12	32 Kwords	028000h-02FFFFh
	SA13	32 Kwords	030000h-037FFFh
	SA14	32 Kwords	038000h-03FFFFh
	SA15	32 Kwords	040000h-047FFFh
	SA16	32 Kwords	048000h-04FFFFh
	SA17	32 Kwords	050000h-057FFFh
	SA18	32 Kwords	058000h-05FFFFh
	SA19	32 Kwords	060000h-067FFFh
	SA20	32 Kwords	068000h-06FFFFh
	SA21	32 Kwords	070000h-077FFFh
	SA22	32 Kwords	078000h-07FFFFh
	SA23	32 Kwords	080000h-087FFFh
	SA24	32 Kwords	088000h-08FFFFh
	SA25	32 Kwords	090000h-097FFFh
	SA26	32 Kwords	098000h-09FFFFh
	SA27	32 Kwords	0A0000h-0A7FFFh
	SA28	32 Kwords	0A8000h-0AFFFFh
	SA29	32 Kwords	0B0000h-0B7FFFh
	SA30	32 Kwords	0B8000h-0BFFFFh
	SA31	32 Kwords	0C0000h-0C7FFFh
	SA32	32 Kwords	0C8000h-0CFFFFh
	SA33	32 Kwords	0D0000h-0D7FFFh
	SA34	32 Kwords	0D8000h-0DFFFFh
	SA35	32 Kwords	0E0000h-0E7FFFh
	SA36	32 Kwords	0E8000h-0EFFFFh
	SA37	32 Kwords	0F0000h-0F7FFFh
	SA38	32 Kwords	0F8000h-0FFFFFh

Table I2. WSI28J Sector Address Table

Bank	Sector	Sector Size	(x16) Address Range
Bank C	SA39	32 Kwords	100000h-107FFFh
	SA40	32 Kwords	108000h-10FFFFh
	SA41	32 Kwords	110000h-117FFFh
	SA42	32 Kwords	118000h-11FFFFh
	SA43	32 Kwords	120000h-127FFFh
	SA44	32 Kwords	128000h-12FFFFh
	SA45	32 Kwords	130000h-137FFFh
	SA46	32 Kwords	138000h-13FFFFh
	SA47	32 Kwords	140000h-147FFFh
	SA48	32 Kwords	148000h-14FFFFh
	SA49	32 Kwords	150000h-157FFFh
	SA50	32 Kwords	158000h-15FFFFh
	SA51	32 Kwords	160000h-167FFFh
	SA52	32 Kwords	168000h-16FFFFh
	SA53	32 Kwords	170000h-177FFFh
	SA54	32 Kwords	178000h-17FFFFh
	SA55	32 Kwords	180000h-187FFFh
	SA56	32 Kwords	188000h-18FFFFh
	SA57	32 Kwords	190000h-197FFFh
	SA58	32 Kwords	198000h-19FFFFh
	SA59	32 Kwords	1A0000h-1A7FFFh
	SA60	32 Kwords	1A8000h-1AFFFFh
	SA61	32 Kwords	1B0000h-1B7FFFh
	SA62	32 Kwords	1B8000h-1BFFFFh
	SA63	32 Kwords	1C0000h-1C7FFFh
	SA64	32 Kwords	1C8000h-1CFFFFh
	SA65	32 Kwords	1D0000h-1D7FFFh
	SA66	32 Kwords	1D8000h-1DFFFFh
	SA67	32 Kwords	1E0000h-1E7FFFh
	SA68	32 Kwords	1E8000h-1EFFFFh
	SA69	32 Kwords	1F0000h-1F7FFFh
	SA70	32 Kwords	1F8000h-1FFFFFh

Table I2. WSI28J Sector Address Table

Bank	Sector	Sector Size	(x16) Address Range
Bank C	SA71	32 Kwords	200000h-207FFFh
	SA72	32 Kwords	208000h-20FFFFh
	SA73	32 Kwords	210000h-217FFFh
	SA74	32 Kwords	218000h-21FFFFh
	SA75	32 Kwords	220000h-227FFFh
	SA76	32 Kwords	228000h-22FFFFh
	SA77	32 Kwords	230000h-237FFFh
	SA78	32 Kwords	238000h-23FFFFh
	SA79	32 Kwords	240000h-247FFFh
	SA80	32 Kwords	248000h-24FFFFh
	SA81	32 Kwords	250000h-257FFFh
	SA82	32 Kwords	258000h-25FFFFh
	SA83	32 Kwords	260000h-267FFFh
	SA84	32 Kwords	268000h-26FFFFh
	SA85	32 Kwords	270000h-277FFFh
	SA86	32 Kwords	278000h-27FFFFh
	SA87	32 Kwords	280000h-287FFFh
	SA88	32 Kwords	288000h-28FFFFh
	SA89	32 Kwords	290000h-297FFFh
	SA90	32 Kwords	298000h-29FFFFh
	SA91	32 Kwords	2A0000h-2A7FFFh
	SA92	32 Kwords	2A8000h-2AFFFFh
	SA93	32 Kwords	2B0000h-2B7FFFh
	SA94	32 Kwords	2B8000h-2BFFFFh
	SA95	32 Kwords	2C0000h-2C7FFFh
	SA96	32 Kwords	2C8000h-2CFFFFh
	SA97	32 Kwords	2D0000h-2D7FFFh
	SA98	32 Kwords	2D8000h-2DFFFFh
	SA99	32 Kwords	2E0000h-2E7FFFh
	SA100	32 Kwords	2E8000h-2EFFFFh
	SA101	32 Kwords	2F0000h-2F7FFFh
	SA102	32 Kwords	2F8000h-2FFFFFh

Table I2. WSI28J Sector Address Table

Bank	Sector	Sector Size	(x16) Address Range
Bank C	SA103	32 Kwords	300000h-307FFFh
	SA104	32 Kwords	308000h-30FFFFh
	SA105	32 Kwords	310000h-317FFFh
	SA106	32 Kwords	318000h-31FFFFh
	SA107	32 Kwords	320000h-327FFFh
	SA108	32 Kwords	328000h-32FFFFh
	SA109	32 Kwords	330000h-337FFFh
	SA110	32 Kwords	338000h-33FFFFh
	SA111	32 Kwords	340000h-347FFFh
	SA112	32 Kwords	348000h-34FFFFh
	SA113	32 Kwords	350000h-357FFFh
	SA114	32 Kwords	358000h-35FFFFh
	SA115	32 Kwords	360000h-367FFFh
	SA116	32 Kwords	368000h-36FFFFh
	SA117	32 Kwords	370000h-377FFFh
	SA118	32 Kwords	378000h-37FFFFh
	SA119	32 Kwords	380000h-387FFFh
	SA120	32 Kwords	388000h-38FFFFh
	SA121	32 Kwords	390000h-397FFFh
	SA122	32 Kwords	398000h-39FFFFh
	SA123	32 Kwords	3A0000h-3A7FFFh
	SA124	32 Kwords	3A8000h-3AFFFFh
	SA125	32 Kwords	3B0000h-3B7FFFh
	SA126	32 Kwords	3B8000h-3BFFFFh
	SA127	32 Kwords	3C0000h-3C7FFFh
	SA128	32 Kwords	3C8000h-3CFFFFh
	SA129	32 Kwords	3D0000h-3D7FFFh
	SA130	32 Kwords	3D8000h-3DFFFFh
	SA131	32 Kwords	3E0000h-3E7FFFh
	SA132	32 Kwords	3E8000h-3EFFFFh
	SA133	32 Kwords	3F0000h-3F7FFFh
	SA134	32 Kwords	3F8000h-3FFFFFh

Table I2. WSI28J Sector Address Table

Bank	Sector	Sector Size	(x16) Address Range
Bank B	SA135	32 Kwords	400000h-407FFFh
	SA136	32 Kwords	408000h-40FFFFh
	SA137	32 Kwords	410000h-417FFFh
	SA138	32 Kwords	418000h-41FFFFh
	SA139	32 Kwords	420000h-427FFFh
	SA140	32 Kwords	428000h-42FFFFh
	SA141	32 Kwords	430000h-437FFFh
	SA142	32 Kwords	438000h-43FFFFh
	SA143	32 Kwords	440000h-447FFFh
	SA144	32 Kwords	448000h-44FFFFh
	SA145	32 Kwords	450000h-457FFFh
	SA146	32 Kwords	458000h-45FFFFh
	SA147	32 Kwords	460000h-467FFFh
	SA148	32 Kwords	468000h-46FFFFh
	SA149	32 Kwords	470000h-477FFFh
	SA150	32 Kwords	478000h-47FFFFh
	SA151	32 Kwords	480000h-487FFFh
	SA152	32 Kwords	488000h-48FFFFh
	SA153	32 Kwords	490000h-497FFFh
	SA154	32 Kwords	498000h-49FFFFh
	SA155	32 Kwords	4A0000h-4A7FFFh
	SA156	32 Kwords	4A8000h-4AFFFFh
	SA157	32 Kwords	4B0000h-4B7FFFh
	SA158	32 Kwords	4B8000h-4BFFFFh
	SA159	32 Kwords	4C0000h-4C7FFFh
	SA160	32 Kwords	4C8000h-4CFFFFh
	SA161	32 Kwords	4D0000h-4D7FFFh
	SA162	32 Kwords	4D8000h-4DFFFFh
	SA163	32 Kwords	4E0000h-4E7FFFh
	SA164	32 Kwords	4E8000h-4EFFFFh
	SA165	32 Kwords	4F0000h-4F7FFFh
	SA166	32 Kwords	4F8000h-4FFFFFh

Table I2. WSI28J Sector Address Table

Bank	Sector	Sector Size	(x16) Address Range
Bank B	SA167	32 Kwords	500000h-507FFFh
	SA168	32 Kwords	508000h-50FFFFh
	SA169	32 Kwords	510000h-517FFFh
	SA170	32 Kwords	518000h-51FFFFh
	SA171	32 Kwords	520000h-527FFFh
	SA172	32 Kwords	528000h-52FFFFh
	SA173	32 Kwords	530000h-537FFFh
	SA174	32 Kwords	538000h-53FFFFh
	SA175	32 Kwords	540000h-547FFFh
	SA176	32 Kwords	548000h-54FFFFh
	SA177	32 Kwords	550000h-557FFFh
	SA178	32 Kwords	558000h-55FFFFh
	SA179	32 Kwords	560000h-567FFFh
	SA180	32 Kwords	568000h-56FFFFh
	SA181	32 Kwords	570000h-577FFFh
	SA182	32 Kwords	578000h-57FFFFh
	SA183	32 Kwords	580000h-587FFFh
	SA184	32 Kwords	588000h-58FFFFh
	SA185	32 Kwords	590000h-597FFFh
	SA186	32 Kwords	598000h-59FFFFh
	SA187	32 Kwords	5A0000h-5A7FFFh
	SA188	32 Kwords	5A8000h-5AFFFFh
	SA189	32 Kwords	5B0000h-5B7FFFh
	SA190	32 Kwords	5B8000h-5BFFFFh
	SA191	32 Kwords	5C0000h-5C7FFFh
	SA192	32 Kwords	5C8000h-5CFFFFh
	SA193	32 Kwords	5D0000h-5D7FFFh
	SA194	32 Kwords	5D8000h-5DFFFFh
	SA195	32 Kwords	5E0000h-5E7FFFh
	SA196	32 Kwords	5E8000h-5EFFFFh
	SA197	32 Kwords	5F0000h-5F7FFFh
	SA198	32 Kwords	5F8000h-5FFFFFh

Table I2. WSI28J Sector Address Table

Bank	Sector	Sector Size	(x16) Address Range
Bank B	SA199	32 Kwords	600000h-607FFFh
	SA200	32 Kwords	608000h-60FFFFh
	SA201	32 Kwords	610000h-617FFFh
	SA202	32 Kwords	618000h-61FFFFh
	SA203	32 Kwords	620000h-627FFFh
	SA204	32 Kwords	628000h-62FFFFh
	SA205	32 Kwords	630000h-637FFFh
	SA206	32 Kwords	638000h-63FFFFh
	SA207	32 Kwords	640000h-647FFFh
	SA208	32 Kwords	648000h-64FFFFh
	SA209	32 Kwords	650000h-657FFFh
	SA210	32 Kwords	658000h-65FFFFh
	SA211	32 Kwords	660000h-667FFFh
	SA212	32 Kwords	668000h-66FFFFh
	SA213	32 Kwords	670000h-677FFFh
	SA214	32 Kwords	678000h-67FFFFh
	SA215	32 Kwords	680000h-687FFFh
	SA216	32 Kwords	688000h-68FFFFh
	SA217	32 Kwords	690000h-697FFFh
	SA218	32 Kwords	698000h-69FFFFh
	SA219	32 Kwords	6A0000h-6A7FFFh
	SA220	32 Kwords	6A8000h-6AFFFFh
	SA221	32 Kwords	6B0000h-6B7FFFh
	SA222	32 Kwords	6B8000h-6BFFFFh
	SA223	32 Kwords	6C0000h-6C7FFFh
	SA224	32 Kwords	6C8000h-6CFFFFh
	SA225	32 Kwords	6D0000h-6D7FFFh
	SA226	32 Kwords	6D8000h-6DFFFFh
	SA227	32 Kwords	6E0000h-6E7FFFh
	SA228	32 Kwords	6E8000h-6EFFFFh
	SA229	32 Kwords	6F0000h-6F7FFFh
	SA230	32 Kwords	6F8000h-6FFFFFh

Table I2. WSI28J Sector Address Table

Bank	Sector	Sector Size	(x16) Address Range
Bank A	SA231	32 Kwords	700000h-707FFFh
	SA232	32 Kwords	708000h-70FFFFh
	SA233	32 Kwords	710000h-717FFFh
	SA234	32 Kwords	718000h-71FFFFh
	SA235	32 Kwords	720000h-727FFFh
	SA236	32 Kwords	728000h-72FFFFh
	SA237	32 Kwords	730000h-737FFFh
	SA238	32 Kwords	738000h-73FFFFh
	SA239	32 Kwords	740000h-747FFFh
	SA240	32 Kwords	748000h-74FFFFh
	SA241	32 Kwords	750000h-757FFFh
	SA242	32 Kwords	758000h-75FFFFh
	SA243	32 Kwords	760000h-767FFFh
	SA244	32 Kwords	768000h-76FFFFh
	SA245	32 Kwords	770000h-777FFFh
	SA246	32 Kwords	778000h-77FFFFh
	SA247	32 Kwords	780000h-787FFFh
	SA248	32 Kwords	788000h-78FFFFh
	SA249	32 Kwords	790000h-797FFFh
	SA250	32 Kwords	798000h-79FFFFh
	SA251	32 Kwords	7A0000h-7A7FFFh
	SA252	32 Kwords	7A8000h-7AFFFFh
	SA253	32 Kwords	7B0000h-7B7FFFh
	SA254	32 Kwords	7B8000h-7BFFFFh
	SA255	32 Kwords	7C0000h-7C7FFFh
	SA256	32 Kwords	7C8000h-7CFFFFh
	SA257	32 Kwords	7D0000h-7D7FFFh
	SA258	32 Kwords	7D8000h-7DFFFFh
	SA259	32 Kwords	7E0000h-7E7FFFh
	SA260	32 Kwords	7E8000h-7EFFFFh
	SA261	32 Kwords	7F0000h-7F7FFFh
	SA262	4 Kwords	7F8000h-7F8FFFh
	SA263	4 Kwords	7F9000h-7F9FFFh
	SA264	4 Kwords	7FA000h-7FAFFFh
	SA265	4 Kwords	7FB000h-7FBFFFh
	SA266	4 Kwords	7FC000h-7FCFFFh
	SA267	4 Kwords	7FD000h-7FDFFFh
	SA268	4 Kwords	7FE000h-7FEFFFh
	SA269	4 Kwords	7FF000h-7FFFFFh

Table 13. WS064J Sector Address Table

Bank	Sector	Sector Size	(x16) Address Range
Bank D	SA0	4 Kwords	000000h-000FFFh
	SA1	4 Kwords	001000h-001FFFh
	SA2	4 Kwords	002000h-002FFFh
	SA3	4 Kwords	003000h-003FFFh
	SA4	4 Kwords	004000h-004FFFh
	SA5	4 Kwords	005000h-005FFFh
	SA6	4 Kwords	006000h-006FFFh
	SA7	4 Kwords	007000h-007FFFh
	SA8	32 Kwords	008000h-00FFFFh
	SA9	32 Kwords	010000h-017FFFh
	SA10	32 Kwords	018000h-01FFFFh
	SA11	32 Kwords	020000h-027FFFh
	SA12	32 Kwords	028000h-02FFFFh
	SA13	32 Kwords	030000h-037FFFh
	SA14	32 Kwords	038000h-03FFFFh
	SA15	32 Kwords	040000h-047FFFh
	SA16	32 Kwords	048000h-04FFFFh
	SA17	32 Kwords	050000h-057FFFh
	SA18	32 Kwords	058000h-05FFFFh
	SA19	32 Kwords	060000h-067FFFh
	SA20	32 Kwords	068000h-06FFFFh
	SA21	32 Kwords	070000h-077FFFh
	SA22	32 Kwords	078000h-07FFFFh

Table 13. WS064J Sector Address Table

Bank	Sector	Sector Size	(x16) Address Range
Bank C	SA23	32 Kwords	080000h-087FFFh
	SA24	32 Kwords	088000h-08FFFFh
	SA25	32 Kwords	090000h-097FFFh
	SA26	32 Kwords	098000h-09FFFFh
	SA27	32 Kwords	0A0000h-0A7FFFh
	SA28	32 Kwords	0A8000h-0AFFFFh
	SA29	32 Kwords	0B0000h-0B7FFFh
	SA30	32 Kwords	0B8000h-0BFFFFh
	SA31	32 Kwords	0C0000h-0C7FFFh
	SA32	32 Kwords	0C8000h-0CFFFFh
	SA33	32 Kwords	0D0000h-0D7FFFh
	SA34	32 Kwords	0D8000h-0DFFFFh
	SA35	32 Kwords	0E0000h-0E7FFFh
	SA36	32 Kwords	0E8000h-0EFFFFh
	SA37	32 Kwords	0F0000h-0F7FFFh
	SA38	32 Kwords	0F8000h-0FFFFFh
	SA39	32 Kwords	100000h-107FFFh
	SA40	32 Kwords	108000h-10FFFFh
	SA41	32 Kwords	110000h-117FFFh
	SA42	32 Kwords	118000h-11FFFFh
	SA43	32 Kwords	120000h-127FFFh
	SA44	32 Kwords	128000h-12FFFFh
	SA45	32 Kwords	130000h-137FFFh
	SA46	32 Kwords	138000h-13FFFFh

Table 13. WS064J Sector Address Table

Bank	Sector	Sector Size	(x16) Address Range
Bank C	SA47	32 Kwords	140000h-147FFFh
	SA48	32 Kwords	148000h-14FFFFh
	SA49	32 Kwords	150000h-157FFFh
	SA50	32 Kwords	158000h-15FFFFh
	SA51	32 Kwords	160000h-167FFFh
	SA52	32 Kwords	168000h-16FFFFh
	SA53	32 Kwords	170000h-177FFFh
	SA54	32 Kwords	178000h-17FFFFh
	SA55	32 Kwords	180000h-187FFFh
	SA56	32 Kwords	188000h-18FFFFh
	SA57	32 Kwords	190000h-197FFFh
	SA58	32 Kwords	198000h-19FFFFh
	SA59	32 Kwords	1A0000h-1A7FFFh
	SA60	32 Kwords	1A8000h-1AFFFFh
	SA61	32 Kwords	1B0000h-1B7FFFh
	SA62	32 Kwords	1B8000h-1BFFFFh
	SA63	32 Kwords	1C0000h-1C7FFFh
	SA64	32 Kwords	1C8000h-1CFFFFh
	SA65	32 Kwords	1D0000h-1D7FFFh
	SA66	32 Kwords	1D8000h-1DFFFFh
	SA67	32 Kwords	1E0000h-1E7FFFh
	SA68	32 Kwords	1E8000h-1EFFFFh
	SA69	32 Kwords	1F0000h-1F7FFFh
	SA70	32 Kwords	1F8000h-1FFFFFh

Table 13. WS064J Sector Address Table

Bank	Sector	Sector Size	(x16) Address Range
Bank B	SA71	32 Kwords	200000h-207FFFh
	SA72	32 Kwords	208000h-20FFFFh
	SA73	32 Kwords	210000h-217FFFh
	SA74	32 Kwords	218000h-21FFFFh
	SA75	32 Kwords	220000h-227FFFh
	SA76	32 Kwords	228000h-22FFFFh
	SA77	32 Kwords	230000h-237FFFh
	SA78	32 Kwords	238000h-23FFFFh
	SA79	32 Kwords	240000h-247FFFh
	SA80	32 Kwords	248000h-24FFFFh
	SA81	32 Kwords	250000h-257FFFh
	SA82	32 Kwords	258000h-25FFFFh
	SA83	32 Kwords	260000h-267FFFh
	SA84	32 Kwords	268000h-26FFFFh
	SA85	32 Kwords	270000h-277FFFh
	SA86	32 Kwords	278000h-27FFFFh
	SA87	32 Kwords	280000h-287FFFh
	SA88	32 Kwords	288000h-28FFFFh
	SA89	32 Kwords	290000h-297FFFh
	SA90	32 Kwords	298000h-29FFFFh
	SA91	32 Kwords	2A0000h-2A7FFFh
	SA92	32 Kwords	2A8000h-2AFFFFh
	SA93	32 Kwords	2B0000h-2B7FFFh
	SA94	32 Kwords	2B8000h-2BFFFFh

Table 13. WS064J Sector Address Table

Bank	Sector	Sector Size	(x16) Address Range
Bank B	SA95	32 Kwords	2C0000h-2C7FFFh
	SA96	32 Kwords	2C8000h-2CFFFFh
	SA97	32 Kwords	2D0000h-2D7FFFh
	SA98	32 Kwords	2D8000h-2DFFFFh
	SA99	32 Kwords	2E0000h-2E7FFFh
	SA100	32 Kwords	2E8000h-2EFFFFh
	SA101	32 Kwords	2F0000h-2F7FFFh
	SA102	32 Kwords	2F8000h-2FFFFFh
	SA103	32 Kwords	300000h-307FFFh
	SA104	32 Kwords	308000h-30FFFFh
	SA105	32 Kwords	310000h-317FFFh
	SA106	32 Kwords	318000h-31FFFFh
	SA107	32 Kwords	320000h-327FFFh
	SA108	32 Kwords	328000h-32FFFFh
	SA109	32 Kwords	330000h-337FFFh
	SA110	32 Kwords	338000h-33FFFFh
	SA111	32 Kwords	340000h-347FFFh
	SA112	32 Kwords	348000h-34FFFFh
	SA113	32 Kwords	350000h-357FFFh
	SA114	32 Kwords	358000h-35FFFFh
	SA115	32 Kwords	360000h-367FFFh
	SA116	32 Kwords	368000h-36FFFFh
	SA117	32 Kwords	370000h-377FFFh
	SA118	32 Kwords	378000h-37FFFFh

Table 13. WS064J Sector Address Table

Bank	Sector	Sector Size	(x16) Address Range
Bank A	SA119	32 Kwords	380000h-387FFFh
	SA120	32 Kwords	388000h-38FFFFh
	SA121	32 Kwords	390000h-397FFFh
	SA122	32 Kwords	398000h-39FFFFh
	SA123	32 Kwords	3A0000h-3A7FFFh
	SA124	32 Kwords	3A8000h-3AFFFFh
	SA125	32 Kwords	3B0000h-3B7FFFh
	SA126	32 Kwords	3B8000h-3BFFFFh
	SA127	32 Kwords	3C0000h-3C7FFFh
	SA128	32 Kwords	3C8000h-3CFFFFh
	SA129	32 Kwords	3D0000h-3D7FFFh
	SA130	32 Kwords	3D8000h-3DFFFFh
	SA131	32 Kwords	3E0000h-3E7FFFh
	SA132	32 Kwords	3E8000h-3EFFFFh
	SA133	32 Kwords	3F0000h-3F7FFFh
	SA134	4 Kwords	3F8000h-3F8FFFh
	SA135	4 Kwords	3F9000h-3F9FFFh
	SA136	4 Kwords	3FA000h-3FAFFFh
	SA137	4 Kwords	3FB000h-3FBFFFh
	SA138	4 Kwords	3FC000h-3FCFFFh
	SA139	4 Kwords	3FD000h-3FDFFFh
	SA140	4 Kwords	3FE000h-3FEFFFh
	SA141	4 Kwords	3FF000h-3FFFFFh

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 18, "Command Definitions," on page 76 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data in asynchronous mode. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. After completing a programming operation in the Erase Suspend mode, the system may once again read array data from any non-erase-suspended sector within the same bank. See the "Erase Suspend/Erase Resume Commands" section on page 71 for more information.

The system must issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the "Reset Command" section on page 66 for more information.

See also "Requirements for Asynchronous Read Operation (Non-Burst)" section on page 25 and "Requirements for Synchronous (Burst) Read Operation" section on page 26 for more information. The Asynchronous Read and Synchronous/Burst Read tables provide the read parameters, and Figure 14, "CLK Synchronous Burst Mode Read (rising active CLK)," on page 92, Figure 16, "Synchronous Burst Mode Read," on page 93, and Figure 19, "Asynchronous Mode Read with Latched Addresses," on page 96 show the timings.

Set Configuration Register Command Sequence

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, active clock edge, RDY configuration, and synchronous mode active. The configuration register must be set before the device will enter burst mode.

The configuration register is loaded with a three-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be C0h, address bits A11–A0 should be 555h, and address bits A19–A12 set the code to be latched. The device will power up or after a hardware reset with the default setting, which is in asynchronous mode. The register must be set before the device can enter synchronous mode. The configuration register can not be changed during device operations (program, erase, or sector lock).

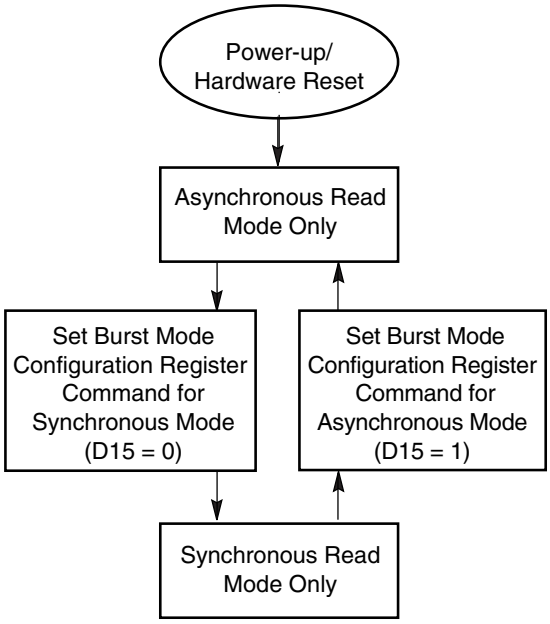


Figure 3. Synchronous/Asynchronous State Diagram

Read Mode Setting

On power-up or hardware reset, the device is set to be in asynchronous read mode. This setting allows the system to enable or disable burst mode during system operations. Address A19 determines this setting: "1' for asynchronous mode, "0" for synchronous mode.

Programmable Wait State Configuration

The programmable wait state feature informs the device of the number of clock cycles that must elapse after AVD# is driven active before data will be available. This value is determined by the input frequency of the device. Address bits A14–A12 determine the setting (see Table 14, "Programmable Wait State Settings," on page 64).

The wait state command sequence instructs the device to set a particular number of clock cycles for the initial access in burst mode. The number of wait states that should be programmed into the device is directly related to the clock frequency.

Table 14. Programmable Wait State Settings

A14	A13	A12	Total Initial Access Cycles
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	7 (default)
1	1	0	Reserved
1	1	1	Reserved

Notes:

1. *Upon power-up or hardware reset, the default setting is seven wait states.*
2. *RDY will default to being active with data when the Wait State Setting is set to a total initial access cycle of 2.*

It is recommended that the wait state command sequence be written, even if the default wait state value is desired, to ensure the device is set as expected. A hardware reset will set the wait state to the default setting.

Standard wait-state Handshaking Option

The host system must set the appropriate number of wait states in the flash device depending upon the clock frequency. The host system should set address bits A14–A12 to 010 for a clock frequency of 66/80 MHz.

Table 15 describes the typical number of clock cycles (wait states) for various conditions.

Table 15. Wait States for Standard wait-state Handshaking

Burst Mode	Conditions	Typical No. of Clock Cycles after AVD# Low
		66/80 MHz
8-Word or 16-Word or Continuous	V_{IO} = 1.8 V	4
32-Word	V_{IO} = 1.8 V	5

** In the 8-, 16- and 32-word burst read modes, the address pointer does not cross 64-word boundaries (addresses which are multiples of 3Fh).*

The host system must set the appropriate number of wait states in the flash device depending upon the clock frequency. The autoselect function allows the host system to determine whether the flash device is enabled for handshaking. See the "Autoselect Command Sequence" section on page 67 for more information.

Read Mode Configuration

The device supports four different read modes: continuous mode, and 8, 16, and 32 word linear wrap around modes. A continuous sequence begins at the starting address and advances the address pointer until the burst operation is complete. If the highest address in the device is reached during the continuous burst read mode, the address pointer wraps around to the lowest address.

For example, an eight-word linear read with wrap around begins on the starting address written to the device and then advances to the next 8 word boundary. The address pointer then returns to the 1st word after the previous eight word boundary, wrapping through the starting location. The sixteen- and thirty-two linear wrap around modes operate in a fashion similar to the eight-word mode.

Table 16 shows the address bits and settings for the four read modes.

Table 16. Read Mode Settings

Burst Modes	Address Bits	
	A16	A15
Continuous	0	0
8-word linear wrap around	0	1
16-word linear wrap around	1	0
32-word linear wrap around	1	1

Note: *Upon power-up or hardware reset the default setting is continuous.*

Burst Active Clock Edge Configuration

By default, the device will deliver data on the rising edge of the clock after the initial synchronous access time. Subsequent outputs will also be on the following rising edges, barring any delays. The device can be set so that the falling clock edge is active for all synchronous accesses. Address bit A17 determines this setting; "1" for rising active, "0" for falling active.

RDY Configuration

By default, the device is set so that the RDY pin will output V_{OH} whenever there is valid data on the outputs. The device can be set so that RDY goes active one data cycle before active data. Address bit A18 determines this setting; "1" for RDY active with data, "0" for RDY active one clock cycle before valid data. In asynchronous mode, RDY is an open-drain output.

Configuration Register

Table 17 shows the address bits that determine the configuration register settings for various device functions.

Table 17. Configuration Register

Address Bit	Function	Settings (Binary)
A19	Set Device Read Mode	0 = Synchronous Read (Burst Mode) Enabled 1 = Asynchronous Mode (default)
A18	RDY	0 = RDY active one clock cycle before data 1 = RDY active with data (default)
A17	Clock	0 = Burst starts and data is output on the falling edge of CLK 1 = Burst starts and data is output on the rising edge of CLK (default)
A16	Read Mode	Synchronous Mode
A15		00 = Continuous (default) 01 = 8-word linear with wrap around 10 = 16-word linear with wrap around 11 = 32-word linear with wrap around
A14	Programmable Wait State	000 = Data is valid on the 2nd active CLK edge after AVD# transition to V_{IH} 001 = Data is valid on the 3rd active CLK edge after AVD# transition to V_{IH} 010 = Data is valid on the 4th active CLK edge after AVD# transition to V_{IH} 011 = Data is valid on the 5th active CLK edge after AVD# transition to V_{IH} 100 = Data is valid on the 6th active CLK edge after AVD# transition to V_{IH} 101 = Data is valid on the 7th active CLK edge after AVD# transition to V_{IH} (default) 110 = Reserved 111 = Reserved
A13		
A12		

Note: *Device will be in the default state upon power-up or hardware reset.*

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins (prior to the third cycle). This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 18, "Command Definitions," on page 76 shows the address and data requirements. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. No subsequent data will be made available if the autoselect data is read in synchronous mode. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence. Read commands to other banks will return data from the array. The following table describes the address requirements for the various autoselect functions, and the resulting data. BA represents the bank address, and SA represents the sector address. The device ID is read in three cycles.

Description	Address	Read Data
Manufacturer ID	(BA) + 00h	0001h
Device ID, Word 1	(BA) + 01h	227Eh
Device ID, Word 2	(BA) + 0Eh	2218h (WS128J) 221Eh (WS064J)
Device ID, Word 3	(BA) + 0Fh	2200h (WS128J) 2201h (WS064J)
Sector Protection Verification	(SA) + 02h	0001 (locked), 0000 (unlocked)
Indicator Bits	(BA) + 03h	DQ15 - DQ8 = 0 DQ7 - Factory Lock Bit 1 = Locked, 0 = Not Locked DQ6 -Customer Lock Bit 1 = Locked, 0 = Not Locked DQ5 - Handshake Bit 1 = Reserved, 0 = Standard Handshake DQ4 & DQ3 - Boot Code 00 = Dual Boot Sector, 01 = Top Boot Sector, 10 = Bottom Boot Sector DQ2 - DQ0 = 001

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Enter/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the

Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. The Secured Silicon Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 18, "Command Definitions," on page 76 shows the address and data requirements for both command sequences.

The following commands are not allowed when the Secured Silicon is accessible.

— CFI
— Unlock Bypass Entry
— Unlock Bypass Program
— Unlock Bypass Reset
— Erase Suspend/Resume
— Chip Erase

Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 18, "Command Definitions," on page 76 shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by monitoring DQ7 or DQ6/DQ2. Refer to the "Write Operation Status" section on page 79 for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from "0" back to a "1." Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bit to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

Unlock Bypass Command Sequence

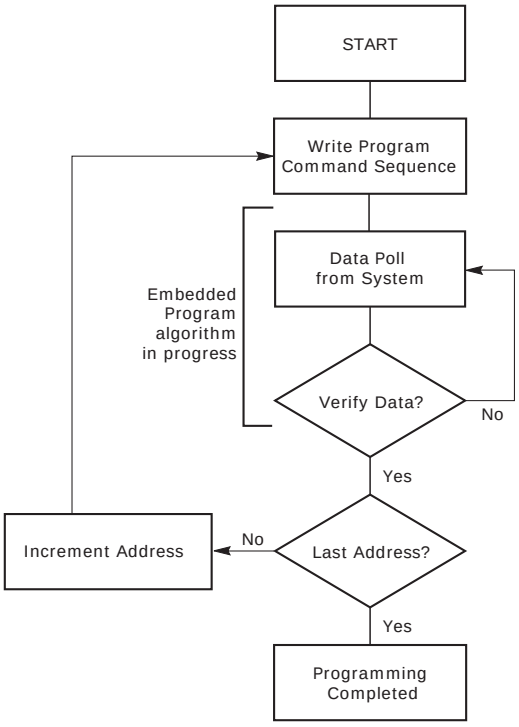
The unlock bypass feature allows the system to primarily program to a array faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. The host system may also initiate the chip erase and sector erase

sequences in the unlock bypass mode. The erase command sequences are four cycles in length instead of six cycles. Table 18, "Command Definitions," on page 76 shows the requirements for the unlock bypass command sequences.

During the unlock bypass mode, only the Read, Unlock Bypass Program, Unlock Bypass Sector Erase, Unlock Bypass Chip Erase, and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The array then returns to the read mode.

The device offers accelerated program operations through the ACC input. When the system asserts V_{HH} on this input, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the ACC input to accelerate the operation.

Figure 4, "Program Operation," on page 69 illustrates the algorithm for the program operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters, and Figure 22, "Asynchronous Program Operation Timings: AVD# Latched Addresses," on page 99 and Figure 24, "Synchronous Program Operation Timings: WE# Latched Addresses," on page 101 for timing diagrams.



Note: *See Table 18 for program command sequence.*

Figure 4. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two

additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 18, "Command Definitions," on page 76 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. Refer to the "Write Operation Status" section on page 79 for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

The host system may also initiate the chip erase command sequence while the device is in the unlock bypass mode. The command sequence is two cycles in length instead of six cycles. See Table 18, "Command Definitions," on page 76 for details on the unlock bypass command sequences.

Figure 5, "Erase Operation," on page 72 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters and timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 18, "Command Definitions," on page 76 shows the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of no less than 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode. The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See "DQ3: Sector Erase Timer" section on page 84.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7 or DQ6/DQ2 in the erasing bank. Refer to the "Write Operation Status" section on page 79 for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

The host system may also initiate the sector erase command sequence while the device is in the unlock bypass mode. The command sequence is four cycles cycles in length instead of six cycles.

Figure 5, "Erase Operation," on page 72 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations table in the Figure , "AC Characteristics," on page 98 for parameters and timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the minimum 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

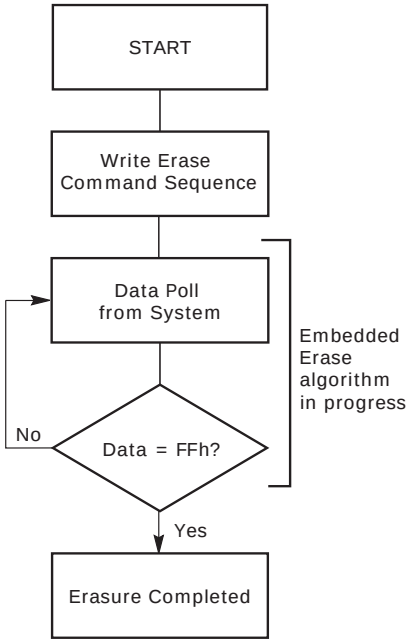
When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 35 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Figure , "Write Operation Status," on page 79 for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. Refer to the "Write Operation Status" section on page 79 for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the "Autoselect Mode" section on page 29 and "Autoselect Command Sequence" section on page 67 for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



Notes:

1. *See Table 18 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 5. Erase Operation

Password Program Command

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. 4 Password Program commands are required to program the password. The user must enter the unlock cycle, password program command (38h) and the program address/data for each portion of the password when programming. There are no provisions for entering the 2-cycle unlock cycle, the password program command, and all the password data. There is no special addressing order required for programming the password. Also, when the password is undergoing programming, Simultaneous Operation is disabled. Read operations to any memory location will return the programming status except DQ7. Once programming is complete, the user must issue a Secured Silicon Exit command to return the device to normal operation. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming "0"s. Programming a "1" after a cell is programmed as a "0" results in a time-out by the Embedded Program Algorithm™ with the cell remaining as a "0". The password is all F's when shipped from the factory. All 64-bit password combinations are valid as a password.

Password Verify Command

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Locking Bit is not programmed. If the Password Mode Locking Bit is programmed and the user attempts to verify the Password, the device will always drive all F's onto the DQ data bus.

Also, the device will not operate in Simultaneous Operation when the Password Verify command is executed. Only the password is returned regardless of the bank address. The lower two address bits (A1–A0) are valid during the Password Verify. Writing the Secured Silicon Exit command returns the device back to normal operation.

Password Protection Mode Locking Bit Program Command

The Password Protection Mode Locking Bit Program Command programs the Password Protection Mode Locking Bit, which prevents further verifies or updates to the password. Once programmed, the Password Protection Mode Locking Bit cannot be erased and the Persistent Protection Mode Locking Bit program circuitry is disabled, thereby forcing the device to remain in the Password Protection Mode. After issuing "PL/68h" at the fourth bus cycle, the device requires a time out period of approximately 150 µs for programming the Password Protection Mode Locking Bit. Then by writing "PL/48h" at the fifth bus cycle, the device outputs verify data at DQ0. If DQ0 = 1, then the Password Protection Mode Locking Bit is programmed. If not, the system must repeat this program sequence from the fourth cycle of "PL/68h". Exiting the Password Protection Mode Locking Bit Program command is accomplished by writing the Secured Silicon Sector command.

Persistent Sector Protection Mode Locking Bit Program Command

The Persistent Sector Protection Mode Locking Bit Program Command programs the Persistent Sector Protection Mode Locking Bit, which prevents the Password Mode Locking Bit from ever being programmed. By disabling the program circuitry of the Password Mode Locking Bit, the device is forced to remain in the Persistent Sector Protection mode of operation, once this bit is set. After issuing "SMPL/68h" at the fourth bus cycle, the device requires a time out period of approximately 150 µs for programming the Persistent Protect ion Mode Locking Bit. Then by writing "SMPL/48h" at the fifth bus cycle, the device outputs verify data at DQ0. If DQ0 = 1, then the Persistent Protection Mode Locking Bit is programmed. If not, the system must repeat this program sequence from the fourth cycle of "PL/68h". Exiting the Persistent Protection Mode Locking Bit Program command is accomplished by writing the Secured Silicon Sector Exit command.

Secured Silicon Sector Protection Bit Program Command

To protect the Secured Silicon Sector, write the Secured Silicon Sector Protect command sequence while in the Secured Silicon Sector mode. After issuing "OPBP/48h" at the fourth bus cycle, the device requires a time out period of approximately 150 µs to protect the Secured Silicon Sector. Then, by writing "OPBP/48" at the fifth bus cycle, the device outputs verify data at DQ0. If DQ0 = 1, then the Secured Silicon Sector is protected. If not, then the system must repeat this program sequence from the fourth cycle of "OPBP/48h".

PPB Lock Bit Set Command

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear or the Password Unlock command is executed. Upon setting the PPB Lock Bit, the PPBs are latched into the DPBs. If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle. Exiting the PPB Lock Bit Set command is accomplished by writing the Secured Silicon Exit command, only while in the Persistent Sector Protection Mode.

DPB Write/Erase/Status Command

The DPB Write command is used to set or clear a DPB for a given sector. The high order address bits (Amax–A11) are issued at the same time as the code 01h or 00h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DPBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. If the PPB is set, the sector is protected regardless of the value of the DPB. If the PPB is cleared, setting the DPB to a 1 protects the sector from programs or erases. Since this is a volatile bit, removing power or resetting the device will clear the DPBs. The programming of the DPB for a given sector can be verified by writing a DPB Status command to the device. Exiting the DPB Write/Erase command is accomplished by writing the Read/Reset command. Exiting the DPB Status command is accomplished by writing the Secured Silicon Sector Exit command

Password Unlock Command

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become accessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than 2 µs at a time to prevent a hacker from running through the all 64-bit combinations in an attempt to correctly match a password. If the command is issued before the 2 µs execution window for each portion of the unlock, the command will be ignored.

The Password Unlock function is accomplished by writing Password Unlock command and data to the device to perform the clearing of the PPB Lock Bit. The password is 64 bits long, so the user must write the Password Unlock command 4 times. A1 and A0 are used for matching. Writing the Password Unlock command is not address order specific. The lower address A1–A0= 00, the next Password Unlock command is to A1–A0= 01, then to A1–A0= 10, and finally to A1–A0= 11.

Once the Password Unlock command is entered for all four words, the RDY pin goes LOW indicating that the device is busy. Also, reading the Bank D results in the DQ6 pin toggling, indicating that the Password Unlock function is in progress. Reading the other bank returns actual array data. Approximately 1µs is required for each portion of the unlock. Once the first portion of the password unlock completes (RDY is not driven and DQ6 does not toggle when read), the Password Unlock command is issued again, only this time with the next part of the password. Four Password Unlock commands are required to successfully clear the PPB Lock Bit. As with the first Password Unlock command, the RDY signal goes LOW and reading the device results in the DQ6 pin toggling on successive read operations until complete. It is the responsibility of the micro-

processor to keep track of the number of Password Unlock commands, the order, and when to read the PPB Lock bit to confirm successful password unlock. In order to re lock the device into the Password Mode, the PPB Lock Bit Set command can be re-issued.

PPB Program Command

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector address (Amax–A12) are written at the same time as the program command 60h with A6 = 0. If the PPB Lock Bit is set and the corresponding PPB is set for the sector, the PPB Program command will not execute and the command will time-out without programming the PPB.

After programming a PPB, two additional cycles are needed to determine whether the PPB has been programmed with margin. After 4th cycle, the device requires approximately 150 µs time out period for programming the PPB. And then after 5th cycle, the device outputs verify data at DQ0.

The PPB Program command does not follow the Embedded Program algorithm. Writing the Secured Silicon Sector Exit command returns the device back to normal operation.

All PPB Erase Command

The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written (60h) and A6 = 1, all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs.

After erasing the PPBs, two additional cycles are needed to determine whether the PPB has been erased with margin. After 4th cycle, the device requires approximately 1.5 ms time out period for erasing the PPB. And then after 5th cycle, the device outputs verify data at DQ0.

It is the responsibility of the user to preprogram all PPBs prior to issuing the All PPB Erase command. If the user attempts to erase a cleared PPB, over-erasure may occur making it difficult to program the PPB at a later time. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed. Writing the Secured Silicon Sector Exit command returns the device back to normal operation.

PPB Status Command

The programming of the PPB for a given sector can be verified by writing a PPB status verify command to the device.

PPB Lock Bit Status Command

The programming of the PPB Lock Bit for a given sector can be verified by writing a PPB Lock Bit status verify command to the device.

Command Definitions

Table 18. Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Asynchronous Read (Note 7)		1	RA	RD												
Reset (Note 8)		1	XXX	F0												
Autoselect (Note 9)	Manufacturer ID	4	555	AA	2AA	55	(BA) 555	90	(BA) X00	0001						
	Device ID (Note 10)	6	555	AA	2AA	55	(BA) 555	90	(BA) X01	227E	(BA)X 0E	(Note 10)	(BA) X0F	(Not e 10)		
	Sector Lock Verify (Note 11)	4	555	AA	2AA	55	(SA) 555	90	(SA) X02	0000/ 0001						
	Indicator Bits	4	555	AA	2AA	55	(BA) 555	90	(BA) X03	(Note 12)						
Program		4	555	AA	2AA	55	555	A0	PA	Data						
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10		
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30		
Erase Suspend (Note 15)		1	BA	B0												
Erase Resume (Note 16)		1	BA	30												
Set Configuration Register (Note 17)		3	555	AA	2AA	55	(CR) 555	C0								
CFI Query (Note 18)		1	55	98												
Unlock Bypass Mode	Unlock Bypass Entry	3	555	AA	2AA	55	555	20								
	Unlock Bypass Program (Notes 13, 14)	2	XX	A0	PA	PD										
	Unlock Bypass Sector Erase (Notes 13, 14)	2	XX	80	SA	30										
	Unlock Bypass Erase (Notes 13, 14)	2	XX	80	XXX	10										
	Unlock Bypass Reset (Notes 13, 14)	2	XX	90	XXX	00										
Sector Protection Command Definitions																
Secured Silicon Sector	Secured Silicon Sector Entry	3	555	AA	2AA	55	555	88								
	Secured Silicon Sector Exit	4	555	AA	2AA	55	555	90	XX	00						
	Secured Silicon Protection Bit Program (Notes 19, 20, 22)	6	555	AA	2AA	55	555	60	OW	68	OW	48	OW	RD (0)		
Password Protection	Password Program (Notes 19, 24)	4	555	AA	2AA	55	555	38	XX0	PD0						
									XX1	PD1						
									XX2	PD2						
									XX3	PD3						
	Password Verify	4	555	AA	2AA	55	555	C8	XX0	PD0						
									XX1	PD1						
									XX2	PD2						
									XX3	PD3						
	Password Unlock (Note 24)	7	555	AA	2AA	55	555	28	XX0	PD0	XX1	PD1	XX2	PD2	XX3	PD3

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 1–6)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
PPB Commands	PPB Program (Notes 19, 20, 22)	6	555	AA	2AA	55	555	60	(SA) + WP	68	(SA) + WP	48	XX	RD (0)		
	All PPB Erase (Notes 19, 20, 23, 25)	6	555	AA	2AA	55	555	60	WP	60	(SA) WP	40	XX	RD (0)		
	PPB Status (Note 26)	4	555	AA	2AA	55	(SA) 555	90	(SA) X02	RD (0)						
PPB Lock Bit	PPB Lock Bit Set	3	555	AA	2AA	55	555	78								
	PPB Lock Bit Status (Note 20)	4	555	AA	2AA	55	(BA) 555	58	BA	RD (1)						
DPB	DPB Write	4	555	AA	2AA	55	555	48	SA	X1						
	DPB Erase	4	555	AA	2AA	55	555	48	SA	X0						
	DPB Status	4	555	AA	2AA	55	(BA) 555	58	SA	RD (0)						
Password Protection Mode Locking Bit Program (Notes 19, 20, 22)		6	555	AA	2AA	55	555	60	PL	68	PL	48	PL	RD (0)		
Persistent Protection Mode Locking Bit Program (Notes 19, 20, 22)		6	555	AA	2AA	55	555	60	SL	68	SL	48	SL	RD (0)		

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the rising edge of the AVD# pulse or active edge of CLK which ever comes first.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits Amax–A12 uniquely select any sector.

BA = Address of the bank (WS128J: A22, A21, A20, WS064J: A21, A20, A19) that is being switched to autoselect mode, is in bypass mode, or is being erased.

SLA = Address of the sector to be locked. Set sector address (SA) and either A6 = 1 for unlocked or A6 = 0 for locked.

CR = Configuration Register address bits A19–A12.

OW = Address (A7–A0) is (00011010).

PD3–PD0 = Password Data. PD3–PD0 present four 16 bit combinations that represent the 64-bit Password

PWA = Password Address. Address bits A1 and A0 are used to select each 16-bit portion of the 64-bit entity.

PWD = Password Data.

PL = Address (A7-A0) is (00001010)

RD(0) = DQ0 protection indicator bit. If protected, DQ0 = 1, if unprotected, DQ0 = 0.

RD(1) = DQ1 protection indicator bit. If protected, DQ1 = 1, if unprotected, DQ1 = 0.

SL = Address (A7-A0) is (00010010)

WD= Write Data. See "Configuration Register" definition for specific write data

WP = Address (A7-A0) is (00000010)

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the following, all bus cycles are write cycle: read cycle, fourth through sixth cycles of the Autoselect commands, fourth cycle of the configuration register verify and password verify commands, and any cycle reading at RD(0) and RD(1).*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD, WD, PWD, and PD3-PD0.*

5. *Unless otherwise noted, address bits Amax–A12 are don't cares.*
6. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
7. *No unlock or command cycles required when bank is reading array data.*
8. *The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information) or performing sector lock/unlock.*
9. *The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address. See the Autoselect Command Sequence section for more information.*
10. *(BA)X0Fh = 2200h (WS128J), (BA)X0Eh = 2218h (WS128J), (BA)X0Fh = 221Eh (WS064J), (BA)X0Eh = 2201h (WS064J)*
11. *The data is 0000h for an unlocked sector and 0001h for a locked sector*
12. *DQ15 - DQ8 = 0, DQ7 - Factory Lock Bit (1 = Locked, 0 = Not Locked), DQ6 -Customer Lock Bit (1 = Locked, 0 = Not Locked), DQ5 = Handshake Bit (1 = Reserved, 0 = Standard Handshake)8, DQ4 & DQ3 - Boot Code (00= Dual Boot Sector, 01= Top Boot Sector, 10= Bottom Boot Sector, 11=No Boot Sector), DQ2 - DQ0 = 001*
13. *The Unlock Bypass command sequence is required prior to this command sequence.*
14. *The Unlock Bypass Reset command is required to return to reading array data.*
15. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
16. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
17. *See "Set Configuration Register Command Sequence" for details.*
18. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
19. *The Reset command returns the device to reading the array.*
20. *Regardless of CLK and AVD# interaction or Control Register bit 15 setting, command mode verifies are always asynchronous read operations.*
21. *ACC must be at V_{HH} during the entire operation of this command*
22. *The fourth cycle programs the addressed locking bit. The fifth and sixth cycles are used to validate whether the bit has been fully programmed. If DQ0 (in the sixth cycle) reads 0, the program command must be issued and verified again.*
23. *The fourth cycle erases all PPBs. The fifth and sixth cycles are used to validate whether the bits have been fully erased. If DQ0 (in the sixth cycle) reads 1, the erase command must be issued and verified again.*
24. *The entire four bus-cycle sequence must be entered for each portion of the password.*
25. *Before issuing the erase command, all PPBs should be programmed in order to prevent over-erasure of PPBs.*
26. *In the fourth cycle, 01h indicates PPB set; 00h indicates PPB not set.*

Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 20, "Write Operation Status," on page 85 and the following subsections describe the function of these bits. DQ7 and DQ6 each offers a method for determining whether a program or erase operation is complete or in progress.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

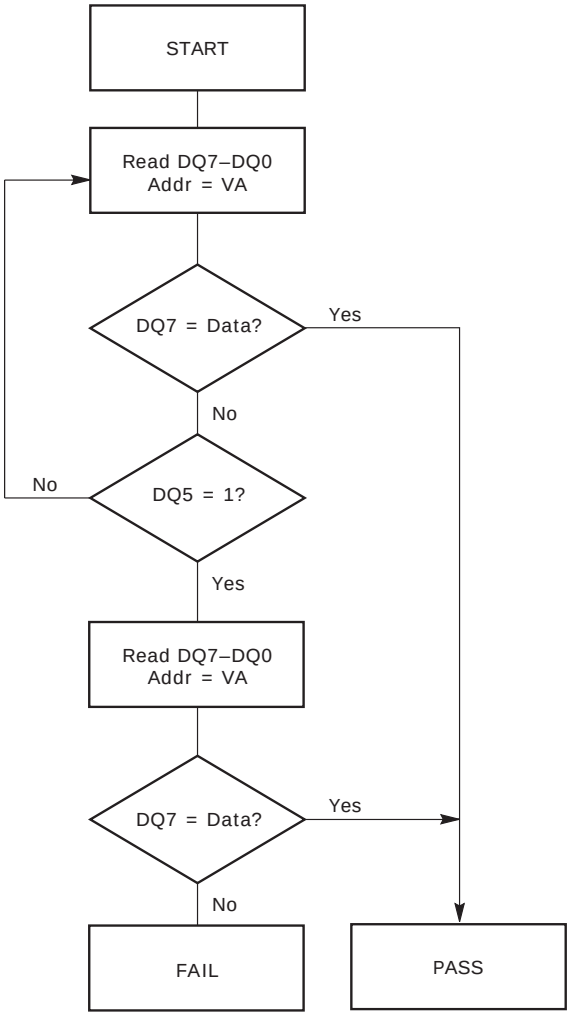
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6-DQ0 may be still invalid. Valid data on DQ7-D00 will appear on successive read cycles.

Table 20, "Write Operation Status," on page 85 shows the outputs for Data# Polling on DQ7. Figure 6, "Data# Polling Algorithm," on page 80 shows the Data# Polling algorithm. Figure 28, "Data# Polling Timings (During Embedded Algorithm)," on page 105 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 6. Data# Polling Algorithm

RDY: Ready

The RDY is a dedicated output that, when the device is configured in the Synchronous mode, indicates (when at logic low) the system should wait 1 clock cycle before expecting the next word of data. The RDY pin is only controlled by CE#. Using the RDY Configuration Command Sequence, RDY can be set so that a logic low indicates the system should wait 2 clock cycles before expecting valid data.

The following conditions cause the RDY output to be low: during the initial access (in burst mode), and after the boundary that occurs every 64 words beginning with the 64th address, 3Fh.

When the device is configured in Asynchronous Mode, the RDY is an open-drain output pin which indicates whether an Embedded Algorithm is in progress or completed. The RDY status is valid after the rising edge of the final WE# pulse in the command sequence.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is in high impedance (Ready), the device is in the read mode, the standby mode, or in the erase-suspend-read mode. Table 20, "Write Operation Status," on page 85 shows the outputs for RDY.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address in the same bank, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

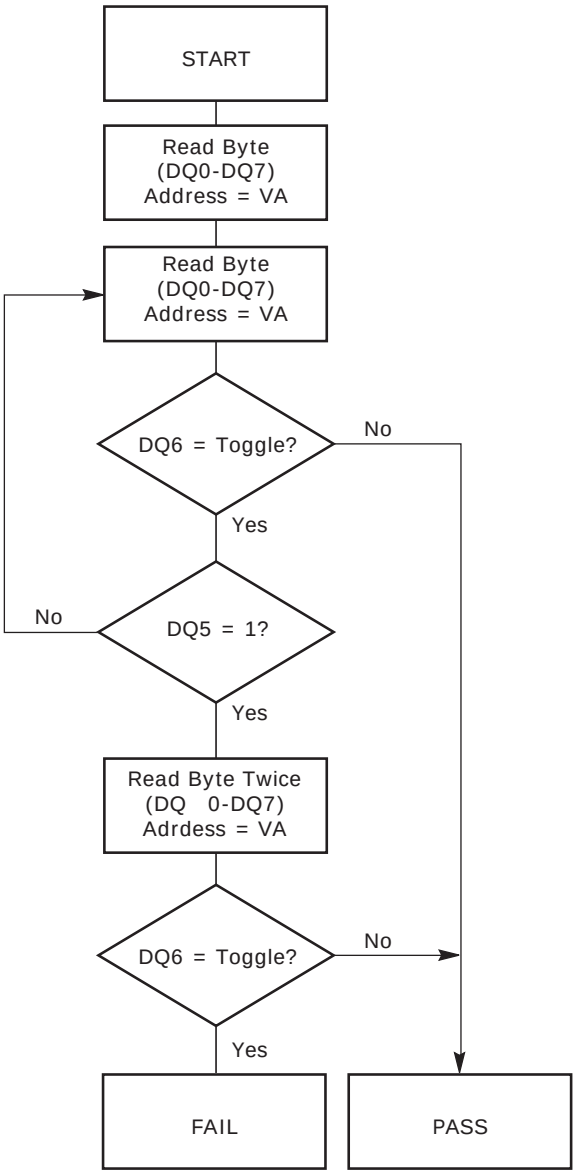
The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 ms after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

See the following for additional information: Figure 7, "Toggle Bit Algorithm," on page 82, "DQ6: Toggle Bit I" on page 81, Figure 29, "Toggle Bit Timings (During Embedded Algorithm)," on page 105 (toggle bit timing diagram), and Table 19, "DQ6 and DQ2 Indications," on page 83.

Toggle Bit I on DQ6 requires either OE# or CE# to be deasserteed and reasserted to show the change in state.



Note: *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.*

Figure 7. Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 19, "DQ6 and DQ2 Indications," on page 83 to compare outputs for DQ2 and DQ6.

See the following for additional information: Figure 7, "Toggle Bit Algorithm," on page 82, "DQ6: Toggle Bit I" on page 81, Figure 29, "Toggle Bit Timings (During Embedded Algorithm)," on page 105, and Table 19, "DQ6 and DQ2 Indications," on page 83.

Table 19. DQ6 and DQ2 Indications

If device is	and the system reads	then DQ6	and DQ2
programming,	at any address,	toggles,	does not toggle.
actively erasing,	at an address within a sector selected for erasure,	toggles,	also toggles.
	at an address within sectors *not* selected for erasure,	toggles,	does not toggle.
erase suspended,	at an address within a sector selected for erasure,	does not toggle,	toggles.
	at an address within sectors *not* selected for erasure,	returns array data,	returns array data. The system can read from any sector not selected for erasure.
programming in erase suspend	at any address,	toggles,	is not applicable.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 7, "Toggle Bit Algorithm," on page 82 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other

system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (Figure 7, "Toggle Bit Algorithm," on page 82).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." Only an erase operation can change a "0" back to a "1." Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also "Sector Erase Command Sequence" on page 70.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 20 shows the status of DQ3 relative to the other status bits.

Table 20. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RDY (Note 5)
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle (Note 6)	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read (Note 4)	Erase Suspended Sector	1	No toggle (Note 6)	0	N/A	Toggle	High Impedance
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	High Impedance
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.*
4. *The system may read either asynchronously or synchronously (burst) while in erase suspend.*
5. *The RDY pin acts a dedicated output to indicate the status of an embedded erase or program operation is in progress. This is available in the Asynchronous mode only.*
6. *When the device is set to Asynchronous mode, these status flags should be read by CE# toggle.*

Absolute Maximum Ratings

Storage Temperature, Plastic Packages ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –65°C to +125°C

Voltage with Respect to Ground:

All Inputs and I/Os except as noted below (Note 1) ..... –0.5 V to V_{IO} + 0.5 V

V_{CC} (Note 1) ..... –0.5 V to +2.5 V

V_{IO} ..... –0.5 V to +2.5 V

A9, RESET#, ACC (Note 1) ..... –0.5 V to +12.5 V

Output Short Circuit Current (Note 3) ..... 100 mA

Notes:

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, inputs or I/Os may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 8. Maximum DC voltage on input or I/Os is V_{CC} + 0.5 V. During voltage transitions outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 9.*
2. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
3. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

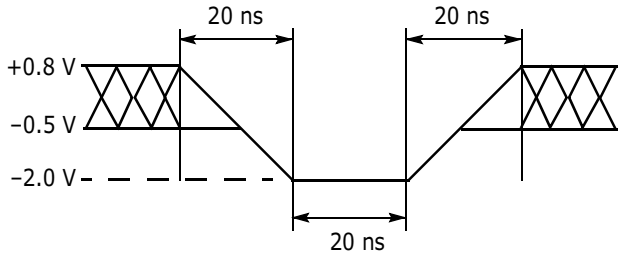


Figure 8. Maximum Negative Overshoot Waveform

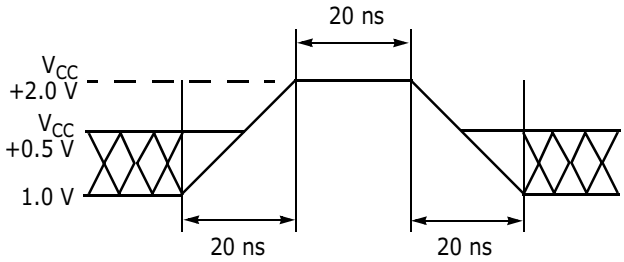


Figure 9. Maximum Positive Overshoot Waveform

Operating Ranges

Commercial (C) Devices

Ambient Temperature (T_A) 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) ..... –40°C to +85°C

Supply Voltages

V_{CC} Supply Voltages ..... +1.65 V to +1.95 V

V_{IO} Supply Voltages: ..... +1.65 V to +1.95 V

V_{CC} >= V_{IO} - 100mV

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics

CMOS Compatible

Parameter	Description	Test Conditions Notes: 1 & 2		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$max				±1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$max				±1	µA
I_{CCB}	V_{CC} Active burst Read Current	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 8	66 MHz		15	30	mA
			80 MHz		18	36	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 16	66 MHz		15	30	mA
			80 MHz		18	36	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = Continuous	66 MHz		15	30	mA
			80 MHz		18	36	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 8			50	200	µA
I_{IO1}	V_{IO} Non-active Output	OE# = V_{IH}			0.2	10	µA
I_{CC1}	V_{CC} Active Asynchronous Read Current (Note 3)	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}	10 MHz		20	30	mA
			5 MHz		12	16	mA
			1 MHz		3.5	5	mA
I_{CC2}	V_{CC} Active Write Current (Note 4)	CE# = V_{IL}, OE# = V_{IH}, ACC = V_{IH}			15	40	mA
I_{CC3}	V_{CC} Standby Current (Note 5)	CE# = RESET# = V_{CC} ± 0.2 V			0.2	50	µA
I_{CC4}	V_{CC} Reset Current	RESET# = V_{IL}, CLK = V_{IL}			0.2	50	µA
I_{CC5}	V_{CC} Active Current (Read While Write)	CE# = V_{IL}, OE# = V_{IH}	66 MHz		22	54	mA
			80 MHz		25	60	mA
I_{CC6}	V_{CC} Sleep Current	CE# = V_{IL}, OE# = V_{IH}			0.2	50	µA
I_{ACC}	Accelerated Program Current (Note 6)	CE# = V_{IL}, OE# = V_{IH}, V_{ACC} = 12.0 ± 0.5 V	V_{ACC}		7	15	mA
			V_{CC}		5	10	mA
V_{IL}	Input Low Voltage	V_{IO} = 1.8 V		–0.5		0.4	V
V_{IH}	Input High Voltage	V_{IO} = 1.8 V		V_{IO} – 0.4		V_{IO} + 0.4	
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, $V_{CC} = V_{CC\ min} = V_{IO}$				0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC\ min} = V_{IO}$		V_{IO} – 0.1			V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 1.8 V		11.5		12.5	V
V_{HH}	Voltage for Accelerated Program			11.5		12.5	V
V_{LKO}	Low V_{CC} Lock-out Voltage			1.0		1.4	V

Notes:

1. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
2. *$V_{CC} = V_{IO}$*
3. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
4. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
5. *Device enters automatic sleep mode when addresses are stable for t_{ACC} + 60 ns. Typical sleep mode current is equal to I_{CC3}.*
6. *Total current during accelerated programming is the sum of V_{ACC} and V_{CC} currents.*

Test Conditions

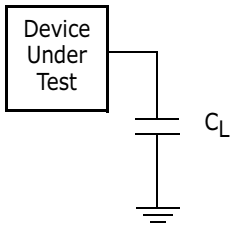
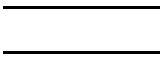
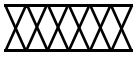
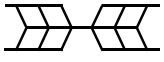


Figure 10. Test Setup

Table 21. Test Specifications

Test Condition	All Speed Options	Unit
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	2.5 - 3	ns
Input Pulse Levels	0.0–V_{IO}	V
Input timing measurement reference levels	$V_{IO}/2$	V
Output timing measurement reference levels	$V_{IO}/2$	V

Key to Switching Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

Switching Waveforms

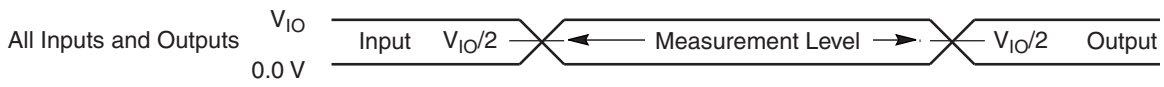


Figure 11. Input Waveforms and Measurement Levels

AC Characteristics

V_{CC} Power-up

Parameter	Description	Test Setup	Speed	Unit
t_{VCS}	V_{CC} Setup Time	Min	50	µs
t_{VIOS}	V_{IO} Setup Time	Min	50	µs
t_{RSTH}	RESET# Low Hold Time	Min	50	µs

Notes:

1. *V_{CC} >= V_{IO} - 100mV and V_{CC} ramp rate is > 1V / 100µs*
2. *V_{CC} ramp rate <1V / 100µs, a Hardware Reset will be required.*

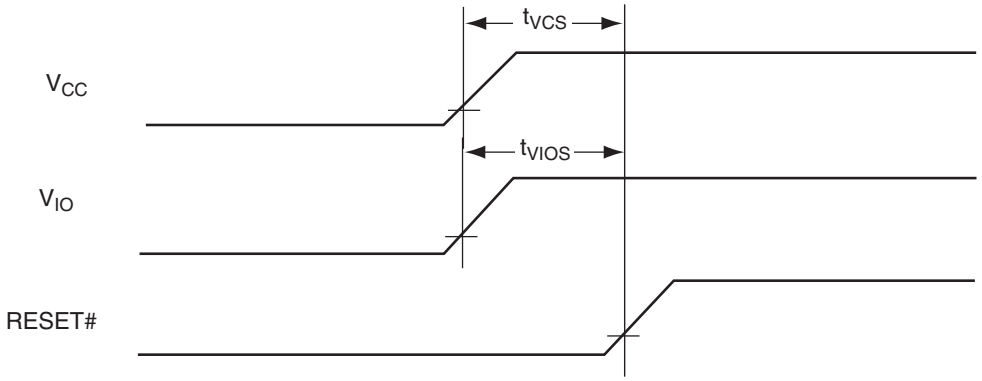


Figure 12. V_{CC} Power-up Diagram

CLK Characterization

Parameter	Description		66 MHz	80 MHz	Unit
f_{CLK}	CLK Frequency	Max	66	80	MHz
t_{CLK}	CLK Period	Min	15	12.5	ns
t_{CKH}	CLK High Time	Min	7.0	5	ns
t_{CKL}	CLK Low Time				
t_{CR}	CLK Rise Time	Max	3	2.5	ns
t_{CF}	CLK Fall Time				

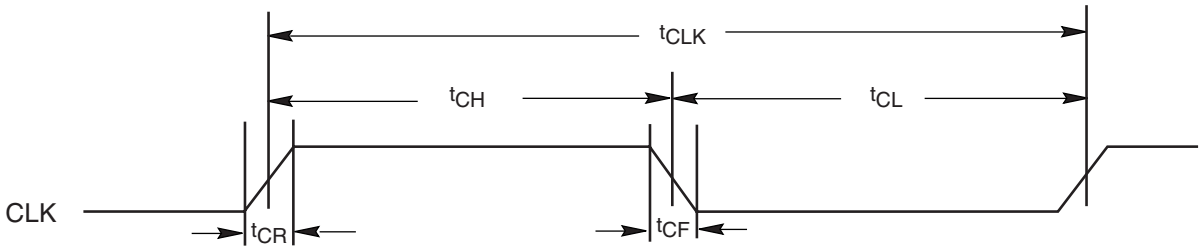


Figure 13. CLK Characterization

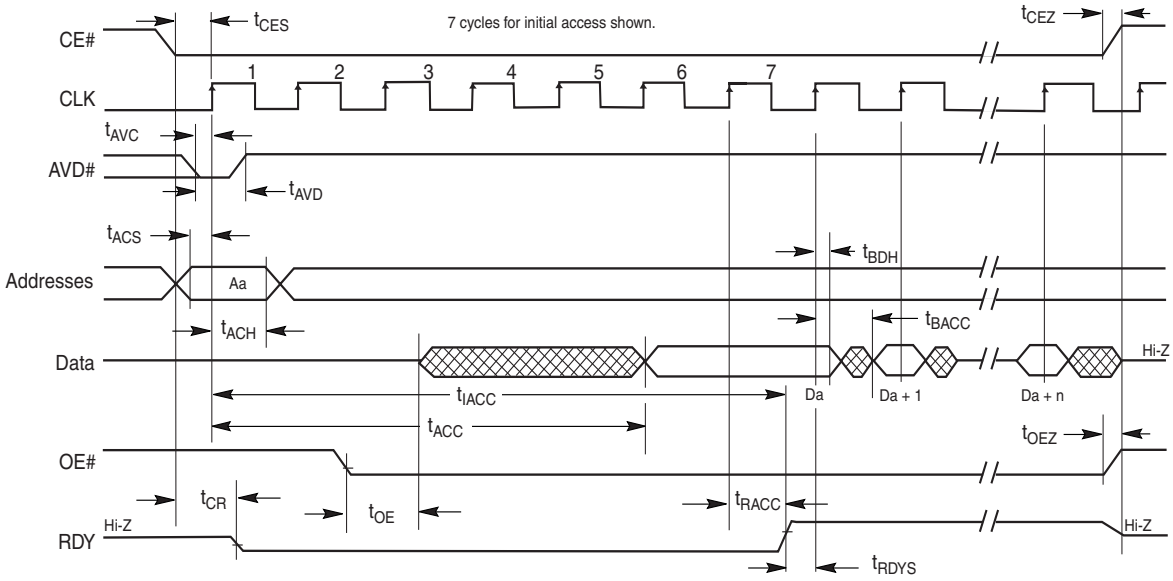
AC Characteristics

Synchronous/Burst Read @ V_{IO} = 1.8 V

Parameter						
JEDEC	Standard	Description		66 MHz	80 MHz	Unit
	t_{IACC}	Latency (Standard wait-state Handshake mode) for 8-Word and 16-Word Burst	Max	56	46	ns
	t_{IACC}	Latency (Standard wait-state Handshake mode) for 32-Word and Continuous Burst	Max	71	58.5	ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	11.2	9.1	ns
	t_{ACS}	Address Setup Time to CLK (See Note)	Min	4		ns
	t_{ACH}	Address Hold Time from CLK (See Note)	Min	5.5		ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Min	2		ns
	t_{CR}	Chip Enable to RDY Valid	Max	11.2	9.1	ns
	t_{OE}	Output Enable to Output Valid	Max	11.2	9.1	ns
	t_{CEZ}	Chip Enable to High Z	Max	8		ns
	t_{OEZ}	Output Enable to High Z	Max	8		ns
	t_{CES}	CE# Setup Time to CLK	Min	4		ns
	t_{RDYS}	RDY Setup Time to CLK	Min	4		ns
	t_{RACC}	Ready Access Time from CLK	Max	11.2	9.1	ns
	t_{AAS}	Address Setup Time to AVD# (See Note)	Min	4		ns
	t_{AAH}	Address Hold Time to AVD# (See Note)	Min	5.5		ns
	t_{CAS}	CE# Setup Time to AVD#	Min	0		ns
	t_{AVC}	AVD# Low to CLK	Min	4		ns
	t_{AVD}	AVD# Pulse	Min	10		ns
	t_{ACC}	Access Time	Max	55	45	ns
	t_{CKA}	CLK to access resume	Max	11.2	9.1	ns
	t_{CKZ}	CLK to High Z	Max	8		ns
	t_{OES}	Output Enable Setup Time	Min	4		ns

Note: *Addresses are latched on the first of either the active edge of CLK or the rising edge of AVD#.*

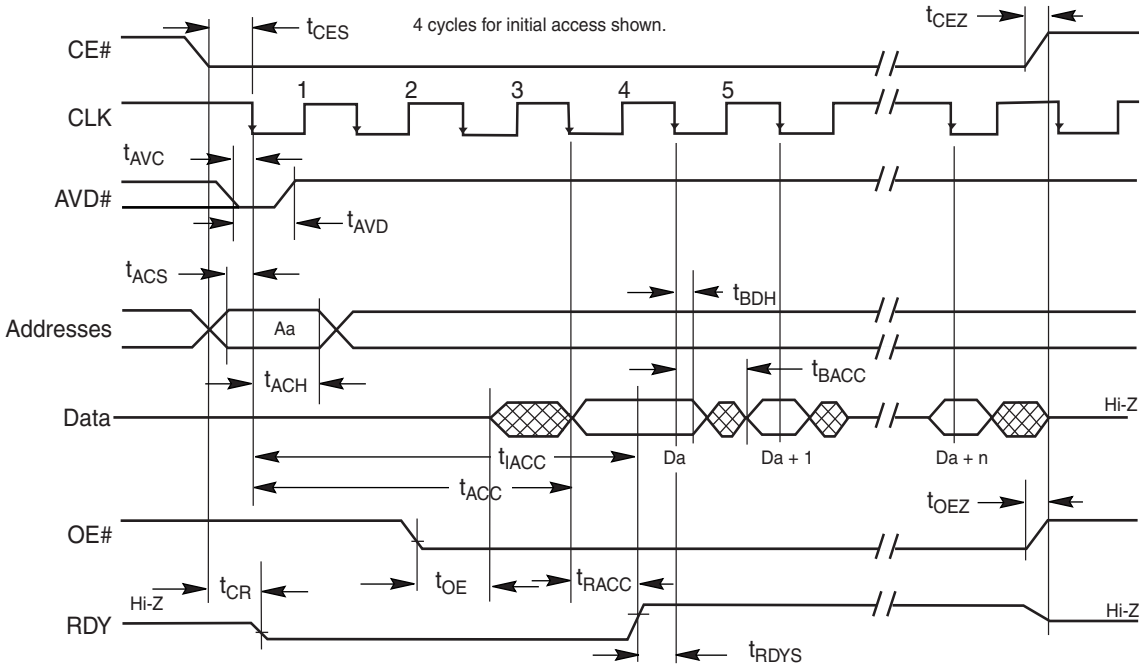
AC CHaracteristics



Notes:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles.*
2. *If any burst address occurs at a 64-word boundary, two additional clock cycle are inserted, and is indicated by RDY.*
3. *The device is in synchronous mode.*

Figure I4. CLK Synchronous Burst Mode Read (rising active CLK)

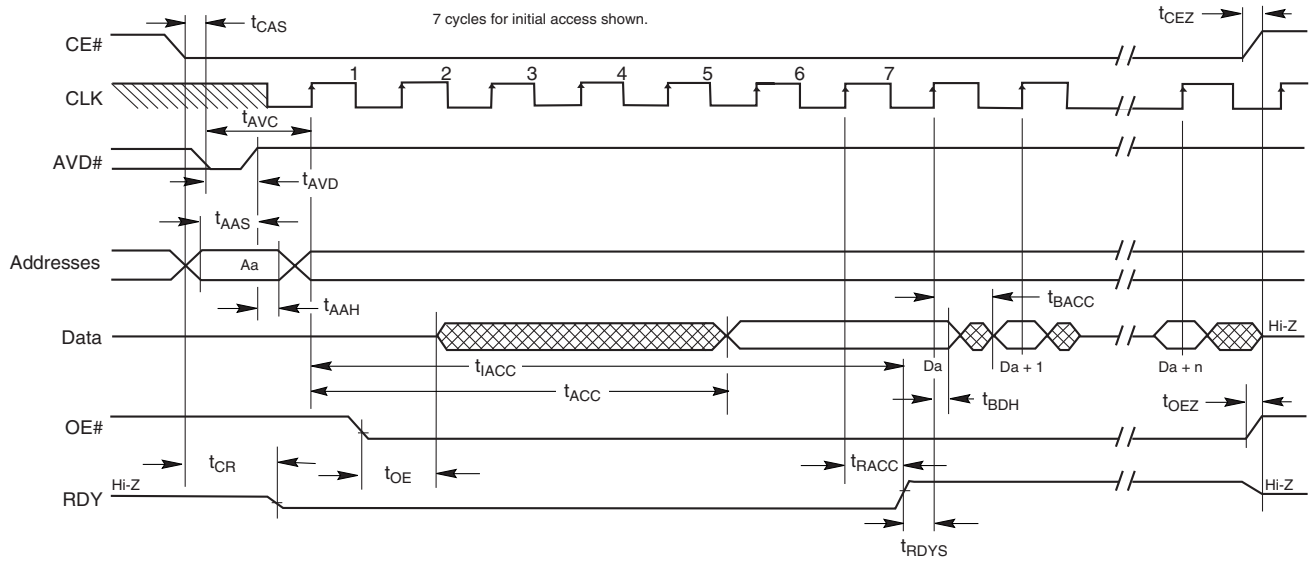


Notes:

1. *Figure shows total number of wait states set to four cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active falling edge.*
2. *If any burst address occurs at a 64-word boundary, two additional clock cycle are inserted, and is indicated by RDY.*
3. *The device is in synchronous mode.*

Figure I5. CLK Synchronous Burst Mode Read (Falling Active Clock)

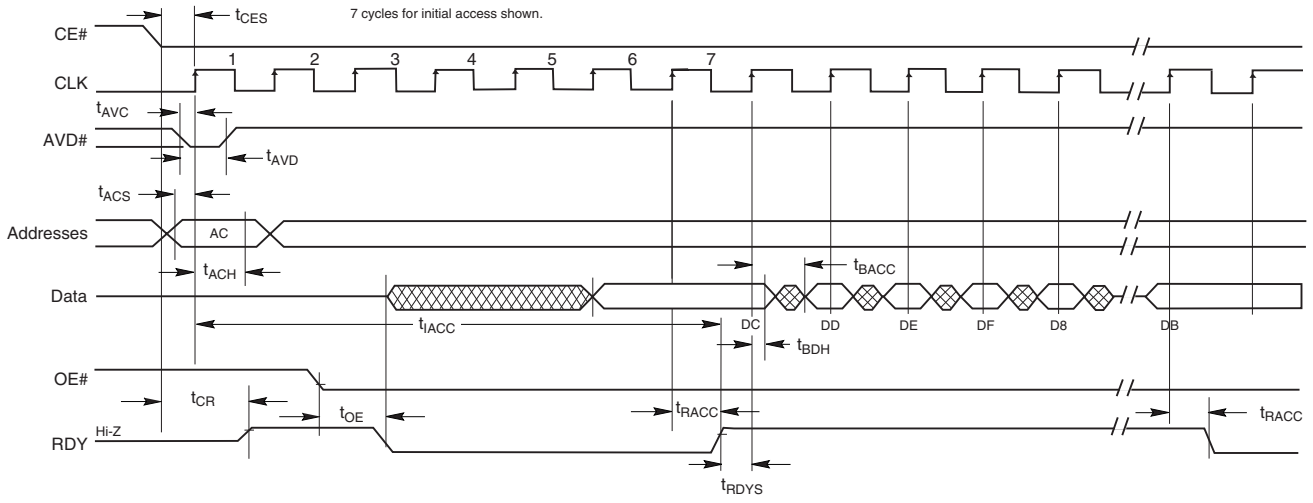
AC Characteristics



Notes:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active rising edge.*
2. *If any burst address occurs at a 64-word boundary, two additional clock cycle are inserted, and is indicated by RDY.*
3. *The device is in synchronous mode.*

Figure 16. Synchronous Burst Mode Read

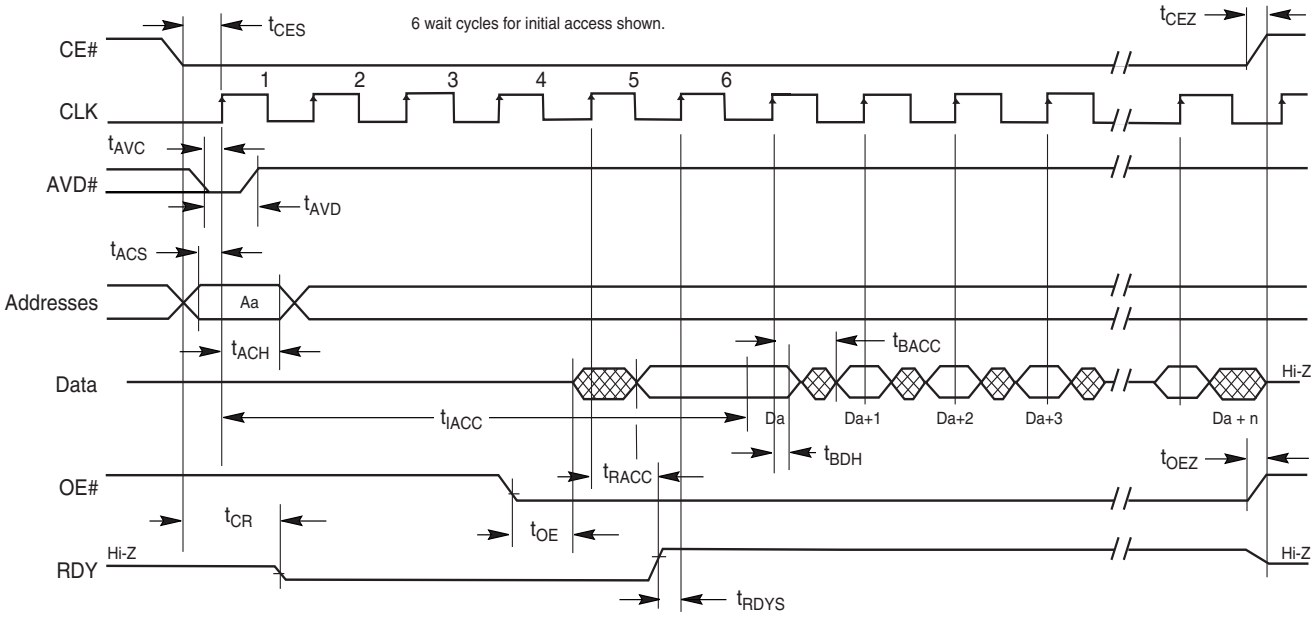


Notes:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active rising edge.*
2. *If any burst address occurs at a 64-word boundary, two additional clock cycle are inserted, and is indicated by RDY.*
3. *The device is in synchronous mode with wrap around.*
4. *D0-D7 in data waveform indicates the order the data within a given 8-word address range, from lowest to highest. Starting address in figure is the 4th address in range (AC)*

Figure 17. 8-word Linear Burst with Wrap Around

AC Characteristics



Notes:

1. *Figure assumes 6 wait states for initial access and synchronous read.*
2. *The Set Configuration Register command sequence has been written with A18=0; device will output RDY one cycle before valid data.*

Figure 18. Linear Burst with RDY Set One Cycle Before Data

AC Characteristics

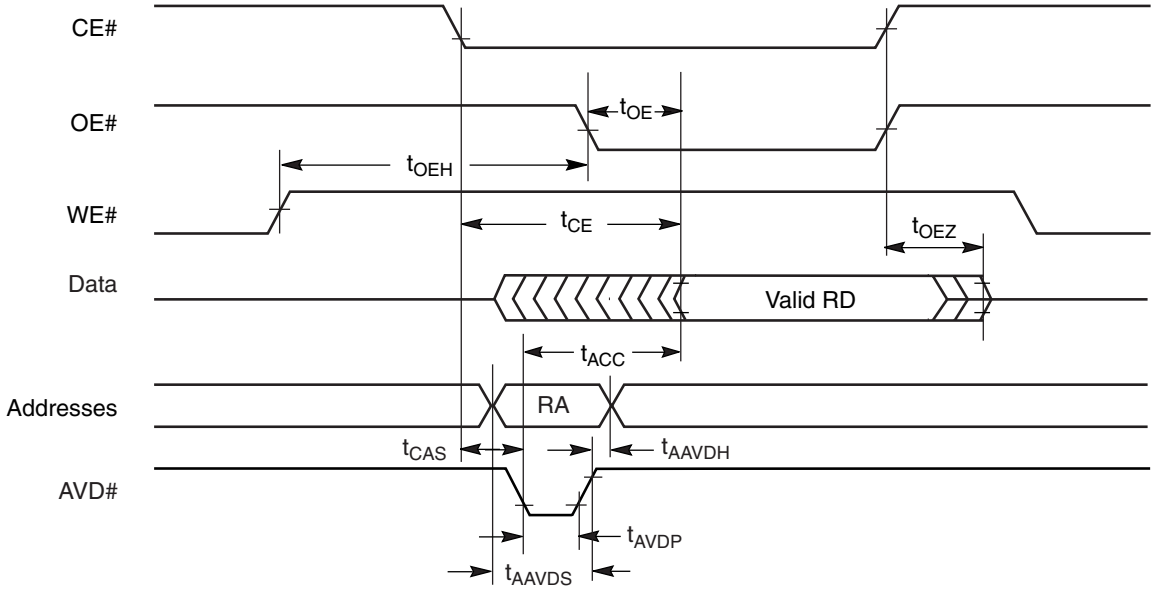
Asynchronous Mode Read @ V_{IO} = 1.8 V

Parameter		Description			66 MHz	80 MHz	Unit
JEDEC	Standard						
	t_{CE}	Access Time from CE# Low		Max	55	45	ns
	t_{ACC}	Asynchronous Access Time (Note 1)		Max	55	45	ns
	t_{AVDP}	AVD# Low Time		Min	10		ns
	t_{AAVDS}	Address Setup Time to Rising Edge of AVD		Min	4		ns
	t_{AAVDH}	Address Hold Time from Rising Edge of AVD		Min	5.5		ns
	t_{OE}	Output Enable to Output Valid		Max	11.2	9.1	ns
	t_{OEH}	Output Enable Hold Time	Read	Min	0		ns
			Toggle and Data# Polling	Min	8		ns
	t_{OEZ}	Output Enable to High Z (Note 2)		Max	8		ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0		ns

Notes:

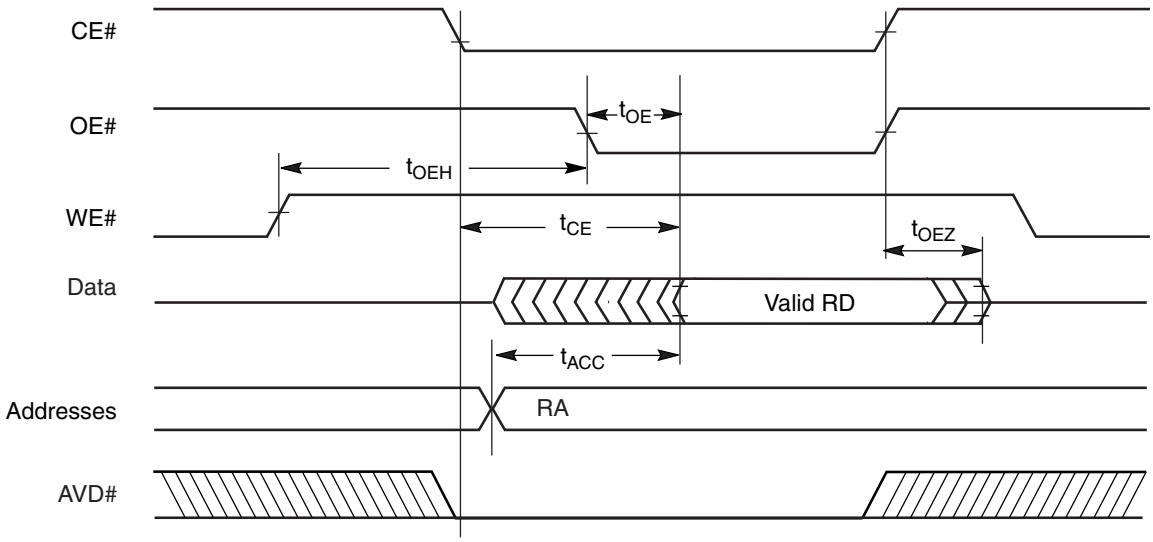
1. *Asynchronous Access Time is from the last of either stable addresses or the falling edge of AVD#.*
2. *Not 100% tested.*

AC Characteristics



Note: *RA = Read Address, RD = Read Data.*

Figure 19. Asynchronous Mode Read with Latched Addresses



Note: *RA = Read Address, RD = Read Data.*

Figure 20. Asynchronous Mode Read

AC Characteristics

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	35	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	200	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs

Note: *Not 100% tested.*

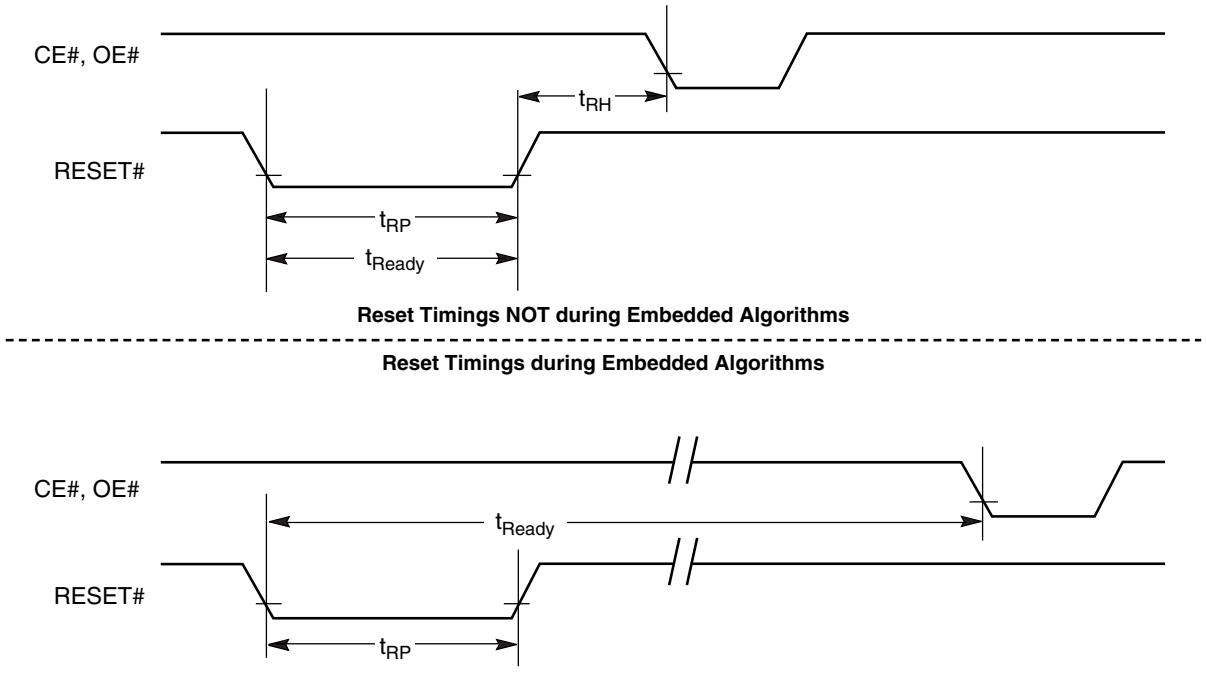


Figure 2I. Reset Timings

AC Characteristics

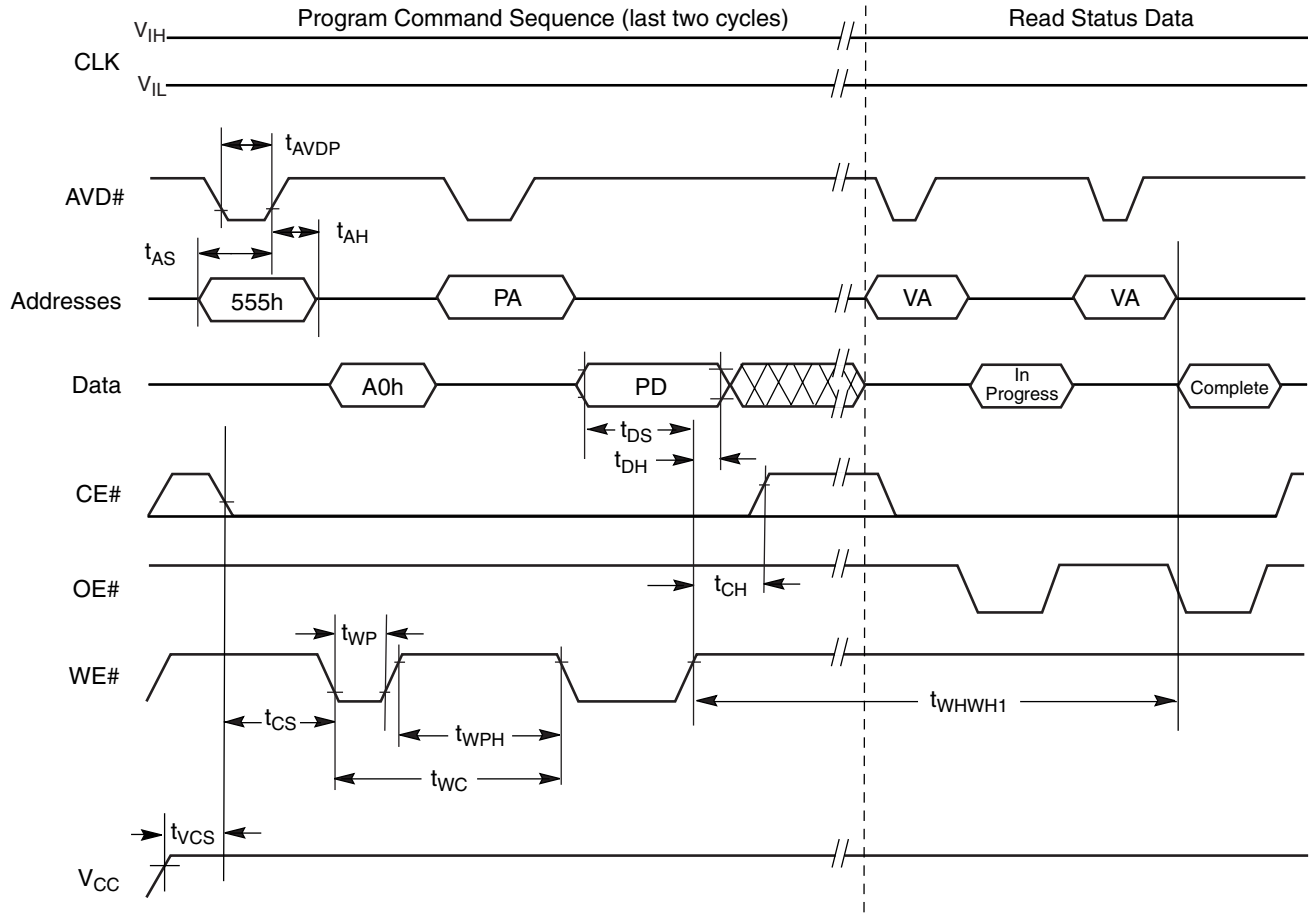
Erase/Program Operations @ V_{IO} = 1.8 V

Parameter		Description			66 MHz	80 MHz	Unit
JEDEC	Standard						
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	45		ns
t_{AVWL}	t_{AS}	Address Setup Time (Notes 2, 3)	Synchronous	Min	4		ns
			Asynchronous		0		
t_{WLAX}	t_{AH}	Address Hold Time (Notes 2, 3)	Synchronous	Min	5.5		ns
			Asynchronous		15		
	t_{AVDP}	AVD# Low Time		Min	10		ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	20		ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write		Min	0		ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	20		ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	20		ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 4)		Typ	<7		µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation (Note 4)		Typ	<4		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Notes 4, 5)		Typ	<0.2		sec
		Chip Erase Operation (Notes 4, 5)			<104		
	t_{VID}	V_{ACC} Rise and Fall Time		Min	500		ns
	t_{VIDS}	V_{ACC} Setup Time (During Accelerated Programming)		Min	1		µs
	t_{VCS}	V_{CC} Setup Time		Min	50		µs
t_{ELWL}	t_{CS}	CE# Setup Time to WE#		Min	0		ns
	t_{AVSW}	AVD# Setup Time to WE#		Min	4		ns
	t_{AVHW}	AVD# Hold Time to WE#		Min	4		ns
	t_{AVHC}	AVD# Hold Time to CLK		Min	4		ns
	t_{CSW}	Clock Setup Time to WE#		Min	5		ns

Notes:

1. *Not 100% tested.*
2. *Asynchronous mode allows both Asynchronous and Synchronous program operation. Synchronous mode allows both Asynchronous and Synchronous program operation.*
3. *In asynchronous program operation timing, addresses are latched on the falling edge of WE# or rising edge of AVD#. In synchronous program operation timing, addresses are latched on the first of either the rising edge of AVD# or the active edge of CLK.*
4. *See the "Erase and Programming Performance" section for more information.*
5. *Does not include the preprogramming time.*

AC Characteristics

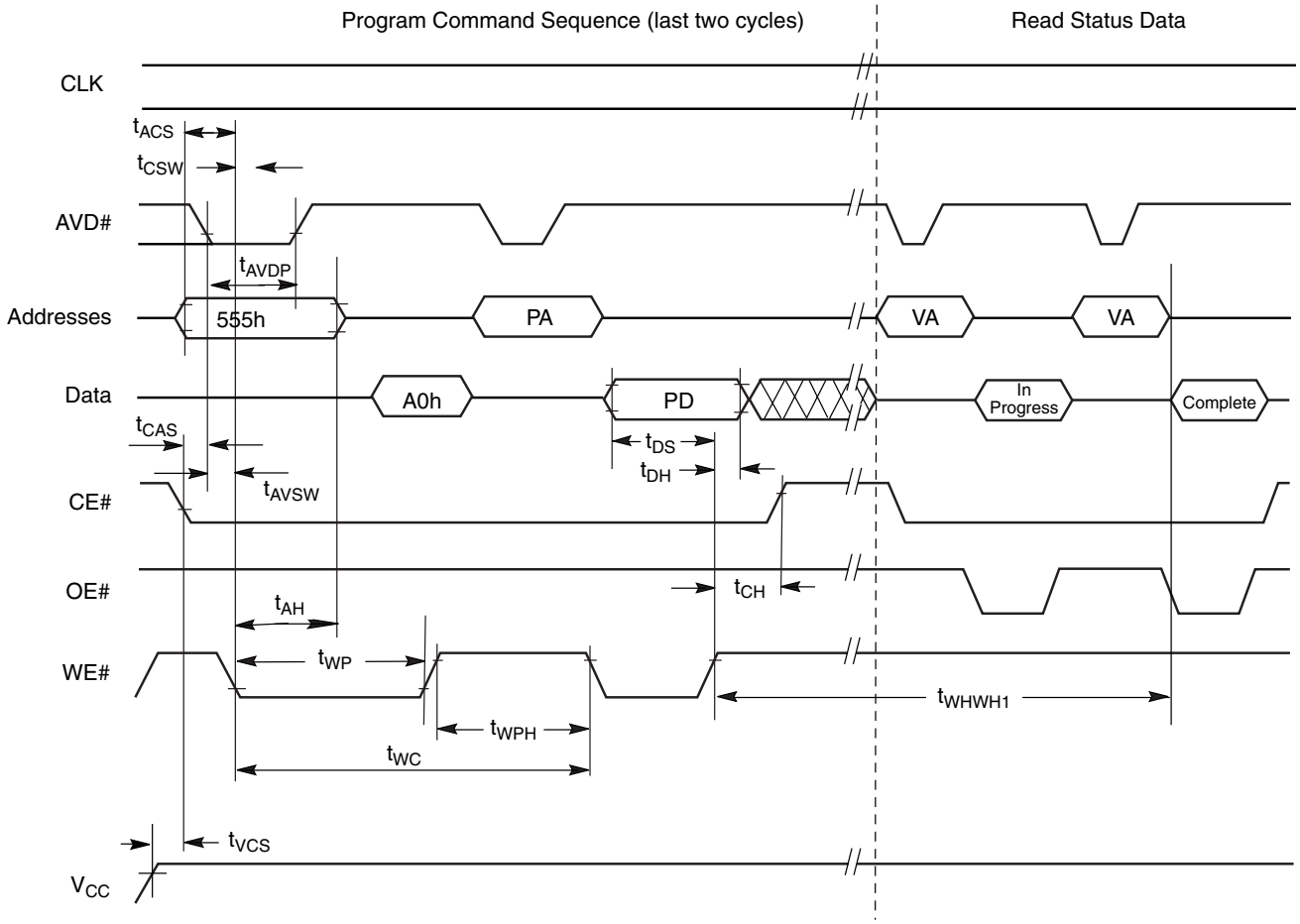


Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A22–A12 are don't care during command sequence unlock cycles.*
4. *CLK can be either V_{IL} or V_{IH}.*
5. *The Asynchronous programming operation is independent of the Set Device Read Mode bit in the Configuration Register.*

Figure 22. Asynchronous Program Operation Timings: AVD# Latched Addresses

AC Characteristics

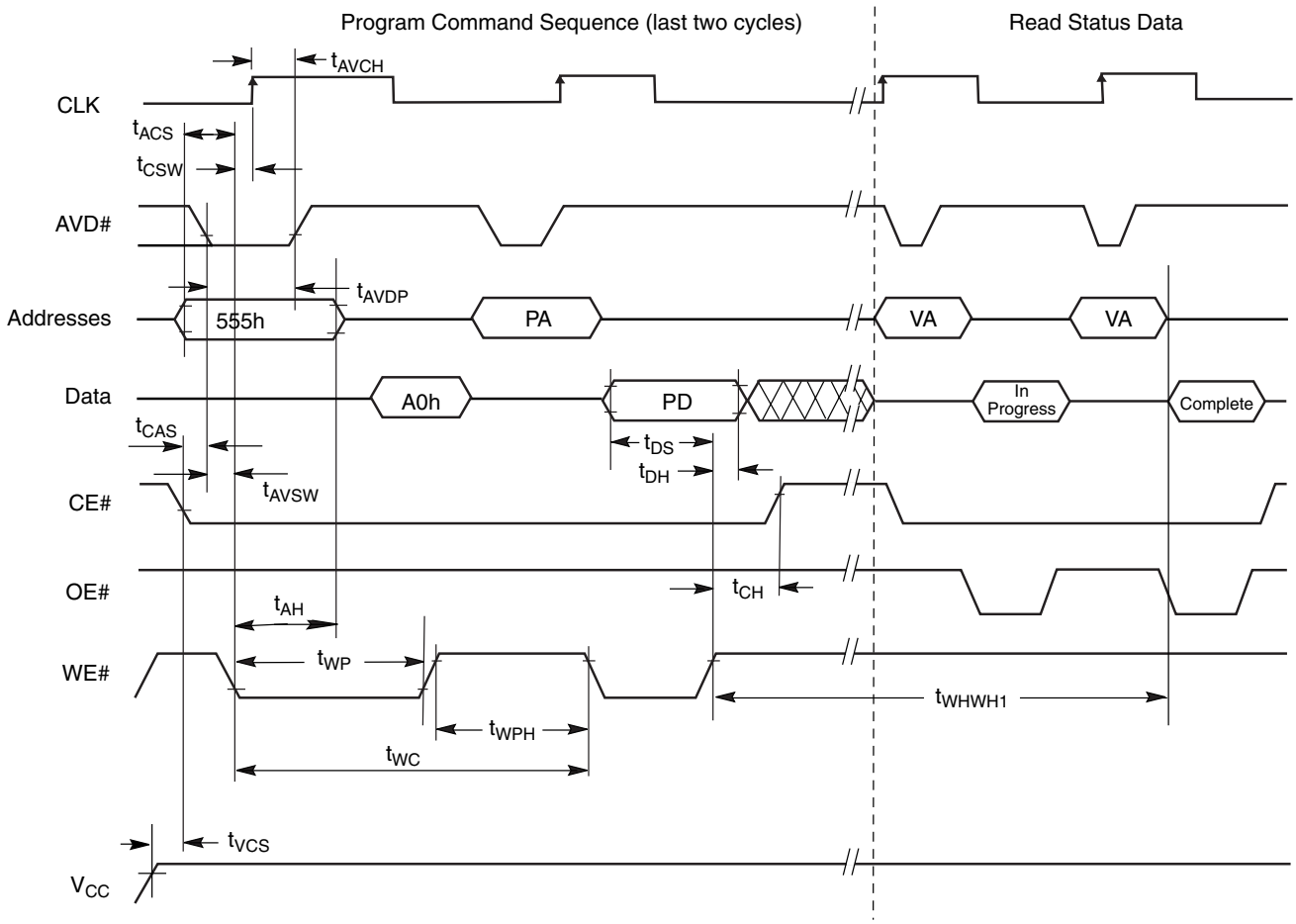


Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A22–A12 are don't care during command sequence unlock cycles.*
4. *CLK can be either V_{IL} or V_{IH}.*
5. *The Asynchronous programming operation is independent of the Set Device Read Mode bit in the Configuration Register.*

Figure 23. Asynchronous Program Operation Timings: WE# Latched Addresses

AC Characteristics

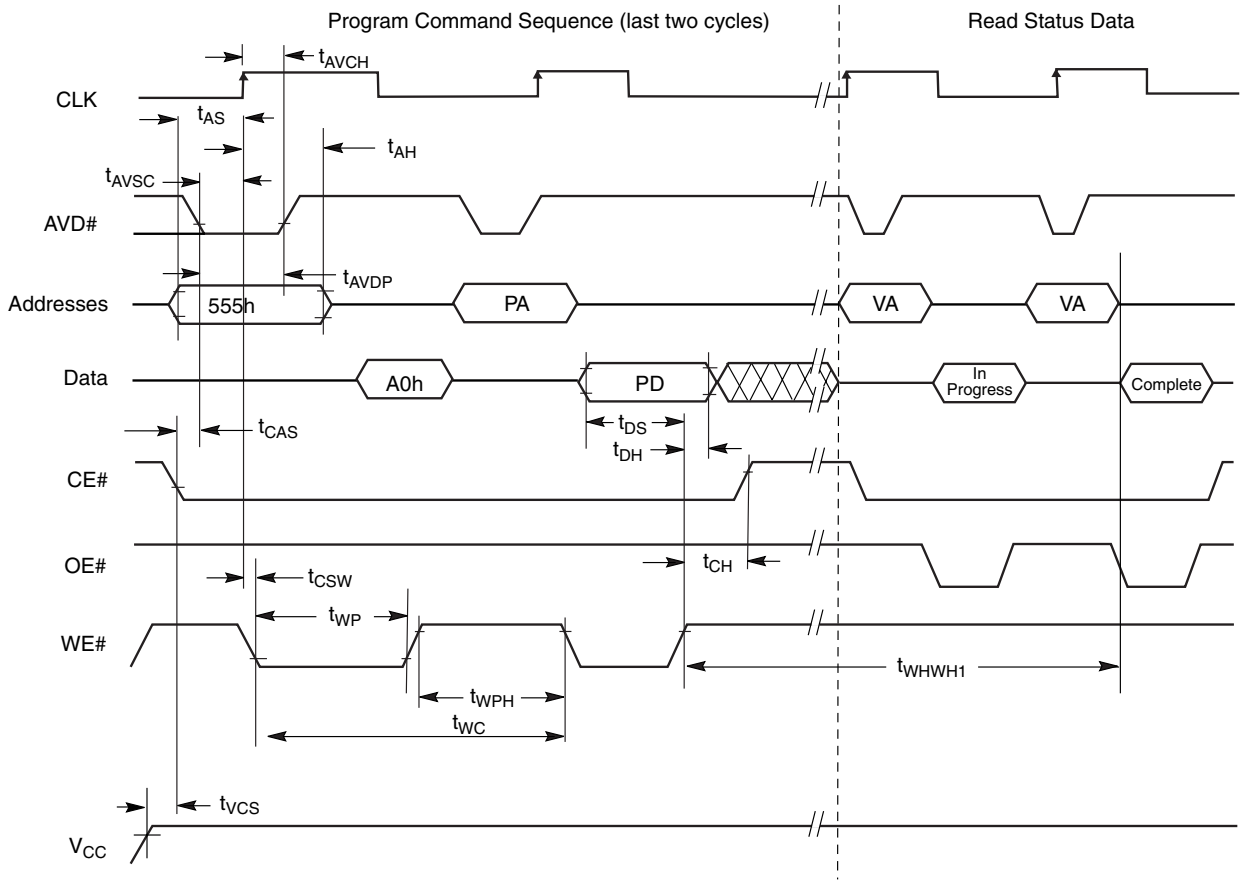


Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A22–A12 are don't care during command sequence unlock cycles.*
4. *Addresses are latched on the first of either the rising edge of AVD# or the active edge of CLK.*
5. *Either CE# or AVD# is required to go from low to high in between programming command sequences.*
6. *The Synchronous programming operation is dependent of the Set Device Read Mode bit in the Configuration Register. The Configuration Register must be set to the Synchronous Read Mode.*

Figure 24. Synchronous Program Operation Timings: WE# Latched Addresses

AC Characteristics



Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *A22–A12 are don't care during command sequence unlock cycles.*
4. *Addresses are latched on the first of either the rising edge of AVD# or the active edge of CLK.*
5. *Either CE# or AVD# is required to go from low to high in between programming command sequences.*
6. *The Synchronous programming operation is dependent of the Set Device Read Mode bit in the Configuration Register. The Configuration Register must be set to the Synchronous Read Mode.*

Figure 25. Synchronous Program Operation Timings: CLK Latched Addresses

AC Characteristics

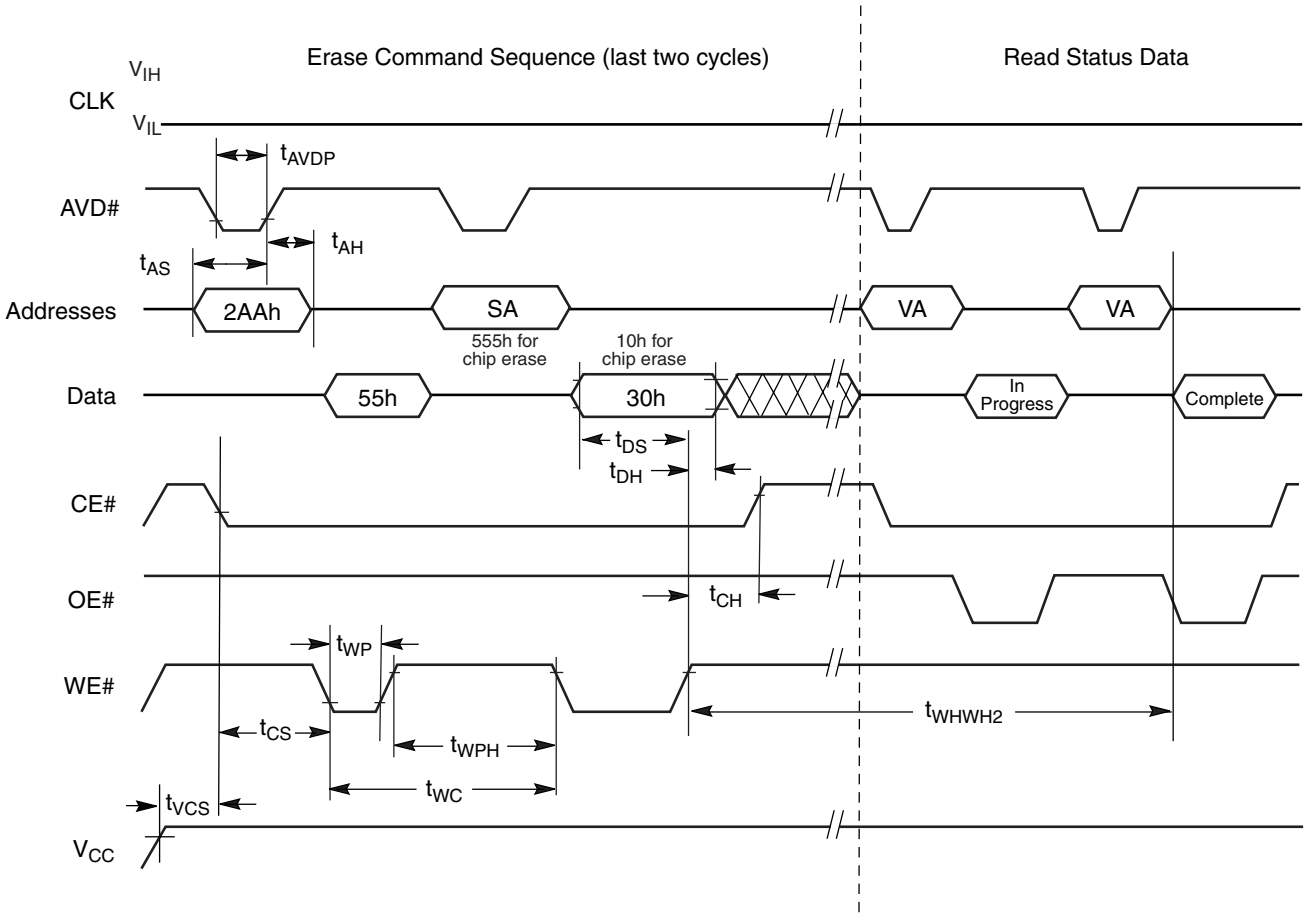
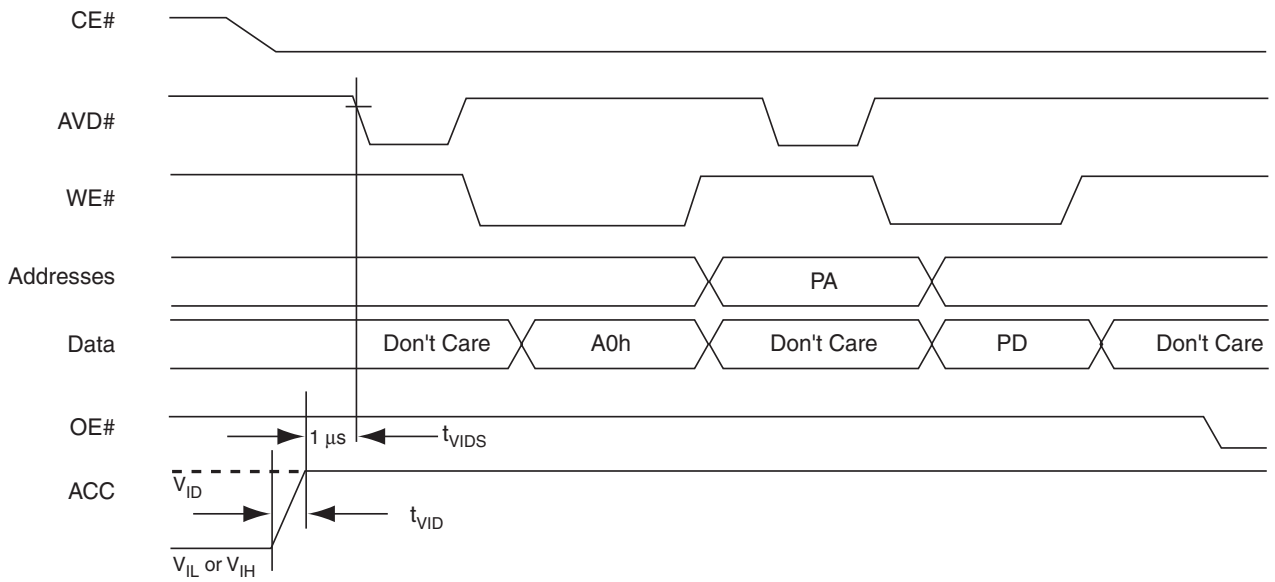


Figure 26. Chip/Sector Erase Command Sequence

Notes:

1. *SA is the sector address for Sector Erase.*
2. *Address bits A22–A12 are don't cares during unlock cycles in the command sequence.*

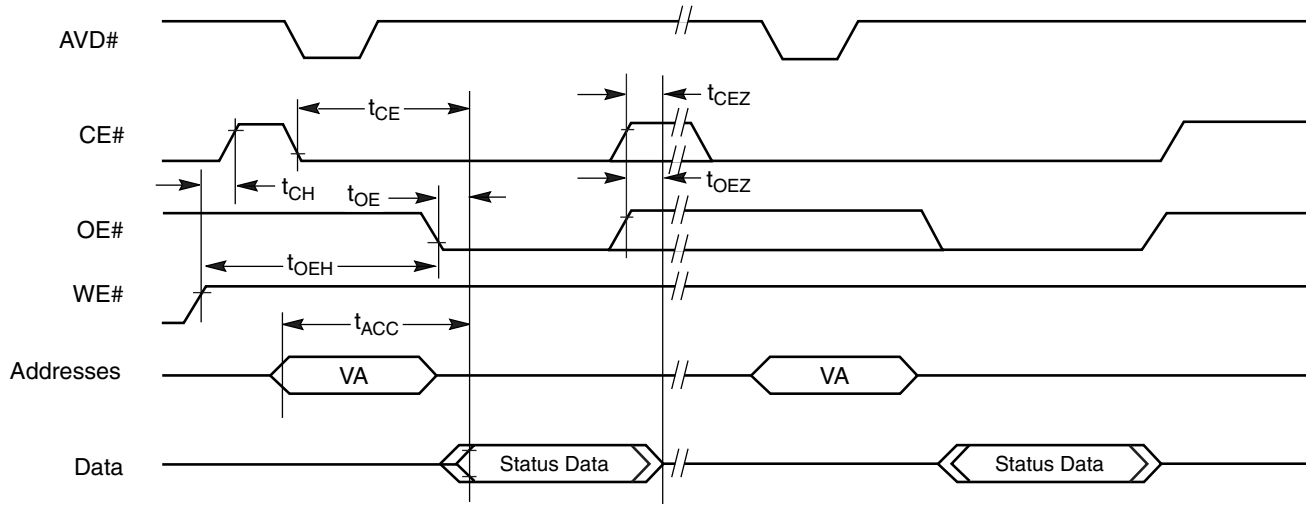
AC Characteristics



Note: *Use setup and hold times from conventional program operation.*

Figure 27. Accelerated Unlock Bypass Programming Timing

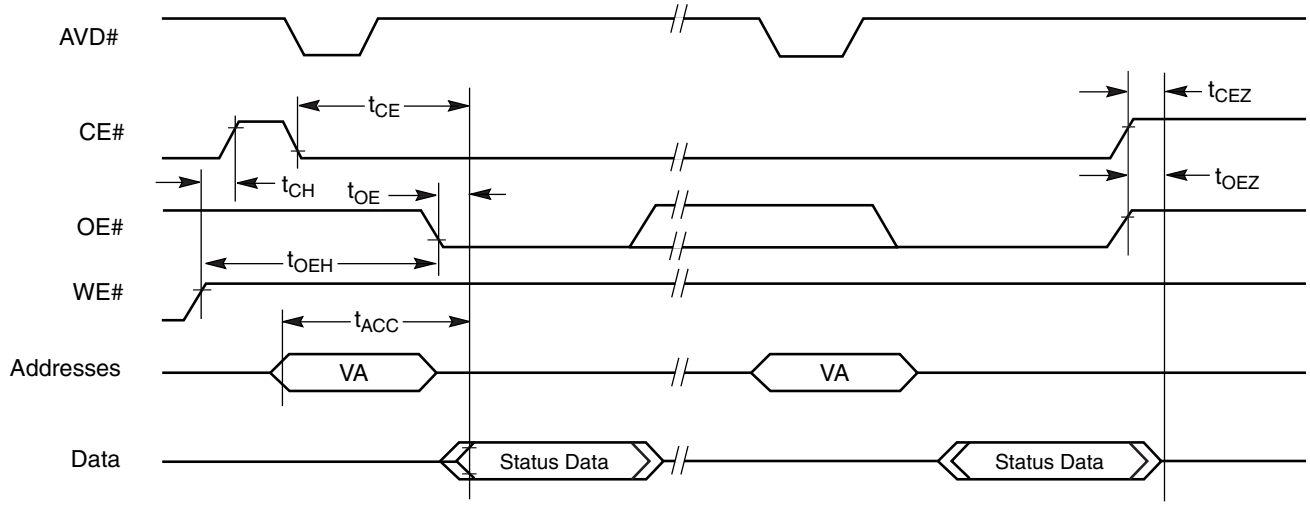
AC Characteristics



Notes:

1. *Status reads in figure are shown as asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, and Data# Polling will output true data.*
3. *While in Asynchronous mode, RDY will be low while the device is in embedded erase or programming mode.*

Figure 28. Data# Polling Timings (During Embedded Algorithm)

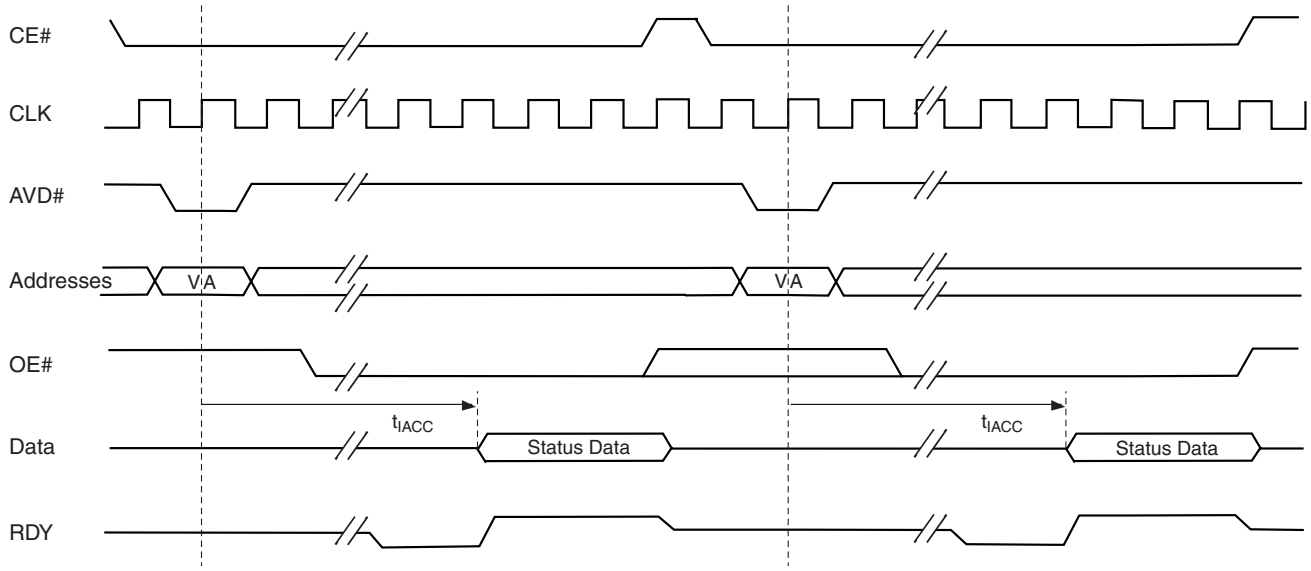


Notes:

1. *Status reads in figure are shown as asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*
3. *While in Asynchronous mode, RDY will be low while the device is in embedded erase or programming mode.*

Figure 29. Toggle Bit Timings (During Embedded Algorithm)

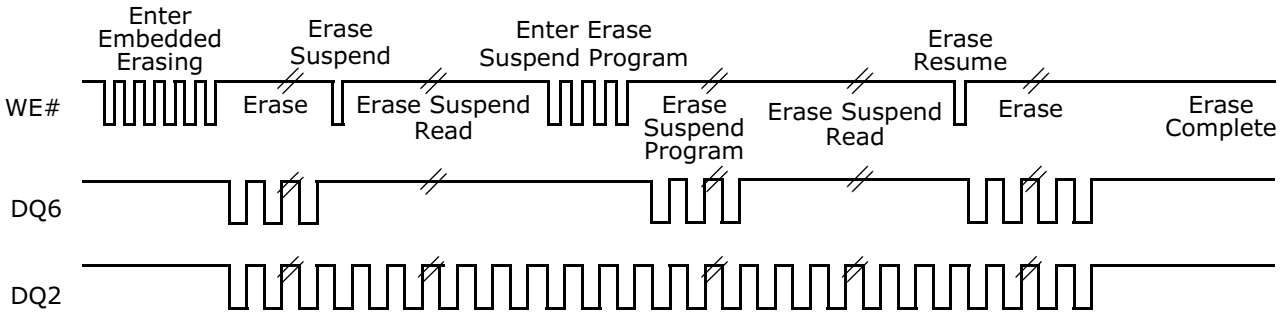
AC Characteristics



Notes:

1. *The timings are similar to synchronous read timings.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*
3. *RDY is active with data (A18 = 0 in the Configuration Register). When A18 = 1 in the Configuration Register, RDY is active one clock cycle before data.*

Figure 30. Synchronous Data Polling Timings/Toggle Bit Timings



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 31. DQ2 vs. DQ6

AC Characteristics

Temporary Sector Unprotect

Parameter					
JEDEC	Std	Description		All Speed Options	Unit
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	250	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RDY High for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*

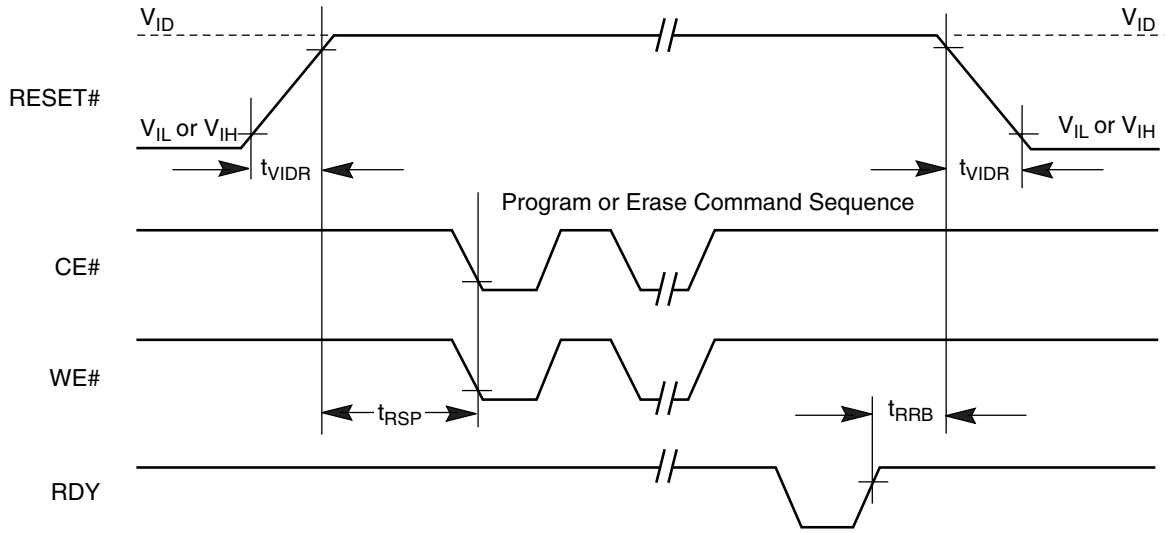
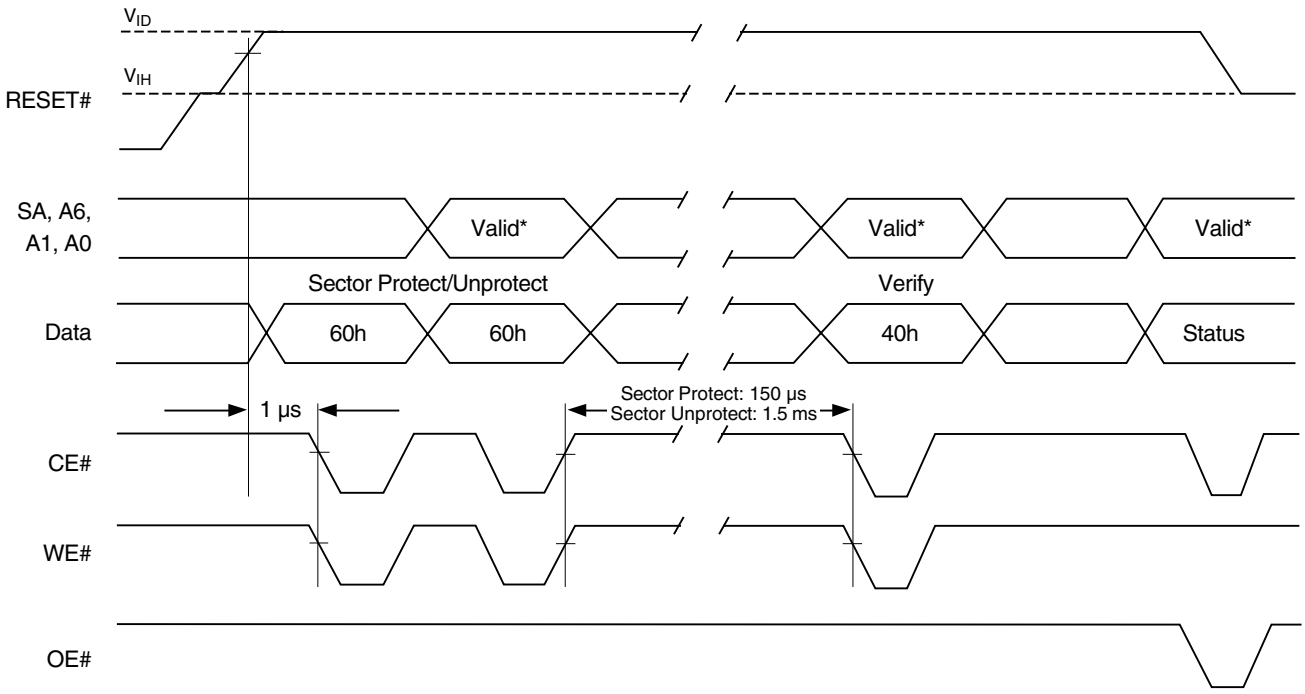


Figure 32. Temporary Sector Unprotect Timing Diagram

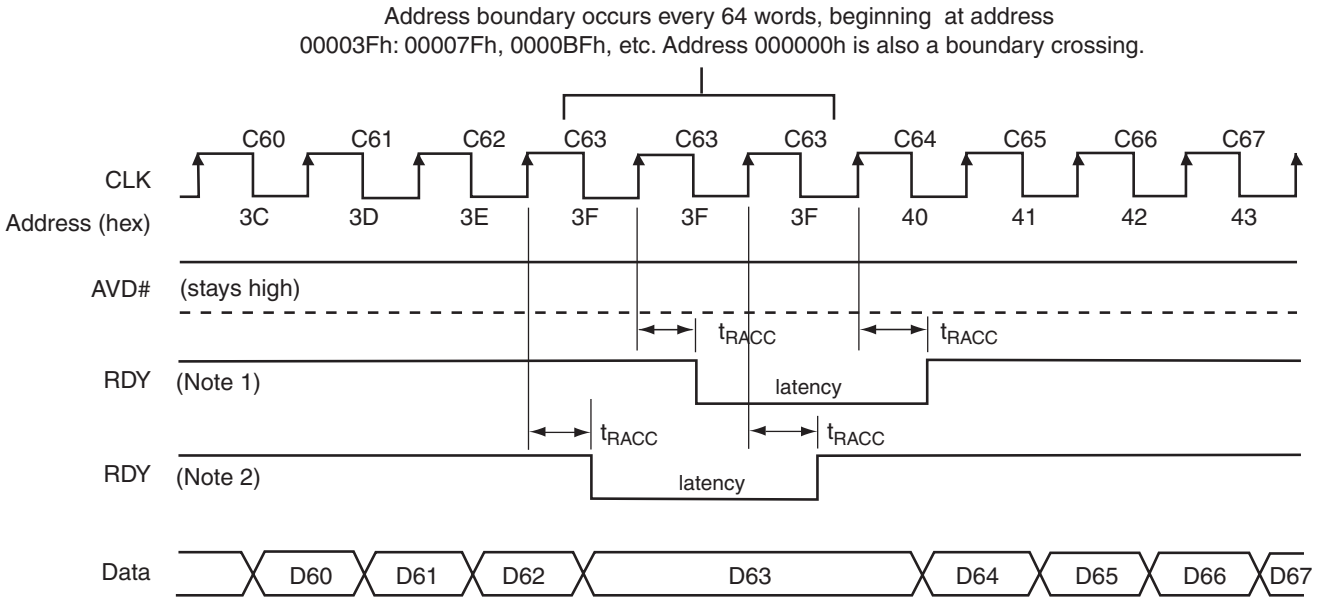
AC Characteristics



* *For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.*

Figure 33. Sector/Sector Block Protect and Unprotect Timing Diagram

AC Characteristics

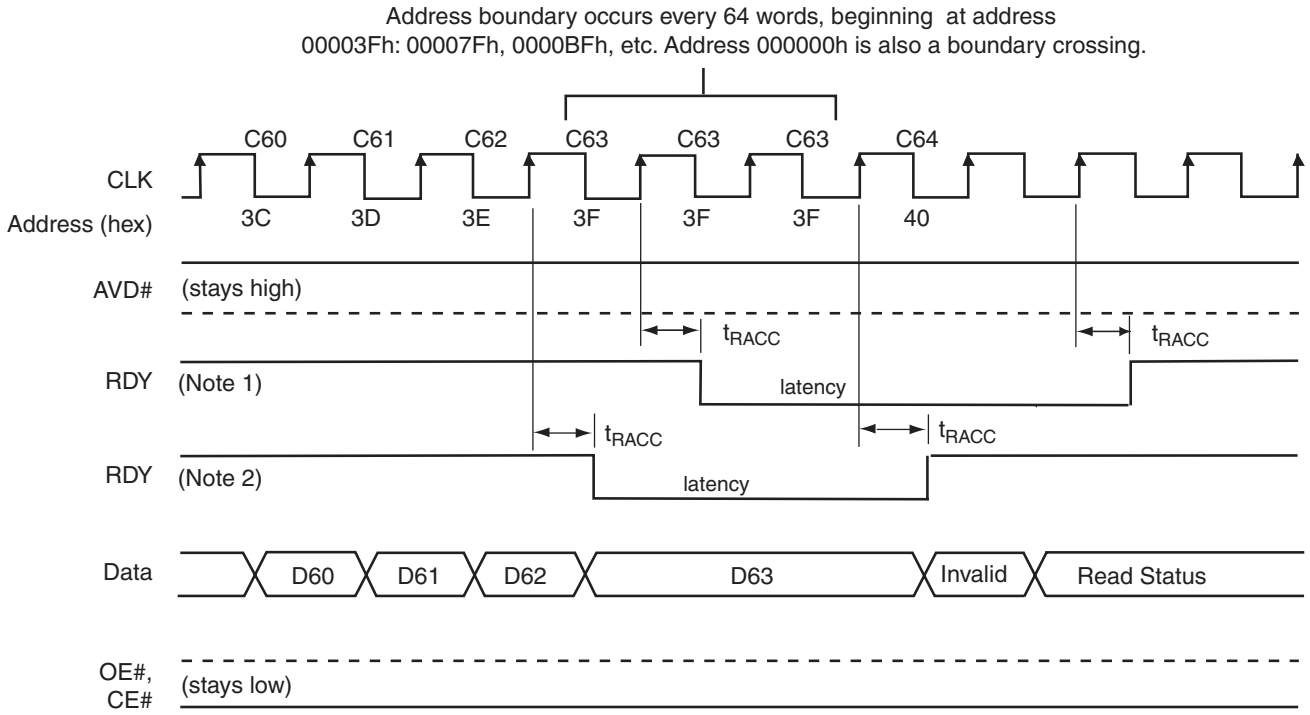


Notes:

1. *RDY active with data (A18 = 0 in the Configuration Register).*
2. *RDY active one clock cycle before data (A18 = 1 in the Configuration Register).*
3. *Cxx indicates the clock that triggers Dxx on the outputs; for example, C60 triggers D60. Figure shows the device not crossing a bank in the process of performing an erase or program.*
4. *If the starting address latched in is either 3Eh or 3Fh (or some 64 multiple of either), there is no additional 2 cycle latency at the boundary crossing.*

Figure 34. Latency with Boundary Crossing

AC Characteristics

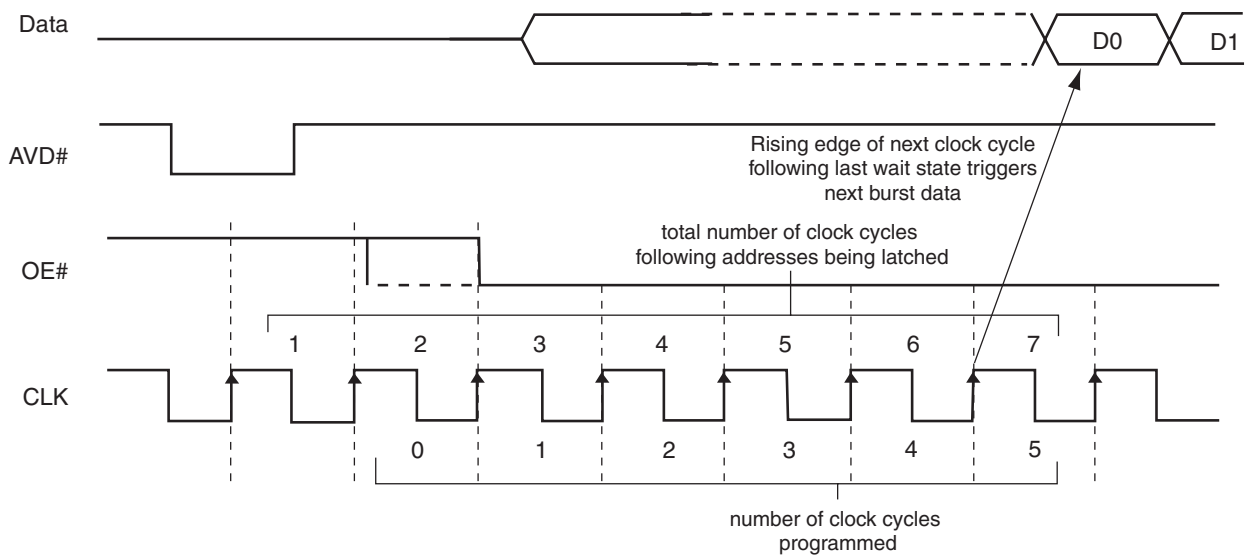


Notes:

1. *RDY active with data (A18 = 0 in the Configuration Register).*
2. *RDY active one clock cycle before data (A18 = 1 in the Configuration Register).*
3. *Cxx indicates the clock that triggers Dxx on the outputs; for example, C60 triggers D60. Figure shows the device crossing a bank in the process of performing an erase or program.*

Figure 35. Latency with Boundary Crossing into Program/Erase Bank

AC Characteristics



Wait State Decoding Addresses:
A14, A13, A12 = "111" ⇒ Reserved

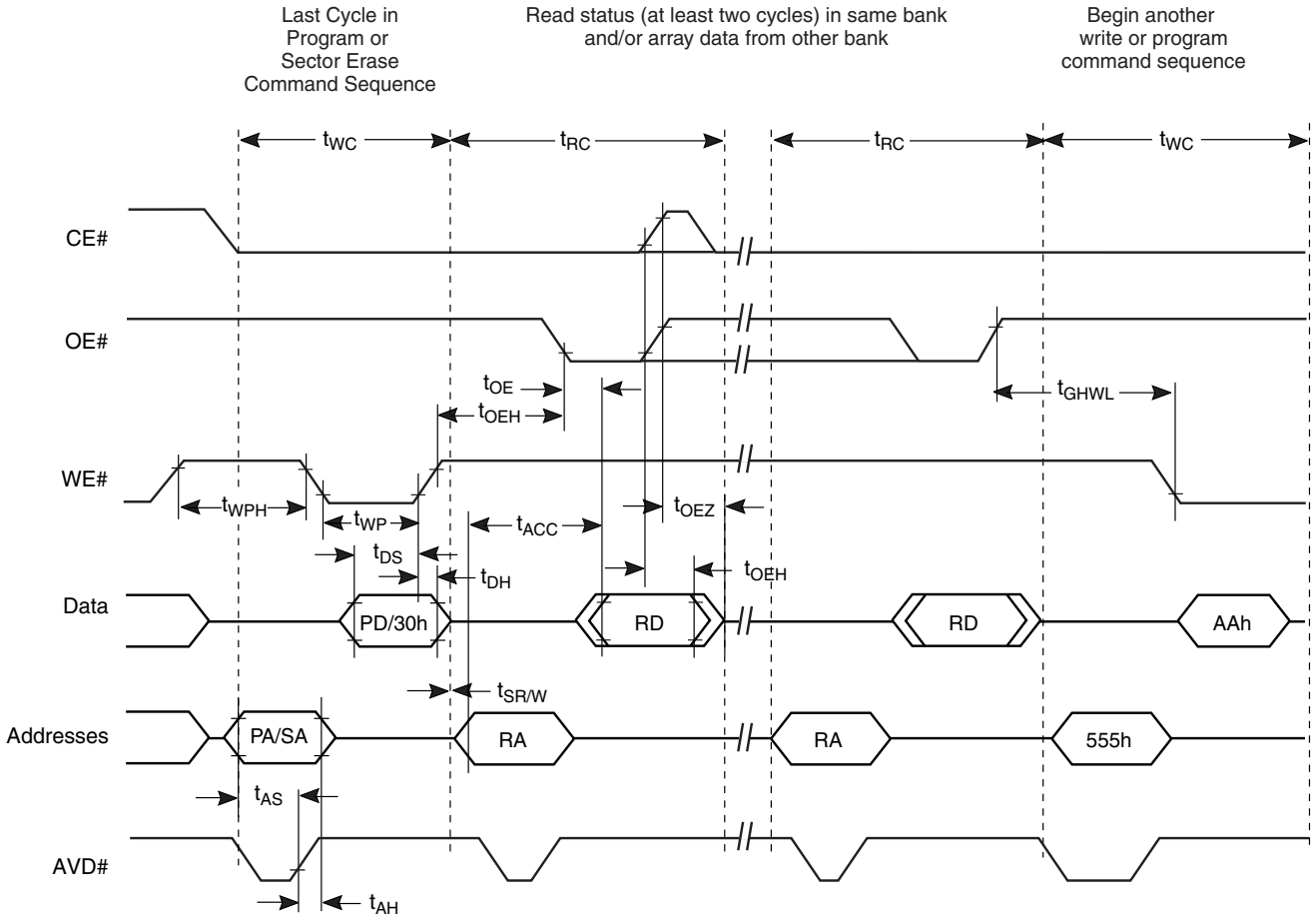
A14, A13, A12 = "110" ⇒ Reserved

A14, A13, A12 = "101" ⇒ 5 programmed, 7 total
A14, A13, A12 = "100" ⇒ 4 programmed, 6 total
A14, A13, A12 = "011" ⇒ 3 programmed, 5 total
A14, A13, A12 = "010" ⇒ 2 programmed, 4 total
A14, A13, A12 = "001" ⇒ 1 programmed, 3 total
A14, A13, A12 = "000" ⇒ 0 programmed, 2 total

Note: *Figure assumes address D0 is not at an address boundary, active clock edge is rising, and wait state is set to "101".*

Figure 36. Example of Wait States Insertion

AC Characteristics



Note: *Breakpoints in waveforms indicate that system may alternately read array data from the "non-busy bank" while checking the status of the program or erase operation in the "busy" bank. The system should read status twice to ensure valid information.*

Figure 37. Back-to-Back Read/Write Cycle Timings

Erase and Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	32 Kword	<0.4	<2	s	Excludes 00h programming prior to erasure (Note 4)
	4 Kword	<0.2	<2		
Chip Erase Time	128J	<103		s	
	064J	<53			
Word Programming Time		<6	<100	µs	Excludes system level overhead (Note 5)
Accelerated Word Programming Time		<4	<67	µs	
Chip Programming Time (Note 3)	128J	<50.4		s	Excludes system level overhead (Note 5)
	064J	<25.2			
Accelerated Chip Programming Time	128J	<33		s	
	064J	<17			

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 100,000 cycles. Additionally, programming typicals assumes a checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.65 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 18, "Command Definitions," on page 76 for further information on command definitions.*
6. *The device has a minimum cycling endurance of 100,000 cycles per sector.*

CosmoRAM

32Mbit (2M word x 16-bit)
64Mbit (4M word x 16-bit)

SPANSION™

PRELIMINARY

Features

- **Asynchronous SRAM Interface**
- **Fast Access Time**
  - $t_{CE} = t_{AA}$ = 70ns max
- **8 words Page Access Capability**
  - t_{PAA} = 20ns max
- **Low Voltage Operating Condition**
  - V_{DD} = +1.65V to +1.95V (32M)
  - +1.70V to +1.95V (64M)
- **Wide Operating Temperature**
  - TA = -30°C to +85°C
- **Byte Control by LB# and UB#**
- **Low Power Consumption**
  - I_{DDA1} = 30mA max (32M), TBDmA max (64M)
  - I_{DDS1} = 80mA max (32M), TBDmA max (64M)
- **Various Power Down mode**
  - Sleep, 4M-bit Partial or 8M-bit Partial (32M)
  - Sleep, 8M-bit Partial or 16M-bit Partial (64M)

Pin Description (32M)

Pin Name	Description
A_{21} to A_0	Address Input: A_{20} to A_0 for 32M, A_{21} to A_0 for 64M
CE1#	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
WE#	Write Enable (Low Active)
OE#	Output Enable (Low Active)
UB#	Upper Byte Control (Low Active)
LB#	Lower Byte Control (Low Active)
CLK	Clock Input
ADV#	Address Valid Input (Low Active)
WAIT#	Wait Signal Output
DQ_{16-9}	Upper Byte Data Input/Output
DQ_{8-1}	Lower Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground

Functional Description

Asynchronous Operation (Page Mode)

Mode	CE2	CE1#	CLK	ADV#	WE#	OE#	LB#	UB#	A_{21-0}	DQ_{8-1}	DQ_{16-9}	WAIT#
Standby (Deselect)	H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
Output Disable (Note 1)	H	L	X	(Note 3)	H	H	X	X	Note 5	High-Z	High-Z	High-Z
Output Disable (No Read)			X		H	L	H	H	Valid	High-Z	High-Z	High-Z
Read (Upper Byte)			X				H	L	Valid	High-Z	Output Valid	High-Z
Read (Lower Byte)			X				L	H	Valid	Output Valid	High-Z	High-Z
Read (Word)			X				L	L	Valid	Output Valid	Output Valid	High-Z
Page Read			X				L/H	L/H	Valid	Note 6	Note 6	High-Z
No Write			X		L	H (Note 4)	H	H	Valid	Invalid	Invalid	High-Z
Write (Upper Byte)			X				H	L	Valid	Invalid	Input Valid	High-Z
Write (Lower Byte)			X				L	H	Valid	Input Valid	Invalid	High-Z
Write (Word)			X				L	L	Valid	Input Valid	Input Valid	High-Z
Power Down (Note 2)	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z

Legend:*L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High Impedance.*

Notes:

1. *Should not be kept at this logic condition longer than 1µs.*
2. *Power Down mode can be entered from Standby state and all DQ pins are in High-Z state. Data retention depends on the selection of Partial Size. Refer to the "Power Down" section in the Functional Description for details.*
3. *"L" for address pass through and "H" for address latch on the rising edge of ADV#.*
4. *OE# can be V_{IL} during Write operation if the following conditions are satisfied:*
   (1) Write pulse is initiated by CE1# (refer to CE1# Controlled Write timing), or cycle time of the previous operation cycle is satisfied.
   (2) OE# stays V_{IL} during Write cycle
5. *Can be either V_{IL} or V_{IH} but must be valid before Read or Write.*
6. *Output is either Valid or High-Z depending on the level of UB# and LB# input.*

Functional Description

Synchronous Operation (Burst Mode)

Mode	CE2	CE1#	CLK	ADV#	WE#	OE#	LB#	UB#	A_{21-0}	DQ_{8-1}	DQ_{16-9}	WAIT#
Standby (Deselect)	H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
Start Address Latch (Note 1)		L	VE (Note 3)	PELP	X (Note 4)	X (Note 4)	X (Note 6)	X (Note 6)	Valid (Note 7)	High-Z (Note 8)	High-Z (Note 8)	High-Z (Note 11)
Advance Burst Read to Next Address (Note 1)			VE (Note 3)	H	H	L			X	Output Valid (Note 9)	Output Valid (Note 9)	Output Valid
Burst Read Suspend (Note 1)			VE (Note 3)			H				High-Z	High-Z	High (Note 12)
Advance Burst Write to Next Address (Note 1)			VE (Note 3)		L (Note 5)	H				Input Valid (Note 10)	Input Valid (Note 10)	High (Note 13)
Burst Write Suspend (Note 1)			VE (Note 3)		H (Note 5)					Iput Invalid	Iput Invalid	High (Note 12)
Terminate Burst Read		VE	X		H	X				High-Z	High-Z	High-Z
Terminate Burst Write		VE	X		X	H				High-Z	High-Z	High-Z
Power Down (Note 2)	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z

Legend: *L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, VE = Valid Edge, PELP = Positive Edge of Low Pulse, High-Z = High Impedance.*

Notes:

1. *Should not be kept this logic condition longer than the specified time of 8µs for 32M and 4µs for 64M.*
2. *Power Down mode can be entered from Standby state and all DQ pins are in High-Z state. Data retention depends on the selection of Partial Size. Refer to the "Power Down" section for details.F*
3. *Valid clock edge shall be set on either positive or negative edge through CR Set. CLK must be started and stable prior to memory access.*
4. *Can be either V_{IL} or V_{IH} except for the case the both of OE# and WE# are V_{IL}. It is prohibited to bring the both of OE# and WE# to V_{IL}.*
5. *When device is operating in "WE# Single Clock Pulse Control" mode, WE# is don't care once write operation is determined by WE# Low Pulse at the beginning of write access together with address latching. Write suspend feature is not supported in "WE# Single Clock Pulse Control" mode.*
6. *Can be either V_{IL} or V_{IH} but must be valid before Read or Write is determined. And once UB# and LB# inputs are determined, they must not be changed until the end of burst.*
7. *Once valid address is determined, input address must not be changed during ADV#=L.*
8. *If OE#=L, output is either Invalid or High-Z depending on the level of UB# and LB# input. If WE#=L, Input is Invalid. If OE#=WE#=H, output is High-Z.*
9. *Output is either Valid or High-Z depending on the level of UB# and LB# input.*
10. *Input is either Valid or Invalid depending on the level of UB# and LB# input.*
11. *Output is either High-Z or Invalid depending on the level of OE# and WE# input.*
12. *Keep the level from previous cycle except for suspending on last data. Refer to "WAIT# Output Function" for details.*
13. *WAIT# output is driven in High level during write operation.*

State Diagrams

Initial/Standby State

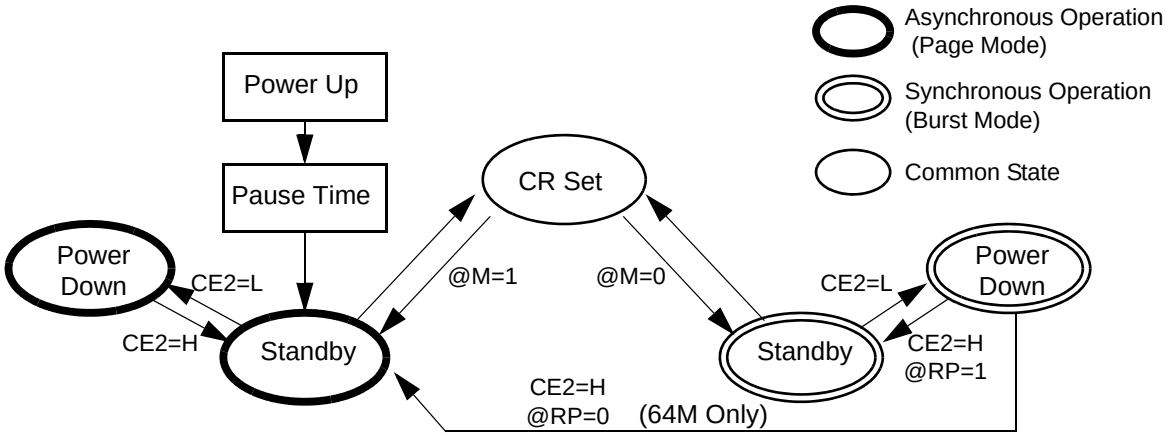


Figure 38. Initial Standby State Diagram

Asynchronous Operation State

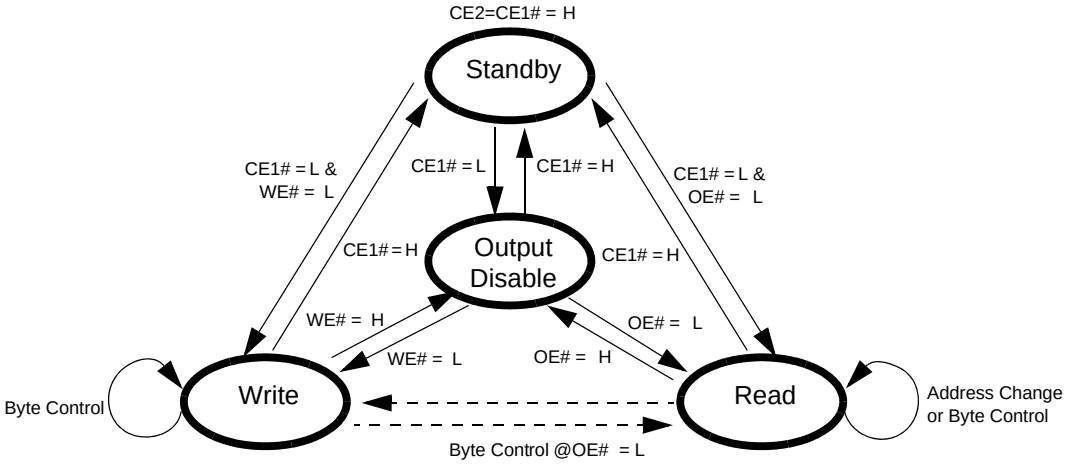


Figure 39. Asynchronous Operation State Diagram

Synchronous Operation State

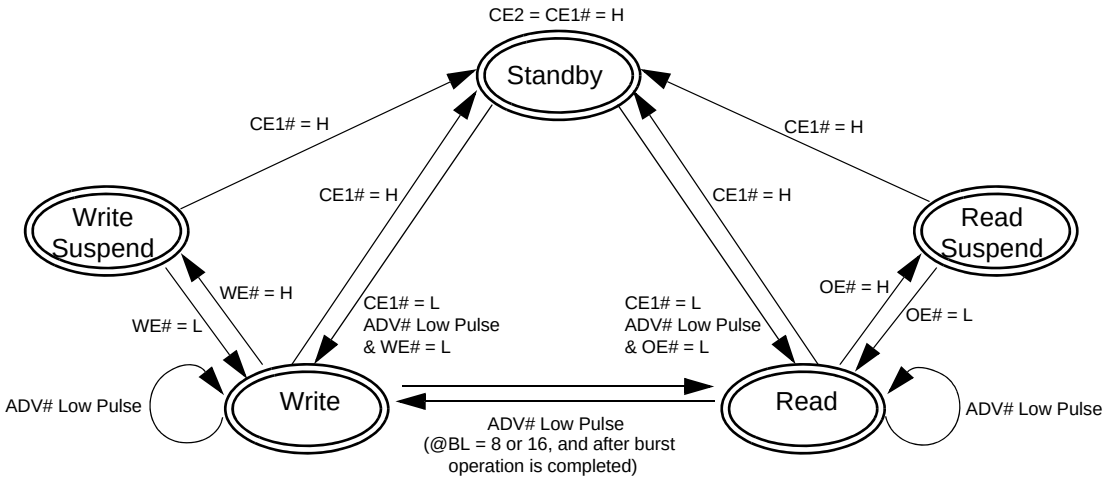


Figure 40. Synchronous Operation Diagram

Notes:

1. *Assumes all the parameters specified in the "AC Characteristics" section are satisfied. Refer to the "Functional Description" section, "AC Characteristics" section, and the "Timing Diagrams" section for details. RP (Reset to Page) mode is available only for 64M.*

Functional Description

This device supports asynchronous page read & normal write operation and synchronous burst read & burst write operation for faster memory access and features three kinds of power down modes for power saving as a user configurable option.

Power-up

It is required to follow the power-up timing to start executing proper device operation. Refer to POWER-UP Timing. After Power-up, the device defaults to asynchronous page read & normal write operation mode with sleep power down feature.

Configuration Register

The Configuration Register (CR) is used to configure the type of device function among optional features. Each selection of features is set through CR Set sequence after Power-up. If CR Set sequence is not performed after power-up, the device is configured for asynchronous operation with sleep power down feature as default configuration.

CR Set Sequence

The CR Set requires total 6 read/write operations with unique address. Between each read/write operation requires the device to be in standby mode. The following table shows the detail sequence.

Cycle #	Operation	Address	Data
1st	Read	3FFFFFh (MSB)	Read Data (RDa)
2nd	Write	3FFFFFh	RDa

Cycle #	Operation	Address	Data
3rd	Write	3FFFFFh	RDa
4th	Write	3FFFFFh	X
5th	Write	3FFFFFh	X
6th	Read	Address Key	Read Data (RDb)

The first cycle is to read from most significant address (MSB).

The second and third cycle are to write to MSB. If the second or third cycle is written into the different address, the CR Set is cancelled and the data written by the second or third cycle is valid as a normal write operation. It is recommended to write back the data (RDa) read by first cycle to MSB in order to secure the data.

The forth and fifth cycle is to write to MSB. The data of forth and fifth cycle is don't-care. If the forth or fifth cycle is written into different address, the CR Set is also cancelled but write data may not be written as normal write operation.

The last cycle is to read from specific address key for mode selection. And read data (RDb) is invalid.

Once this CR Set sequence is performed from an initial CR set to the other new CR set, the written data stored in memory cell array may be lost. So, CR Set sequence should be performed prior to regular read/write operation if necessary to change from default configuration.

Address Key

The address key has the following format.

Address Pin	Register Name	Function	Key	Description		Note
				32M	64M	
A21	—	—	1	—	Unused bits muse be 1	1
A20-A19	PS	Partial Size	00	8M Partial	16M Partial	
			01	4M Partial	8M Partial	
			10	Reserved for future use		2
			11	Sleep [Default]		
A18-A16	BL	Burst Length	000 to 001	Reserved for future use		2
			010	8 words		
			011	16 words		
			100 to 110	Reserved for future use		2
			111	Continuous		
A15	M	Mode	0	Synchronous Mode (Burst Read / Write)		3
			1	Asynchronous Mode [Default] (Page Read / Normal Write)		4
A14-A12	RL	Read Latency	000	Reserved for future use		2
			001	3 clocks		
			010	4 clocks		
			011	5 clocks		
			100	Reserved for future use	6 clocks	
			101 to 111	Reserved for future use		2
A11	BS	Burst Sequence	0	Reserved for future use		2
			1	Sequential		
A10	SW	Single Write	0	Burst Read & Burst Write		
			1	Burst Read & Single Write		5
A9	VE	Valid Clock Edge	0	Falling Clock Edge		
			1	Rising Clock Edge		
A8	RP	Reset to Page	0	Unused bits must be 1	Reset to Page mode	6
			1		Remain the previous mode	
A7	WC	Write Control	0	WE# Single Clock Pulse Control without Write Suspend Function		5
			1	WE# Level Control with Write Suspend Function		
A6-A0	—	—	1	Unused bits muse be 1		1

Notes:

1. *A21 and A6 to A0 must be all "1" in any case.*
2. *It is prohibited to apply this key.*
3. *If M=0, all the registers must be set with appropriate Key input at the same time.*
4. *If M=1, PS must be set with appropriate Key input at the same time. Except for PS, all the other key inputs must be "1".*
5. *Burst Read & Single Write is not supported at WE# Single Clock Pulse Control.*
6. *Effective only when PS=11. RP (Reset to Page) mode is available only for 64M.*

Power Down

The Power Down is low power idle state controlled by CE2. CE2 Low drives the device in power down mode and maintains low power idle state as long as CE2 is kept Low. CE2 High resumes the device from power down mode. These devices have three power down mode. These can be programmed by series of read/write operations. Each mode has following features.

32M			64M		
Mode	**Data Retention Size**	**Retention Address**	**Mode**	**Data Retention Size**	**Retention Address**
Sleep (default)	No	N/A	Sleep (default)	No	N/A
4M Partial	4M bit	000000h to 03FFFFh	8M Partial	8M bit	000000h to 07FFFFh
8M Partial	8M bit	000000h to 07FFFFh	16M Partial	16M bit	000000h to 0FFFFFh

The default state is Sleep and it is the lowest power consumption but all data will be lost once CE2 is brought to Low for Power Down. It is not required to program to Sleep mode after power-up.

64M supports Reset to Page (RP) mode. When RP=0, Power Down comprehends a function to reset the device to default configuration (asynchronous mode). After resuming from power down mode, the device is back in default configurations. This is effective only when PS is set on Sleep mode. When Partial mode is selected, RP=0 is not effective.

Burst Read/Write Operation

Synchronous burst read/write operation provides faster memory access that synchronized to microcontroller or system bus frequency. Configuration Register Set is required to perform burst read & write operation after power-up. Once CR Set sequence is performed to select synchronous burst mode, the device is configured to synchronous burst read/write operation mode with corresponding RL and BL that is set through CR Set sequence together with operation mode. In order to perform synchronous burst read & write operation, it is required to control new signals, CLK, ADV# and WAIT# that Low Power SRAMs don't have.

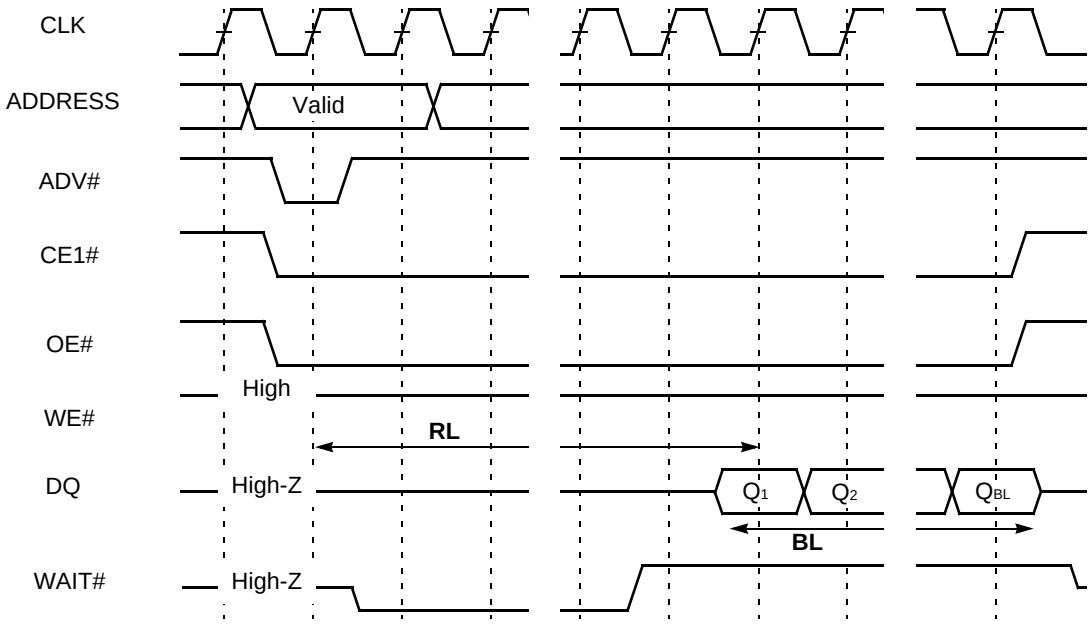


Figure 41. Burst Read Operation

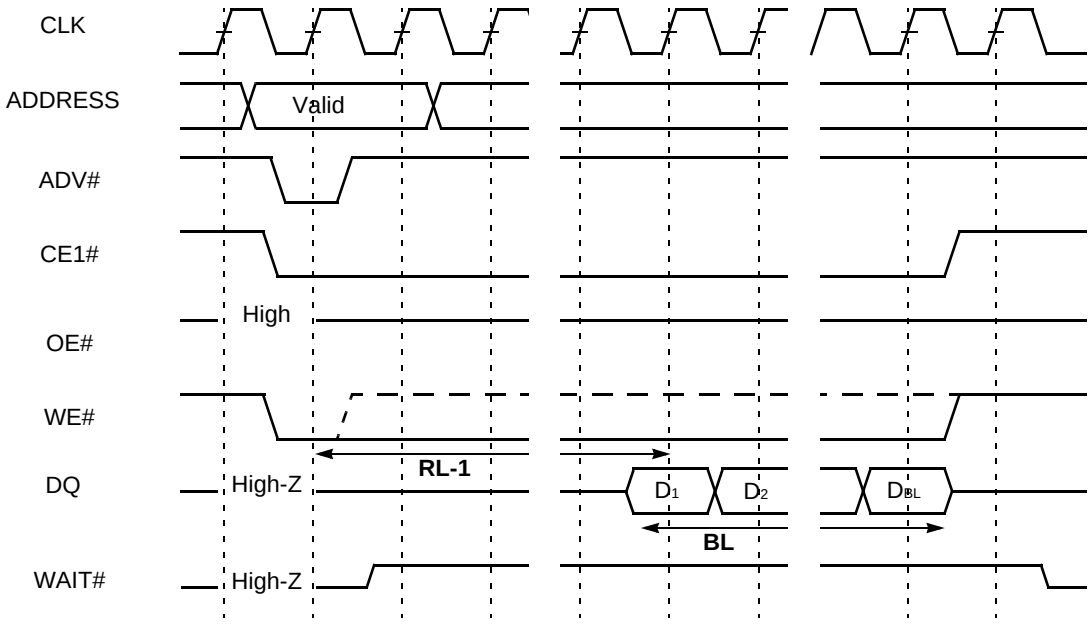


Figure 42. Burst Write Operation

CLK Input Function

The CLK is input signal to synchronize memory to microcontroller or system bus frequency during synchronous burst read & write operation. The CLK input increments device internal address counter and the valid edge of CLK is referred for latency counts from address latch, burst write data latch, and burst read data out. During synchronous operation mode, CLK input must be supplied except for standby state and power down state. CLK is don't care during asynchronous operation.

ADV# Input Function

The ADV# is input signal to indicate valid address presence on address inputs. It is applicable to synchronous operation as well as asynchronous operation. ADV# input is active during CE1#=L and CE1#=H disables ADV# input. All addresses are determined on the positive edge of ADV#.

During synchronous burst read/write operation, ADV#=H disables all address inputs. Once ADV# is brought to High after valid address latch, it is inhibited to bring ADV# Low until the end of burst or until burst operation is terminated. ADV# Low pulse is mandatory for synchronous burst read/write operation mode to latch the valid address input.

During asynchronous operation, ADV#=H also disables all address inputs. ADV# can be tied to Low during asynchronous operation and it is not necessary to control ADV# to High.

WAIT# Output Function

The WAIT# is output signal to indicate data bus status when the device is operating in synchronous burst mode.

During burst read operation, WAIT# output is enabled after specified time duration from OE#=L or CE1#=L whichever occurs last. WAIT# output Low indicates data out at next clock cycle is invalid, and WAIT# output becomes High one clock cycle prior to valid data out. During OE# read suspend, WAIT# output doesn't indicate data bus status but carries the same level from previous clock cycle (kept High) except for read suspend on the final data output. If final read data out is suspended, WAIT# output become high impedance after specified time duration from OE#=H.

In case of continuous burst read operation of 32M, an additional output delay may occur when a burst sequence crosses it's device-row boundary. The WAIT# output indicates this delay. Refer to the "Burst Length" section for the additional delay cycles in details.

During burst write operation, WAIT# output is enabled to High level after specified time duration from WE#=L or CE1#=L whichever occurs last and kept High for entire write cycles including WE# write suspend. The actual write data latching starts on the appropriate clock edge with respect to Valid Clock Edge, Read Latency and Burst Length. During WE# write suspend, WAIT# output doesn't indicate data bus status but carries the same level from previous clock cycle (kept High) except for write suspend on the final data input. If final write data in is suspended, WAIT# output become high impedance after specified time duration from WE#=H.

The burst write operation of 32M and the both burst read/write operation of 64M are always started after fixed latency with respect to Read Latency set in CR.

When the device is operating in asynchronous mode, WAIT# output is always in High Impedance.

Latency

Read Latency (RL) is the number of clock cycles between the address being latched and first read data becoming available during synchronous burst read operation. It is set through CR Set sequence after power-up. Once specific RL is set through CR Set sequence, write latency, that is the number of clock cycles between address being latched and first write data being latched, is automatically set to RL-1.The burst operation is always started after fixed latency with respect to Read Latency set in CR. RL=6 is available only for 64M.

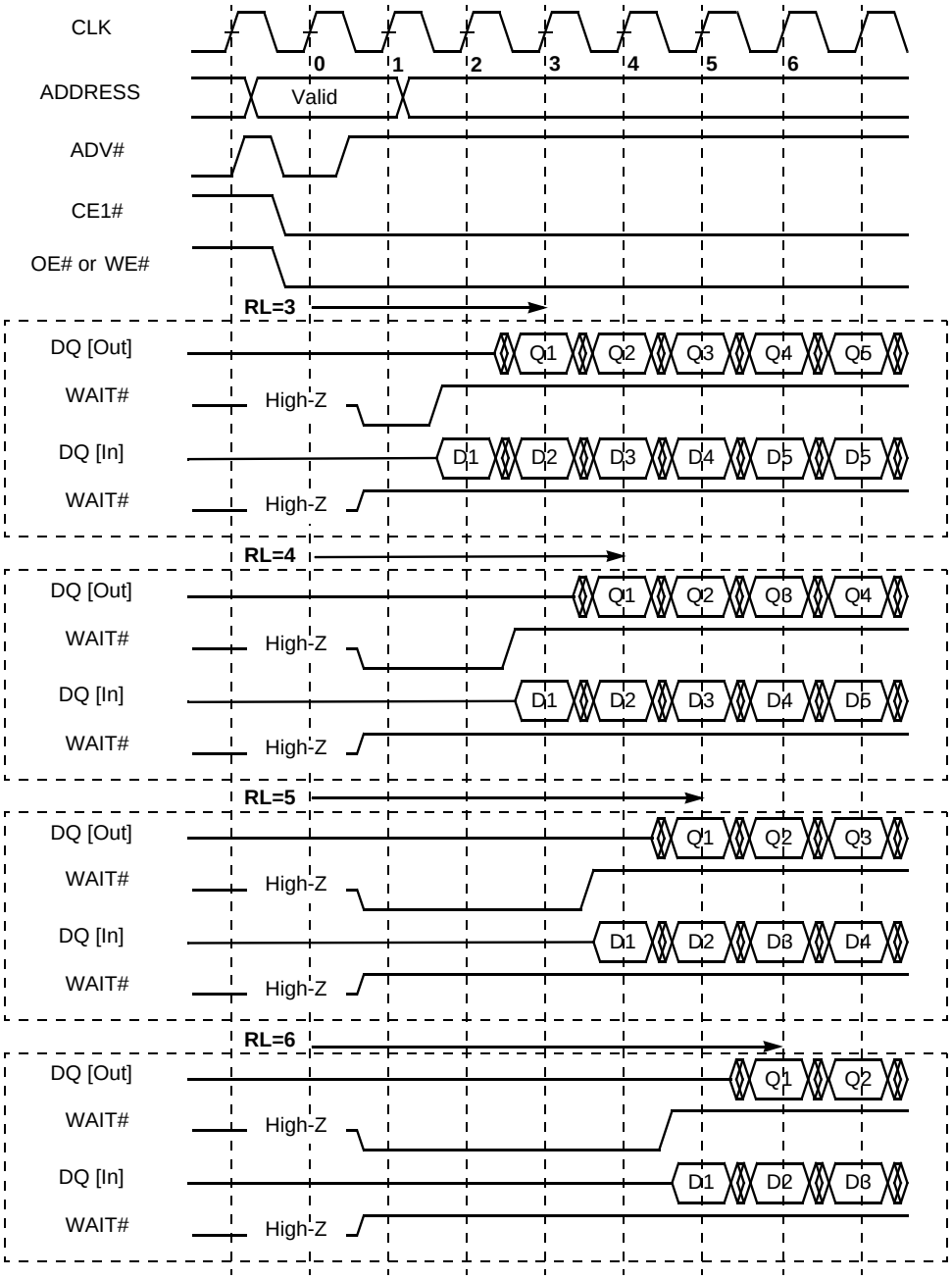


Figure 43. Read Latency Diagram

Address Latch by ADV#

The ADV# indicates valid address presence on address inputs. During synchronous burst read/write operation mode, all the address are determined on the positive edge of ADV# when CE1#=L. The specified minimum value of ADV#=L setup time and hold time against valid edge of clock where RL count begin must be satisfied for appropriate RL counts. Valid address must be determined with specified setup time against either the negative edge of ADV# or negative edge of CE1# whichever comes late. And the determined valid address must not be changed during ADV#=L period.

Burst Length

Burst Length is the number of word to be read or write during synchronous burst read/write operation as the result of a single address latch cycle. It can be set on 8, 16 words boundary or continuous for entire address through CR Set sequence. The burst type is sequential that is incremental decoding scheme within a boundary address. Starting from initial address being latched, device internal address counter assign +1 to the previous address until reaching the end of boundary address and then wrap round to least significant address (=0). After completing read data out or write data latch for the set burst length, operation automatically ended except for continuous burst length. When continuous burst length is set, read/write is endless unless it is terminated by the positive edge of CE1#.

During continuous burst read of 32M, an additional output delay may occur when a burst sequence cross it's device-row boundary. This is the case when A0 to A6 of starting address is either 7Dh, 7Eh, or 7Fh as shown in the following table. The WAIT# signal indicates this delay. The 64M device has no additional output delay.

Start Address (A6-A0)	Read Address Sequence		
	BL = 8	BL = 16	Continuous
00h	00-01-02-...-06-07	00-01-02-...-0E-0F	00-01-02-03-04-...
01h	01-02-03-...-07-00	01-02-03-...-0F-00	01-02-03-04-05-...
02h	02-03-...-07-00-01	02-03-...-0F-00-01	02-03-04-05-06-...
03h	03-...-07-00-01-02	03-...-0F-00-01-02	03-04-05-06-07-...
...	...	...	...
7Ch	7C-...-7F-78-...-7B	7C-...-7F-70-...-7B	7C-7D-7E-7F-80-81-...
7Dh	7D-7E-7F-78-...-7C	7D-7E-7F-70-...-7C	7D-7E-7F-**WAIT**-80-81-...
7Eh	7E-7F-78-79-...-7D	7E-7F-70-71-...-7D	7E-7F-**WAIT**-**WAIT**-80-81-...
7Fh	7F-78-79-7A-...-7E	7F-70-71-72-...-7E	7F-**WAIT**-**WAIT**-**WAIT**-80-81

Note: *Read address in Hexadecimal.*

Single Write

Single Write is synchronous write operation with Burst Length =1. The device can be configured either to "Burst Read & Single Write" or to "Burst Read & Burst Write" through CR set sequence. Once the device is configured to "Burst Read & Single Write" mode, the burst length for synchronous write operation is always fixed 1 regardless of BL values set in CR, while burst length for read is in accordance with BL values set in CR.

Write Control

The device has two types of WE# signal control method, "WE# Level Control" and "WE# Single Clock Pulse Control", for synchronous write operation. It is configured through CR set sequence.

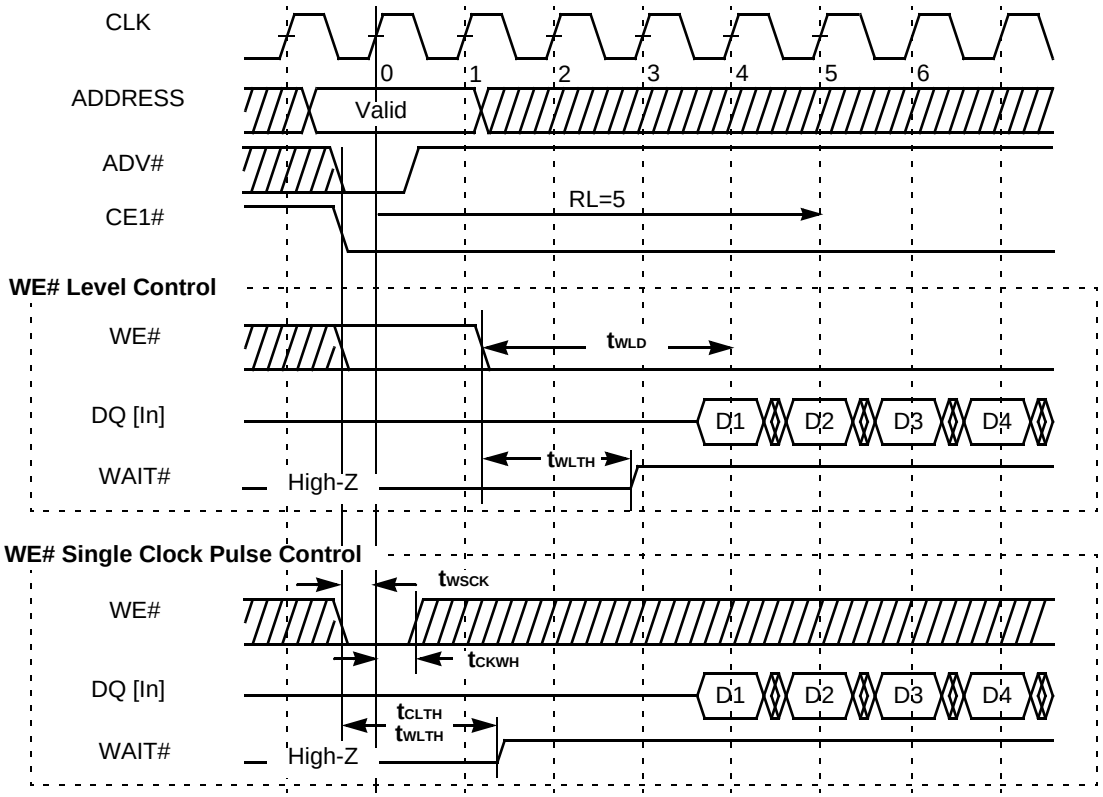


Figure 44. Write Controls

Burst Read Suspend

Burst read operation can be suspended by OE# High pulse. During burst read operation, OE# brought to High suspends burst read operation. Once OE# is brought to High with the specified set up time against clock where the data being suspended, the device internal counter is suspended, and the data output become high impedance after specified time duration. It is inhibited to suspend the first data out at the beginning of burst read.

OE# brought to Low resumes burst read operation. Once OE# is brought to Low, data output become valid after specified time duration, and internal address counter is reactivated. The last data out being suspended as the result of OE#=H and first data out as the result of OE#=L are from the same address.

In order to guarantee to output last data before suspension and first data after resumption, the specified minimum value of OE#=L hold time and setup time against clock edge must be satisfied respectively.

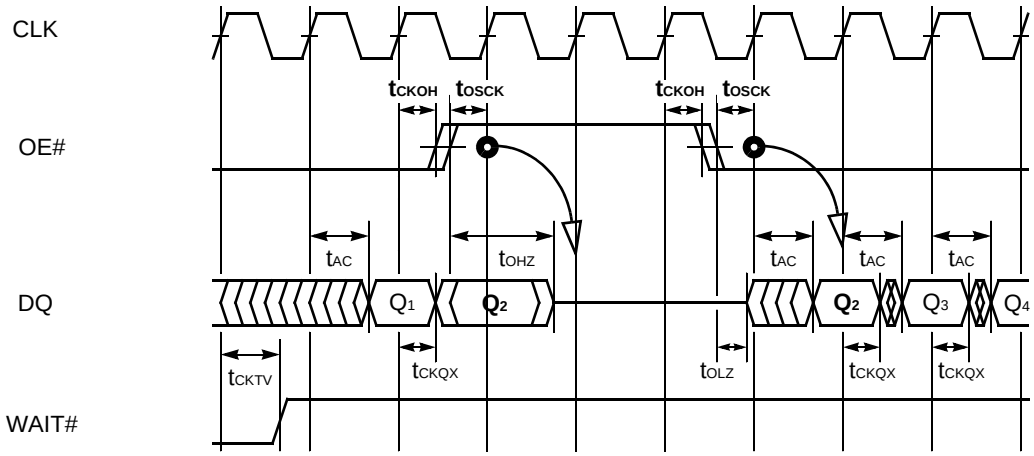


Figure 45. Burst Read Suspend Diagram

Burst Write Suspend

Burst write operation can be suspended by WE# High pulse. During burst write operation, WE# brought to High suspends burst write operation. Once WE# is brought to High with the specified set up time against clock where the data being suspended, device internal counter is suspended, data input is ignored. It is inhibited to suspend the first data input at the beginning of burst write.

WE# brought to Low resumes burst write operation. Once WE# is brought to Low, data input become valid after specified time duration, and internal address counter is reactivated. The write address of the cycle where data being suspended and the first write address as the result of WE#=L are the same address.

In order to guarantee to latch the last data input before suspension and first data input after resumption, the specified minimum value of WE#=L hold time and setup time against clock edge must be satisfied respectively. Burst write suspend function is available when the device is operating in WE# level controlled burst write only.

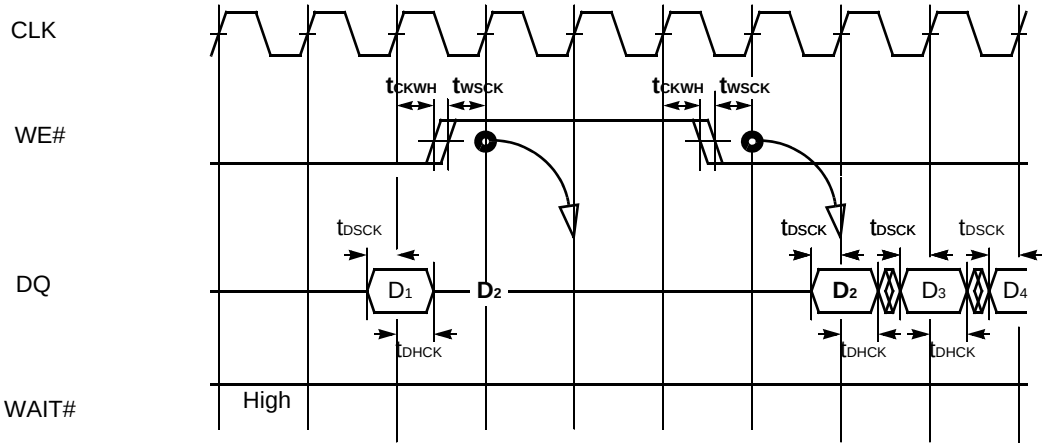


Figure 46. Burst Write Suspend Diagram

Burst Read Termination

Burst read operation can be terminated by CE1# brought to High. If BL is set on Continuous, burst read operation is continued endless unless terminated by

CE1#=H. It is inhibited to terminate burst read before first data out is completed. In order to guarantee last data output, the specified minimum value of CE1#=L hold time from clock edge must be satisfied. After termination, the specified minimum recovery time is required to start new access.

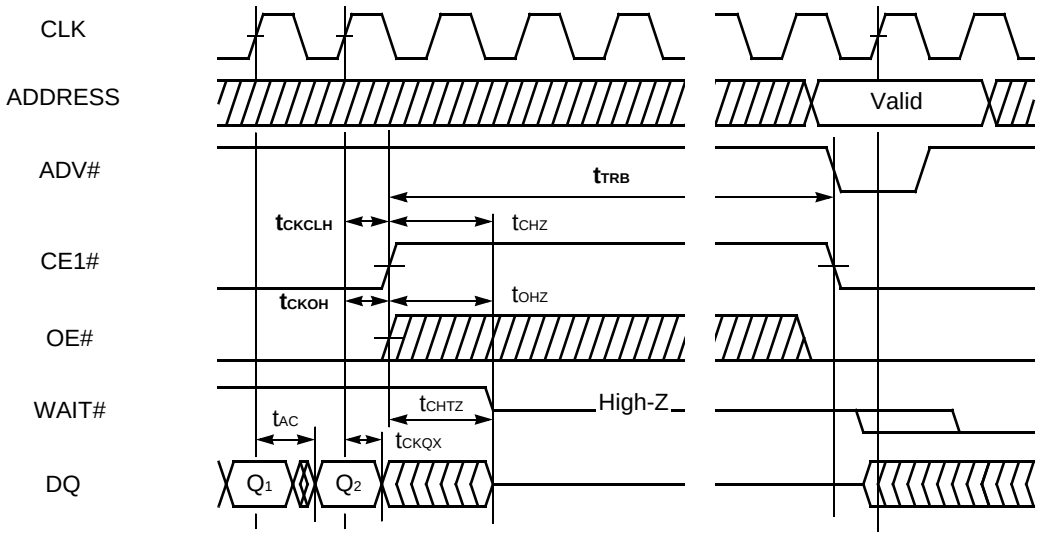


Figure 47. Burst Read Termination Diagram

Burst Write Termination

Burst write operation can be terminated by CE1# brought to High. If BL is set on Continuous, burst write operation is continued endless unless terminated by CE1#=H. It is inhibited to terminate burst write before first data in is completed. In order to guarantee last write data being latched, the specified minimum values of CE1#=L hold time from clock edge must be satisfied. After termination, the specified minimum recovery time is required to start new access.

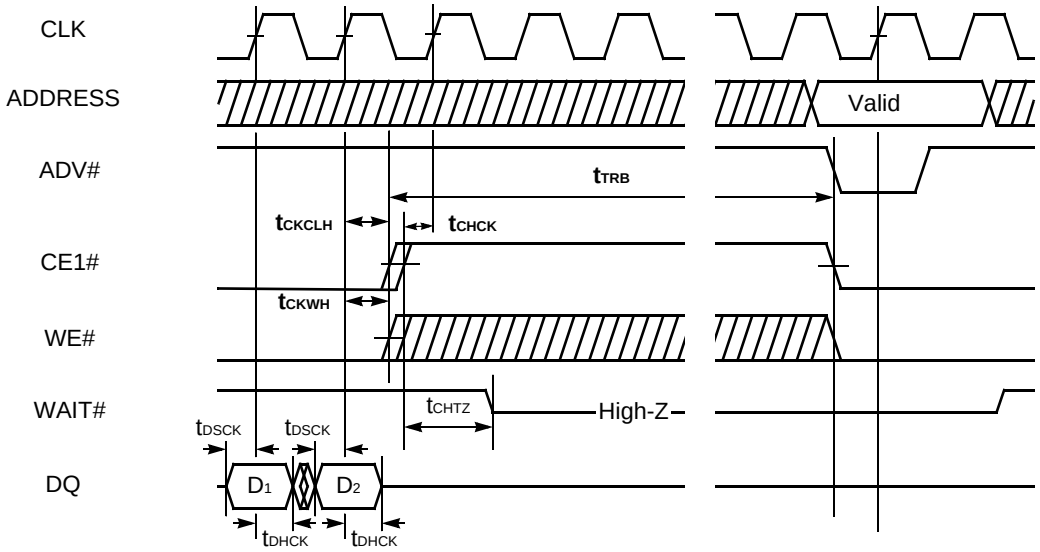


Figure 48. Burst Write Termination Diagram

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage of V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to +3.6	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +3.6	V
Short Circuit Output Current	I_{OUT}	±50	mA
Storage temperature	T_{STG}	-55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions (See Warning Below)

Parameter	Symbol	32M		64M		Unit
		Min	Max	Min	Max	
Supply Voltage	V_{DD}	1.65	1.95	1.7	1.95	V
	V_{SS}	0	0	0	0	V
High Level Input Voltage (Note 1)	V_{IH}	V_{DD} x 0.8	V_{DD}+0.2	V_{DD} x 0.8	V_{DD}+0.2	V
High Level Input Voltage (Note 2)	V_{IL}	-0.3	V_{DD} x 0.2	-0.3	V_{DD} x 0.2	V
Ambient Temperature	T_A	-30	85	-30	85	°C

Notes:

1. *Maximum DC voltage on input and I/O pins are V_{DD}+0.2V. During voltage transitions, inputs may positive overshoot to V_{DD}+1.0V for periods of up to 5 ns.*
2. *Minimum DC voltage on input or I/O pins are -0.3V. During voltage transitions, inputs may negative overshoot V_{SS} to -1.0V for periods of up to 5ns.*

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.

Package Pin Capacitance

Test conditions: T_A = 25°C, f = 1.0 MHz

Symbol	Description	Test Setup	Typ	Max	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0V	—	5	pF
C_{IN2}	Control Input Capacitance	V_{IN} = 0V	—	5	pF
C_{IO}	Data Input/Output Capacitance	V_{IO} = 0V	—	8	pF

DC Characteristics

(Under Recommended Conditions Unless Otherwise Noted)

Parameter	Symbol	Test Conditions		32M		64M		Unit
				Min.	Max.	Min.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}		-1.0	+1.0	-1.0	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{DD}, Output Disable		-1.0	+1.0	-1.0	+1.0	µA
Output High Voltage Level	V_{OH}	V_{DD} = V_{DD}(min), I_{OH} = –0.5mA		2.4	—	2.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 1mA		—	0.4	—	0.4	V
V_{DD} Power Down Current	I_{DDPS}	V_{DD} = V_{DD} max., V_{IN} = V_{IH} or V_{IL}, CE2 ≤ 0.2V	SLEEP	—	10	—	TBD	µA
	I_{DDP4}		4M Partial	—	40	N/A		µA
	I_{DDP8}		8M Partial	—	50	—	TBD	µA
	I_{DDP16}		16M Partial	N/A		—	TBD	
V_{DD} Standby Current	I_{DDS}	V_{DD} = V_{DD} max., V_{IN} (including CLK)= V_{IH} or V_{IL}, CE1# = CE2 = V_{IH}		—	1.5	—	TBD	mA
	I_{DDS1}	V_{DD} = V_{DD} max., V_{IN} (including CLK) ≤ 0.2V or V_{IN} (including CLK) ≥ V_{DD} – 0.2V, CE1# = CE2 ≥ V_{DD} – 0.2V	TA ≤ +85°C	—	80	—	TBD	µA
			TA ≤ +40°C	—	80	—	TBD	µA
		V_{DD} = V_{DD} max., t_{CK}=min. V_{IN} ≤ 0.2V or V_{IN} ≥ V_{DD} – 0.2V, CE1# = CE2 ≥ V_{DD} – 0.2V		—	200	—	TBD	µA
V_{DD} Active Current	I_{DDA1}	V_{DD} = V_{DD} max., V_{IN} = V_{IH} or V_{IL}, CE1# = V_{IL} and CE2= V_{IH}, I_{OUT}=0mA	t_{RC} / t_{WC} = minimum	—	30	—	35	mA
	I_{DDA2}		t_{RC} / t_{WC} = 1µs	—	3	—	5	mA
V_{DD} Page Read Current	I_{DDA3}	V_{DD} = V_{DD} max., V_{IN} = V_{IH} or V_{IL}, CE1# = V_{IL} and CE2= V_{IH}, I_{OUT}=0mA, t_{PRC} = min.		—	10	—	TBD	mA
V_{DD} Burst Access Current	I_{DDA4}	V_{DD} = V_{DD} max., V_{IN} = V_{IH} or V_{IL}, CE1# = V_{IL} and CE2= V_{IH}, t_{CK} = t_{CK} min., BL = Continuous, I_{OUT}=0mA		—	15	—	TBD	mA

Notes:

1. *All voltages are referenced to V_{SS}.*
2. *DC Characteristics are measured after following POWER-UP timing.*
3. *I_{OUT} depends on the output load conditions.*

AC Characteristics

(Under Recommended Operating Conditions Unless Otherwise Noted)

Read Operation

Parameter	Symbol	32M		64M		Unit	Notes
		Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	70	1000	70	1000	ns	1, 2
CE1# Access Time	t_{CE}	—	70	—	70	ns	3
OE# Access Time	t_{OE}	—	40	—	40	ns	3
Address Access Time	t_{AA}	—	70	—	70	ns	3, 5
ADV# Access Time	t_{AV}		70		70	ns	3
LB# / UB# Access Time	t_{BA}	—	30	—	30	ns	3
Page Address Access Time	t_{PAA}	—	20	—	20	ns	3,6
Page Read Cycle Time	t_{PRC}	20	1000	20	1000	ns	1, 6, 7
Output Data Hold Time	t_{OH}	5	—	5	—	ns	3
CE1# Low to Output Low-Z	t_{CLZ}	5	—	5	—	ns	4
OE# Low to Output Low-Z	t_{OLZ}	10	—	0	—	ns	4
LB# / UB# Low to Output Low-Z	t_{BLZ}	0	—	0	—	ns	4
CE1# High to Output High-Z	t_{CHZ}	—	20	—	20	ns	3
OE# High to Output High-Z	t_{OHZ}	—	20	—	20	ns	3
LB# / UB# High to Output High-Z	t_{BHZ}	—	20	—	20	ns	3
Address Setup Time to CE1# Low	t_{ASC}	–5	—	–5	—	ns	
Address Setup Time to OE# Low	t_{ASO}	10	—	10	—	ns	
ADV# Low Pulse Width	t_{VPL}	10	—	10	—	ns	8
ADV# High Pulse Width	t_{VPH}	15	—	15	—	ns	8
Address Setup Time to ADV High	t_{ASV}	5	—	5	—	ns	
Address Hold Time from ADV# High	t_{AHV}	10	—	5	—	ns	
Address Invalid Time	t_{AX}	—	10	—	10	ns	5, 9
Address Hold Time from CE1# High	t_{CHAH}	–5	—	–5	—	ns	10
Address Hold Time from OE# High	t_{OHAH}	–5	—	–5	—	ns	10
WE# High to OE# Low Time for Read	t_{WHOL}	15	1000	25	1000	ns	11
CE1# High Pulse Width	t_{CP}	15	—	15	—	ns	

Notes:

1. *Maximum value is applicable if CE#1 is kept at Low without change of address input of A3 to A21.*
2. *Address should not be changed within minimum t_{RC}.*
3. *The output load 50pF with 50ohm termination to V_{DD}*0.5 V.*

4. *The output load 5pF without any other load.*
5. *Applicable to A3 to A21 when CE1# is kept at Low.*
6. *Applicable only to A0, A1 and A2 when CE1# is kept at Low for the page address access.*
7. *In case Page Read Cycle is continued with keeping CE1# stays Low, CE1# must be brought to High within 4µs. In other words, Page Read Cycle must be closed within 4µs.*
8. *t_{VPL} is specified from the negative edge of either CE1# or ADV# whichever comes late. The sum of t_{VPL} and t_{VPH} must be equal or greater than tRC for each access.*
9. *Applicable to address access when at least two of address inputs are switched from previous state.*
10. *t_{RC}(min) and t_{PRC}(min) must be satisfied.*
11. *If actual value of t_{WHOL} is shorter than specified minimum values, the actual t_{AA} of following Read may become longer by the amount of subtracting actual value from specified minimum value.*

Write Operation

Parameter	Symbol	32M		64M		Unit	Notes
		Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	70	1000	70	1000	ns	1, 2
Address Setup Time	t_{AS}	0	—	0	—	ns	3
ADV# Low Pulse Width	t_{VPL}	10	—	10	—	ns	4
ADV# High Pulse Width	t_{VPH}	15	—	15	—	ns	
Address Setup Time to ADV# High	t_{ASV}	5	—	5	—	ns	
Address Hold Time from ADV# High	t_{AHV}	10	—	5	—	ns	
CE1# Write Pulse Width	t_{CW}	45	—	45	—	ns	3
WE# Write Pulse Width	t_{WP}	45	—	45	—	ns	3
LB# / UB# Write Pulse Width	t_{BW}	45	—	45	—	ns	3
LB# / UB# Byte Mask Setup Time	t_{BS}	-5	—	-5	—	ns	5
LB# / UB# Byte Mask Hold Time	t_{BH}	-5	—	-5	—	ns	6
CE1# Write Recovery Time	t_{WRC}	15	—	15	—	ns	7
Write Recovery Time	t_{WR}	15	1000	15	1000	ns	7
CE1# High Pulse Width	t_{CP}	15	—	15	—	ns	
WE# High Pulse Width	t_{WHP}	15	1000	15	1000	ns	
LB# / UB# High Pulse Width	t_{BHP}	15	1000	15	1000	ns	
Data Setup Time	t_{DS}	15	—	15	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	ns	
OE# High to CE1# Low Setup Time for Write	t_{OHCL}	-5	—	-5	—	ns	8
OE# High to Address Setup Time for Write	t_{OES}	0	—	0	—	ns	9
LB# / UB# Write Pulse Overlap	t_{BWO}	30	—	30	—	ns	

Notes:

1. *Maximum value is applicable if CE1# is kept at Low without any address change.*
2. *Minimum value must be equal or greater than the sum of write pulse (t_{CW}, t_{WP} or t_{BW}) and write recovery time (t_{WR}).*
3. *Write pulse is defined from High to Low transition of CE1#, WE#, or LB# / UB#, whichever occurs last.*
4. *t_{VPL} is specified from the negative edge of either CE#1 or ADV# whichever comes late. The sum of t_{VPL} and t_{VPH} must be equal or greater than t_{WC} for each access.*
5. *Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of CE1# or WE# whichever occurs last.*
6. *Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of CE1# or WE# whichever occurs first.*
7. *Write recovery is defined from Low to High transition of CE1#, WE#, or LB# / UB#, whichever occurs first.*
8. *If OE# is Low after minimum t_{OHCL}, read cycle is initiated. In other words, OE# must be brought to High within 5ns after CE1# is brought to Low. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.*
9. *If OE# is Low after new address input, read cycle is initiated. In other word, OE# must be brought to High at the same time or before new address valid. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met and data bus is in High-Z.*

Synchronous Operation - Clock Input (Burst Mode)

Parameter		Symbol	32M		64M		Unit	Notes
			Min.	Max.	Min.	Max.		
Clock Period	RL = 6	t_{CK}	N/A		13	—	ns	1
	RL = 5		15	—	15	—	ns	
	RL = 4		20	—	18	—	ns	
	RL = 3		30	—	30		ns	
Clock High Time		t_{CKH}	5	—	4	—	ns	
Clock Low Time		t_{CKL}	5	—	4	—	ns	
Clock Rise/Fall Time		t_{CKT}	—	3	—	3	ns	2

Notes:

1. *Clock period is defined between valid clock edges.*
2. *Clock rise/fall time is defined between V_{IH} Min. and V_{IL} Max.*

Synchronous Operation - Address Latch (Burst Mode)

Parameter		Symbol	32M		64M		Unit	Notes
			Min.	Max.	Min.	Max.		
Address Setup Time to ADV# Low		t_{ASVL}	-5	—	-5	—	ns	1
Address Setup Time to CE1# Low		t_{ASCL}	-5	—	-5	—	ns	2
Address Hold Time from ADV# High		t_{AHV}	10	—	5	—	ns	
ADV# Low Pulse Width		t_{VPL}	10	—	10	—	ns	3
ADV# Low Setup Time to CLK	RL = 6, 5	t_{VSCK}	7	—	5	—	ns	4
	RL = 4, 3			—	7	—	ns	4
CE1 Low Setup Time to CLK	RL = 6, 5	t_{CLCK}	7	—	5	—	ns	4
	RL = 4, 3			—	7	—	ns	4
ADV# Low Hold Time from CLK		t_{CKVH}	1	—	1	—	ns	4
Burst End ADV# High Hold Time from CLK		t_{VHVL}	15	—	13	—	ns	

Notes:

1. *t_{ASCL} is applicable if CE1# is brought to Low after ADV# is brought to Low.*
2. *t_{ASVL} is applicable if ADV# is brought to Low after CE1# is brought to Low.*
3. *t_{VPL} is specified from the negative edge of either CE1# or ADV# whichever comes late.*
4. *Applicable to the 1st valid clock edge.*

Synchronous Read Operation (Burst Mode)

Parameter		Symbol	32M		64M		Unit	Notes
			Min.	Max.	Min.	Max.		
Burst Read Cycle Time		t_{RCB}	—	8000	—	4000	ns	
CLK Access Time	RL = 6, 5	t_{AC}	—	12	—	10	ns	1
	RL = 4, 3				—	12	ns	1
Output Hold Time from CLK		t_{CKQX}	3	—	3	—	ns	1
CE1# Low to WAIT# Low		t_{CLTL}	5	20	5	20	ns	1
OE# Low to WAIT# Low		t_{OLTL}	0	20	0	20	ns	1, 2
ADV# Low to WAIT# Low		t_{VLTL}	N/A		0	20	ns	1
CLK to WAIT# Valid Time		t_{CKTV}	—	12	—	10	ns	1, 3
WAIT# Valid Hold Time from CLK		t_{CKTX}	3	—	3	—	ns	1
CE1# Low to Output Low-Z		t_{CLZ}	5	—	5	—	ns	4
OE# Low to Output Low-Z		t_{OLZ}	10	—	10	—	ns	4
LB#, UB# Low to Output Low-Z		t_{BLZ}	0	—	0	—	ns	4
CE1# High to Output High-Z		t_{CHZ}	—	14	—	20	ns	1
OE# High to Output High-Z		t_{OHZ}	—	14	—	20	ns	1
LB#, UB# High to Output High-Z		t_{BHZ}	—	14	—	20	ns	1
CE1# High to WAIT High-Z		t_{CHTZ}	—	20	—	20	ns	1
OE# High to WAIT High-Z		t_{OHTZ}	—	20	—	20	ns	1
OE# Low Setup Time to 1st Data-out		t_{OLQ}	30	—	30	—	ns	
UB#, LB# Setup Time to 1st Data-out		t_{BLQ}	30	—	26	—	ns	5
OE# Setup Time to CLK		t_{OSCK}	5	—	5	—	ns	
OE# Hold Time from CLK		t_{CKOH}	5	—	5	—	ns	
Burst End CE1# Low Hold Time from CLK		t_{CKCLH}	5	—	5	—	ns	
Burst End UB#, LB# Hold Time from CLK		t_{CKBH}	5	—	5	—	ns	
Burst Terminate Recovery Time	BL=8, 16	t_{TRB}	30	—	26	—	ns	6
	BL=Continuous		70	—	70	—	ns	6

Notes:

1. *The output load 50pF with 50ohm termination to V_{DD}*0.5 V.*
2. *WAIT# drives High at the beginning depending on OE# falling edge timing.*
3. *t_{CKTV} is guaranteed after t_{OLTL} (max) from OE# falling edge and t_{OSCK} must be satisfied.*
4. *The output load is 5pF without any other load.*
5. *Once they are determined, they must not be changed until the end of burst.*
6. *Defined from the Low to High transition of CE1# to the High to Low transition of either ADV# or CE1# whichever occurs late.*

Synchronous Write Operation (Burst Mode)

Parameter		Symbol	32M		64M		Unit	Notes
			Min.	Max.	Min.	Max.		
Burst Write Cycle Time		t_{WCB}	—	8000	—	4000	ns	
Data Setup Time to Clock		t_{DSCK}	7	—	5	—	ns	
Data Hold Time from CLK		t_{DHCK}	3	—	3	—	ns	
WE# Low Setup Time to 1st Data In		t_{WLD}	30	—	30	—	ns	
UB#, LB# Setup Time for Write		t_{BS}	-5	—	-5	—	ns	1
WE# Setup Time to CLK		t_{WSCK}	5	—	5	—	ns	
WE# Hold Time from CLK		t_{CKWH}	5	—	5	—	ns	
CE1# Low to WAIT# High		t_{CLTH}	5	20	5	20	ns	2
WE# Low to WAIT# High		t_{WLTH}	0	20	0	20	ns	2
CE1# High to WAIT# High-Z		t_{CHTZ}	—	20	—	20	ns	2
WE# High to WAIT# High-Z		t_{WHTZ}	—	20	—	20	ns	2
Burst End CE1# Low Hold Time from CLK		t_{CKCLH}	5	—	5	—	ns	
Burst End CE1# High Setup Time to next CLK		t_{CHCK}	5	—	5	—	ns	
Burst End UB#, LB# Hold Time from CLK		t_{CKBH}	5	—	5	—	ns	
Burst Write Recovery Time		t_{WRB}	30		26		ns	
Burst Terminate Recovery Time	BL=8, 16	t_{TRB}	30	—	26	—	ns	3
	BL=Continuous	t_{TRB}	70	—	70	—	ns	4

Notes:

1. *Defined from the valid input edge to the High to Low transition of either ADV#, CE1#, or WE#, whichever occurs last. And once they are determined, they must not be changed until the end of burst.*
2. *The output load 50pF with 50ohm termination to V_{DD}*0.5 V.*
3. *Defined from the valid clock edge where last data-in being latched at the end of burst write to the High to Low transition of either ADV# or CE1# whichever occurs late for the next access.*
4. *Defined from the Low to High transition of CE1# to the High to Low transition of either ADV# or CE1# whichever occurs late for the next access.*

Power Down Parameters

Parameter	Symbol	32M		64M		Unit	Notes
		Min.	Max.	Min.	Max.		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	20	—	10	—	ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	70	—	70	—	ns	
CE2 Low Hold Time for Reset to Asynchronous Mode	t_{C2LPR}	N/A		50	—	µs	1
CE1# High Hold Time following CE2 High after Power Down Exit [SLEEP mode only]	t_{CHH}	300	—	300	—	µs	2
CE1# High Hold Time following CE2 High after Power Down Exit [not in SLEEP mode]	t_{CHHP}	70	—	70	—	µs	3
CE1# High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0	—	0	—	ns	2

Notes:

1. *Applicable when RP=0 (Reset to Page mode). RP (Reset to Page) mode is available only for 64M.*
2. *Applicable also to power-up.*
3. *Applicable when Partial mode is set.*

Other Timing Parameters

Parameter	Symbol	32M		64M		Unit	Notes
		Min.	Max.	Min.	Max.		
CE1 High to OE Invalid Time for Standby Entry	t_{CHOX}	10	—	10	—	ns	
CE1 High to WE Invalid Time for Standby Entry	t_{CHWX}	10	—	10	—	ns	1
CE2 Low Hold Time after Power-up	t_{C2LH}	50	—	50	—	µs	
CE1 High Hold Time following CE2 High after Power-up	t_{CHH}	300	—	300	—	µs	
Input Transition Time	t_T	1	25	1	25	ns	2

Notes:

1. *Some data might be written into any address location if t_{CHWX}(min) is not satisfied.*
2. *Except for clock input transition time.*
3. *The Input Transition Time (t_T) at AC testing is 5ns for Asynchronous operation and 3ns for Synchronous operation respectively. If actual t_T is longer than 5ns or 3ns specified as AC test condition, it may violate AC specification of some timing parameters. See the "AC Test Conditions" section*

AC Test Conditions

Symbol	Description		Test Setup	Value	Unit	Note
V_{IH}	Input High Level			V_{DD} * 0.8	V	
V_{IL}	Input Low Level			V_{DD} * 0.2	V	
V_{REF}	Input Timing Measurement Level			V_{DD} * 0.5	V	
t_T	Input Transition Time	Async.	Between V_{IL} and V_{IH}	5	ns	
		Sync.		3	ns	

AC Measurement Output Load Circuit

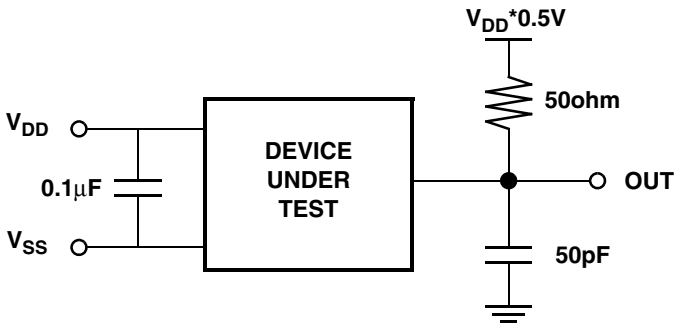


Figure 49. Output Load Circuit

Timing Diagrams

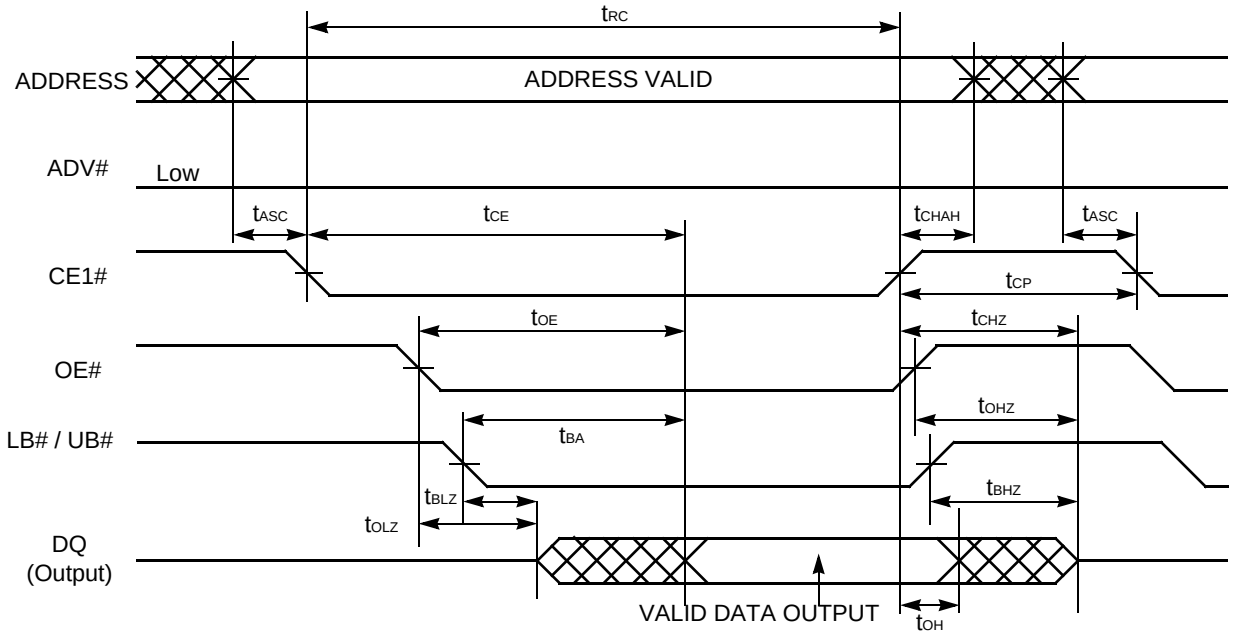


Figure 50. Asynchronous Read Timing #I-I (Basic Timing)

Note: *This timing diagram assumes CE2=H and WE#=H.*

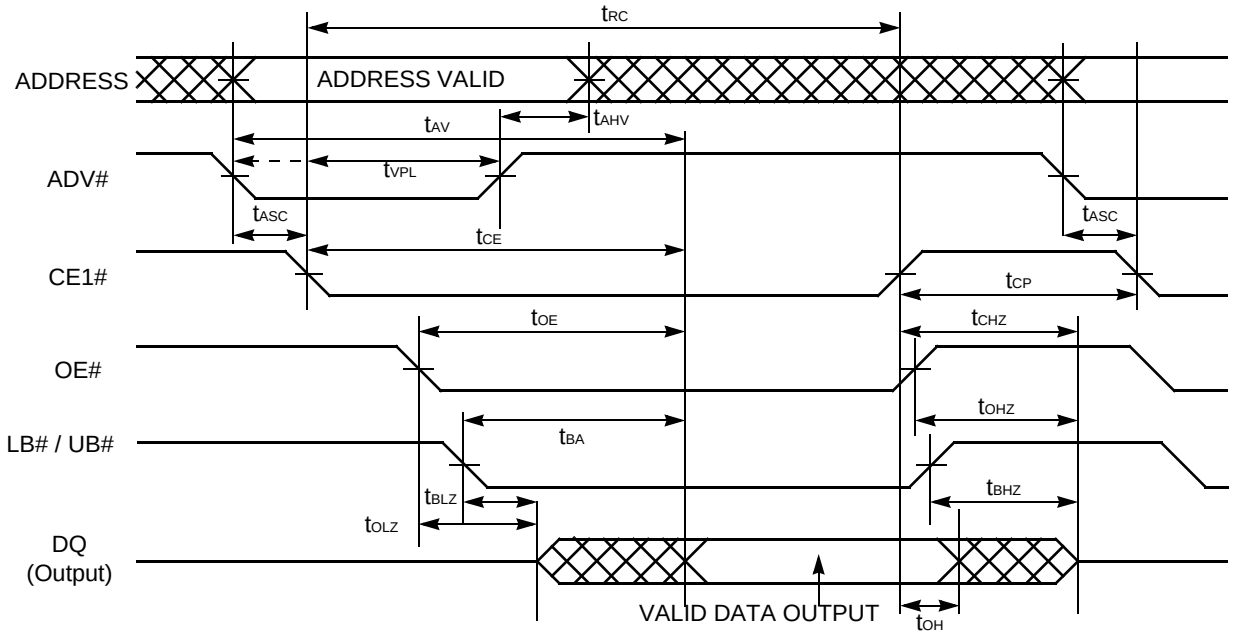


Figure 5I. Asynchronous Read Timing #I-2 (Basic Timing)

Note: *This timing diagram assumes CE2=H and WE#=H.*

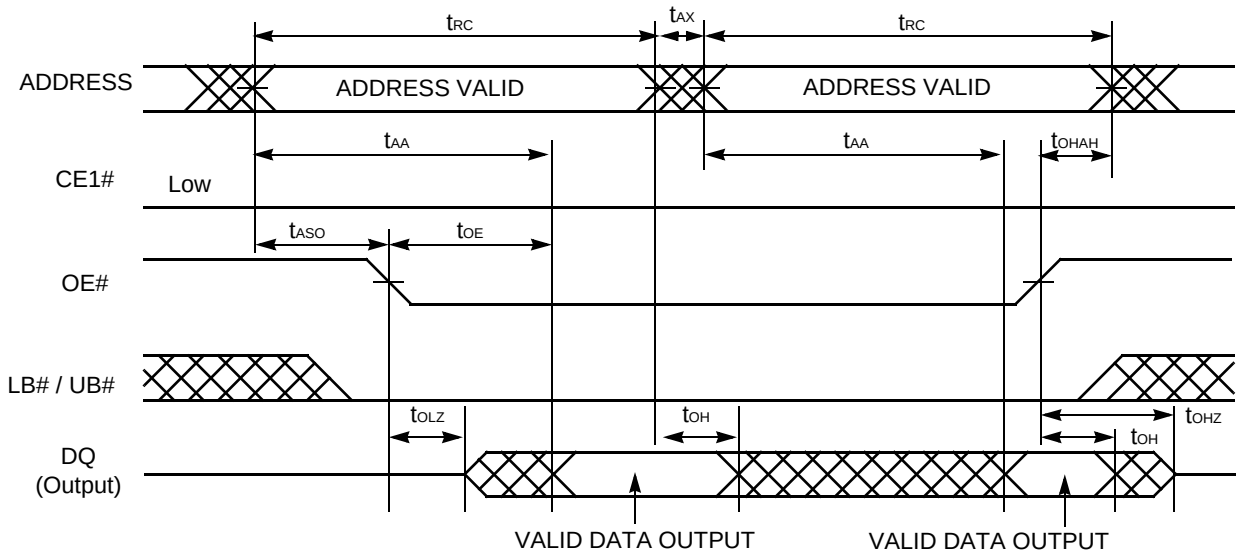


Figure 52. Asynchronous Read Timing #2 (OE# & Address Access)

Note: *This timing diagram assumes CE2=H, ADV#=L and WE#=H.*

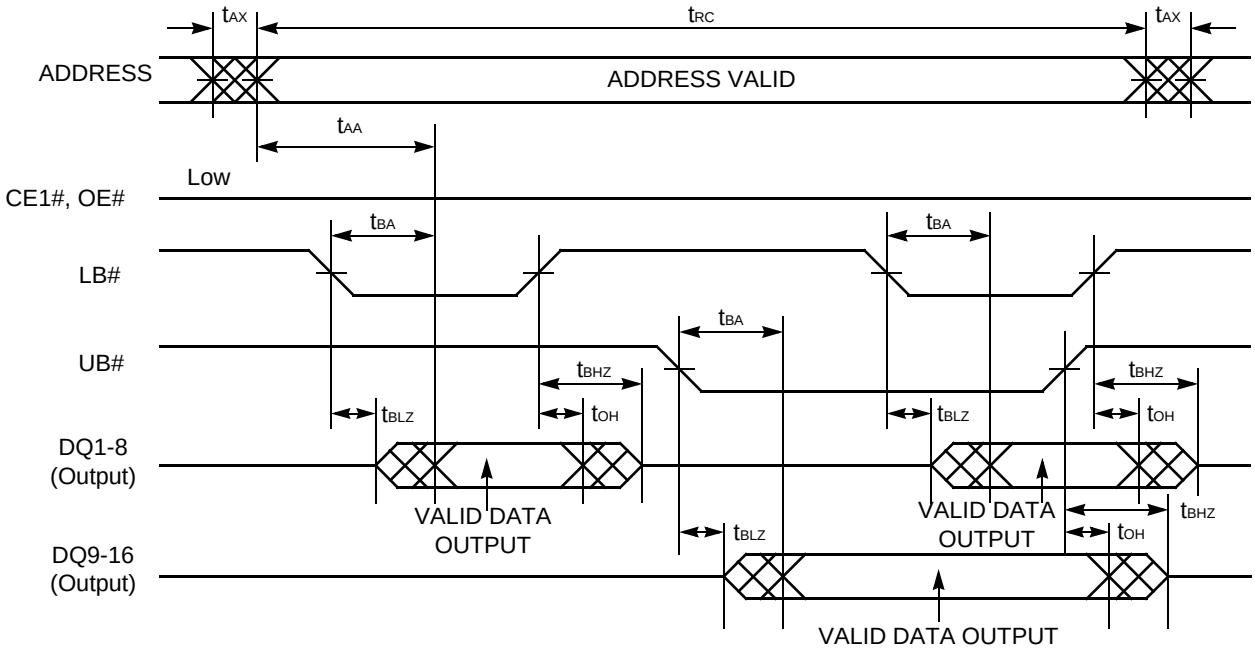


Figure 53. Asynchronous Read Timing #3 (LB# / UB# Byte Access)

Note: *This timing diagram assumes CE2=H, ADV#=L and WE#=H.*

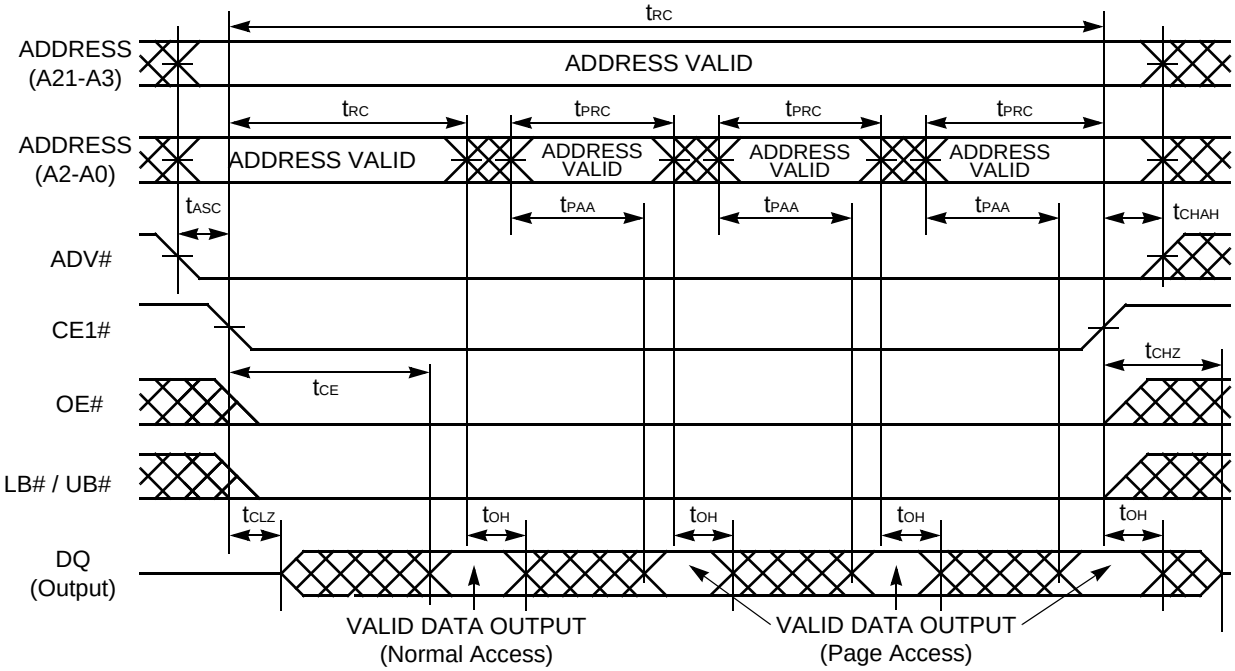


Figure 54. Asynchronous Read Timing #4 (Page Address Access after CEI# Control Access)

Note: *This timing diagram assumes CE2=H and WE#=H.*

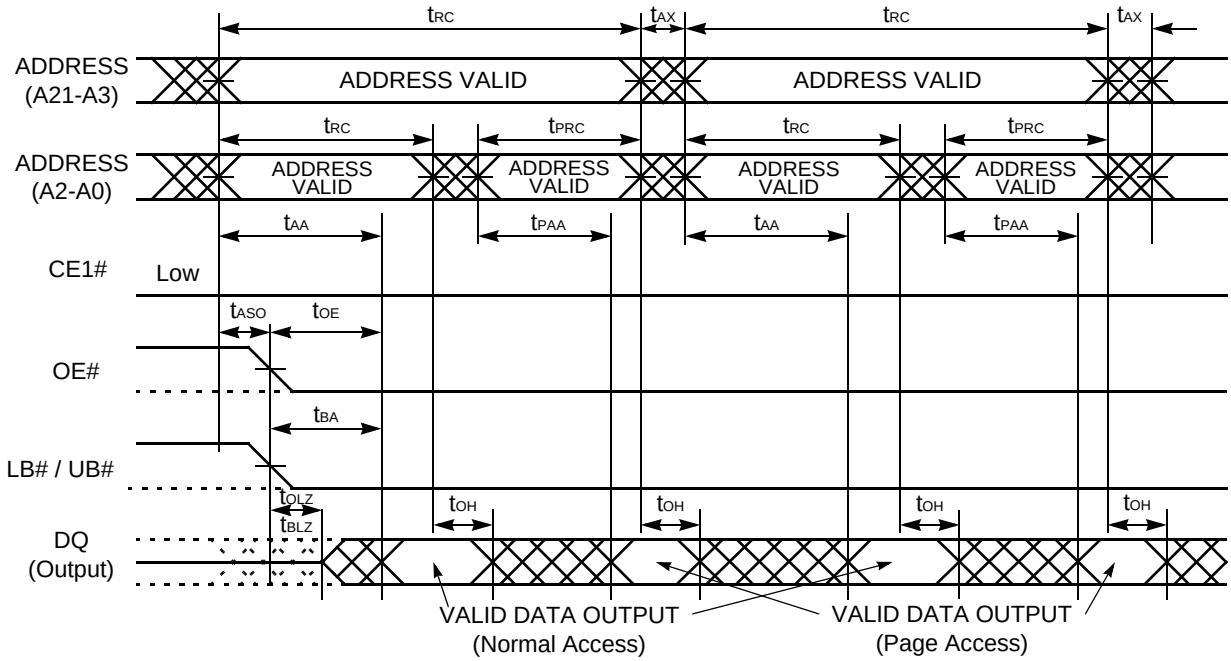


Figure 55. Asynchronous Read Timing #5 (Random and Page Address Access)

Notes:

1. *This timing diagram assumes CE2=H, ADV#=L and WE#=H.*
2. *Either or both LB# and UB# must be Low when both CE1# and OE# are Low.*

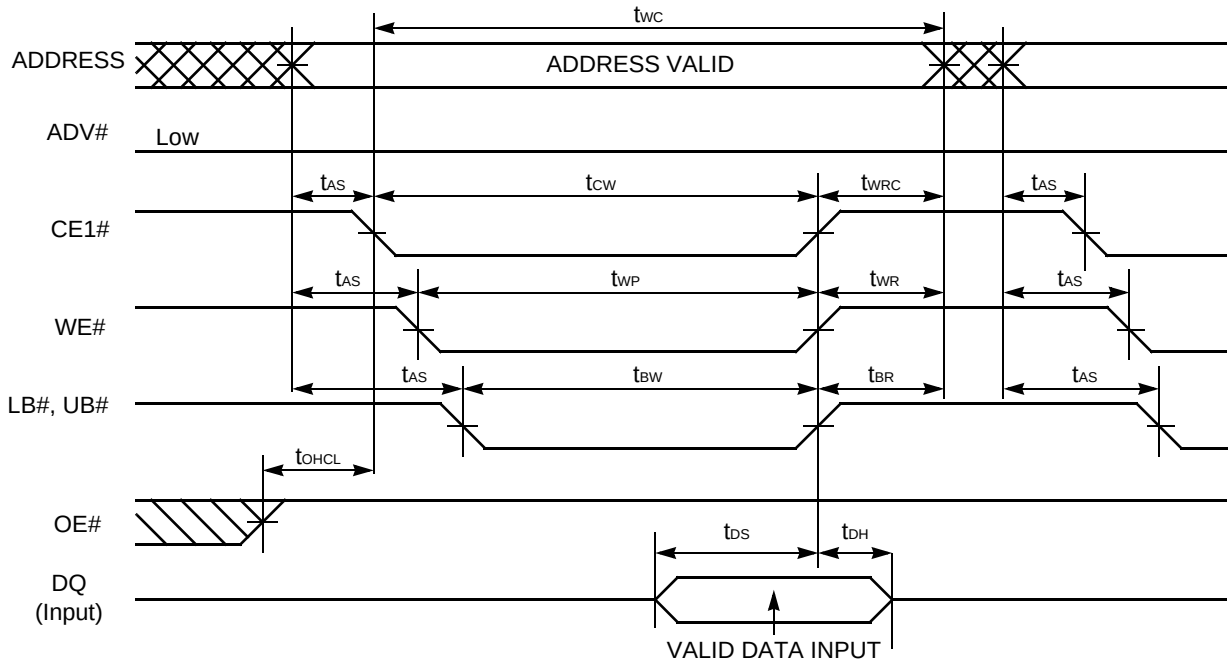


Figure 56. Asynchronous Write Timing #I-I (Basic Timing)

Note: *This timing diagram assumes CE2=H and ADV#=L.*

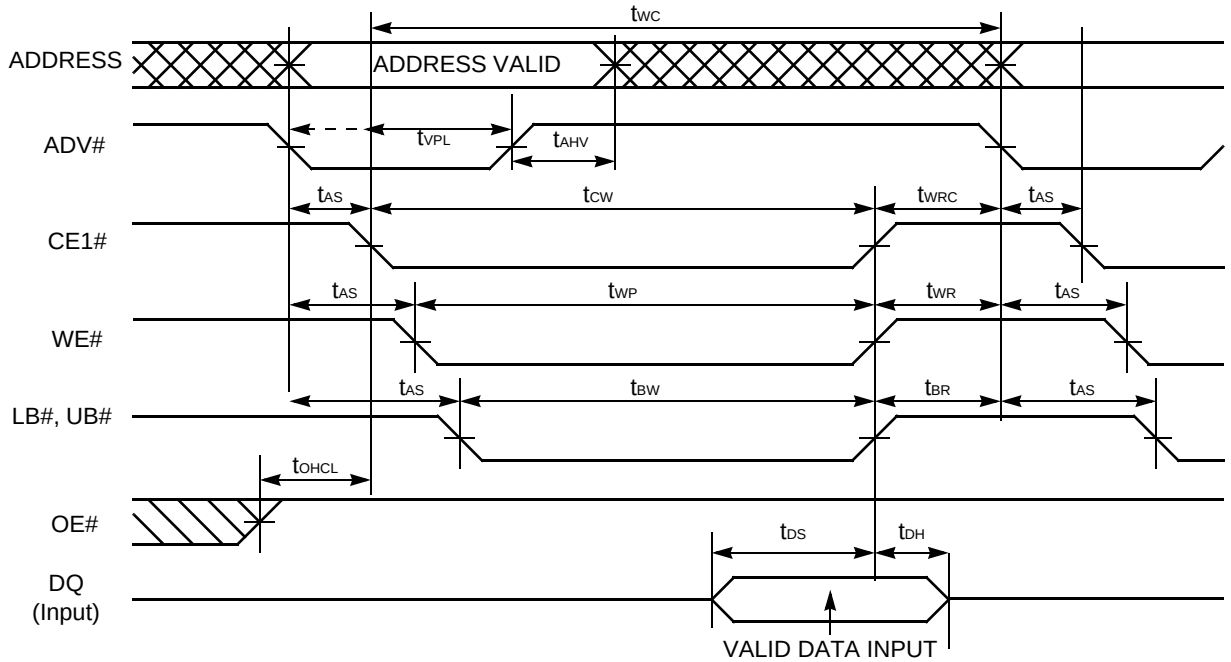


Figure 57. Asynchronous Write Timing #I-2 (Basic Timing)

Note: *This timing diagram assumes CE2=H.*

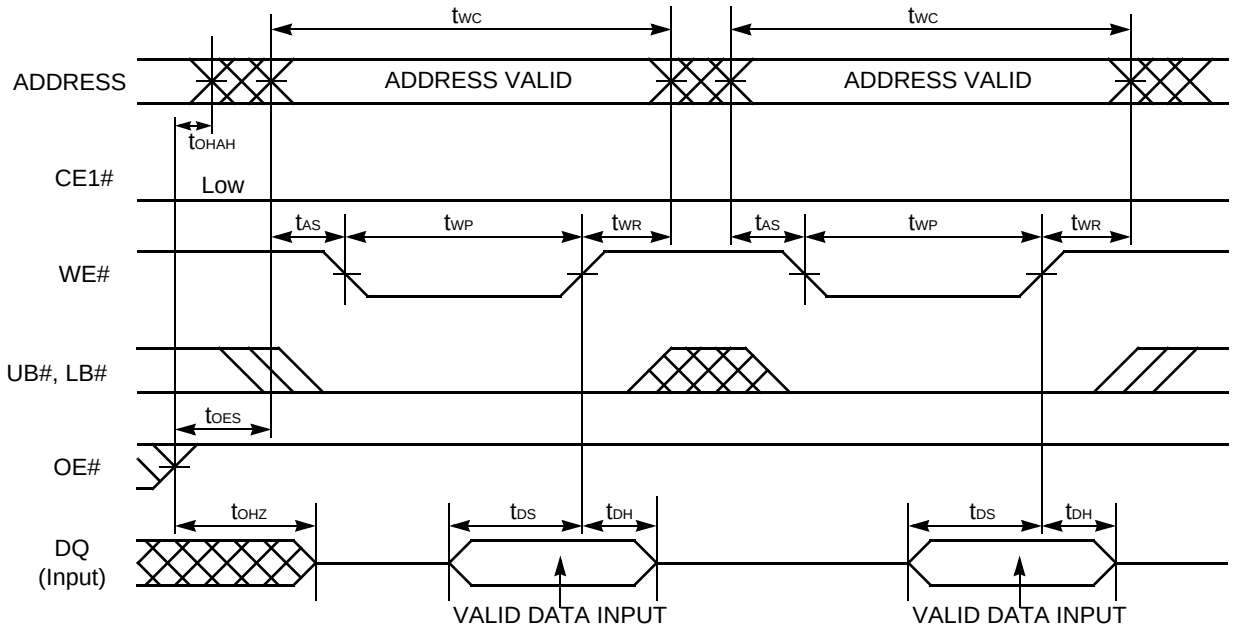


Figure 58. Asynchronous Write Timing #2 (WE# Control)

Note: *This timing diagram assumes CE2=H and ADV#=L.*

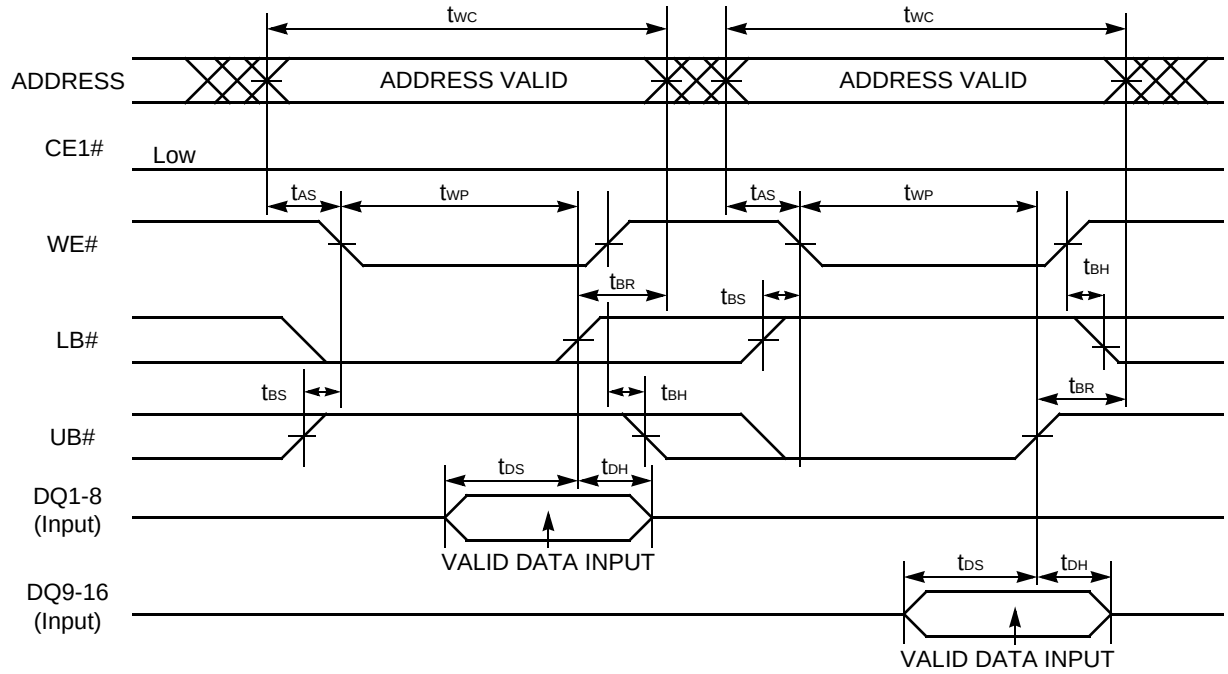


Figure 59. Asynchronous Write Timing #3-1 (WE# / LB# / UB# Byte Write Control)

Note: *This timing diagram assumes CE2=H, ADV#=L and OE#=H.*

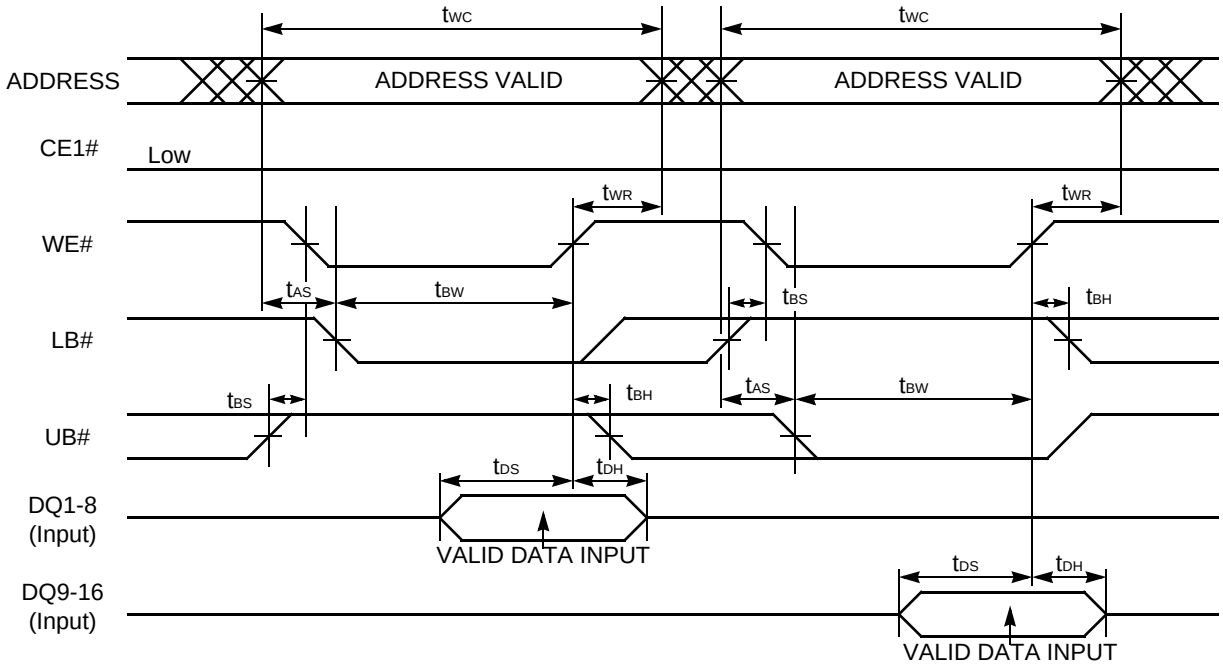


Figure 60. Asynchronous Write Timing #3-2 (WE# / LB# / UB# Byte Write Control)

Note: *This timing diagram assumes CE2=H, ADV#=L and OE#=H.*

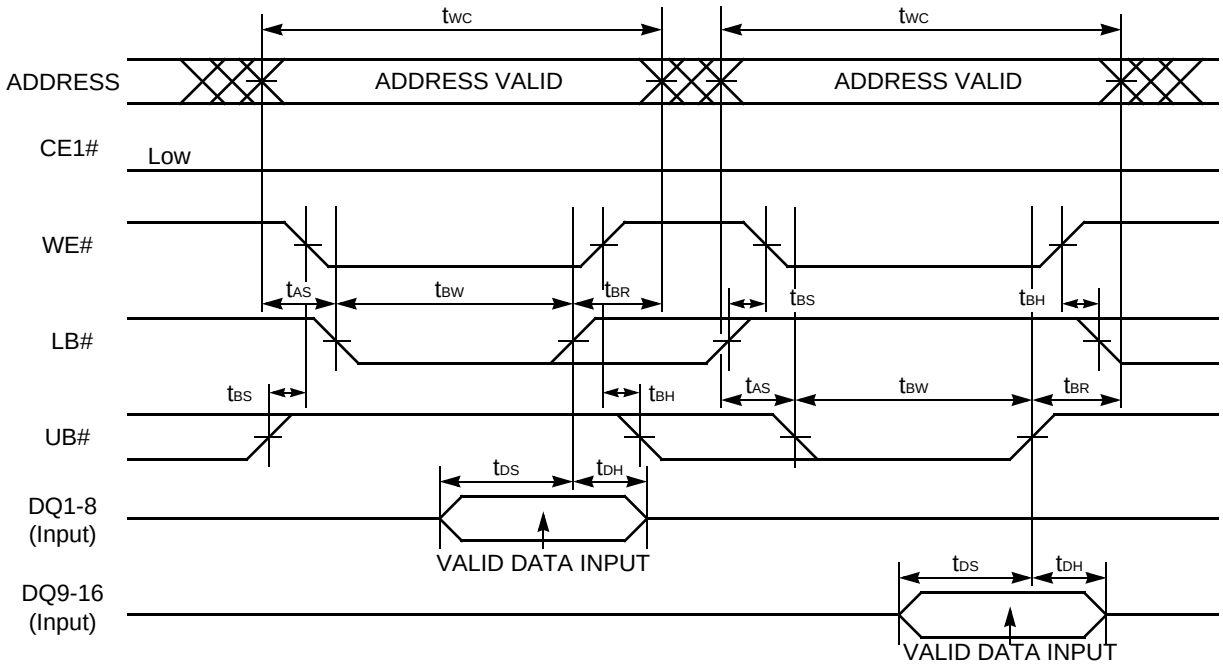


Figure 61. Asynchronous Write Timing #3-3 (WE# / LB# / UB# Byte Write Control)

Note: *This timing diagram assumes CE2=H, ADV#=L and OE#=H.*

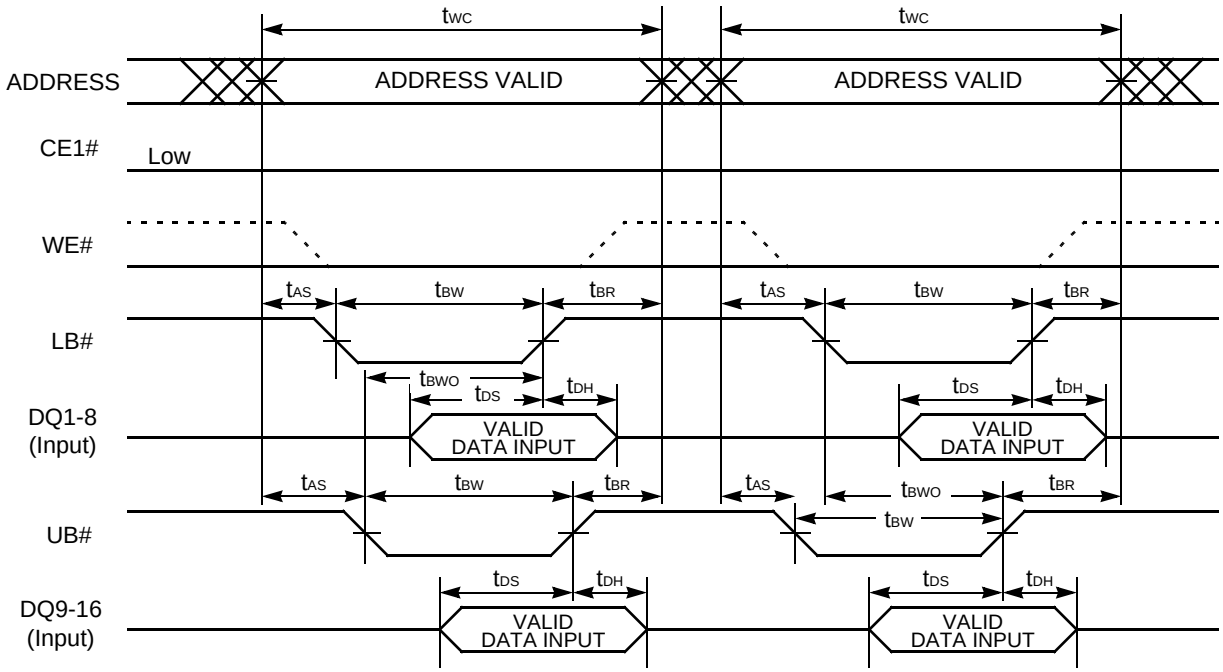


Figure 62. Asynchronous Write Timing #3-4 (WE# / LB# / UB# Byte Write Control)

Note: *This timing diagram assumes CE2=H, ADV#=L and OE#=H.*

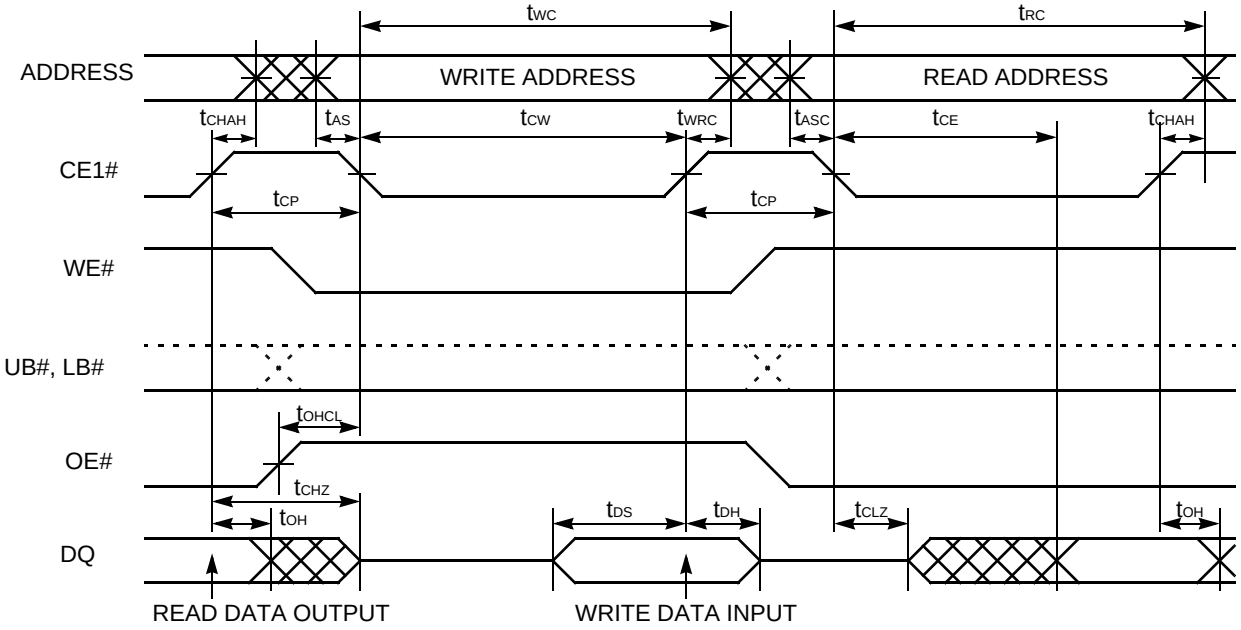


Figure 63. Asynchronous Read / Write Timing #I-I (CEI# Control)

Notes:

1. *This timing diagram assumes CE2=H and ADV#=L.*
2. *Write address is valid from either CE1# or WE# of last falling edge.*

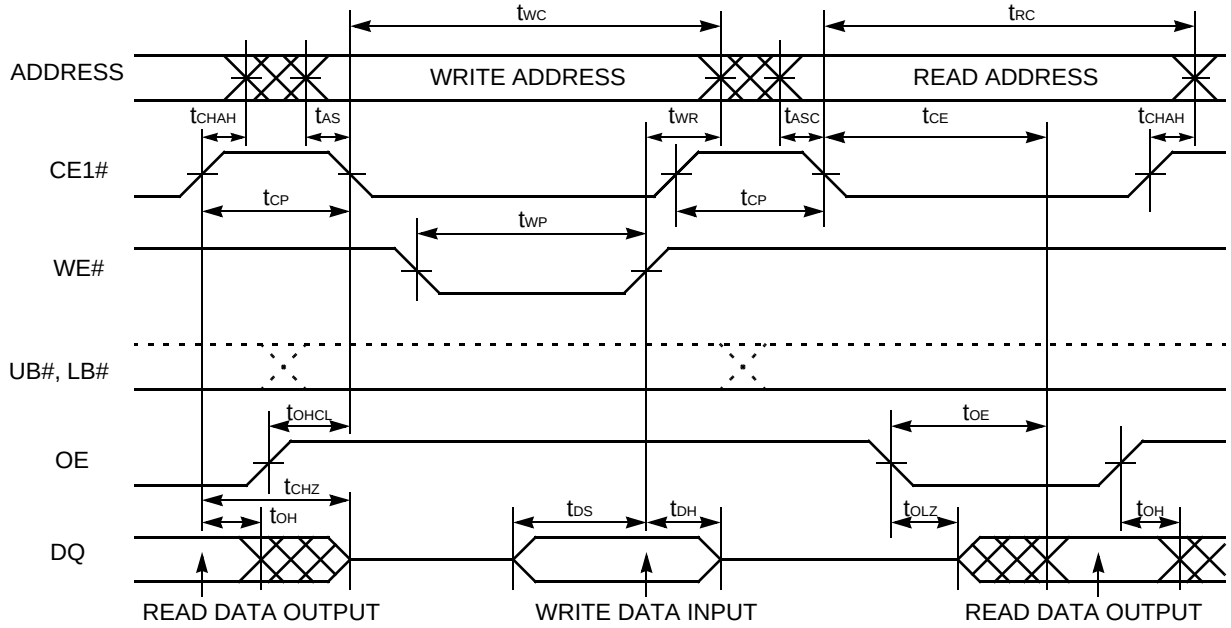


Figure 64. Asynchronous Read / Write Timing #I-2 (CEI# / WE# / OE# Control)

Notes:

1. *This timing diagram assumes CE2=H and ADV#=L.*
2. *OE# can be fixed Low during write operation if it is CE1# controlled write at Read-Write-Read Sequence.*

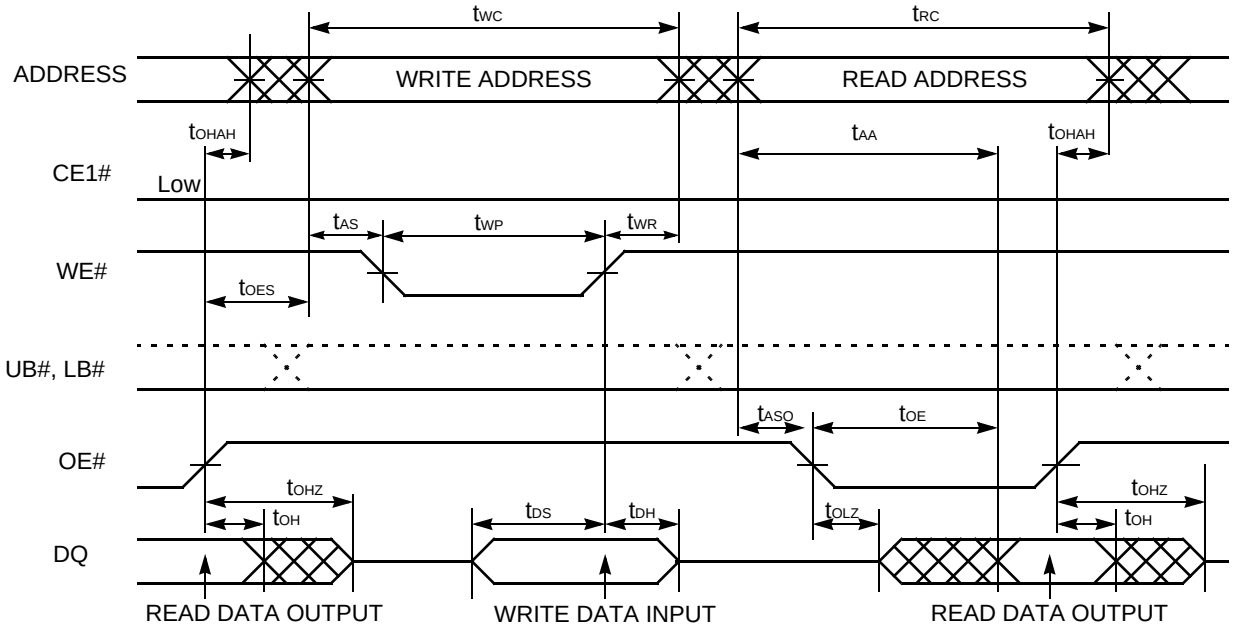


Figure 65. Asynchronous Read / Write Timing #2 (OE#, WE# Control)

Notes:

1. *This timing diagram assumes CE2=H and ADV#=L.*
2. *CE1# can be tied to Low for WE# and OE# controlled operation.*

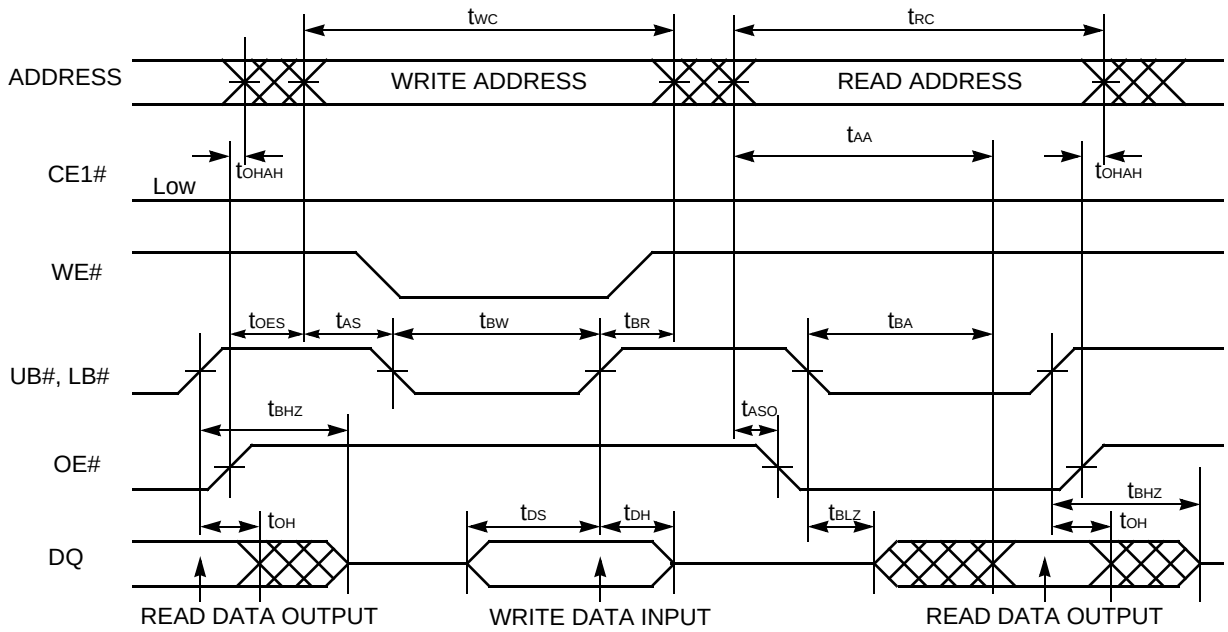


Figure 66. Asynchronous Read / Write Timing #3 (OE,# WE#, LB#, UB# Control)

Notes:

1. *This timing diagram assumes CE2=H and ADV#=L.*
2. *CE1# can be tied to Low for WE# and OE# controlled operation.*

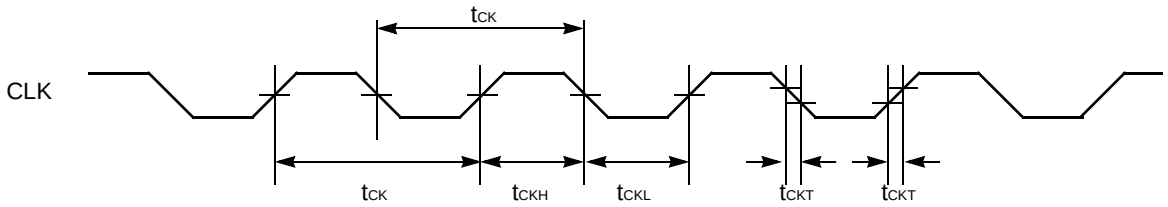


Figure 67. Clock Input Timing

Notes:

1. *Stable clock input must be required during CE1#=L.*
2. *t_{CK} is defined between valid clock edges.*
3. *t_{CKT} is defined between V_{IH} Min. and V_{IL} Max*

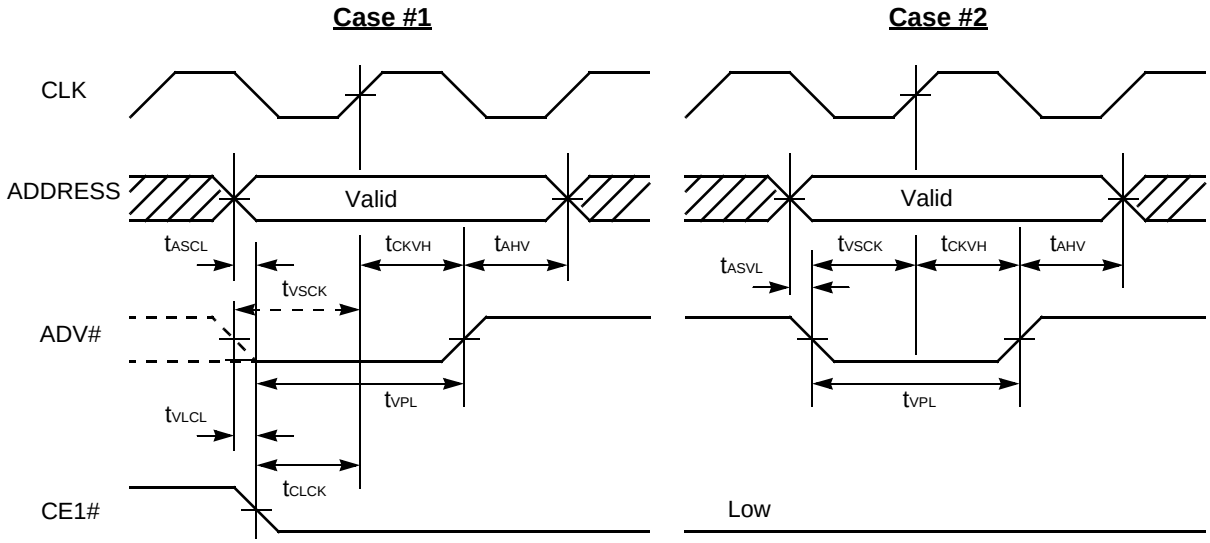


Figure 68. Address Latch Timing (Synchronous Mode)

Notes:

1. *Case #1 is the timing when CE1# is brought to Low after ADV# is brought to Low. Case #2 is the timing when ADV# is brought to Low after CE1# is brought to Low.*
2. *t_{VPL} is specified from the negative edge of either CE1# or ADV# whichever comes late. At least one valid clock edge must be input during ADV#=L.*
3. *t_{VSCK} and t_{CLCK} are applied to the 1st valid clock edge during ADV#=L.*

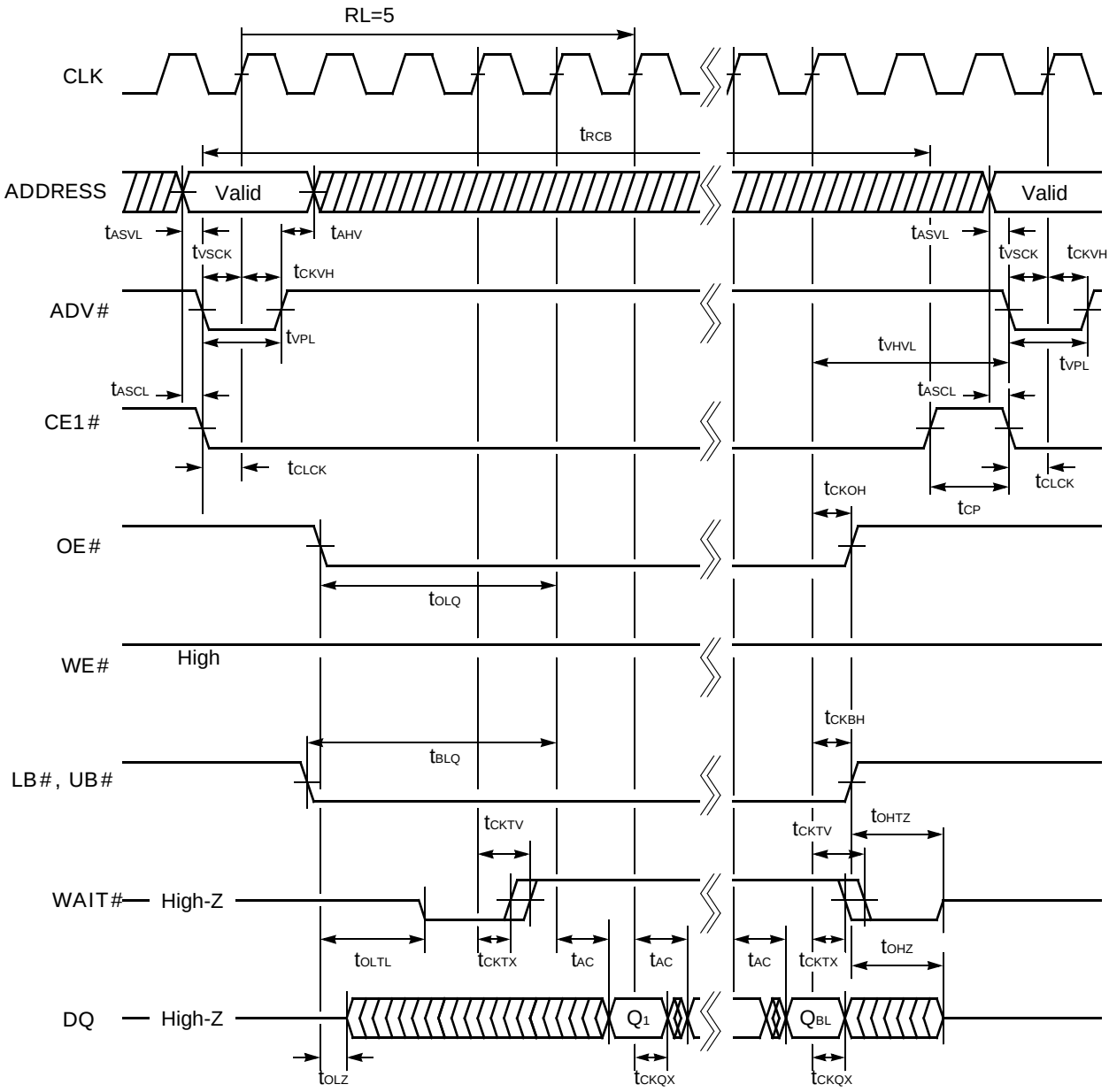


Figure 69. 32M Synchronous Read Timing #I (OE# Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

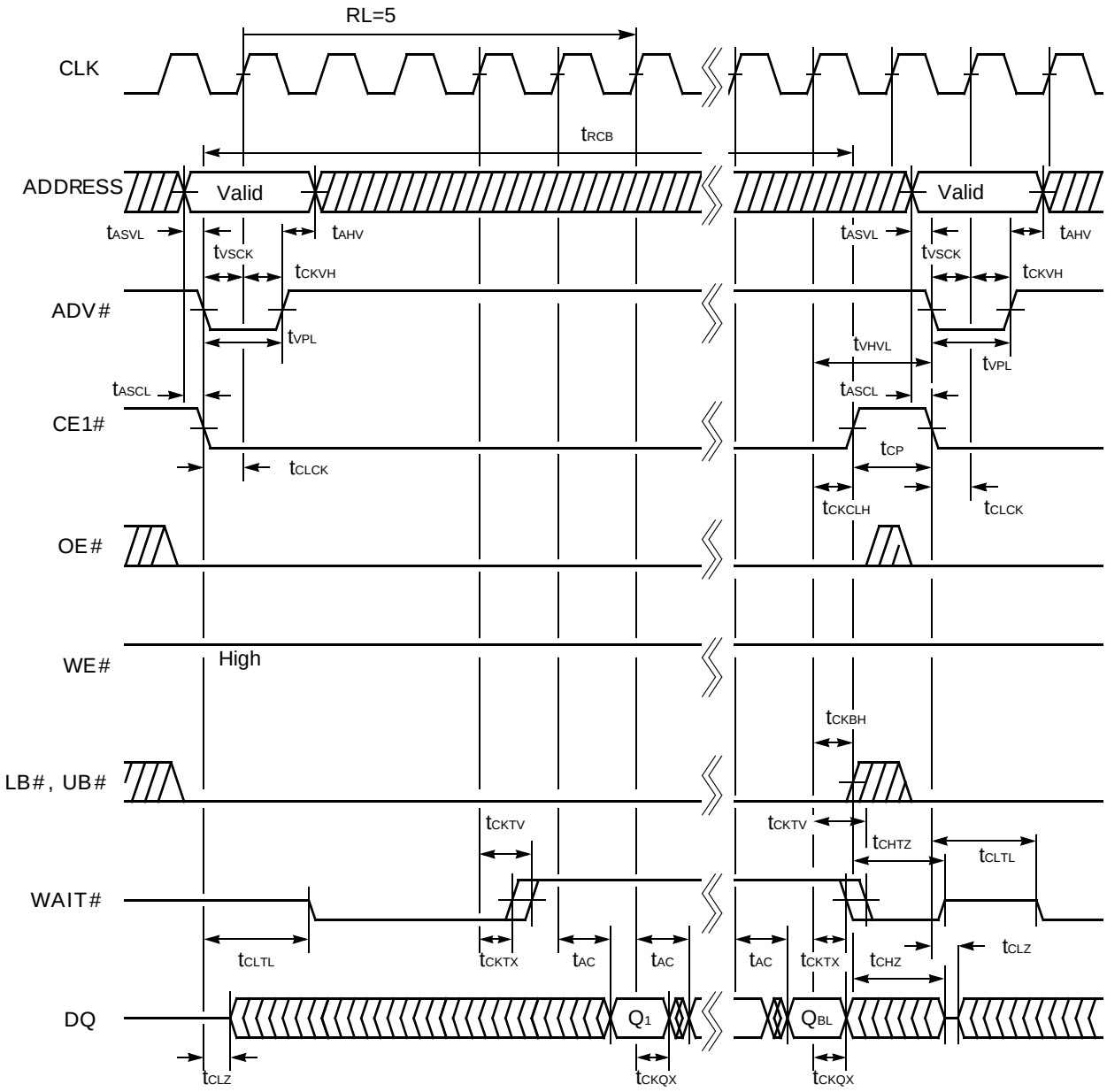


Figure 70. 32M Synchronous Read Timing #2 (CEI# Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

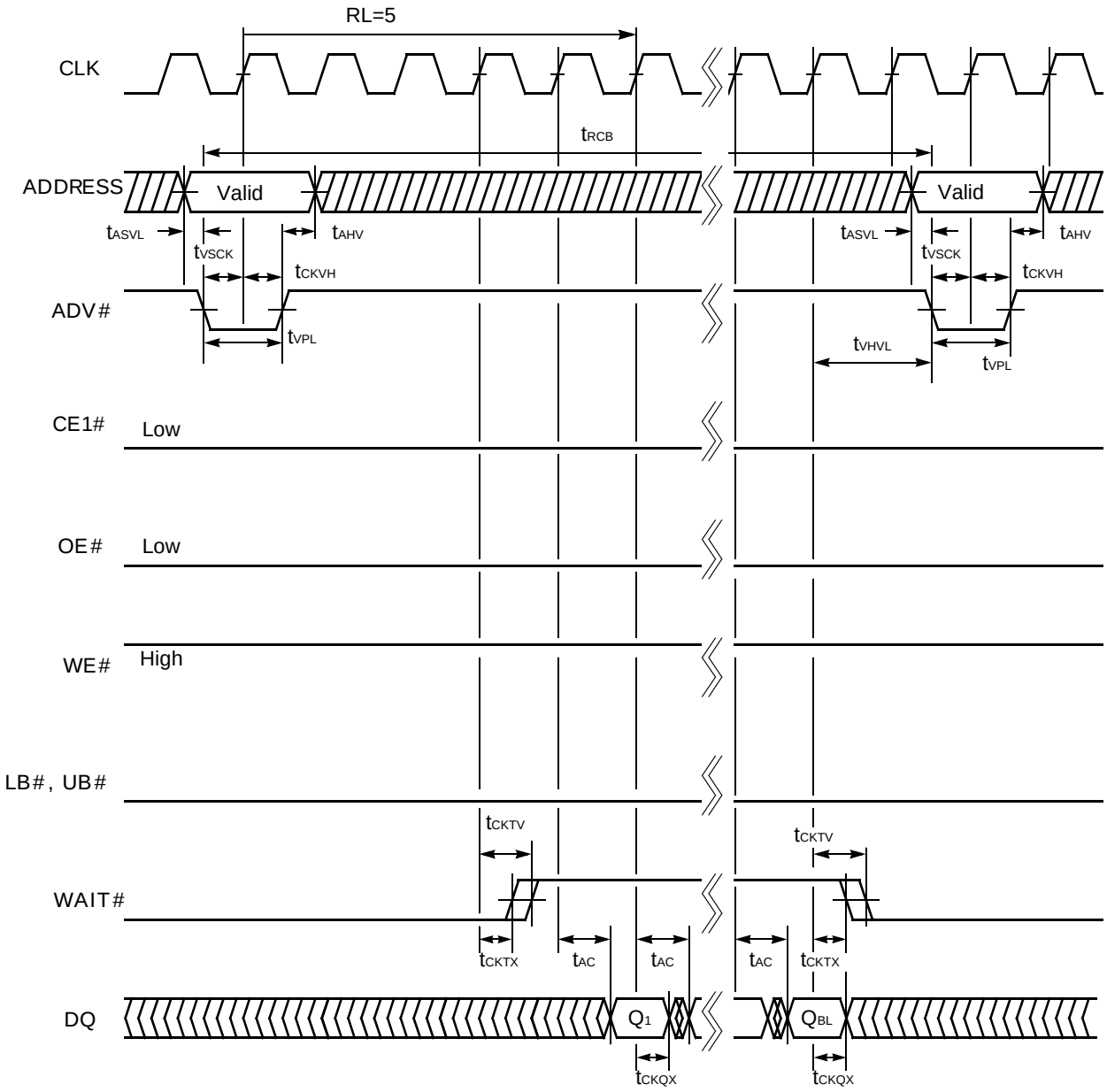


Figure 71. 32M Synchronous Read Timing #3 (ADV# Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

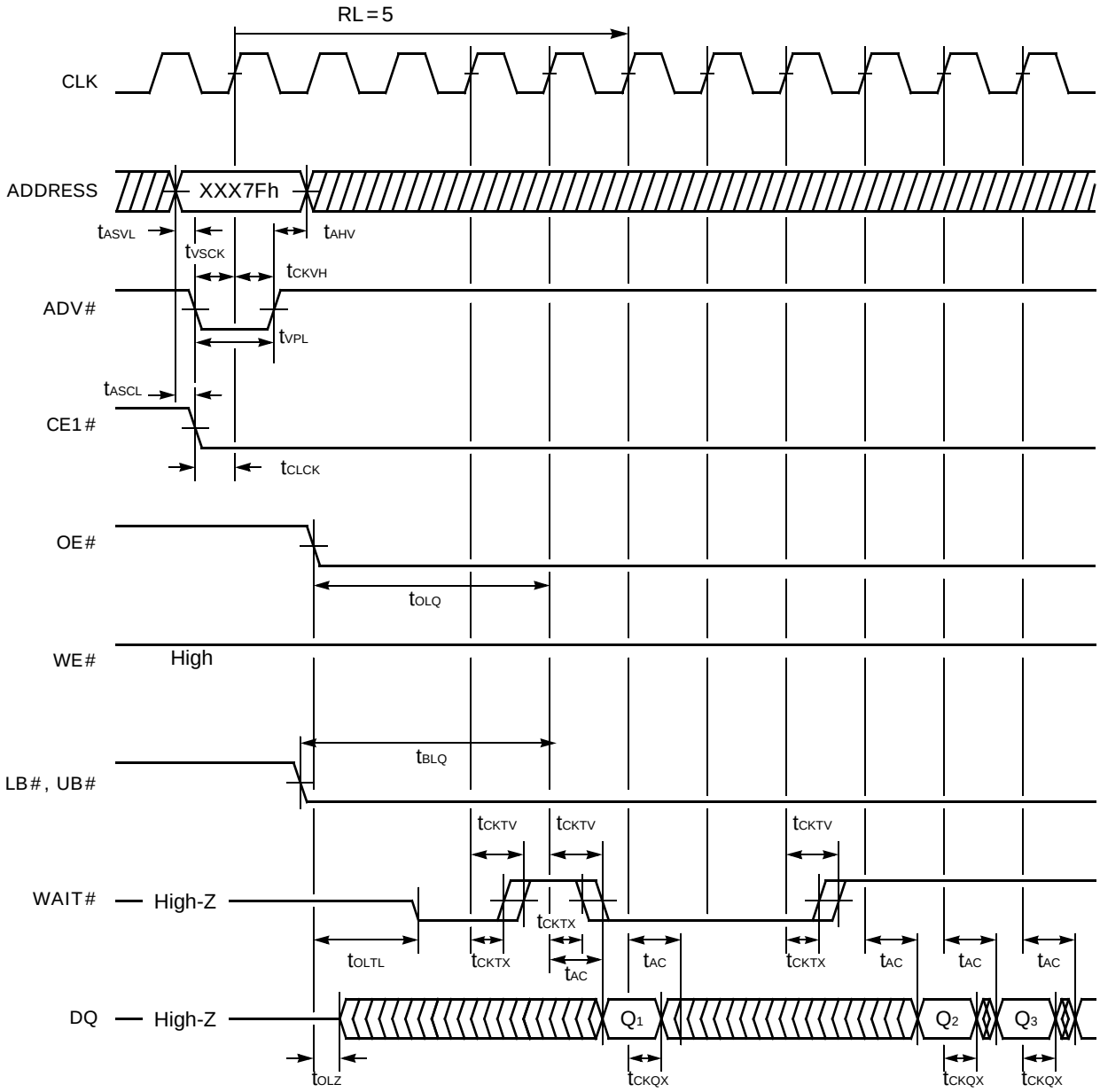


Figure 72. Synchronous Read - WAIT# Output Timing (Continuous Read)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

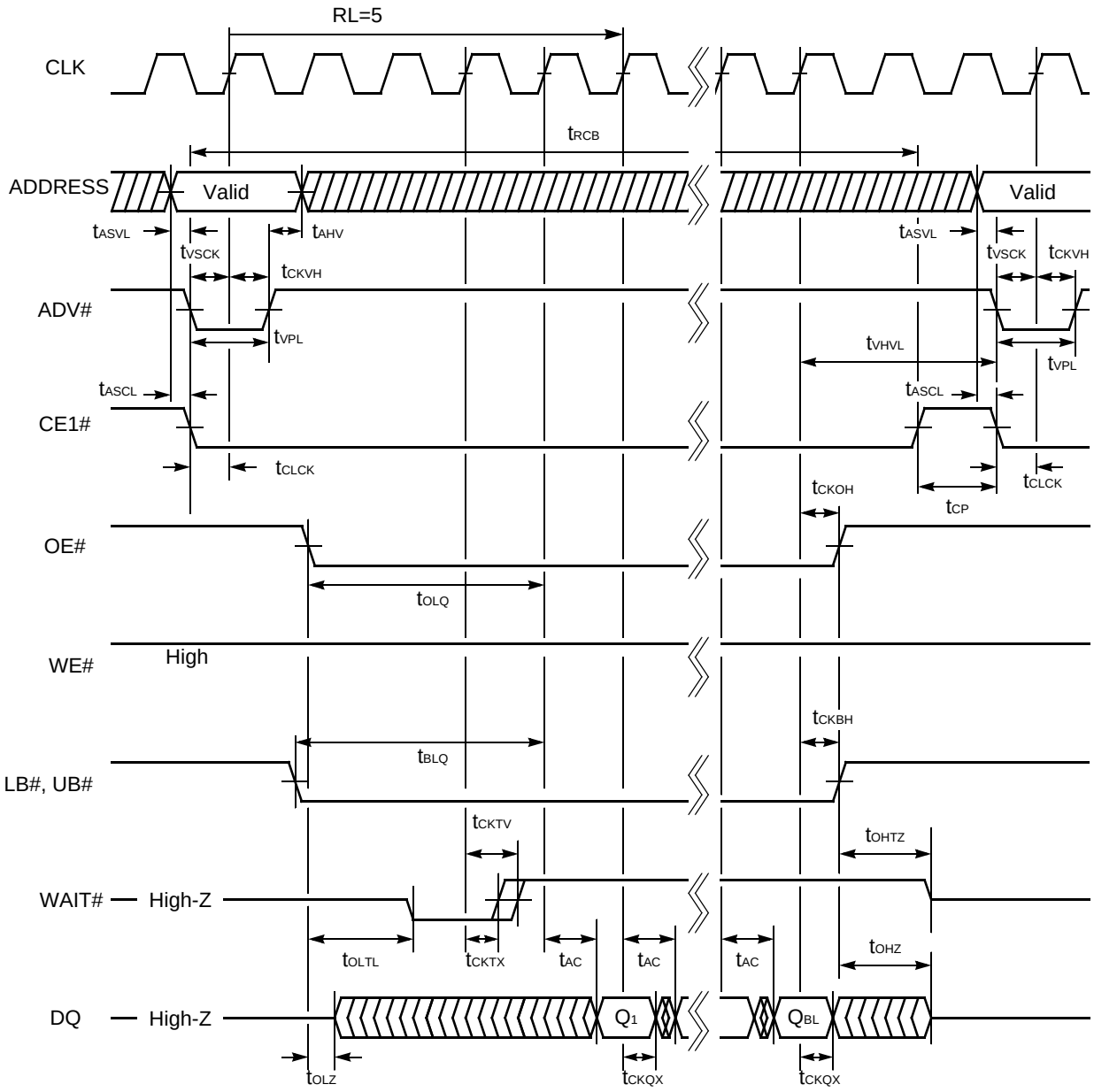


Figure 73. 64M Synchronous Read Timing #I (OE# Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

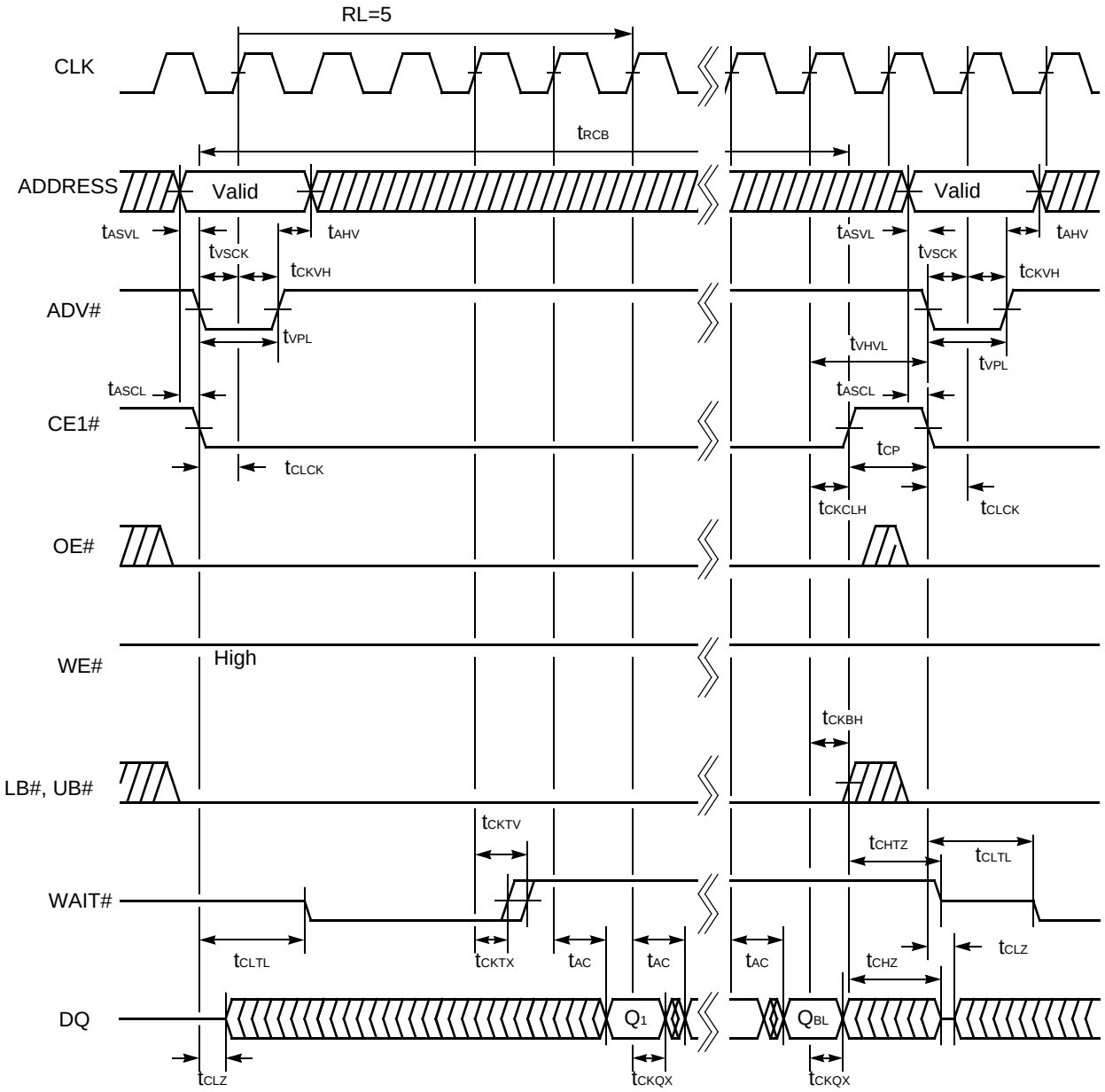


Figure 74. 64M Synchronous Read Timing #2 (CEI# Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

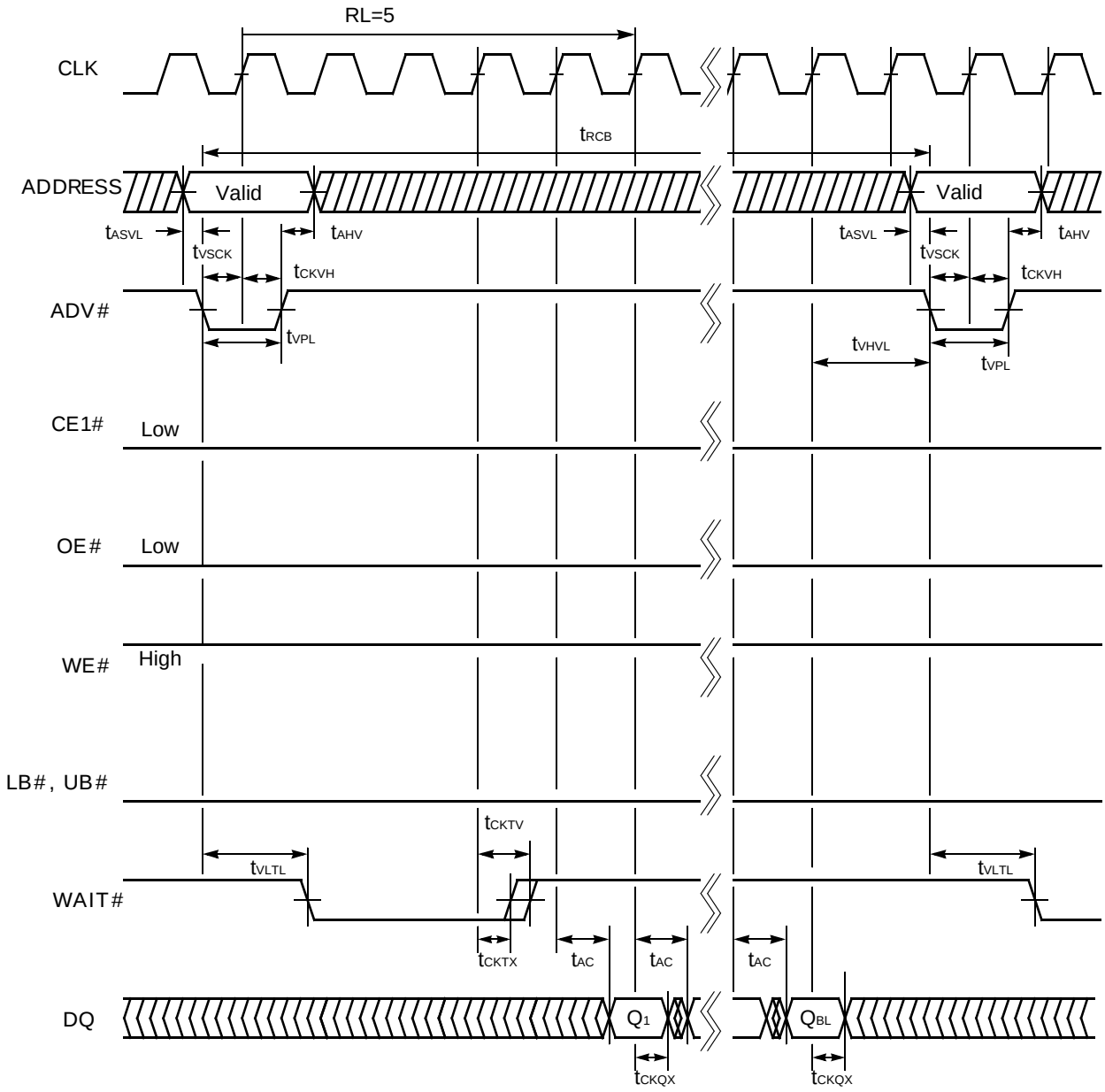


Figure 75. 64M Synchronous Read Timing #3 (ADV# Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

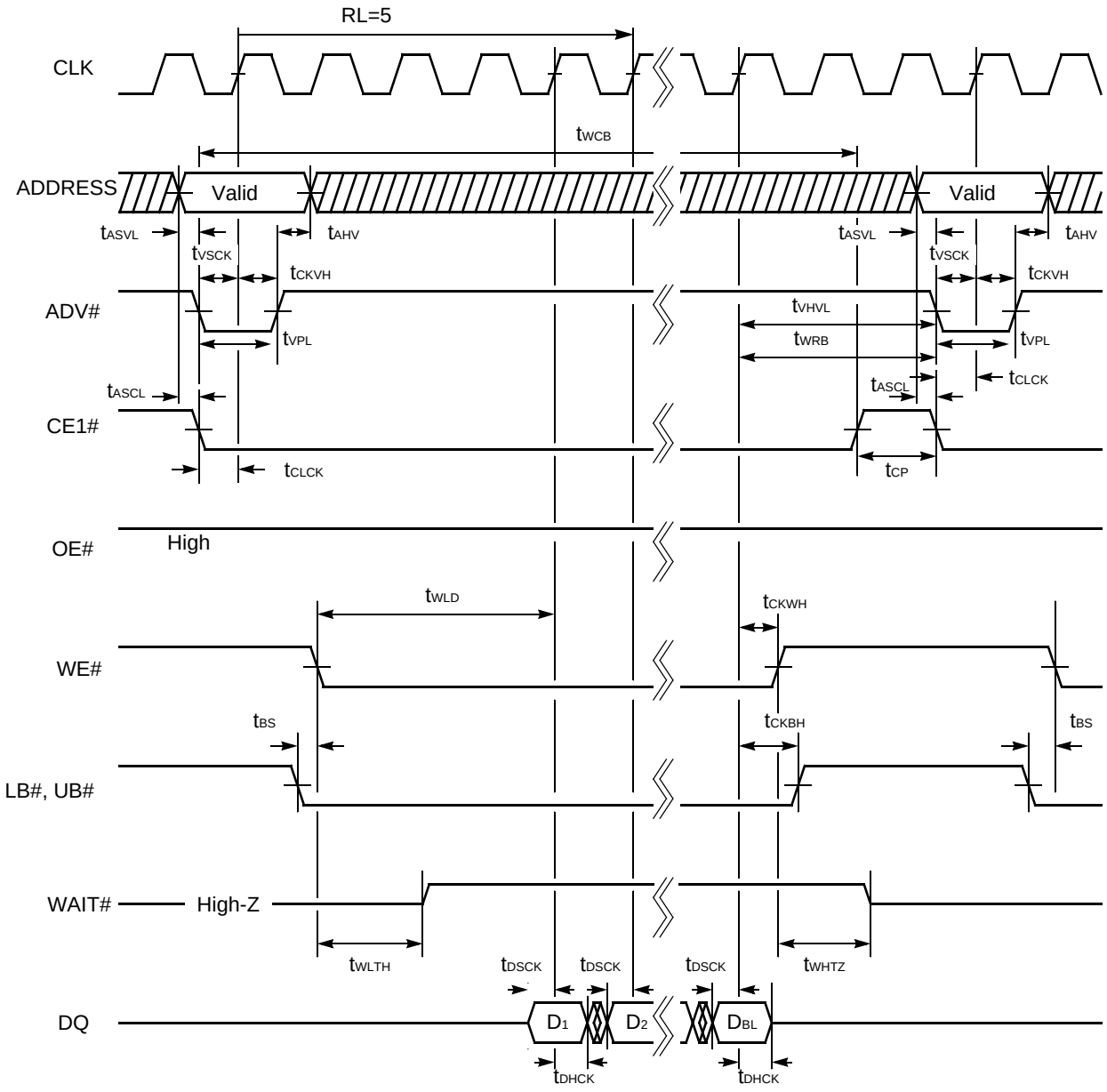


Figure 76. Synchronous Write Timing #I (WE# Level Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

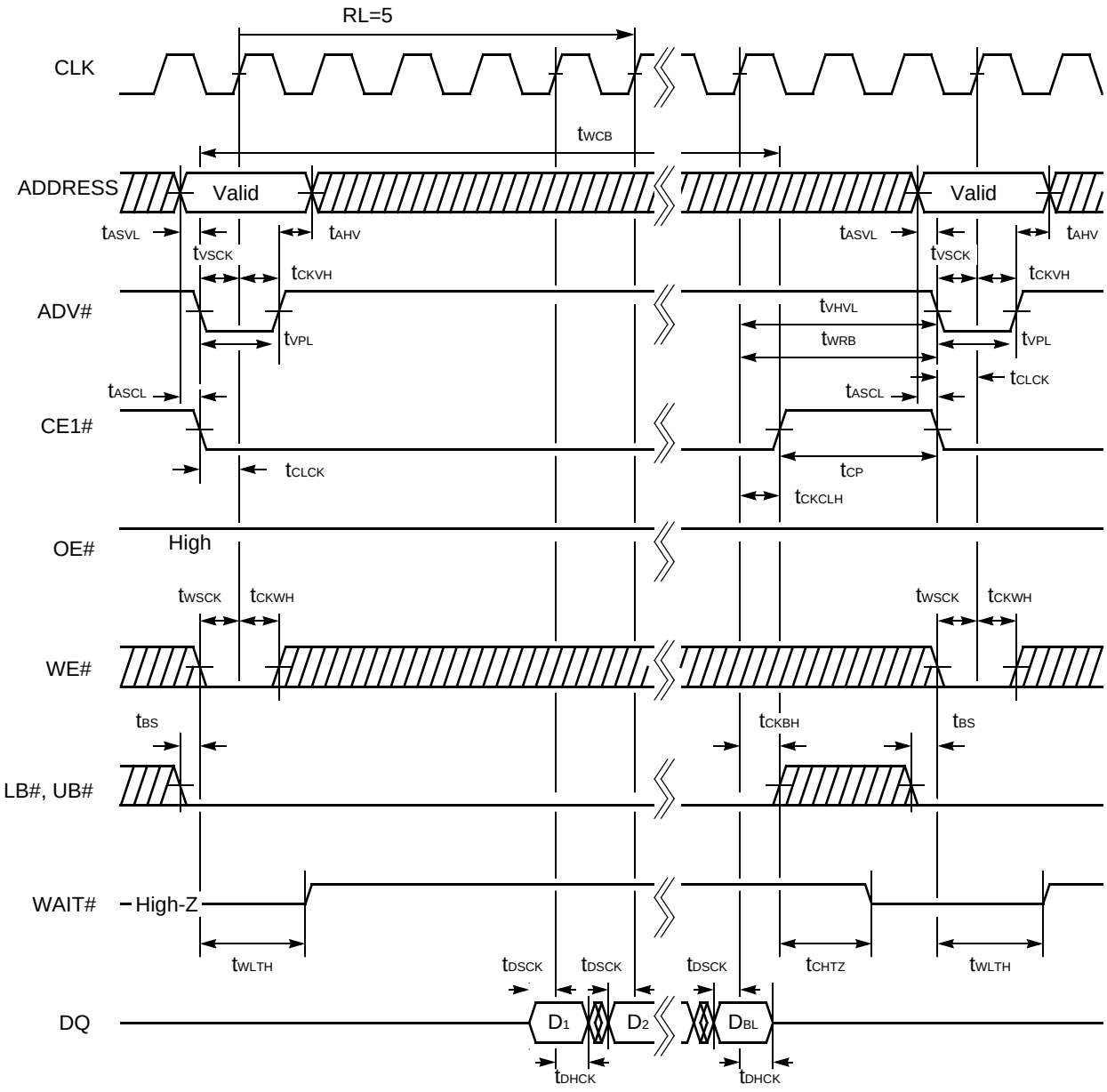


Figure 77. Synchronous Write Timing #2 (WE# Single Clock Pulse Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

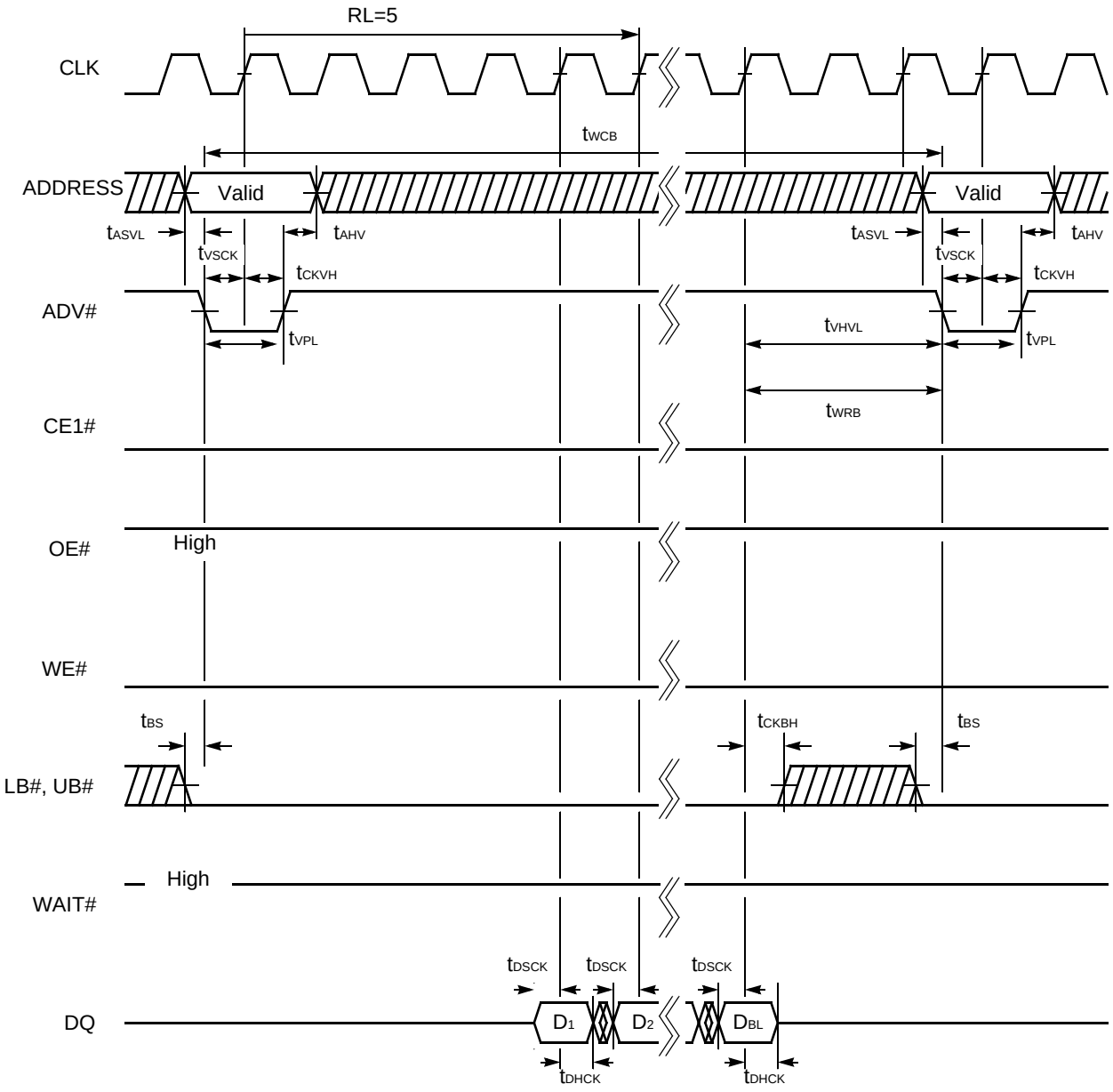


Figure 78. Synchronous Write Timing #3 (ADV# Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

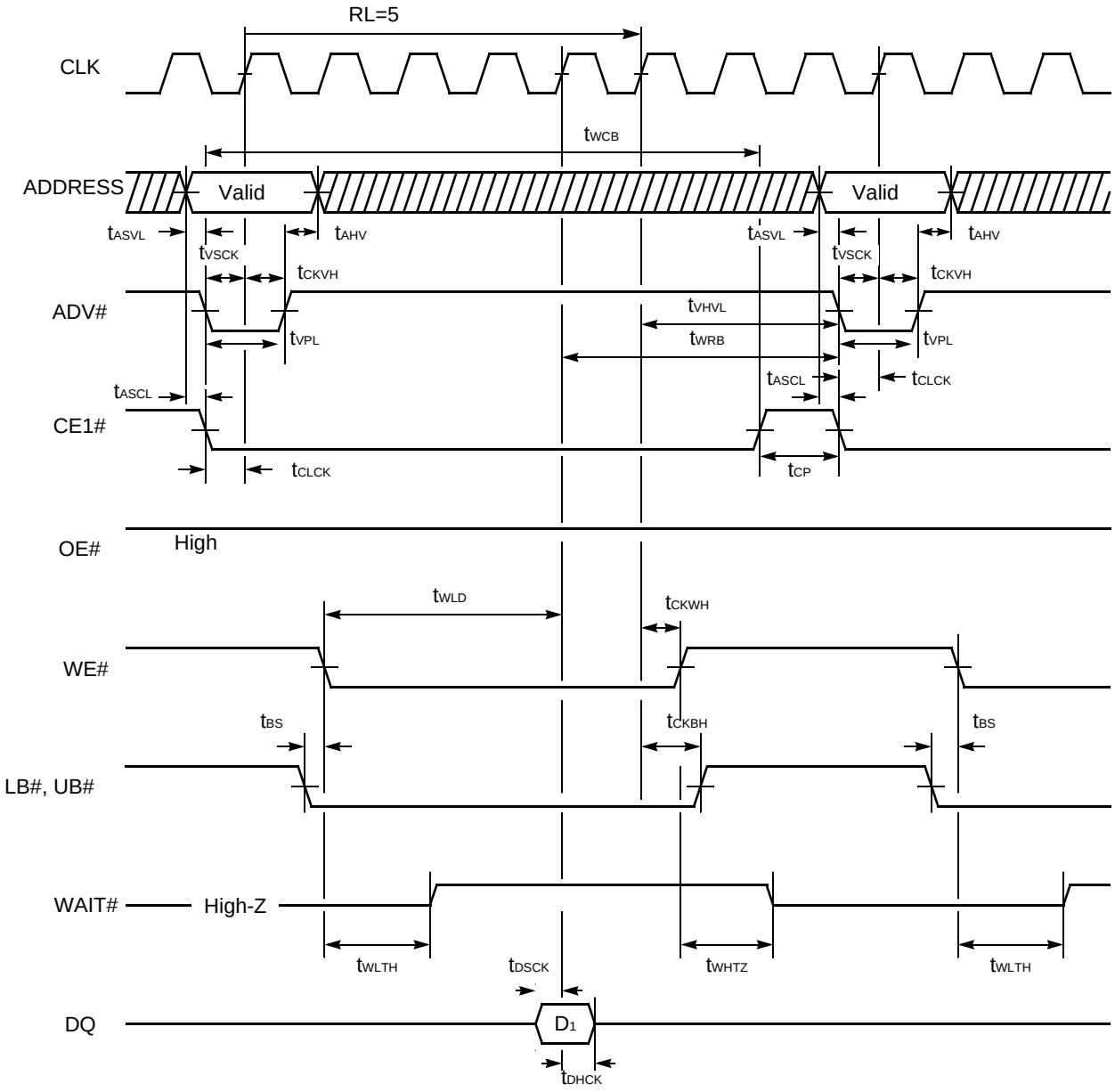


Figure 79. Synchronous Write Timing #4 (WE# Level Control, Single Write)

Notes:

1. *This timing diagram assumes CE2=H, the valid clock edge on rising edge and single write operation.*
2. *Write data is latched on the valid clock edge.*

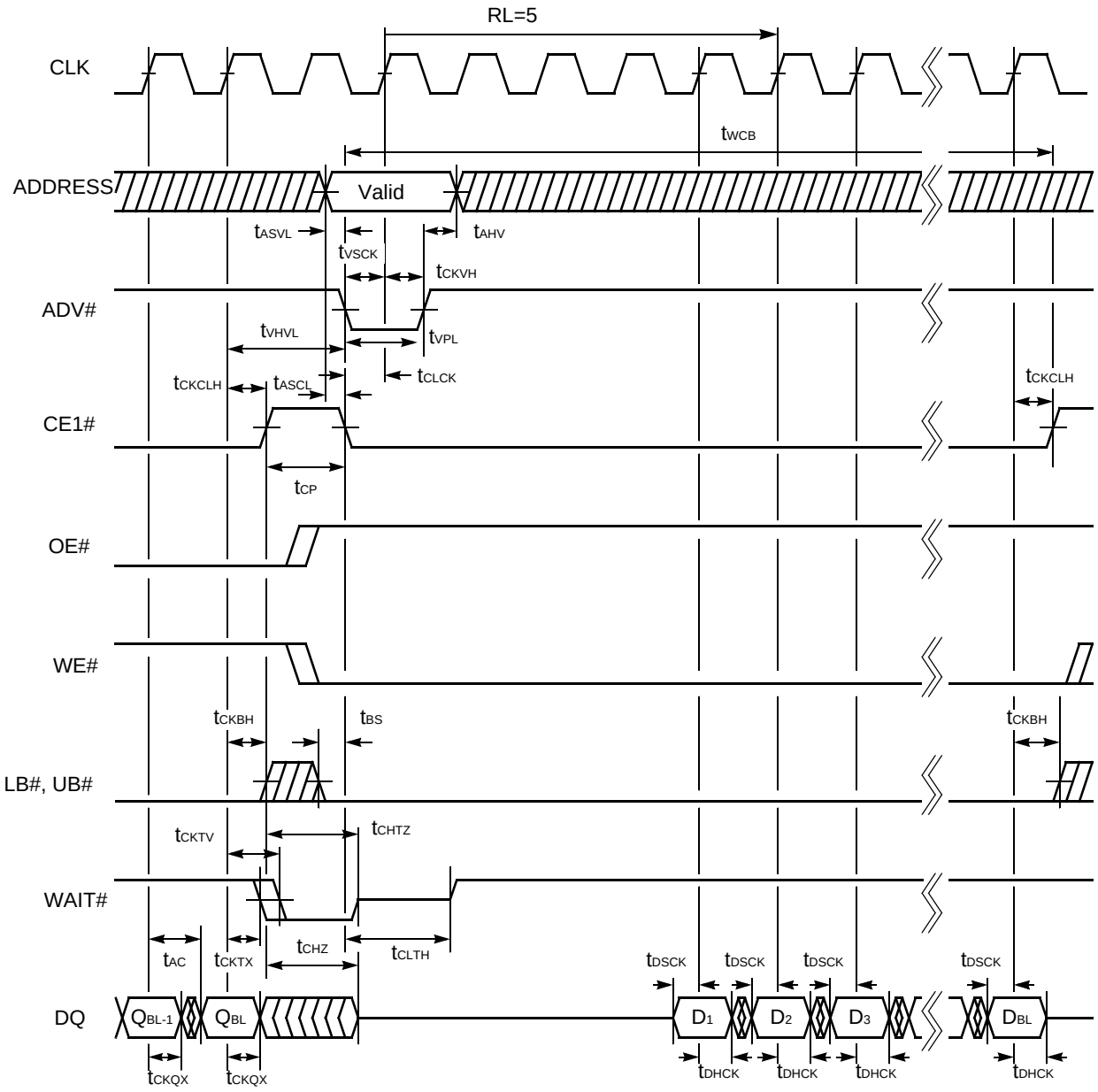


Figure 80. 32M Synchronous Read to Write Timing #I(CEI# Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

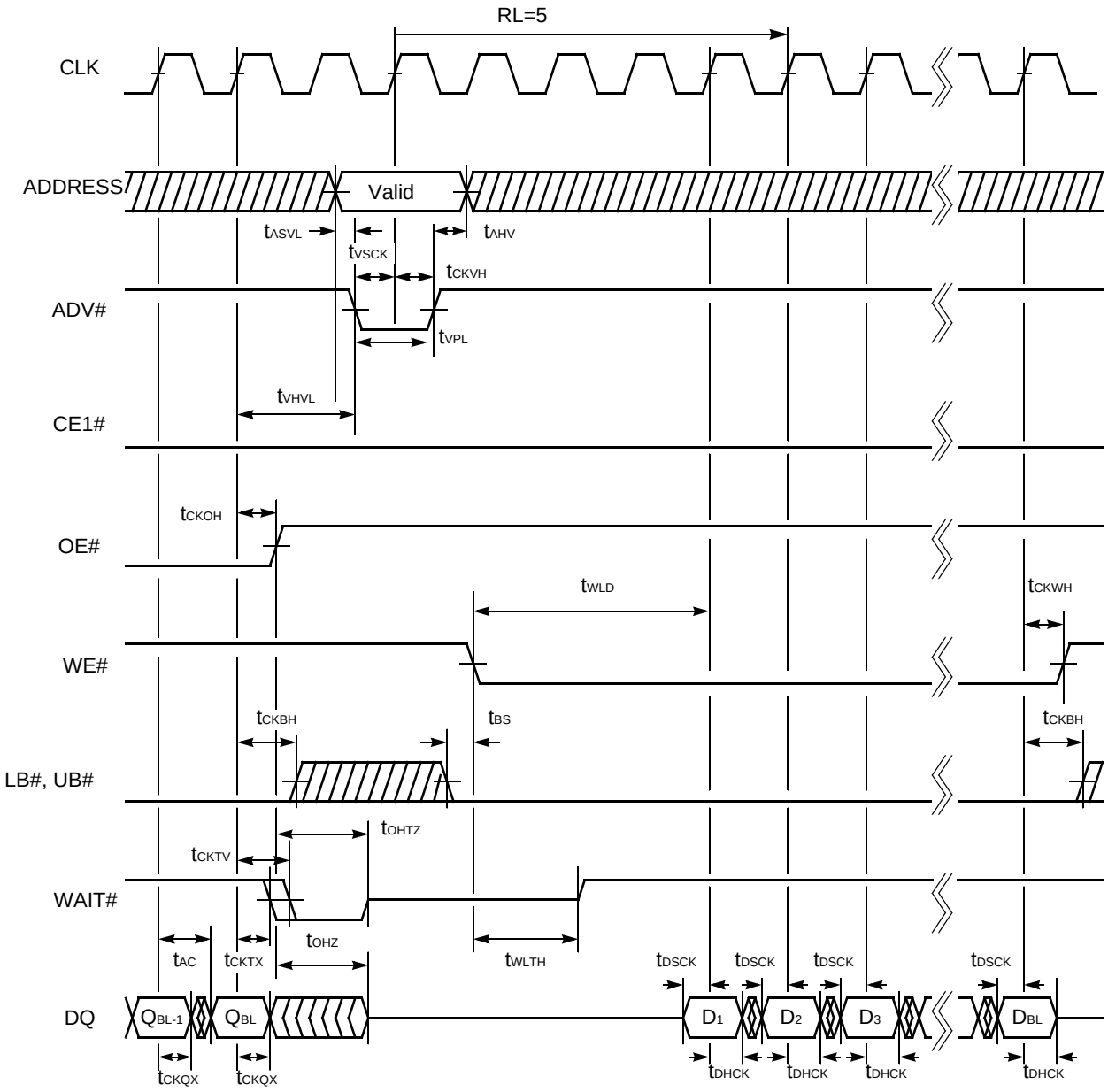


Figure 81. 32M Synchronous Read to Write Timing #2(ADV# Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

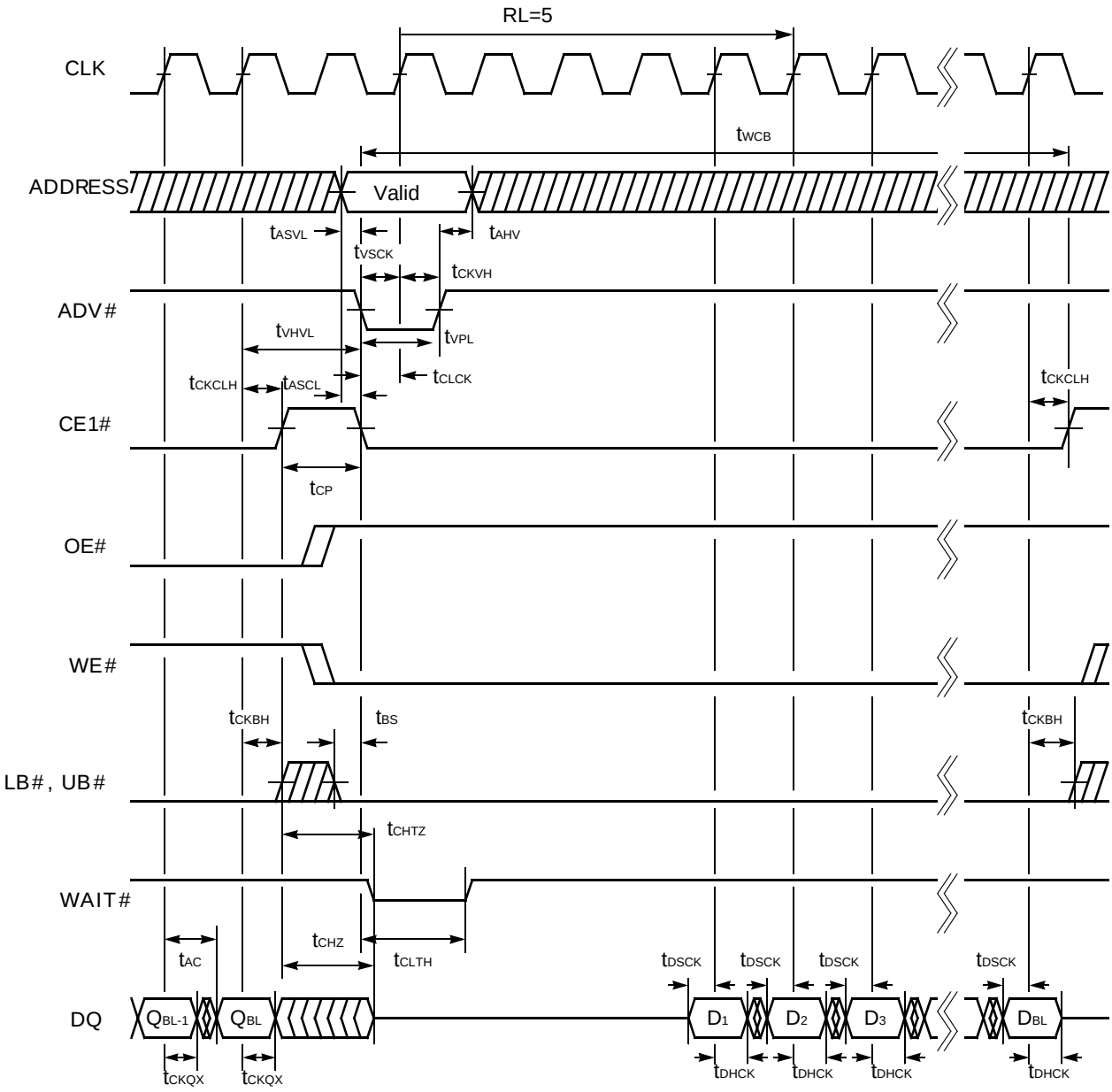


Figure 82. 64M Synchronous Read to Write Timing #I(CEI# Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

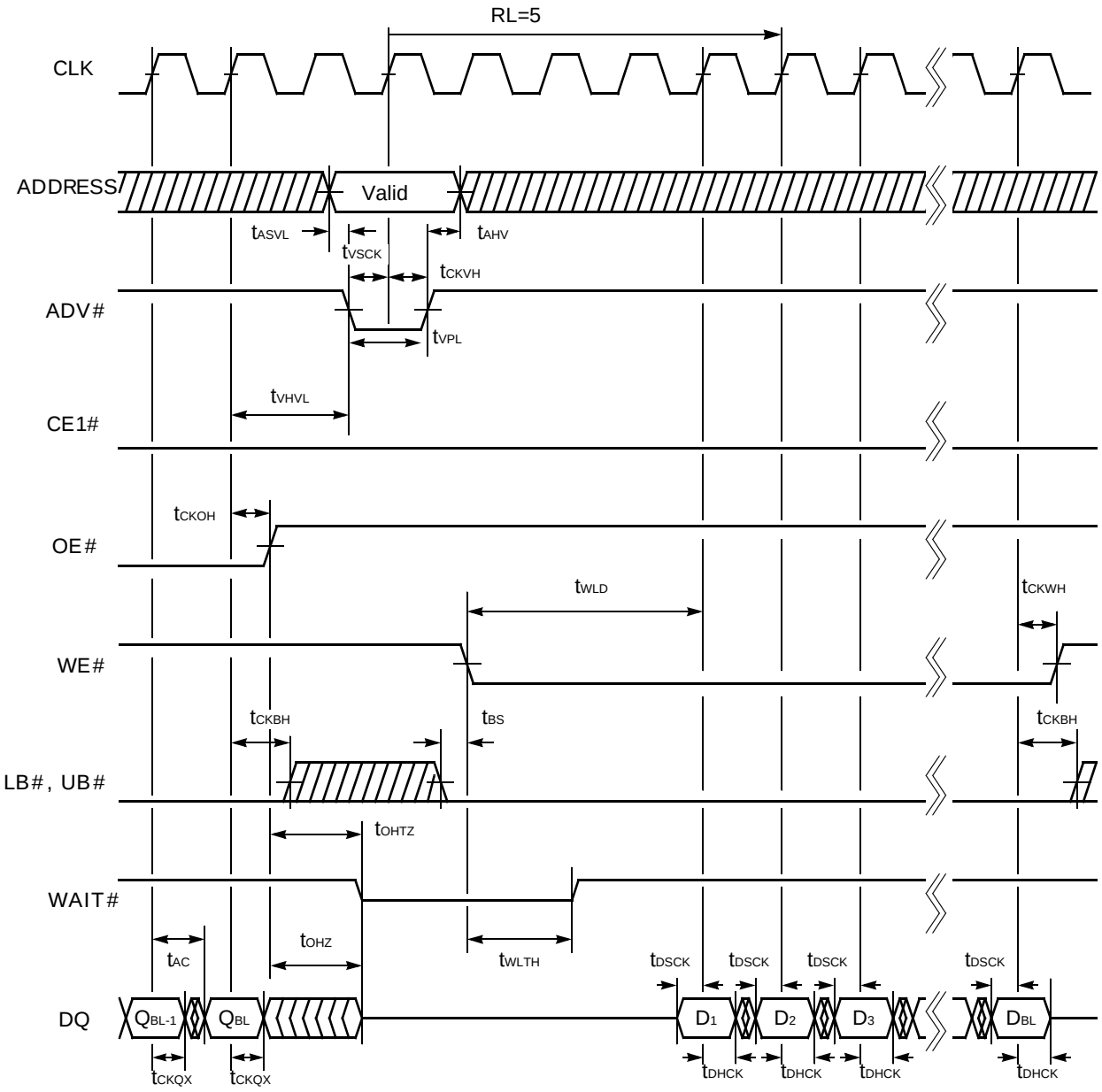


Figure 83. 64M Synchronous Read to Write Timing #2(ADV# Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

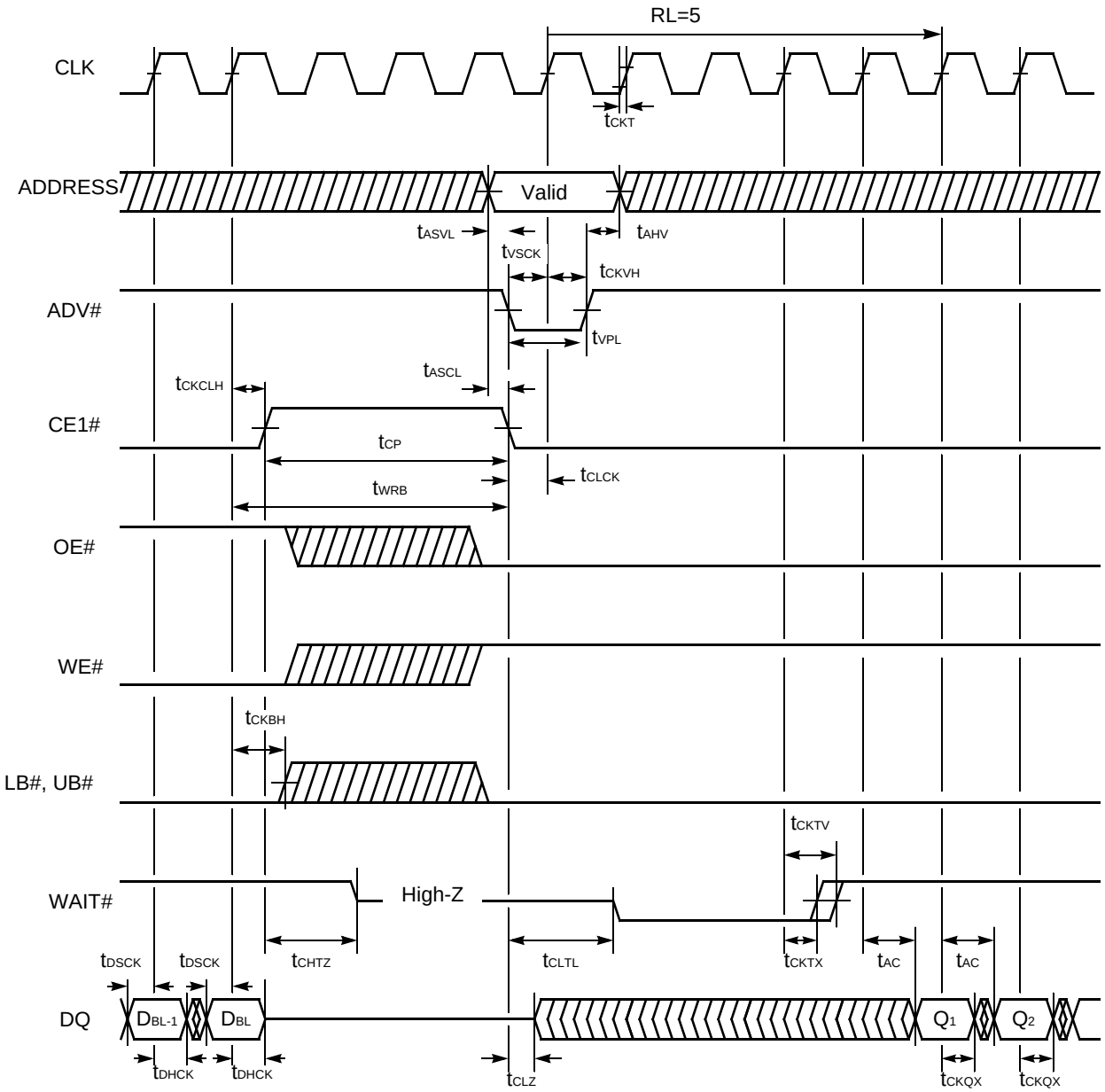


Figure 84. Synchronous Write to Read Timing #I (CEI# Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

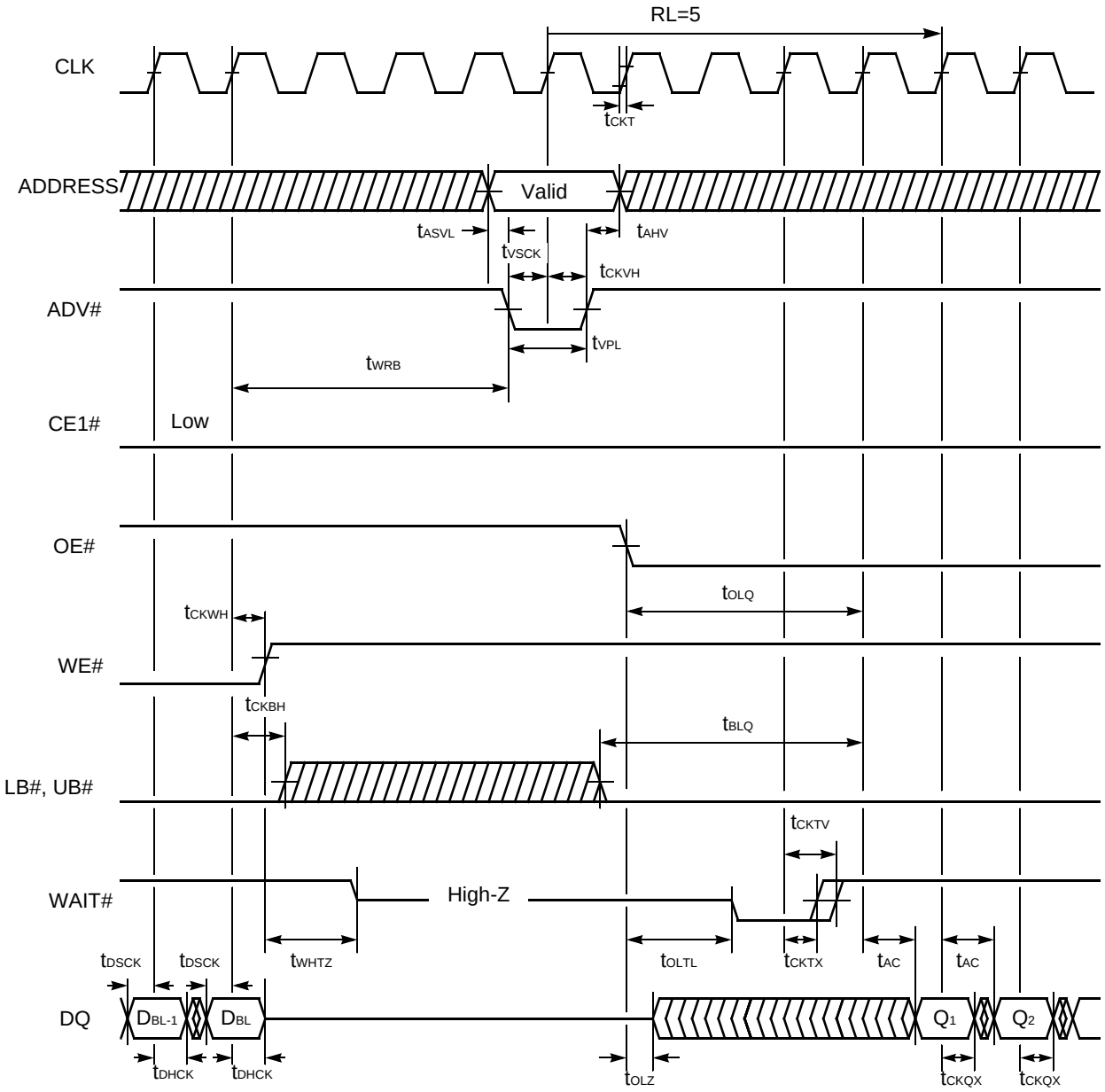


Figure 85. Synchronous Write to Read Timing #2 (ADV# Control)

Note: *This timing diagram assumes CE2=H, the valid clock edge on rising edge and BL=8 or 16.*

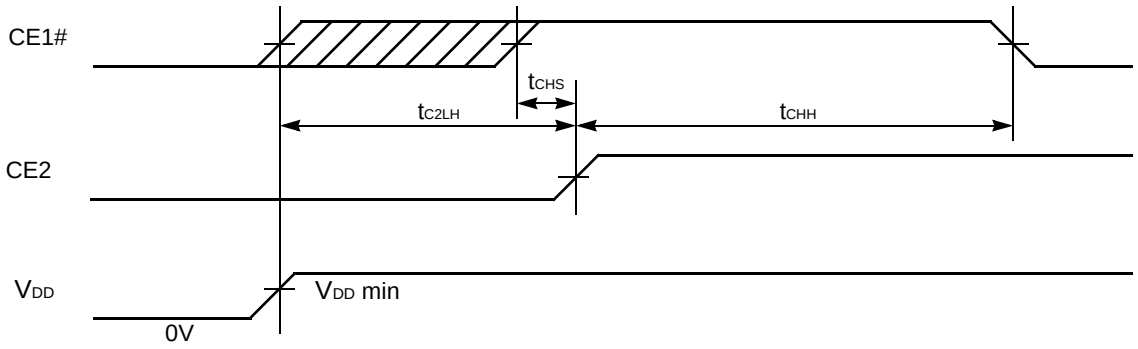


Figure 86. Power-up Timing #l

Note: *The t_{C2LH} specifies after V_{DD} reaches specified minimum level.*

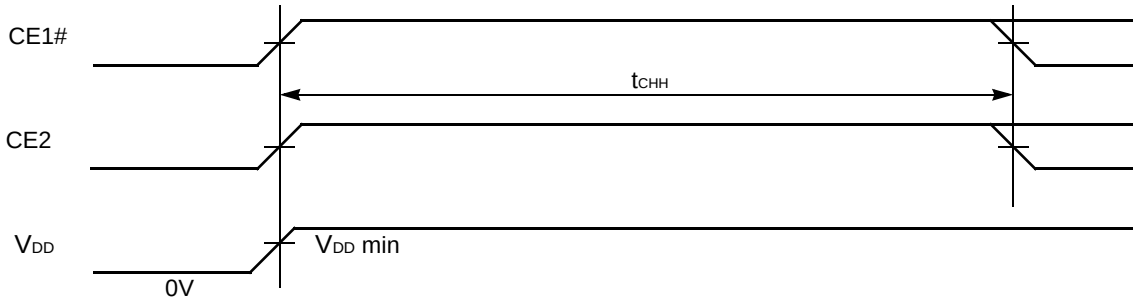


Figure 87. Power-up Timing #2

Note: *The t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable to both CE1# and CE2.*

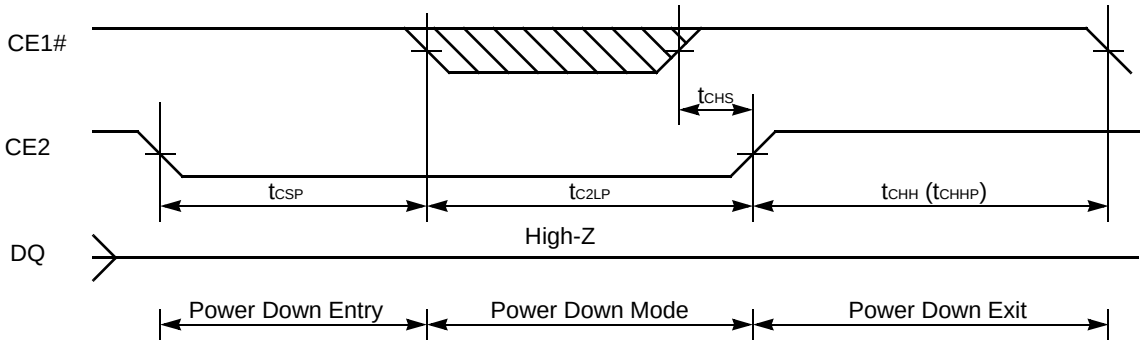


Figure 88. Power Down Entry and Exit Timing

Note: *This Power Down mode can be also used as a reset timing if the POWER-UP timing above could not be satisfied and Power-Down program was not performed prior to this reset.*

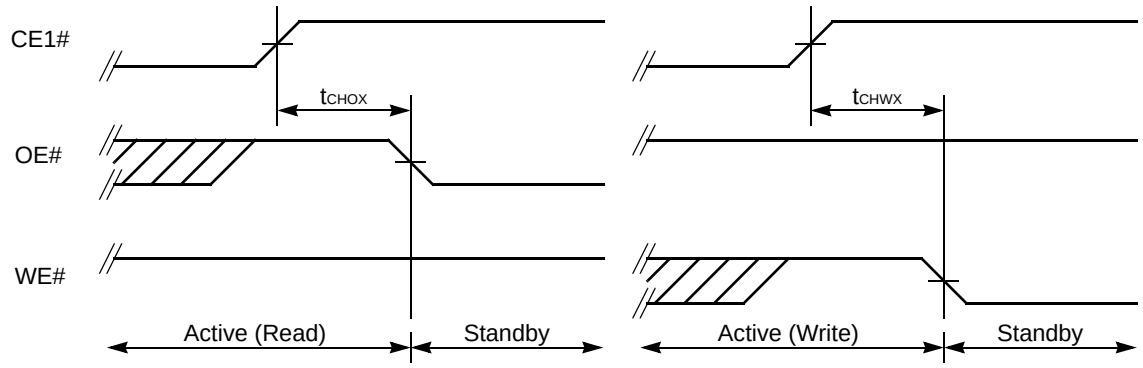


Figure 89. Standby Entry Timing after Read or Write

Note: *Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes t_{RC} (min) period for Standby mode from CE1# Low to High transition.*

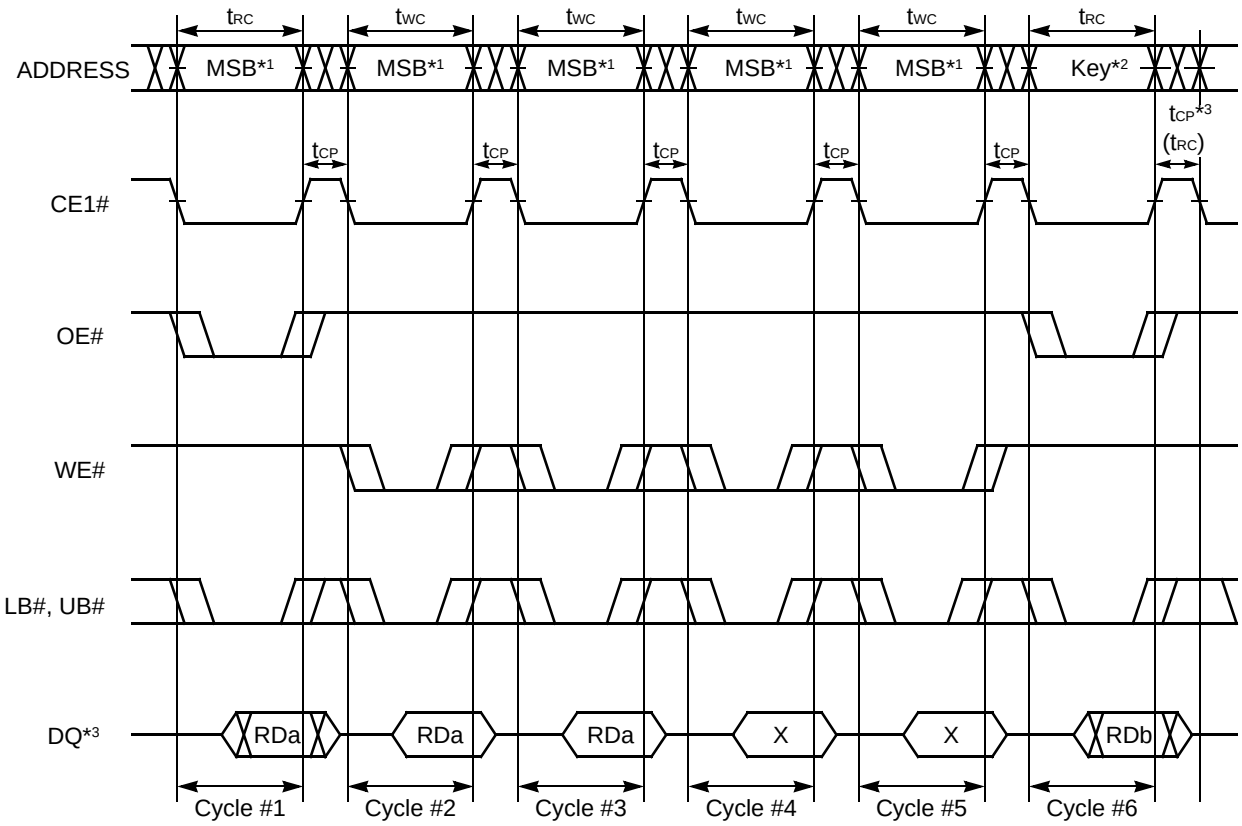


Figure 90. Configuration Register Set Timing #I (Asynchronous Operation)

Notes:

1. *The all address inputs must be High from Cycle #1 to #5.*
2. *The address key must confirm the format specified in the "Functional Description" section. If not, the operation and data are not guaranteed.*
3. *After t_{CP} or t_{RC} following Cycle #6, the Configuration Register Set is completed and returned to the normal operation. t_{CP} and t_{RC} are applicable to returning to asynchronous mode and to synchronous mode respectively.*
4. *Byte read or write is available in addition to Word read or write. At least one byte control signal (LB# or UB#) need to be Low.*

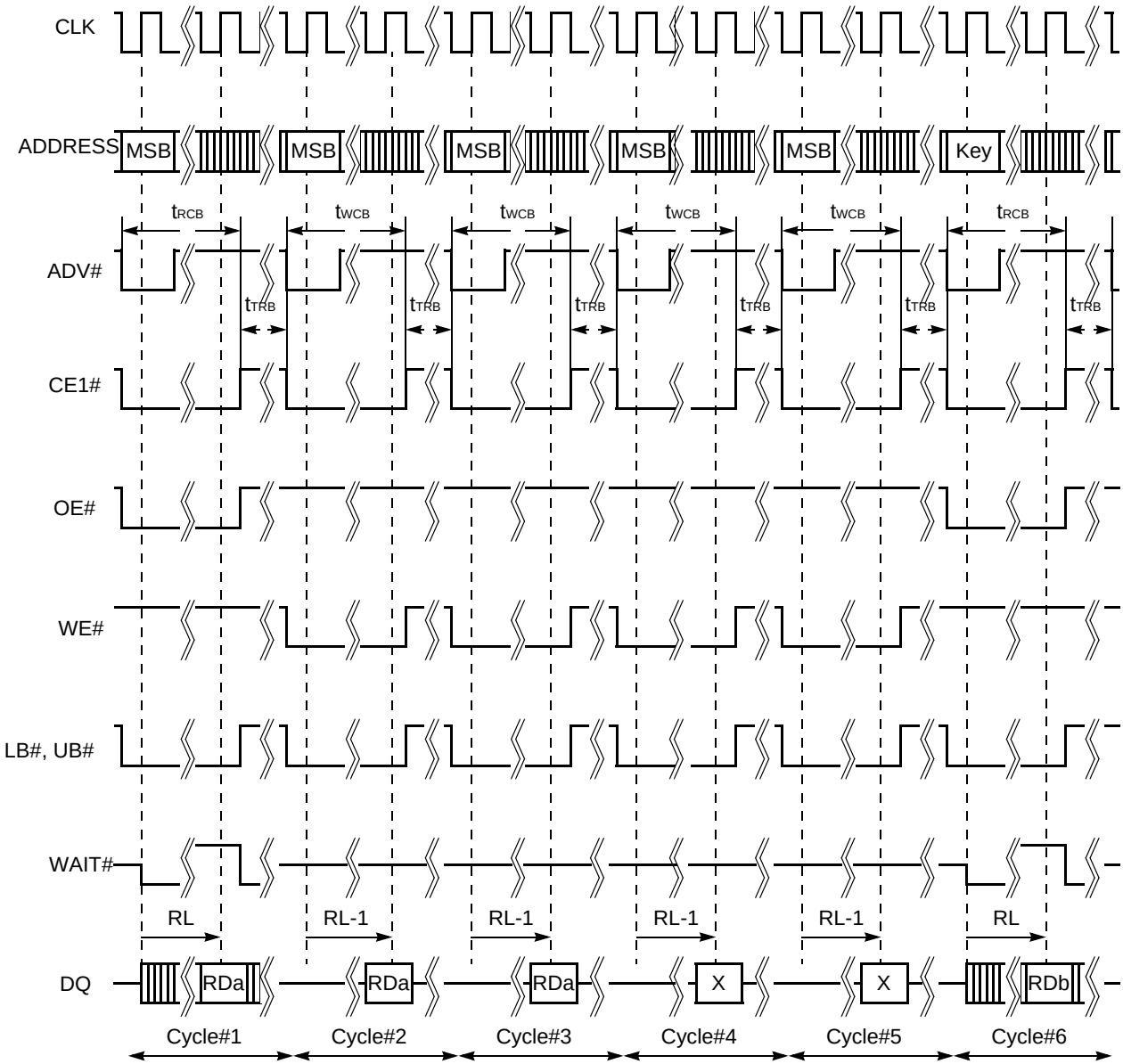


Figure 91. Configuration Register Set Timing #2 (Synchronous Operation)

Notes:

1. *The all address inputs must be High from Cycle #1 to #5.*
2. *The address key must confirm the format specified in the "Functional Description" section. If not, the operation and data are not guaranteed.*
3. *After t_{TRB} following Cycle #6, the Configuration Register Set is completed and returned to the normal operation.*
4. *Byte read or write is available in addition to Word read or write. At least one byte control signal (LB# or UB#) need to be Low.*

COSMORAM Type 1 – 1.8 V, 16 Mb

CMOS 1,048,576-Word x 16 Bit pSRAM

PRELIMINARY

Features

- **Asynchronous SRAM Interface**
- **Fast Random Access Time**
  - t_{CE} = 70 ns (–70)
- **Low Voltage Operating Condition**
  - V_{DD} = +1.7 V to +1.95 V
- **Wide Operating Temperature**
  - T_A = –30°C to +85°C
- **Byte Control by UB# and LB#**
- **Low Power Consumption**
  - I_{DDA1} = 20 mA max
  - I_{DDS1} = 100 µA max
- **Power Down Mode**

General Description

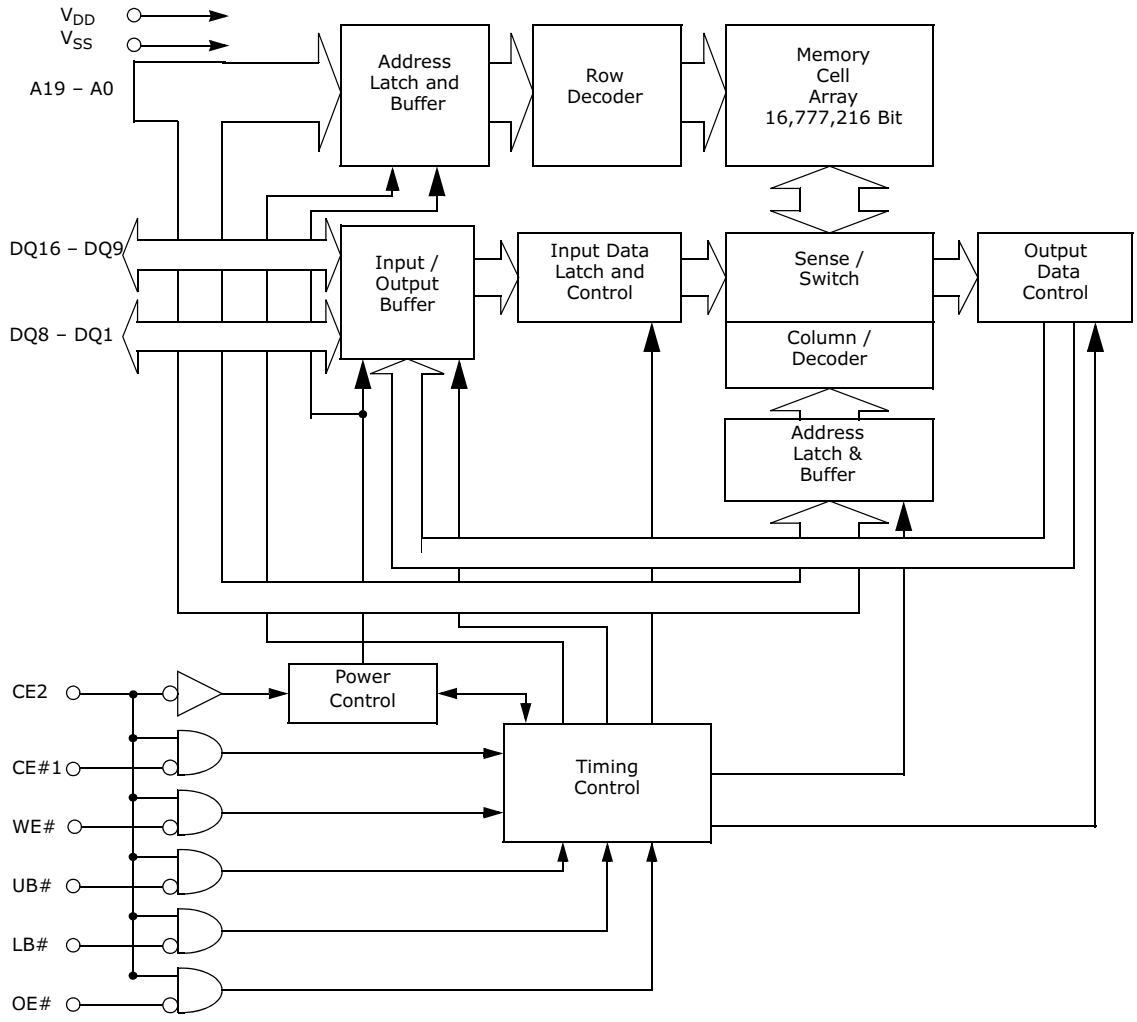
The COSMORAM Type 1 is a CMOS pSRAM with asynchronous Static Random Access Memory (SRAM) interface containing 16,777,216 storages accessible in a 16-bit format. This COSMORAM Type 1 is suited for mobile applications such as Cellular Handset and PDA.

Pin Description

Pin Name	Description
A_{19} to A_0	Address Input
CE1#	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
WE#	Write Enable (Low Active)
OE#	Output Enable (Low Active)
UB#	Upper Byte Control (Low Active)

Pin Name	Description
LB#	Lower Byte Control (Low Active)
DQ_{16-9}	Upper Byte Data Input/Output
DQ_{8-1}	Lower Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground

Block Diagram



Function Truth Table

Mode	CE2	CE#1	WE#	OE#	LB#	UB#	A19-0	DQ8-1	DQ16-9	I_{DD}	Data Retention
Standby (Deselect)	H	H	X	X	X	X	X	High-Z	High-Z	I_{DDS}	Yes
Output Disable (Note 1)	H	L	H	H	X	X	(Note 3)	High-Z	High-Z	I_{DDA}	
Output Disable (No Read)			H	L	H	H	Valid	High-Z	High-Z		
Read (Upper Byte)					H	L	Valid	High-Z	Output Valid		
Read (Lower Byte)					L	H	Valid	Output Valid	High-Z		
Read (Word)					L	L	Valid	Output Valid	Output Valid		
No Write			L	H	H	H	Valid	Invalid	Invalid		
Write (Upper Byte)					H	L	Valid	Invalid	Input Valid		
Write (Lower Byte)					L	H	Valid	Input Valid	Invalid		
Write (Word)					L	L	Valid	Input Valid	Input Valid		
Power Down(Note 2)	L	X	X	X	X	X	X	High-Z	High-Z	I_{DDP}	No

Legend: *L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High Impedance*

Notes:

1. *This logic condition should not be kept any longer than 1 µs.*
2. *Power Down mode can be entered from Standby state and all DQ pins are in High-Z state.*
3. *Can be either V_{IL} or V_{IH} but must be valid before Read or Write.*

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage of V_{DD} Supply Relative to V_{SS}	V_{DD}	–0.5 to +3.6	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to +3.6	V
Short Circuit Output Current	I_{OUT}	±50	mA
Storage Temperature	T_{STG}	–55 to +125	°C

Note: *Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, and so on) in excess of absolute maximum ratings. Do not exceed these ratings.*

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	1.7	1.95	V
	V_{SS}	0	0	V
High Level Input Voltage (Note 1)	V_{IH}	V_{DD}*0.8	V_{DD}+0.2	V
Low Level Input Voltage (Note 2)	V_{IL}	-0.3	V_{DD}*0.2	V
Ambient Temperature	T_A	-30	85	°C

Notes: *(Referenced to V_{SS})*

1. *Maximum DC voltage on input and I/O pins are V_{DD} + 0.2 V. During voltage transitions, inputs may overshoot to V_{DD}+1.0 V for periods of up to 5 ns.*
2. *Minimum DC voltage on input or I/O pins are -0.3 V. During voltage transitions, inputs may overshoot V_{SS} to –1.0 V for periods of up to 5 ns.)*
3. *Recommended operating conditions are normal operating ranges for the semiconductor device. All the device electrical characteristics are warranted when operated within these ranges.*
4. *Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may affect device reliability and result in device failure.*
5. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*

Package Pin Capacitance

Symbol	Description	Test Setup	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0V	—	5	pF
C_{IN2}	Control Input Capacitance	V_{IN} = 0V	—	5	pF
C_{IO}	Data Input/Output Capacitance	V_{IO} = 0V	—	8	pF

Note: *Test conditions: T_A = 25°C, f = 1.0 MHz*

DC Characteristics

Parameter	Symbol	Test Conditions		Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}		–1.0	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{DD}, Output Disable		–1.0	+1.0	µA
Output High Voltage Level	V_{OH}	V_{DD} = V_{DD}(min), I_{OH} = –0.5 mA		1.4	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 1 mA		—	0.4	V
V_{DD} Power Down Current	I_{DDPS}	V_{DD} = V_{DD} max., V_{IN} = V_{IH} or V_{IL}, CE2 ≤ 0.2V		—	10	µA
V_{DD} Standby Current	I_{DDS}	V_{DD} = V_{DD} max., V_{IN} = V_{IH} or V_{IL}, CE#1 = CE2 = V_{IH}		—	1	mA
	I_{DDS1}	V_{DD} = V_{DD} max., V_{IN} ≤ 0.2V or V_{IN} ≥ V_{DD} – 0.2 V, CE#1 = CE2 ≥ V_{DD} – 0.2 V		—	100	µA
V_{DD} Active Current	I_{DDA1}	V_{DD} = V_{DD} max., V_{IN} = V_{IH} or V_{IL}, CE#1 = V_{IL} and CE2= V_{IH}, I_{OUT}=0mA	t_{RC} / t_{WC} = minimum	—	20	mA
	I_{DDA2}		t_{RC} / t_{WC} = 1µs	—	3	mA

Notes:
1. *All voltages are referenced to V_{SS}.*
2. *DC Characteristics are measured after following power-up timing.*
3. *I_{OUT} depends on the output load conditions.*
4. *DC Characteristics apply under recommended operating conditions unless otherwise noted*

AC Characteristics

Read Operation

Parameter (Notes)	Symbol	Value		Unit
		Min.	Max.	
Read Cycle Time (1, 2)	t_{RC}	80	1000	ns
CE#1 Access Time (3)	t_{CE}	—	70	ns
OE# Access Time (3)	t_{OE}	—	45	ns
Address Access Time (3, 5)	t_{AA}	—	70	ns
LB# / UB# Access Time (3)	t_{BA}	—	30	ns
Output Data Hold Time (3)	t_{OH}	5	—	ns
CE#1 Low to Output Low-Z (4)	t_{CLZ}	5	—	ns
OE# Low to Output Low-Z (4)	t_{OLZ}	0	—	ns
LB# / UB# Low to Output Low-Z (4)	t_{BLZ}	0	—	ns
CE#1 High to Output High-Z (3)	t_{CHZ}	—	20	ns
OE# High to Output High-Z (3)	t_{OHZ}	—	20	ns
LB# / UB# High to Output High-Z (3)	t_{BHZ}	—	20	ns
Address Setup Time to CE#1 Low	t_{ASC}	–5	—	ns
Address Setup Time to OE# Low	t_{ASO}	10	—	ns
Address Invalid Time (5)	t_{AX}	—	10	ns
Address Hold Time from CE#1 High (6)	t_{CHAH}	–5	—	ns
Address Hold Time from OE# High	t_{OHAH}	–5	—	ns

Parameter (Notes)	Symbol	Value		Unit
		Min.	Max.	
WE# High to OE# Low Time for Read (7)	t_{WHOL}	15	1000	ns
CE#1 High Pulse Width	t_{CP}	15	—	ns

Notes:
1. *Maximum value is applicable if CE#1 is kept at Low without any address change.*
2. *Address should not be changed within minimum t_{RC}.*
3. *The output load 50 pF with 50-Ω termination to V_{DD}*0.5 V.*
4. *The output load 5 pF without any other load.*
5. *Applicable when CE#1 is kept at Low.*
6. *t_{RC} (min) must be satisfied.*
7. *If actual value of t_{WHOL} is shorter than specified minimum values, the actual t_{AA} of following Read may become longer by the amount of subtracting actual value from specified minimum value.*
8. *AC Characteristics apply under recommended operating conditions unless otherwise noted*

Write Operation

Parameter (Notes)	Symbol	Value		Unit
		Min.	Max.	
Write Cycle Time (1, 2)	t_{WC}	80	1000	ns
Address Setup Time (2)	t_{AS}	0	—	ns
CE#1 Write Pulse Width (3)	t_{CW}	45	—	ns
WE# Write Pulse Width (3)	t_{WP}	45	—	ns
LB# / UB# Write Pulse Width (3)	t_{BW}	45	—	ns
LB# / UB# Byte Mask Setup Time (4)	t_{BS}	–5	—	ns
LB# / UB# Byte Mask Hold Time (5)	t_{BH}	–5	—	ns
Write Recovery Time (6)	t_{WR}	0	—	ns
CE#1 High Pulse Width	t_{CP}	15	—	ns
WE# High Pulse Width	t_{WHP}	15	1000	ns
LB# / UB# High Pulse Width	t_{BHP}	15	1000	ns
Data Setup Time	t_{DS}	20	—	ns
Data Hold Time	t_{DH}	0	—	ns
OE# High to CE#1 Low Setup Time for Write (7)	t_{OHCL}	–5	—	ns
OE# High to Address Setup Time for Write (8)	t_{OES}	0	—	ns
LB# and UB# Write Pulse Overlap	t_{BWO}	20	—	ns

Notes:
1. *Maximum value is applicable if CE#1 is kept at Low without any address change.*
2. *Minimum value must be equal or greater than the sum of write pulse (t_{CW}, t_{WP} or t_{BW}) and write recovery time (t_{WRC}, t_{WR} or t_{BR}).*
3. *Write pulse is defined from High to Low transition of CE#1, WE#, or LB# / UB#, whichever occurs last.*
4. *Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of CE#1 or WE whichever occurs last.*
5. *Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of CE#1 or WE# whichever occurs first.*
6. *Write recovery is defined from Low to High transition of CE#1, WE#, or LB# / UB#, whichever occurs first.*
7. *If OE# is Low after minimum t_{OHCL}, read cycle is initiated. In other word, $\overline{OE\#}$ must be brought to High within 5 ns after CE#1 is brought to Low. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.*
8. *If OE# is Low after new address input, read cycle is initiated. In other word, OE# must be brought to High at the same time or before new address valid. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.*
9. *AC Characteristics apply under recommended operating conditions unless otherwise noted*

Power Down Parameters

Parameter (Notes)	Symbol	Value		Unit
		Min.	Max.	
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10	—	ns
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	80	—	ns
CE#1 High Hold Time following CE2 High after Power Down Exit [SLEEP mode only] (See Note)	t_{CHH}	300	—	µs
CE#1 High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0	—	ns

Note: *Applicable also to power-up.*

Other Timing Parameters

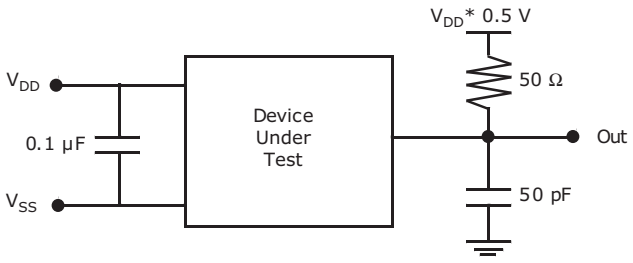
Parameter (Notes)	Symbol	Value		Unit
		Min.	Max.	
CE#1 High to OE# Invalid Time for Standby Entry	t_{CHOX}	10	—	ns
CE#1 High to WE# Invalid Time for Standby Entry (1)	t_{CHWX}	10	—	ns
CE#1 High Hold Time following CE2 High after Power-up	t_{CHH}	300	—	µs
Input Transition Time (2)	t_T	1	25	ns

Notes:
1. *Some data might be written into any address location if t_{CHWX}(min) is not satisfied.*
2. *The Input Transition Time (t_T) at AC testing is 5 ns as shown in below. If actual t_T is longer than 5 ns, it may violate AC specification of some timing parameters.*

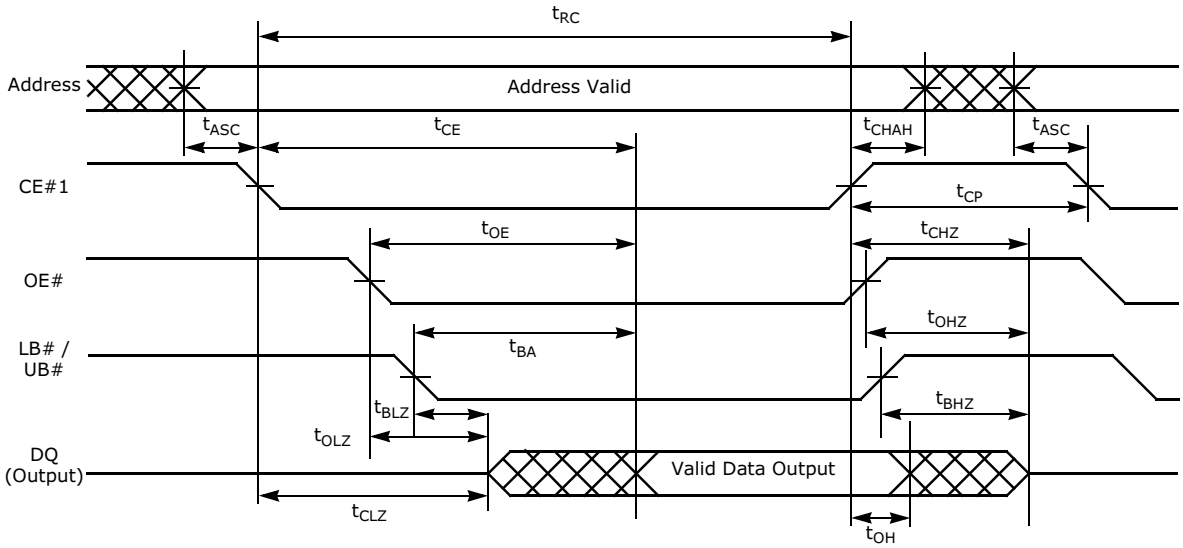
AC Test Conditions

Symbol	Description	Test Setup	Value	Unit
V_{IH}	Input High Level		V_{DD} * 0.8	V
V_{IL}	Input Low Level		V_{DD} * 0.2	V
V_{REF}	Input Timing Measurement Level		V_{DD} * 0.5	V
t_T	Input Transition Time	Between V_{IL} and V_{IH}	5	ns

AC Measurement Output Load Circuit

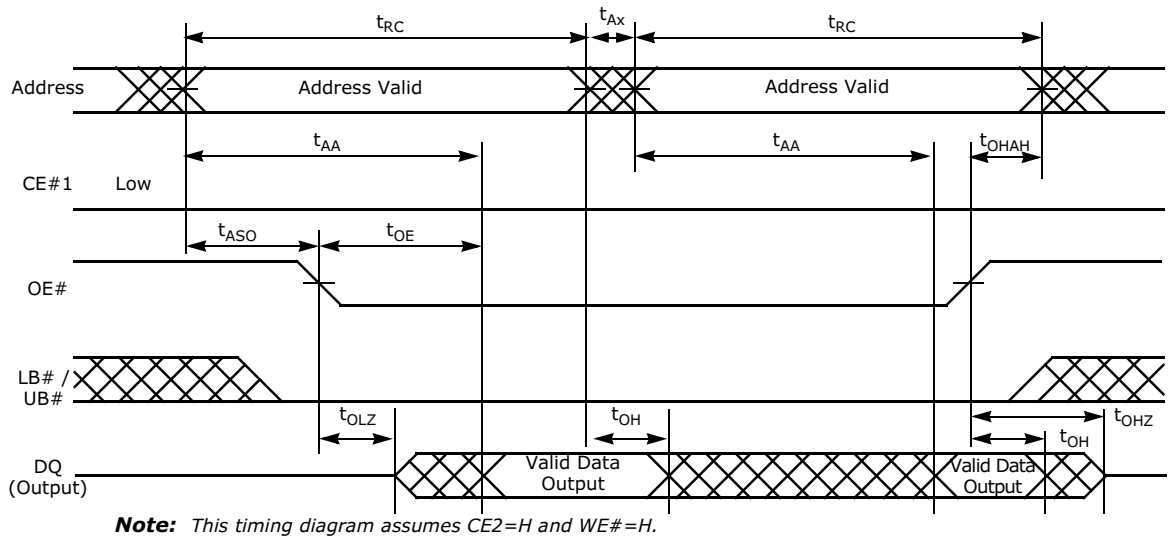


Timing Diagrams



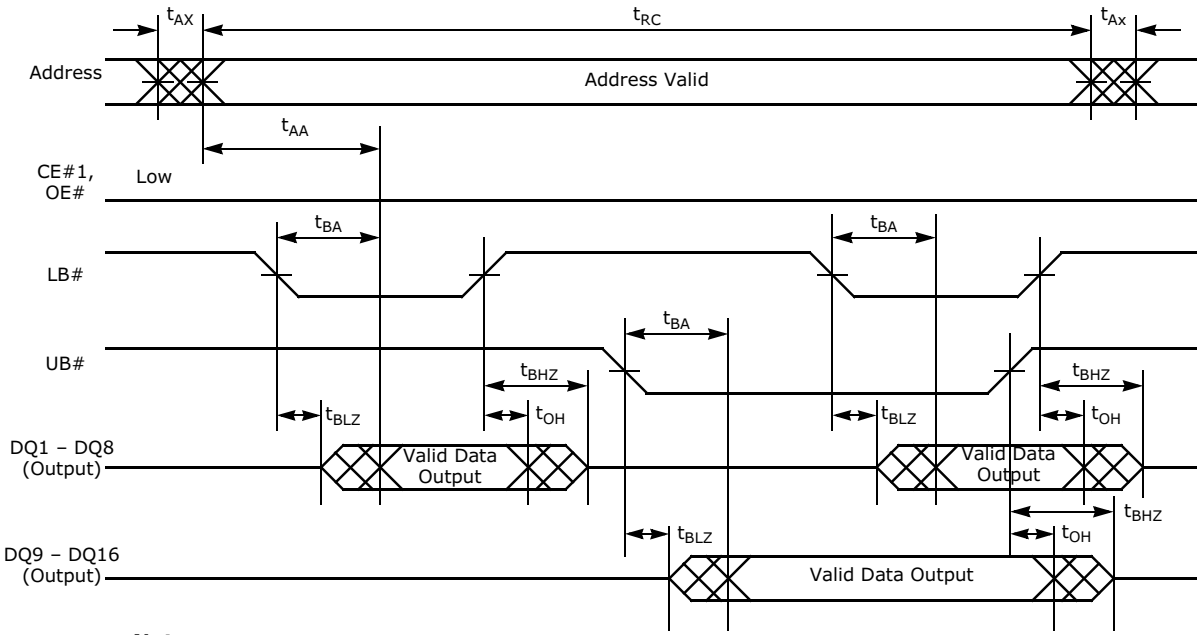
Note: *This timing diagram assumes CE2=H and WE#=H.*

Figure 92. Read Timing #I (Basic Timing)



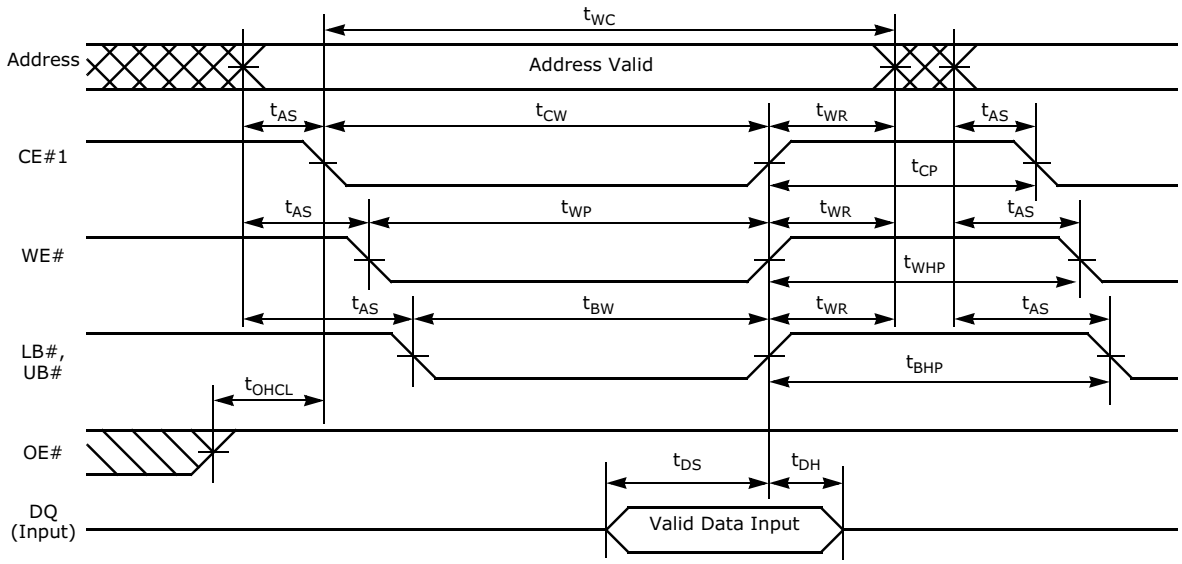
Note: *This timing diagram assumes CE2=H and WE#=H.*

Figure 93. Read Timing #2 (OE# and Address Access)



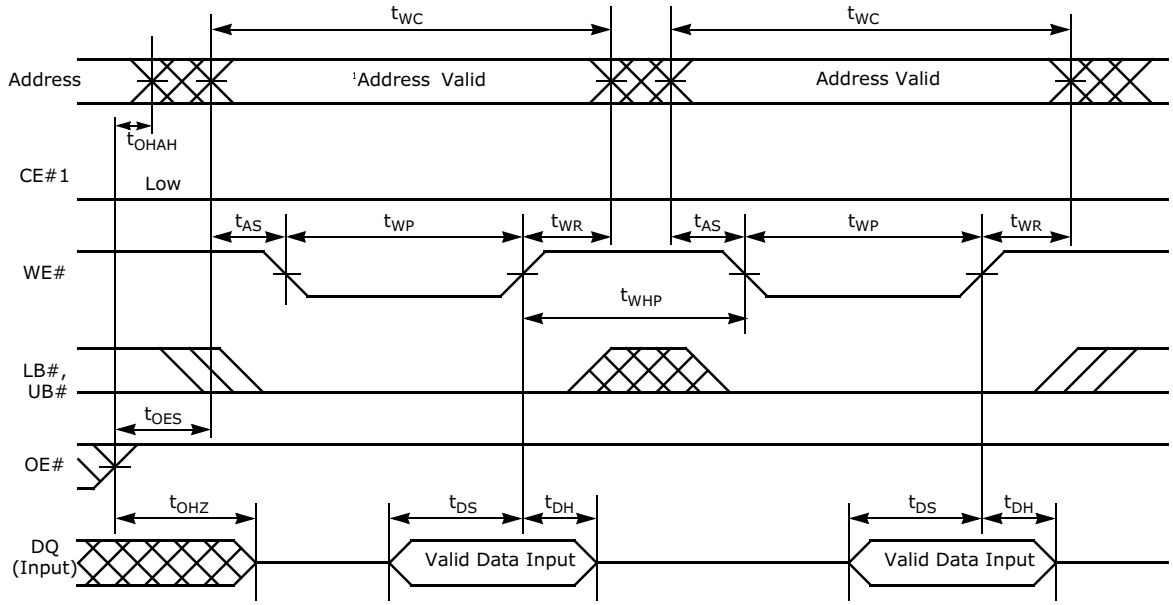
Note: *This timing diagram assumes CE2=H and WE#=H.*

Figure 94. Read Timing #3 (LB# / UB# Byte Access)



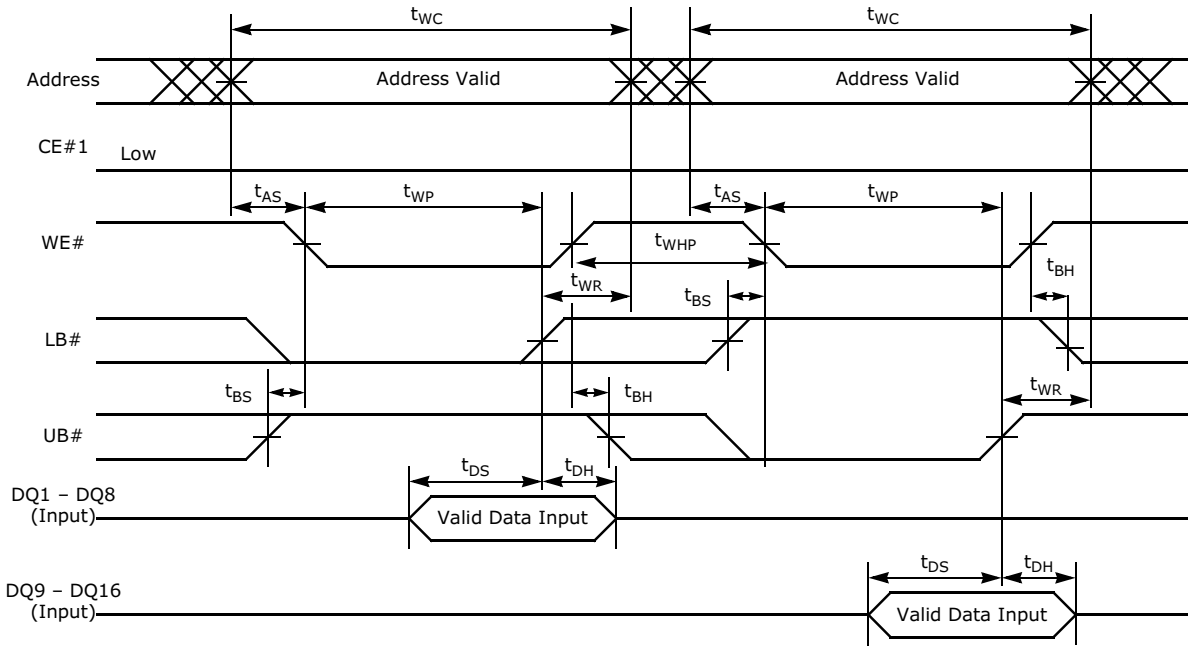
Note: *This timing diagram assumes CE2=H.*

Figure 95. Write Timing #I (Basic Timing)



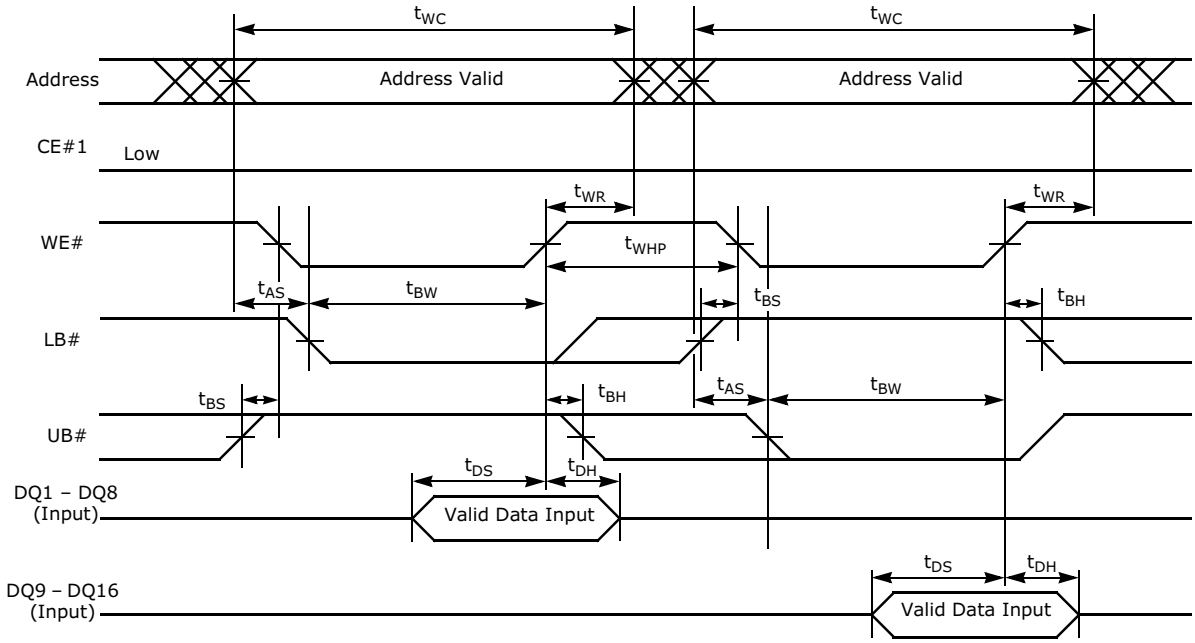
Note: *This timing diagram assumes CE2=H.*

Figure 96. Write Timing #2 (WE# Control)



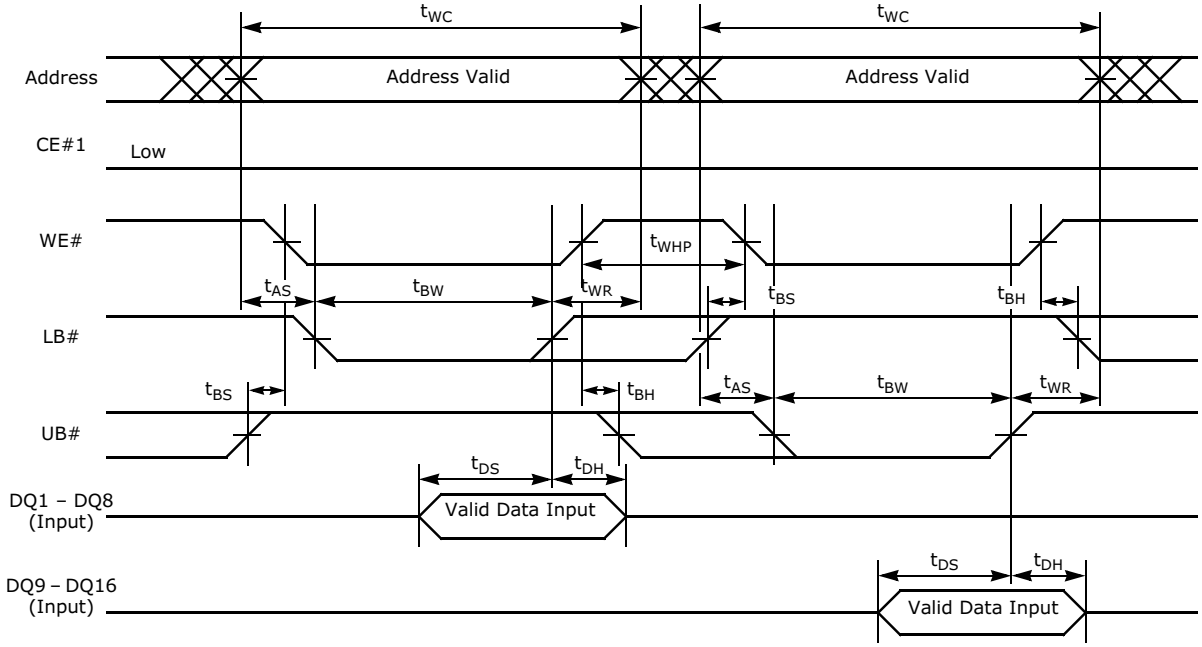
Note: *This timing diagram assumes CE2=H and OE#=H.*

Figure 97. Write Timing #3 – I (WE# / LB# / UB# Byte Write Control)



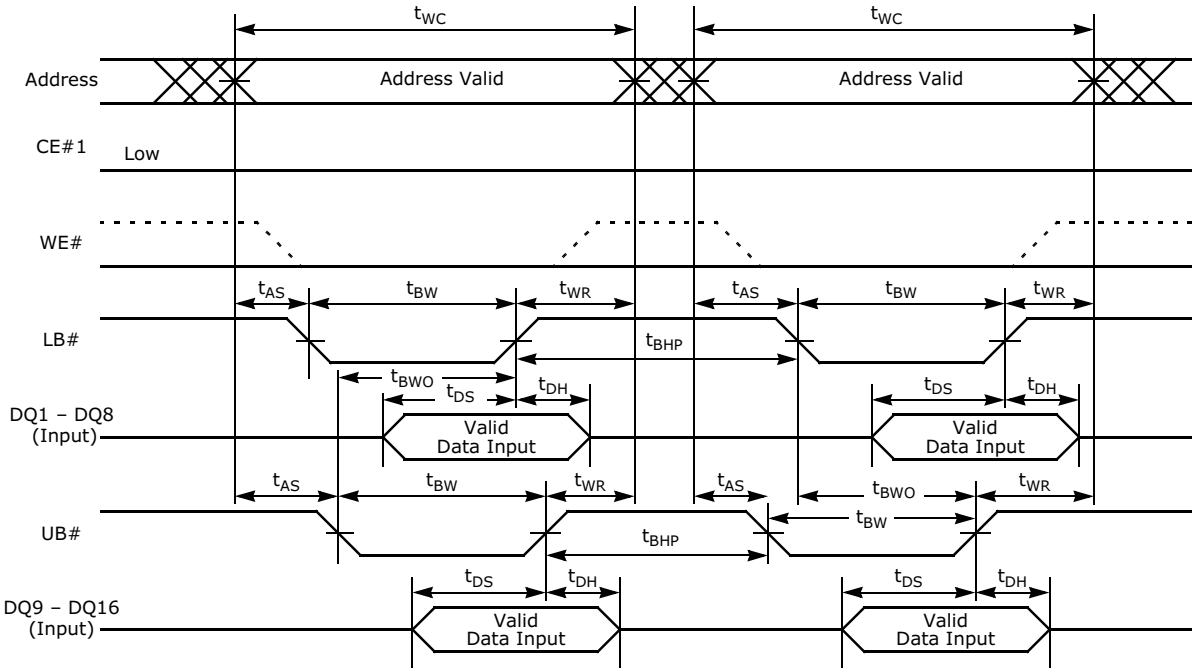
Note: *This timing diagram assumes CE2=H and OE#=H.*

Figure 98. Write Timing #3 – 2 (WE# / LB# / UB# Byte Write Control)



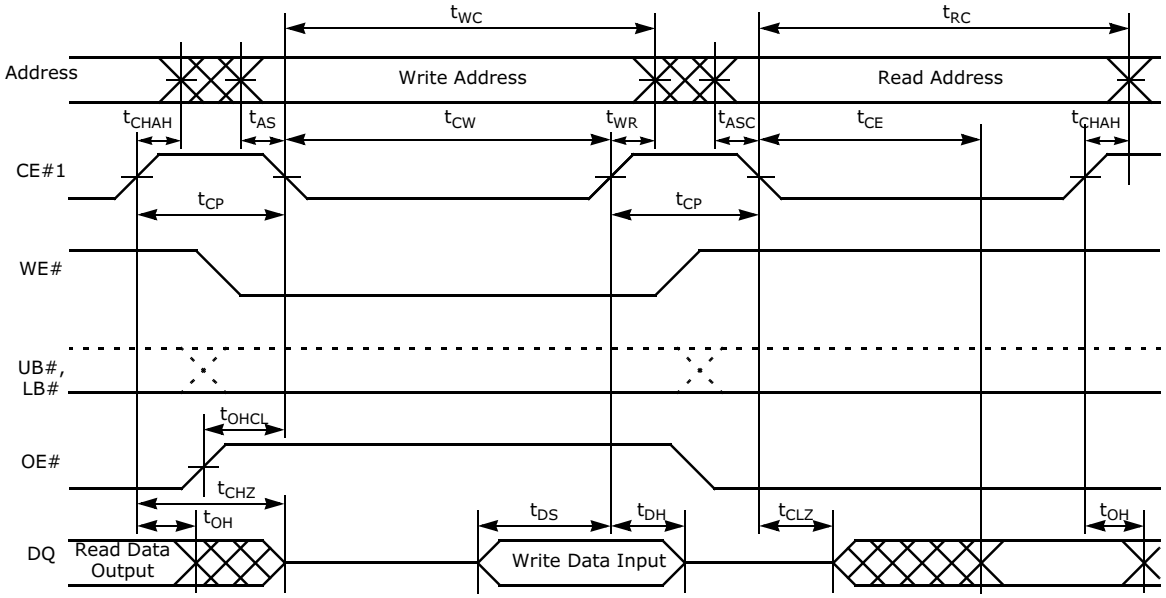
Note: *This timing diagram assumes CE2=H and OE#=H.*

Figure 99. Write Timing #3 – 3 (WE# / LB# / UB# Byte Write Control)



Note: *This timing diagram assumes CE2=H and OE#=H.*

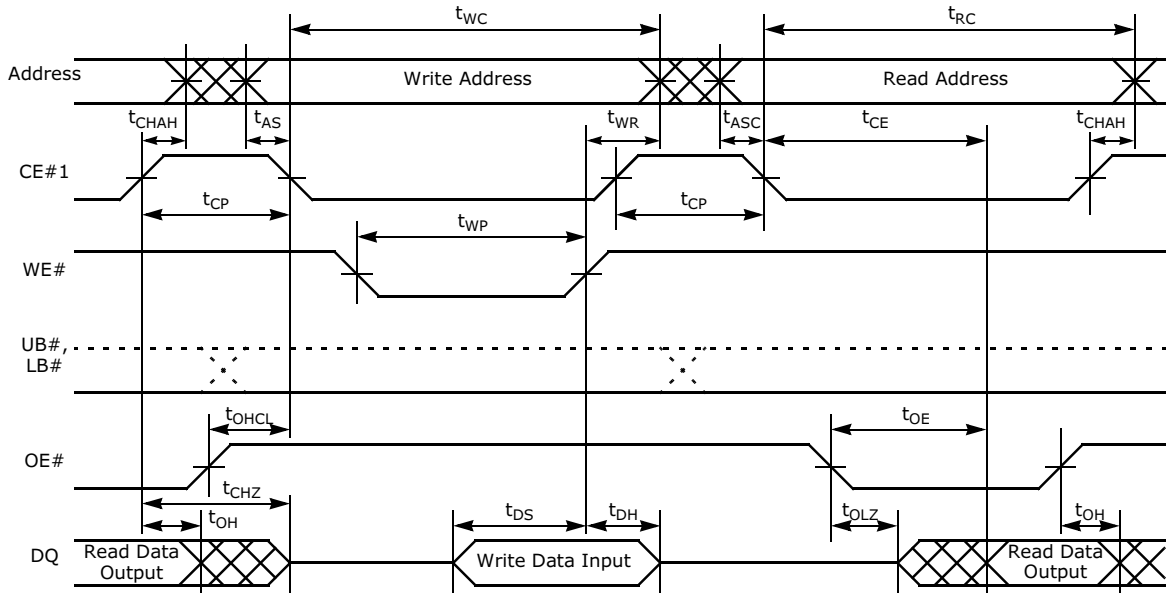
Figure 100. Write Timing #3 – 4 (WE# / LB# / UB# Byte Write Control)



Notes:

1. *This timing diagram assumes CE2=H.*
2. *Write address is valid from either CE#1 or WE# of last falling edge.*

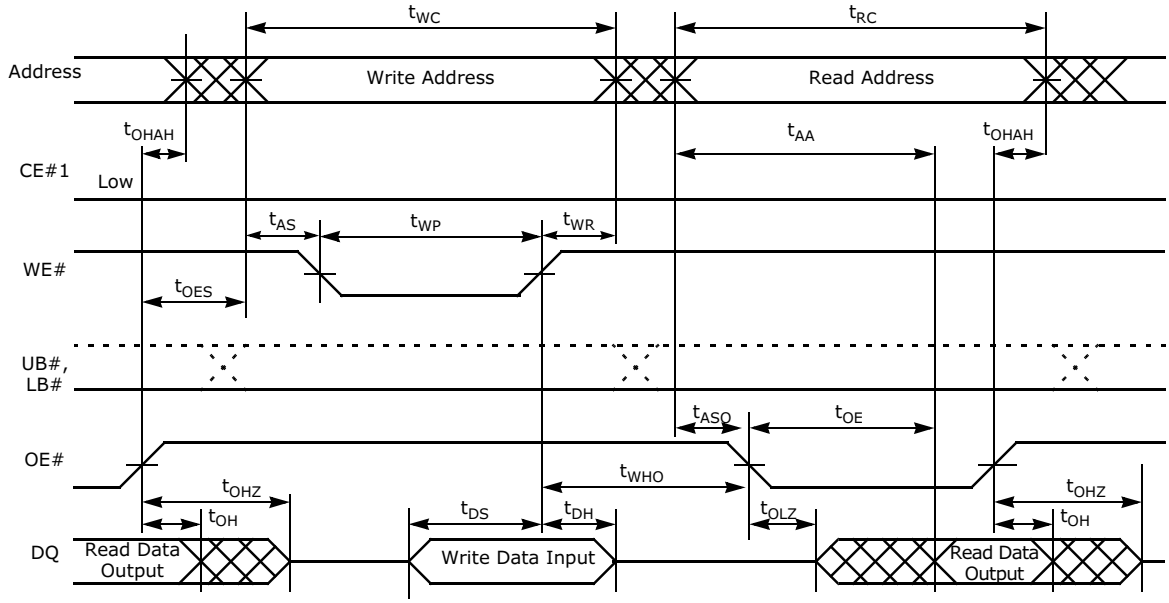
Figure 101. Read / Write Timing #1 – 1 (CE#1 Control)



Notes:

1. *This timing diagram assumes CE2=H.*
2. *OE# can be fixed Low during write operation if it is CE#1 controlled write at Read-Write-Read sequence.*

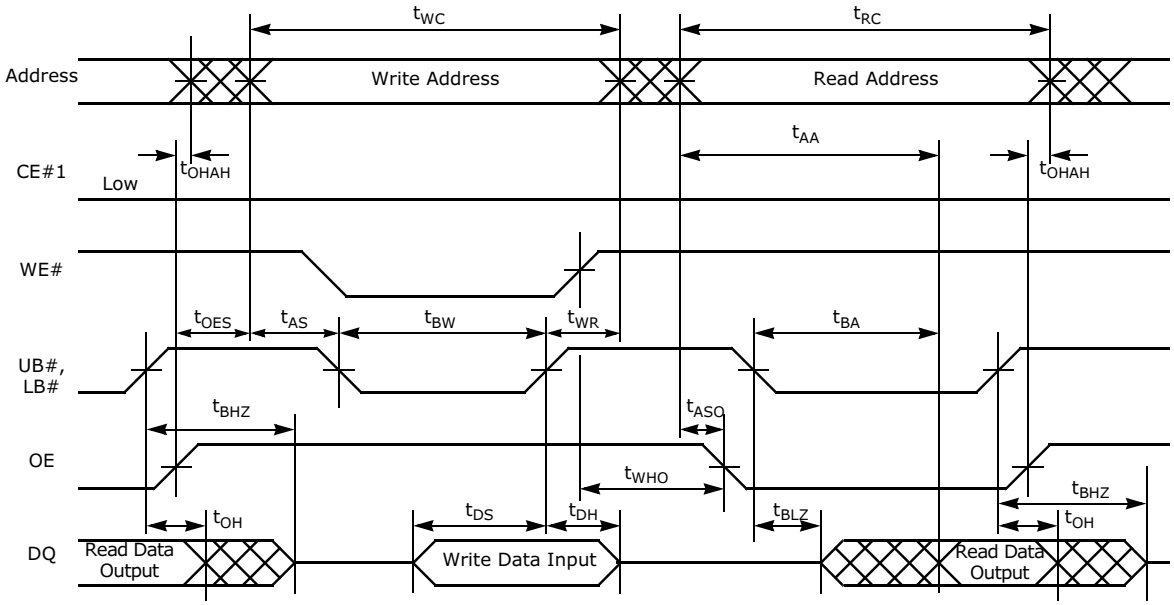
Figure 102. Read / Write Timing #1 – 2 (CE#1 / WE# / OE# Control)



Notes:

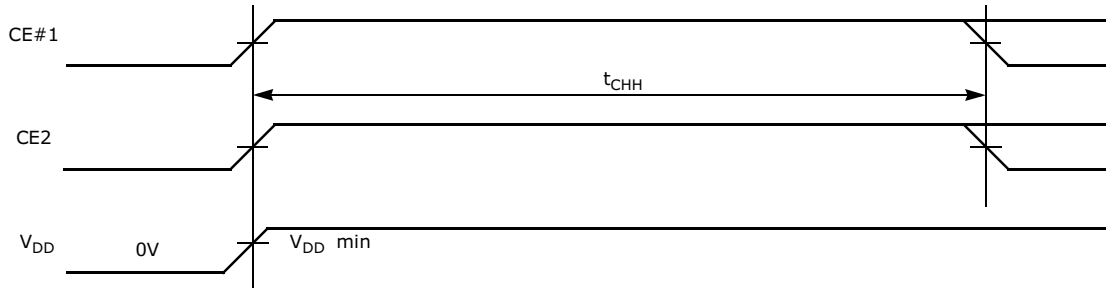
1. *This timing diagram assumes CE2=H.*
2. *CE#1 can be tied to Low for WE# and OE #controlled operation.*

Figure 103. Read / Write Timing #2 (OE#, WE# Control)



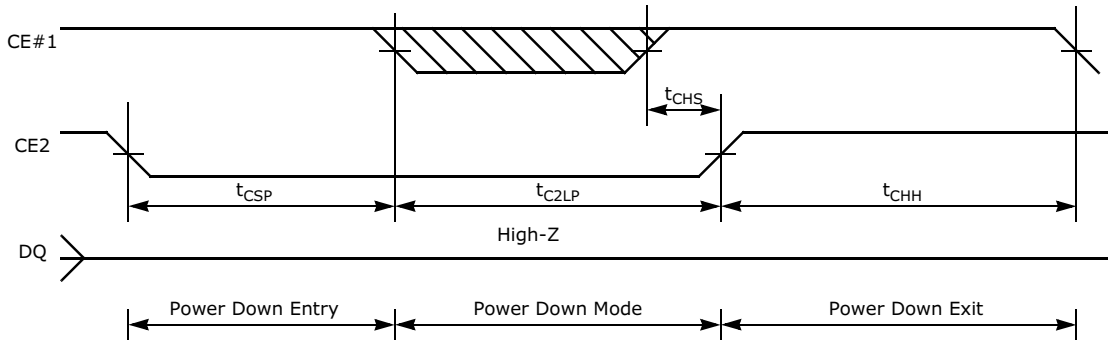
Notes:
1. *This timing diagram assumes CE2=H.*
2. *CE#1 can be tied to Low for WE# and OE# controlled operation.*

Figure 104. Read / Write Timing #3 ($\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Control



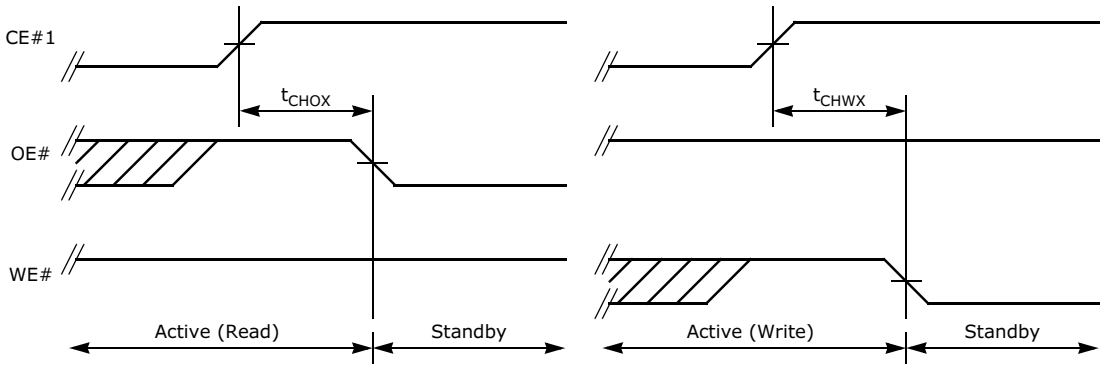
Note: *The t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable both CE#1 and CE2.*

Figure 105. Power-Up Timing



Note: *This Power-down mode can be also used as a reset timing if Power-up timing above could not be satisfied and Power-down program was not performed prior to this reset.*

Figure 106. Power-Down Entry and Exit Timing



Note: *Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes t_{RC} (min) period for Standby mode from CE#1 Low to High transition.*

Figure 107. Standby Entry Timing after Read or Write

COSMORAM Type I Revision Summary

Revision A0 (August 2, 2005)

Initial release.

Revision Summary

Revision A0 (October 27, 2004)

Initial release.

Revision A1 (July 5, 2005)

Added TSC080 Package Drawing
Minor corrections and changes

Initial release.

Revision A2 (August 19, 2005)

Added 16 Mb COSMORAM Type 1 module