2.7 V TO 5.5 V, 1-/8-CHANNEL, 10-BIT, PARALLEL ANALOG-TO-DIGITAL CONVERTERS

SLAS170D –MARCH 1999 – REVISED JULY 2000

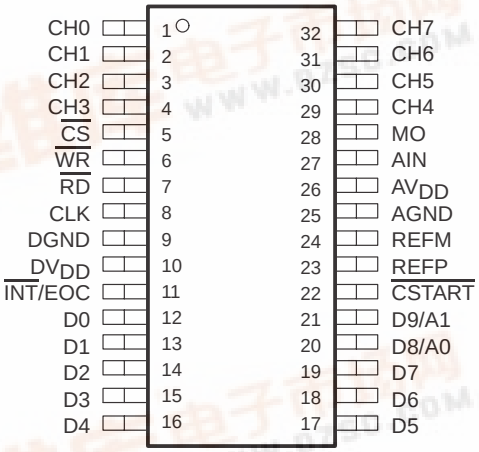
features

- Fast Throughput Rate: 1.25 MSPS at 5 V, 625 KSPS at 3 V
- Wide Analog Input: 0 V to AV_{DD}
- Differential Nonlinearity Error: < ± 1 LSB
- Integral Nonlinearity Error: < ± 1 LSB
- 8-to-1 Analog MUX – TLV1578
- Internal OSC
- Single 2.7-V to 5.5-V Supply Operation
- Low Power: 12 mW at 3 V and 35 mW at 5 V
- Auto Power Down of 1 mA Max
- Software Power Down: 10 μA Max
- Hardware Configurable
- DSP and Microcontroller Compatible Parallel Interface
- Binary/Twos Complement Output
- Hardware Controlled Extended Sampling
- Channel Sweep Mode Operation and Channel Select
- Hardware or Software Start of Conversion

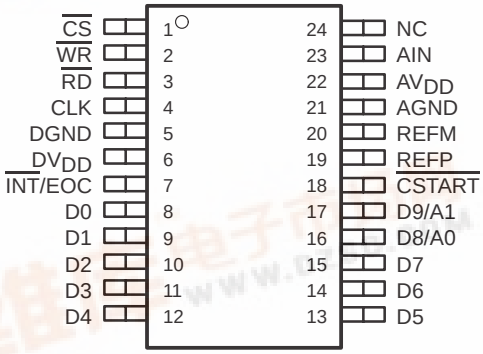
applications

- Mass Storage and HDD
- Automotive
- Digital Servos
- Process Control
- General-Purpose DSP
- Image Sensor Processing

TLV1578
DA PACKAGE
(TOP VIEW)



TLV1571
DW OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLV1571/1578 is a 10-bit data acquisition system that combines an 8-channel input multiplexer (MUX), a high-speed 10-bit ADC, and a parallel interface. The device contains two on-chip control registers allowing control of channel selection, software conversion start, and power down via the bidirectional parallel port. The control registers can be set to a default mode by applying a dummy $\overline{RD}$ signal when $\overline{WR}$ is tied low. This allows the TLV1571/1578 to be configured by hardware. The MUX is independently accessible. This allows the user to insert a signal conditioning circuit such as an antialiasing filter or an amplifier, if required, between the MUX and the ADC. Therefore, one signal conditioning circuit can be used for all eight channels. The TLV1571 is a single channel analog input device with all the same functions as the TLV1578.

The TLV1571/TLV1578 operates from a single 2.7-V to 5.5-V power supply. It accepts an analog input range from 0 V to AV_{DD} and digitizes the input at a maximum 1.25 MSPS throughput rate at 5 V. The power dissipations are only 12 mW with a 3-V supply or 35 mW with a 5-V supply. The device features an auto power-down mode that automatically powers down to 1 mA 50 ns after conversion is performed. In software power-down mode, the ADC is further powered down to only 10 μA.

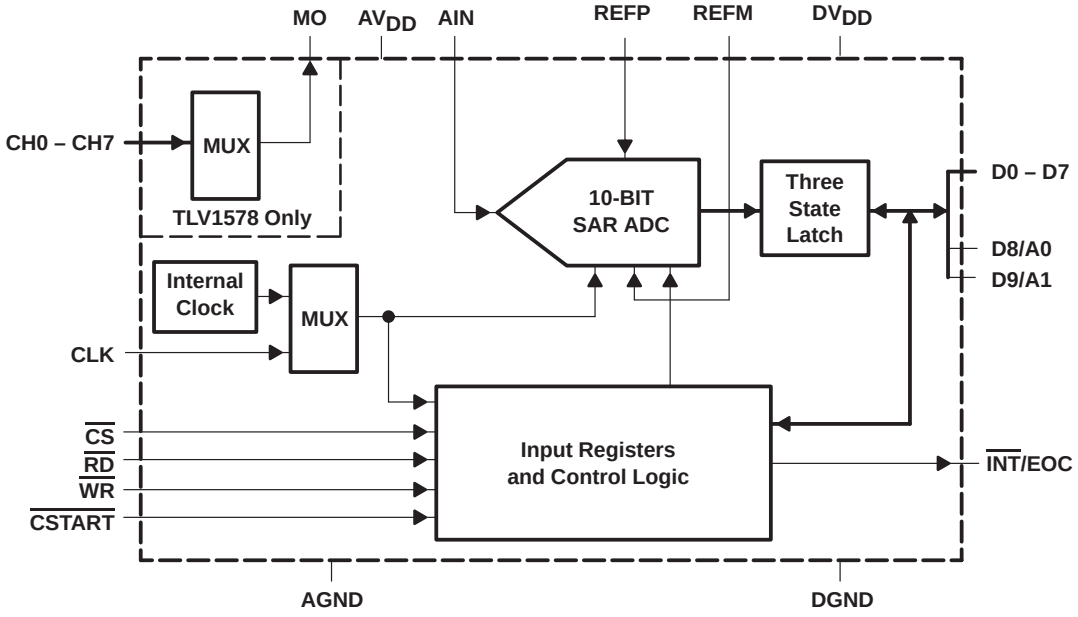
description (continued)

Very high throughput rate, simple parallel interface, and low power consumption make the TLV1571/TLV1578 an ideal choice for high-speed digital signal processing requiring multiple analog inputs.

AVAILABLE OPTIONS

T_A	PACKAGE		
	32 TSSOP (DA)	24 SOP (DW)	24 TSSOP (PW)
0°C to 70°C	TLV1578CDA	TLV1571CDW	TLV1571CPW
–40°C to 85°C	TLV1578IDA	TLV1571IDW	TLV1571IPW

functional block diagram – TLV1571/78



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	TLV1571	TLV1578		
AGND	21	25		Analog ground
AIN	23	27	I	ADC analog input (used as single analog input channel for TLV1571)
AV_{DD}	22	26		Analog supply voltage, 2.7 V to 5.5 V
CH0 – CH7	–	1–4, 29–32	I	Analog input channels
CLK	4	8	I	External clock input
$\overline{CS}$	1	5	I	Chip select. A logic low on $\overline{CS}$ enables the TLV1571/TLV1578.
$\overline{CSTART}$	18	22	I	Hardware sample and conversion start input. The falling edge of $\overline{CSTART}$ starts sampling and the rising edge of $\overline{CSTART}$ starts conversion.
DGND	5	9		Digital ground
DV_{DD}	6	10		Digital supply voltage, 2.7 V to 5.5 V
D0 – D7	8–12, 13–15	12–16, 17–19	I/O	Bidirectional 3-state data bus
D8/A0	16	20	I/O	Bidirectional 3-state data bus. D8/A0 along with D9/A1 is used as address lines to access CR0 and CR1 for initialization.
D9/A1	17	21	I/O	Bidirectional 3-state data bus. D9/A1 along with D8/A0 is used as address lines to access CR0 and CR1 for initialization.
$\overline{INT}$/EOC	7	11	O	End-of-conversion/interrupt
MO		28	O	On-chip MUX analog output
NC	24			Not connected
$\overline{RD}$	3	7	I	Read data. A falling edge on $\overline{RD}$ enables a read operation on the data bus when $\overline{CS}$ is low.
REFM	20	24	I	Lower reference voltage (nominally ground). REFM must be supplied or REFM pin must be grounded.
REFP	19	23	I	Upper reference voltage (nominally AV_{DD}). The maximum input voltage range is determined by the difference between the voltage applied to REFP and REFM.
$\overline{WR}$	2	6	I	Write data. A rising edge on the $\overline{WR}$ latches in configuration data when $\overline{CS}$ is low. When using software conversion start, a rising edge on $\overline{WR}$ also initiates an internal sampling start pulse. When $\overline{WR}$ is tied to ground, the ADC in nonprogrammable (hardware configuration mode).

detailed description

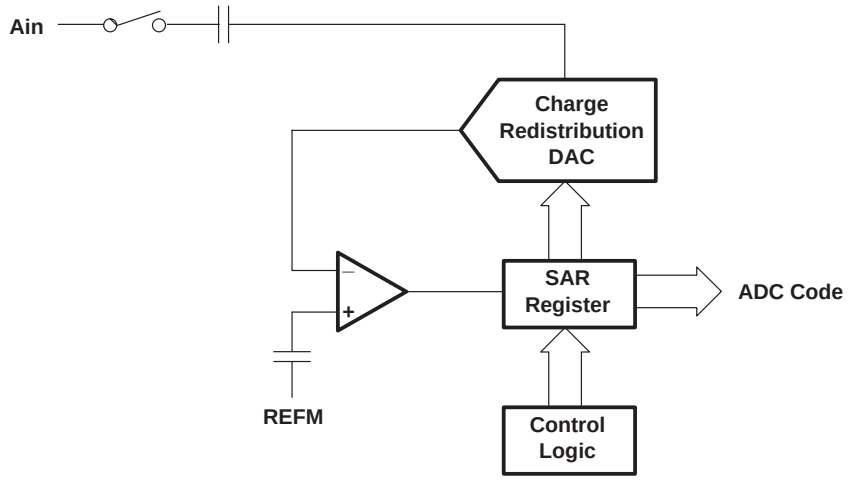


Figure 1. Analog-to-Digital SAR Converter

The TLV1571/78 is a successive-approximation ADC utilizing a charge redistribution DAC. Figure 1 shows a simplified version of the ADC.

The sampling capacitor acquires the signal on AIN during the sampling period. When the conversion process starts, the SAR control logic and charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator into a balanced condition. When the comparator is balanced, the conversion is complete and the ADC output code is generated.

sampling frequency, f_S

The TLV1571/TLV1578 requires 16 CLKs for each conversion, (assuming the read cycle takes 1 CLK). The equivalent maximum sampling frequency achievable with a given CLK frequency is:

$$f_{s(max)} = (1/17)\, f_{CLK}$$

The TLV1571 and TLV1578 are software configurable. The first two MSB bits, D(9,8) are used to address which register to set. The rest of the eight bits are used as control data bits. There are two control registers, CR0 and CR1, that are user configurable. All of the register bits are written to the control register during write cycles. A description of the control registers is shown in Figure 2.

detailed description (continued)

control registers

A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Control Register Zero (CR0)

	D7	D6	D5	D4	D3	D2	D1	D0
A(1:0)=00	STARTSEL	PROGEOC	CLKSEL	SWPWDN	MODESEL	CHSEL(2–0)†		

D7	D6	D5	D4	D3
0: HARDWARE START (CSTART) 1: SOFTWARE START	0: INT 1: EOC	0: Internal Clock 1: External Clock	0: NORMAL 1: Power Down	0: Single Channel 1: Sweep Mode

D(2–0)	Single Input	Channels Swept
0h	0	0,1
1h	1	0,1,2,3
2h	2	0,1,2,3,4,5,
3h	3	0,1,2,3,4,5,6,7
4h	4	N/A
5h	5	N/A
6h	6	N/A
7h	7	N/A

Control Register One (CR1)

	D7‡	D6	D5‡	D4‡	D3	D2	D1	D0
A(1:0)=01	RESERVED	OSCSPD	0 Reserved	0 Reserved	OUTCODE	READREG	STEST1	STEST0

D7	D6	D5	D4	D3	D2
0: Reserved Bit Always Write 0	0: INT. OSC. SLOW 1: INT. OSC. FAST	0: Reserved Bit Always Write 0	0: Reserved Bit, Always Write 0	0: Binary 1: 2s Complement	0: Enable Self Test 1: Enable Register Read back

CR1.(1–0)	IF READREG = 0 ACTION
0h	Output = CONVERSION result
1h	Output = SELF TEST 1 result
2h	Output = SELF TEST 2 result
3h	Output = SELF TEST 3 result

CR1.(1–0)	IF READREG = 1
0h	Output Contents of CR0
1h	Output Contents of CR1
2h	RESERVED
3h	RESERVED

† Don't care for TLV1571
‡ When in read back mode, the values read from the control register reserved bits are don't care.

Figure 2. Input Data Format

detailed description (continued)

hardware configuration option

The TLV1571/TLV1578 can configure itself. This option is enabled when the $\overline{WR}$ pin is tied to ground and a dummy $\overline{RD}$ signal is applied. The ADC is now fully configured. Zeros or default values are applied to both control registers. The ADC is configured ideally for 3-V operation, which means the internal OSC is set at 10 MHz, single channel input mode, and hardware start of conversion using $\overline{CSTART}$.

ADC conversion modes

The TLV1571/TLV1578 provides two conversion modes and two start of conversion modes. In single channel input mode, a single channel is continuously sampled and converted. In sweep mode (only available for the TLV1578), a predetermined set of channels is continuously sampled and converted. Table 1 explains these modes in more detail.

Table 1. Conversion Modes

MODES	START OF CONVERSION	OPERATION	COMMENT–SET BITS CR0.D(2–0) FOR INPUT
Single Channel Input† CR0.D3 = 0 CR1.D7 = 0	Hardware Start ($\overline{CSTART}$) CR0.D7 = 0	• Repeated conversions from a selected channel • $\overline{CSTART}$ falling edge to start sampling • $\overline{CSTART}$ rising edge to start conversion • If in INT mode, one $\overline{INT}$ pulse generated after each conversion • If in EOC mode, EOC will go high to low at start of conversion, and return high at end of conversion.	$\overline{CSTART}$ rising edge must be applied a minimum of 5 ns before or after CLK rising edge.
	Software Start CR0.D7 = 1	• Repeated conversions from a selected channel • $\overline{WR}$ rising edge to start sampling initially. Thereafter, sampling occurs at the rising edge of $\overline{RD}$. • Conversion begins after 6 clocks after sampling has begun. Thereafter, if in INT mode, one $\overline{INT}$ pulse is generated after each conversion • If in EOC mode, EOC will go high to low at start of conversion and return high at end of conversion.	With external clock, $\overline{WR}$ and $\overline{RD}$ rising edge must be a minimum 5 ns before or after CLK rising edge.
Channel Sweep CR0.D3 = 1 CR1.D7 = 0	Hardware Start ($\overline{CSTART}$) CR0.D7 = 0	• One conversion per channel from a predetermined sequence of channels • $\overline{CSTART}$ falling edge to start sampling • $\overline{CSTART}$ rising edge to start conversion • If in INT mode, one INT pulse generated after each conversion • If in EOC mode, EOC will go high to low at start of conversion, and return high at end of conversion.	$\overline{CSTART}$ rising edge must be applied a minimum of 5 ns before or after CLK rising edge.
	Software Start CR0.D7 = 1	• One conversion per channel from a sequence of channels • $\overline{WR}$ rising edge to start sampling • ADC proceeds to sample next channel at rising edge of $\overline{RD}$. Conversion begins after 6 clocks and lasts 10 clocks • If in INT mode, one $\overline{INT}$ pulse generated after each conversion • If in EOC mode, EOC will go high to low at start of conversion and return high at end of conversion.	With external clock, $\overline{WR}$ and $\overline{RD}$ rising edge must be a minimum 5 ns before or after CLK rising edge.

† Single channel input mode repeatedly samples and converts from the channel until $\overline{WR}$ is applied.

detailed description (continued)

configure the device

The device can be configured by writing to control registers CR0 and CR1.

Table 2. TLV1571/TLV1578 Programming Examples

REGISTER	INDEX		D7	D6	D5	D4	D3	D2	D1	D0	COMMENT
	D9	D8									
EXAMPLE1											
CR0	0	0	0	0	0	0	0	0	0	0	Single channel
CR1	0	1	0	0	0	0	0	1	0	0	Single Input
EXAMPLE2											
CR0	0	0	0	1	1	0	1	0	1	1	Sweep mode
CR1	0	1	0	0	0	0	1	1	0	0	2s complement output

register read back

Control data written to the TLV1571/78 can be read back from the control registers CR0 and CR1. See Figure 2.

NOTE:
Data read out of CR1 reserved bits is don't care.

power down

The TLV1571/TLV1578 offers two power down modes, auto power down and software power down. This device will automatically proceed to auto power-down mode if $\overline{RD}$ is not present one clock after conversion. Software power down is controlled directly by the user by pulling $\overline{CS}$ to DV_{DD}.

Table 3. Power Down Modes

PARAMETERS/MODES	AUTO POWER DOWN	SOFTWARE POWER DOWN ($\overline{CS}$ = DV_{DD})
Maximum power down dissipation current	1 mA	10 μA
Comparator	Power down	Power down
Clock buffer	Power down	Power down
Reference	Active	Power down
Control registers	Saved	Saved
Minimum power down time	1 CLK	2 CLK
Minimum resume time	1 CLK	2 CLK

self-test modes

The TLV1571/TLV1578 provides three self test modes. These modes can be used to check whether the ADC itself is working properly without having to supply an external signal. There are three tests that are controlled by writing to CR1(D1,D0) (see Table 4).

Table 4. Self Tests

CR1(D1,D0)	SELF TEST VOLTAGE APPLIED	DIGITAL OUTPUT
0h	Normal, no self test applied	N/A
1h	VREFM applied to ADC input internally	000h
2h	(VREFP–VREFM)/2 applied to ADC input internally	200h
3h	VIN = VREFP applied to ADC input internally	3FFh

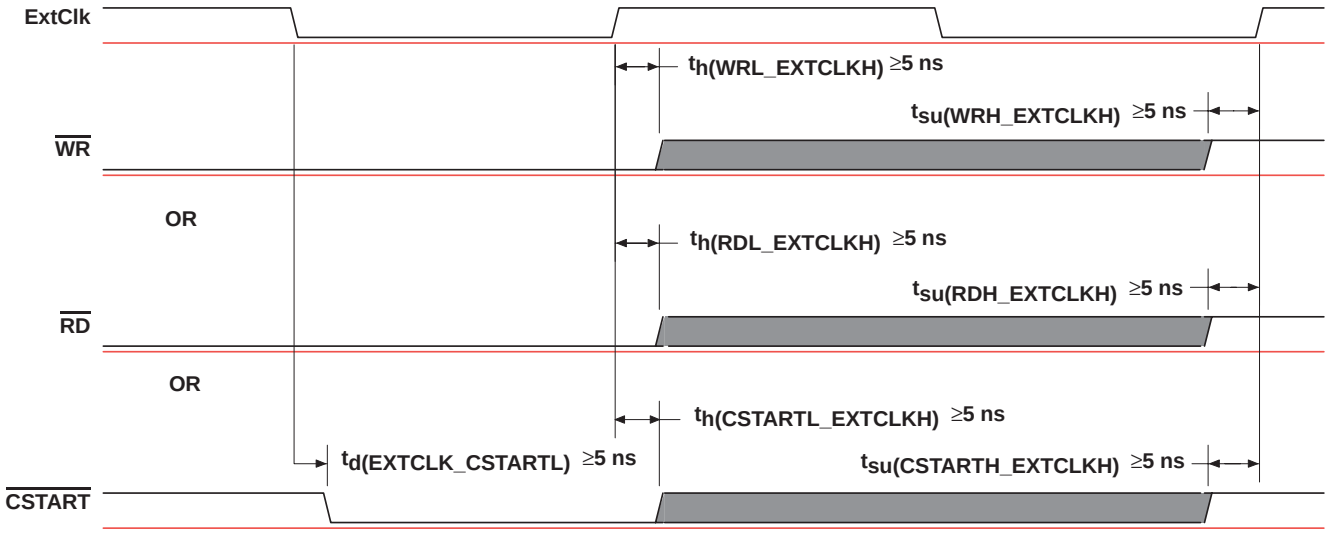
detailed description (continued)

reference voltage input

The TLV1571/TLV1578 has two reference input pins: REFP and REFM. The voltage levels applied to these pins establish the upper and lower limits of the analog inputs to produce a full-scale and zero-scale reading respectively. The values of REFP, REFM, and the analog input should not exceed the positive supply or be less than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REFP and is at zero when the input signal is equal to or lower than REFM.

sampling/conversion

All sampling, conversion, and data output in the device are started by a trigger. This could be the $\overline{RD}$, $\overline{WR}$, or $\overline{CSTART}$ signal depending on the mode of conversion and configuration. The rising edge of $\overline{RD}$, $\overline{WR}$, and $\overline{CSTART}$ signal are extremely important, since they are used to start the conversion. These edges need to stay close to the rising edge of the external clock (if external clock is used as source of conversion clock). The minimum setup and hold time with respect to the rising edge of the external clock should be 5 ns minimum. When the internal clock is used, this is not an issue since these two edges will start the internal clock automatically. Therefore, the setup time is always met. Software controlled sampling lasts 6 clock cycles. This is done via the CLK input or the internal oscillator if enabled. The input clock frequency can be 1 MHz to 20 MHz, translating into a sampling time from 0.6 µs to 0.3 µs. The internal oscillator frequency is 9 MHz minimum (oscillator frequency is between 9 MHz to 22 MHz), translating into a sampling time from 0.6 µs to 0.3 µs. Conversion begins immediately after sampling and lasts 10 clock cycles. This is again done using the external clock input (1 MHz–20 MHz) or the internal oscillator (9 MHz minimum) if enabled. Hardware controlled sampling, via $\overline{CSTART}$, begins on falling $\overline{CSTART}$ lasts the length of the active $\overline{CSTART}$ signal. This allows more control over the sampling time, which is useful when sampling sources with large output impedances. On rising $\overline{CSTART}$, conversion begins. Conversion in hardware controlled mode also lasts 10 clock cycles. This is done using the external clock input (1 MHz–20 MHz) or the internal oscillator (9 MHz minimum) as is the case in software controlled mode.



NOTE: t_{su} = setup time, t_h = hold time

Figure 3. Trigger Timing – Software Start Mode Using External Clock

start of conversion mechanism

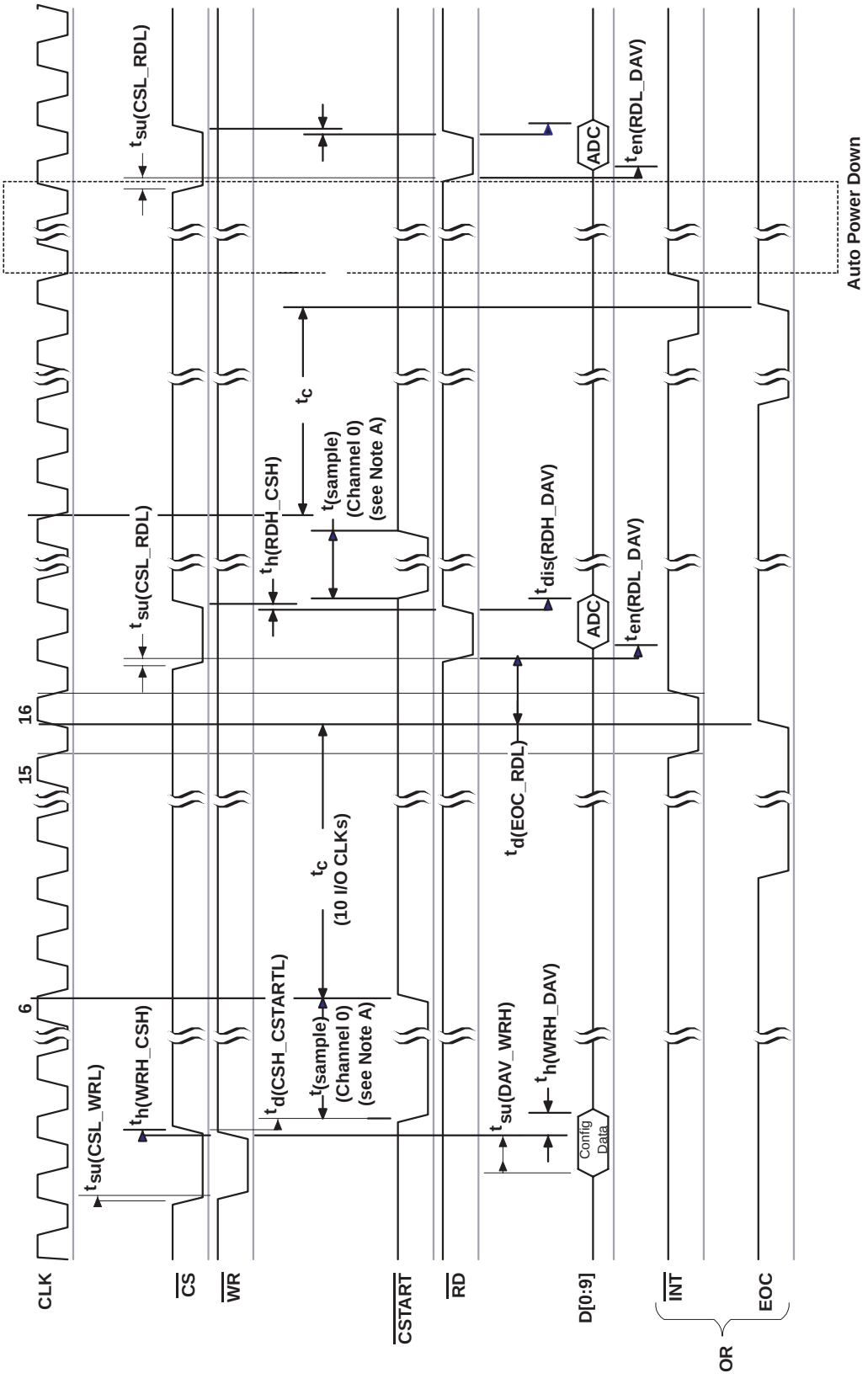
There are two ways to convert data: hardware and software. In the hardware conversion mode the ADC begins sampling at the falling edge of $\overline{\text{CSTART}}$ and begins conversion at the rising edge of $\overline{\text{CSTART}}$. Software start mode ADC samples for 6 clocks, then conversion occurs for ten clocks. The total sampling and conversion process lasts only 16 clocks in this case. If $\overline{\text{RD}}$ is not detected during the next clock cycle, the ADC automatically proceeds to a power-down state. Data is valid on the rising edge of $\overline{\text{INT}}$ in both conversion modes.

hardware CSTART conversion

external clock

With $\overline{\text{CS}}$ low and $\overline{\text{WR}}$ low, data is written into the ADC. The sampling begins at the falling edge of $\overline{\text{CSTART}}$ and conversion begins at the rising edge of $\overline{\text{CSTART}}$. At the end of conversion, EOC goes from low to high, telling the host that conversion is ready to be read out. The external clock is active and is used as the reference at all times. With this mode, it is required that $\overline{\text{CSTART}}$ is not applied at the rising edge of the clock (see Figure 4).

start of conversion mechanism (continued)

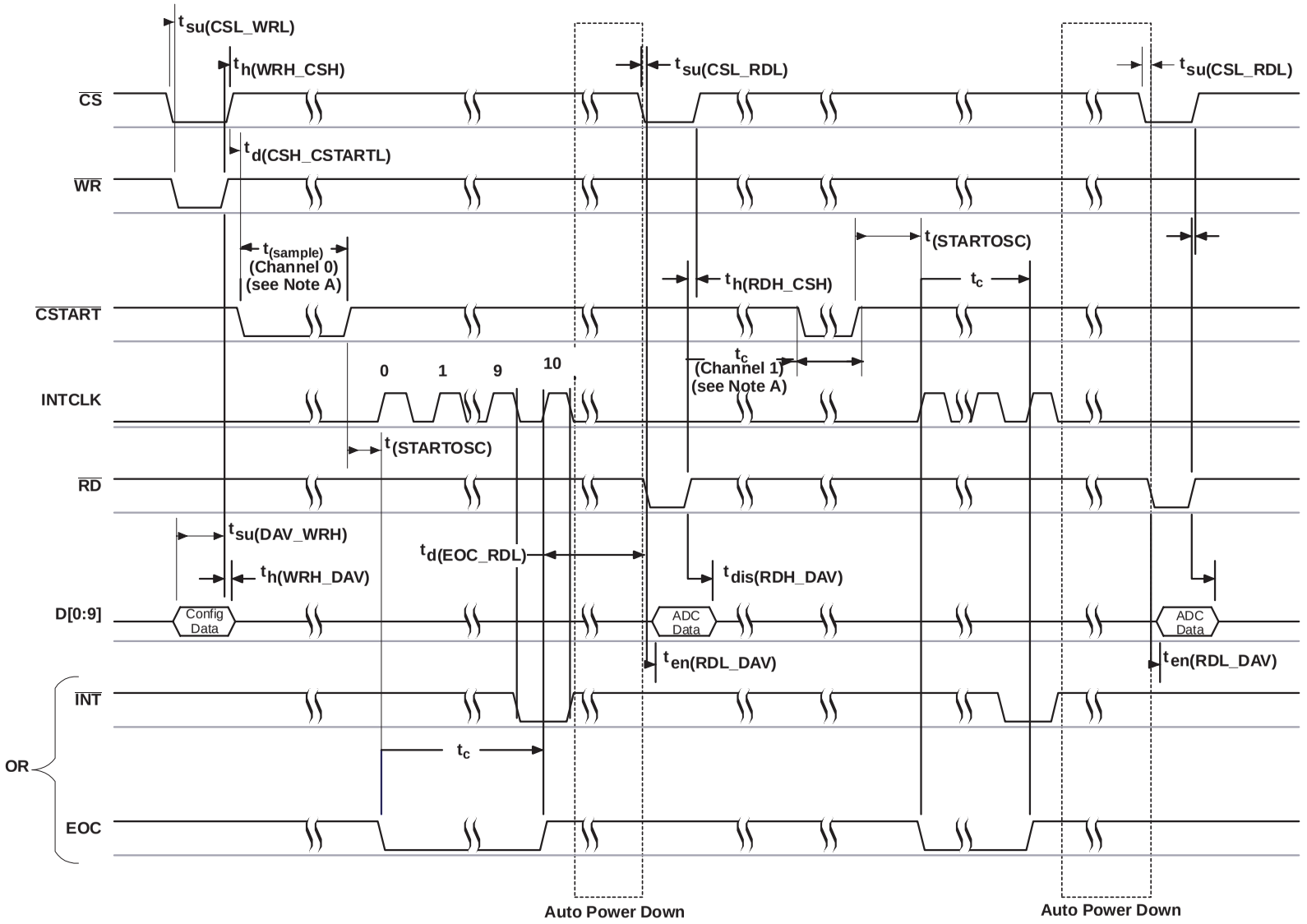


NOTE A: AIN for TLV1571; channels sweep according to register settings.

Figure 4. Multichannel Input Mode Conversion – Hardware $\overline{\text{CSTART}}$, External Clock

internal clock

In single channel input mode, with $\overline{CS}$ low and $\overline{WR}$ low, data is written into the ADC. The sampling begins at the falling edge of $\overline{CSTART}$, and conversion begins at the rising edge of $\overline{CSTART}$. The internal clock turns on at the rising edge of $\overline{CSTART}$. The internal clock is disabled after each conversion.



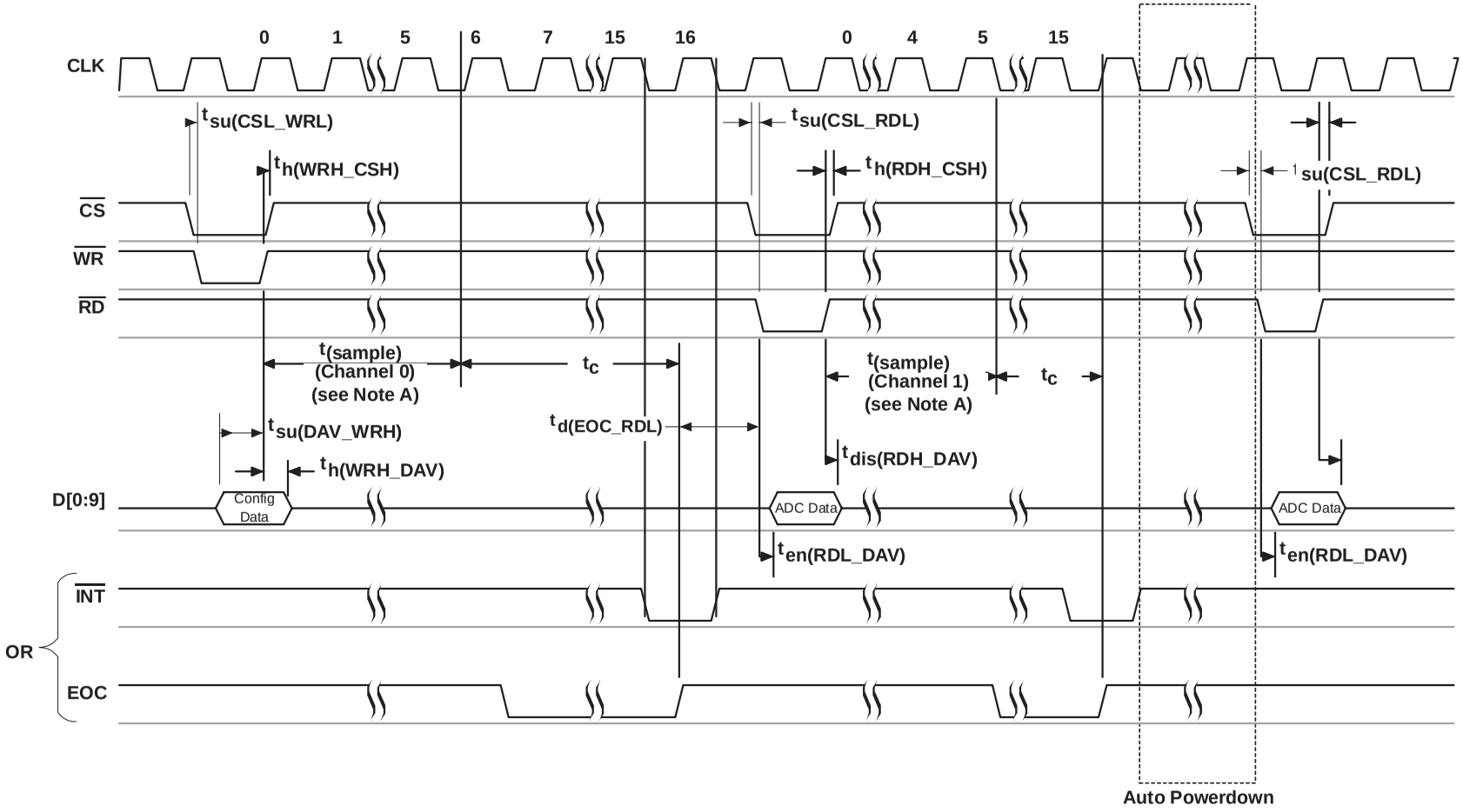
NOTE A: AIN for TLV1571; channels sweep according to register settings.

Figure 5. Multichannel Input Mode Conversion – Hardware $\overline{CSTART}$, Internal Clock

software START conversion

external clock

With $\overline{CS}$ low and $\overline{WR}$ low, data is written into the ADC. Sampling begins at the rising edge of $\overline{WR}$. The conversion process begins 6 clocks after sampling begins. At the end of conversion, INT goes low telling the host that conversion is ready to be read out. EOC is low during the conversion and makes a high-to-low transition at the end of the conversion. The external clock is active and is used as the reference at all times. With this mode, $\overline{WR}$ and $\overline{RD}$ should not be applied at the rising edge of the clock (see Figure 3).



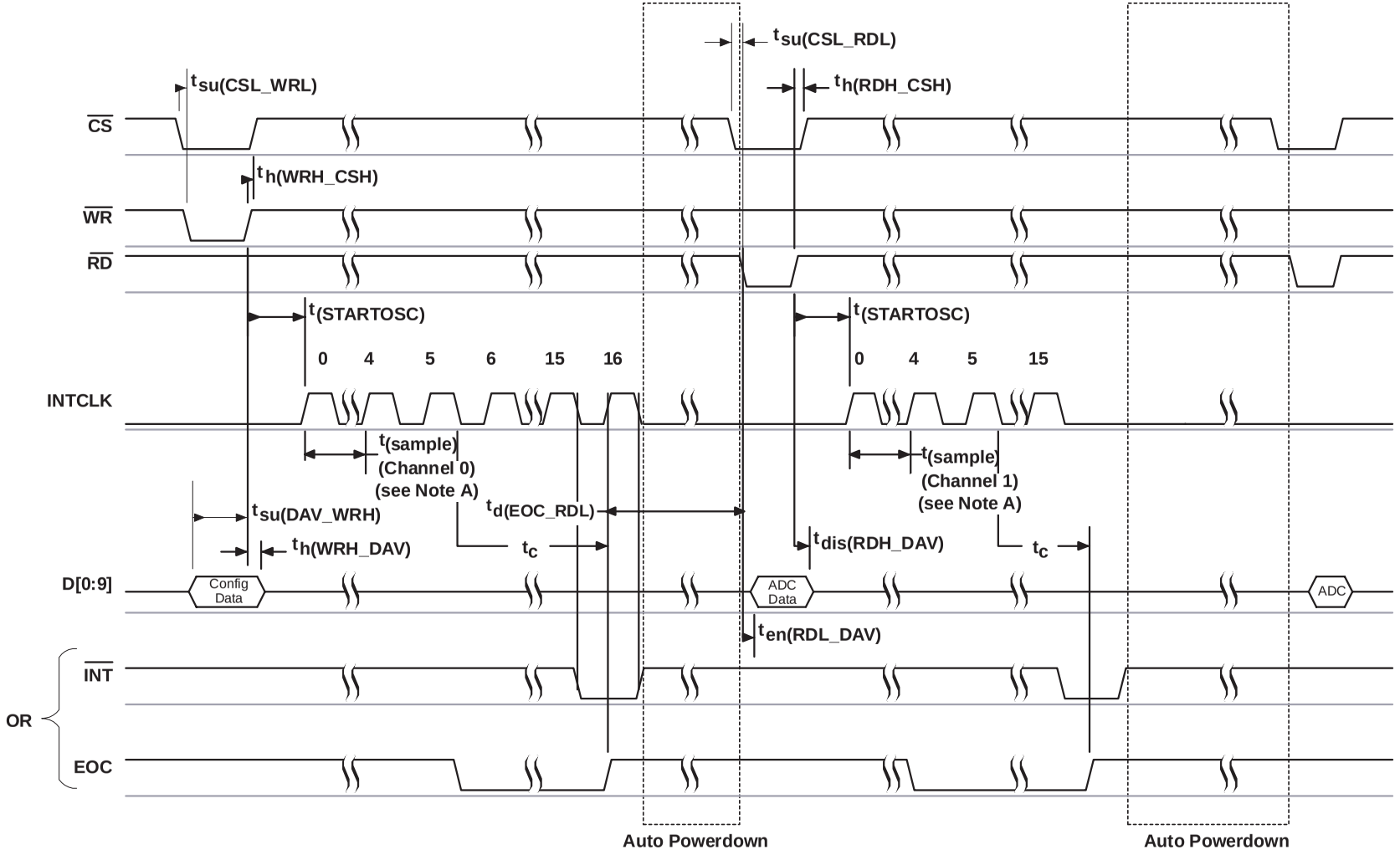
NOTE A: AIN for TLV1571; channels sweep according to register settings.

Figure 6. Multichannel Input Mode Conversion – Software Start, External Clock

software START conversion (continued)

internal clock

With $\overline{CS}$ low and $\overline{WR}$ low, data is written into the ADC. Sampling begins at the rising edge of $\overline{WR}$. Conversion begins 6 clocks after sampling begins. The internal clock begins at the rising edge of $\overline{WR}$. The internal clock is disabled after each conversion. Subsequent sampling begins at the rising edge of $\overline{RD}$.



NOTE A: AIN for TLV1571; channels sweep according to register settings.

Figure 7. Multichannel Input Mode Conversion – Software Start, Internal Clock

software START conversion (continued)

system clock source

The TLV1571/TLV1578 internally derives multiple clocks from the SYSCLK for different tasks. SYSCLK is used for most conversion subtasks. The source of SYSCLK is programmable via control register zero bit 5. The source of SYSCLK is changed at the rising edge of $\overline{WR}$ of the cycle when CR0.D5 is programmed.

internal clock (CR0.D5 = 0, SYSCLK = internal OSC)

The TLV1571/TLV1578 has a built-in 10 MHz OSC. When the internal OSC is selected as the source of SYSCLK, the internal clock starts with a delay (one half of the OSC period max) after the falling edge of the conversion trigger (either $\overline{WR}$, $\overline{RD}$, or $\overline{CSTART}$). The OSC speed can be set to 10 ± 1 MHz or 20 ± 2 MHz by setting register bit CR1.6.

external clock (CR0.D5 = 1, SYSCLK = external clock)

The TLV1571/TLV1578 is designed to accept an external clock input (CMOS/TTL logic) with frequencies from 1 MHz to 20 MHz.

host processor interface

The TLV1571/TLV1578 provides a generic high-speed parallel interface that is compatible with high-performance DSPs and general-purpose microprocessors. The interface includes D(0–9), $\overline{INT}$/EOC, $\overline{RD}$, and $\overline{WR}$.

output format

The data output format is unipolar (code 0 to 1023) when the device is operated in single-ended input mode. The output code format can be either binary or twos complement by setting register bit CR1.D3.

power up and initialization

After power up, $\overline{CS}$ must be low to begin an I/O cycle. $\overline{INT}$/EOC is initially high. The TLV1571/TLV1578 requires two write cycles to configure the two control registers. The first conversion after the device has returned from the power-down state may be invalid and should be disregarded.

definitions of specifications and terminology

integral nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

differential nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

zero offset

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

gain error

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

software START conversion (continued)

signal-to-noise ratio + distortion (SINAD)

Signal-to-noise ratio + distortion is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

effective number of bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)/6.02$$

it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, the effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

total harmonic distortion (THD)

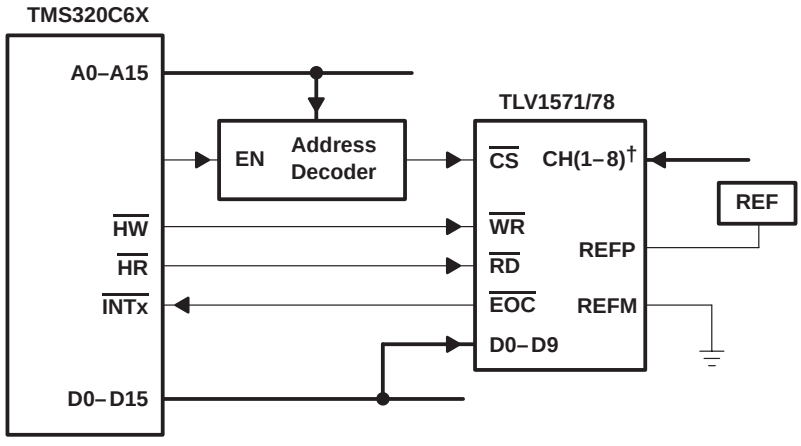
Total harmonic distortion is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

spurious free dynamic range (SFDR)

Spurious free dynamic range is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

DSP interface

The TLV1571/TLV1578 is a 10-bit 1-/8-analog input channel analog-to-digital converter with throughput up to 1.25 MSPS at 5 V and up to 625 KSPS at 3 V. To achieve 1.25 MSPS throughput, the ADC must be clocked at 20 MHz. Likewise to achieve 625 KSPS throughout, the ADC must be clocked at 10 MHz. The TLV1571/TLV1578 can be easily interfaced to microcontrollers, ASICs, and DSPs. Figure 8 shows the pin connections to interface the TLV1571/TLV1578 to the TMS320C6x DSP.



† The TLV1571 has only one analog input (AIN).

Figure 8. TMS320C6x DSP Interface

grounding and decoupling considerations

General practices should apply to the PCB design to limit high frequency transients and noise that are fed back into the supply and reference lines. This requires that the supply and reference pins be sufficiently bypassed. In most cases 0.1-μF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Since their effectiveness depends largely on the proximity to the individual supply pin, they should be placed as close to the supply pins as possible.

To reduce high frequency and noise coupling, it is highly recommended that digital and analog grounds be shorted immediately outside the package. This can be accomplished by running a low impedance line between DGND and AGND under the package.

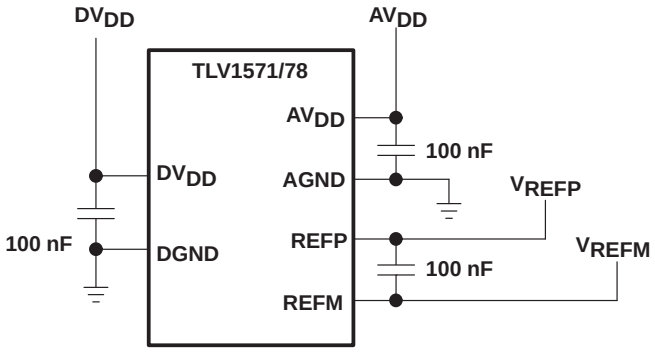
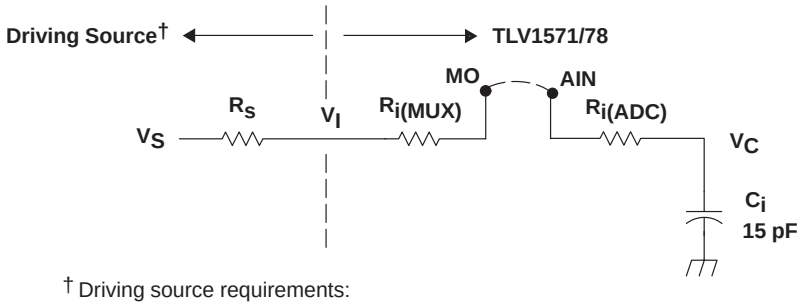


Figure 9. Placement for Decoupling Capacitors

power supply ground layout

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the ADC AGND terminal to the system analog ground plane making sure that analog ground currents are well managed.



V_I = Input Voltage at AIN
V_S = External Driving Source Voltage
R_S = Source Resistance
$R_{i(ADC)}$ = Input Resistance of ADC
$R_{i(MUX)}$ = Input Resistance (MUX on resistance)
C_i = Input Capacitance
V_C = Capacitance Charging Voltage

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 10. Equivalent Input Circuit Including the Driving Source

simplified analog input analysis

Using the equivalent circuit in Figure 9, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB, t_{ch}(1/2 LSB), can be derived as follows.

The capacitance charging voltage is given by:

$$V_{C(t)} = V_S\left(1-e^{-t_{ch}/R_tC_i}\right) \quad (1)$$

Where:

$R_t = R_S + R_i$

$R_i = R_{i(ADC)} + R_{i(MUX)}$

t_{ch} = Charge time

The input impedance R_i is 718 Ω at 5 V, and is higher (~ 1.25 kΩ) at 2.7 V. The final voltage to 1/2 LSB is given by:

$$V_C\ (1/2\ LSB) = V_S - (V_S/2048) \quad (2)$$

Equating equation 1 to equation 2 and solving for cycle time t_c gives:

$$V_S - \left(V_S/2048\right) = V_S\left(1-e^{-t_{ch}/R_tC_i}\right) \quad (3)$$

and time to change to 1/2 LSB (minimum sampling time) is:

$$t_{ch}\ (1/2\ LSB) = R_t \times C_i \times \ln(2048)$$

Where:

$\ln(2048) = 7.625$

Therefore, with the values given, the time for the analog input signal to settle is:

$$t_{ch}\,(1/2\,LSB) = (R_S + 718\,\Omega) \times 15\,pF \times \ln(2048) \quad (4)$$

This time must be less than the converter sample time shown in the timing diagrams, which is 6x SCLK.

$$t_{ch}\ (1/2\ LSB) \le 6x\ 1/f_{(SCLK)} \quad (5)$$

Therefore the maximum SCLK frequency is:

$$Max(f_{(SCLK)}) = 6/t_{ch}\,(1/2\,LSB) = 6/(\ln(2048) \times R_t \times C_i) \quad (6)$$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, GND to V_{CC} . . . . . –0.3 V to 6.5 V
Analog input voltage range . . . . . –0.3 V to AV_{DD} + 0.3 V
Reference input voltage range . . . . . AV_{DD} + 0.3 V
Digital input voltage range . . . . . –0.3 V to DV_{DD} + 0.3 V
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A: TLV1571C, TLV1578C . . . . . 0°C to 70°C
TLV1571I, TLV1578I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

power supplies

	MIN	MAX	UNIT
Analog supply voltage, AV_{DD}	2.7	5.5	V
Digital supply voltage, DV_{DD}	2.7	5.5	V

NOTE 1: Abs (AV_{DD} – DV_{DD}) < 0.5 V

analog inputs

	MIN	MAX	UNIT
Analog input voltage, AIN	AGND	VREFP	V

digital inputs

		MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	DV_{DD} = 2.7 V to 5.5 V	2.1	2.4		V
Low level input voltage, V_{IL}	DV_{DD} = 2.7 V to 5.5 V			0.8	V
Input CLK frequency	DV_{DD} = 4.5 V to 5.5 V			20	MHz
	DV_{DD} = 2.7 V to 3.3 V			10	MHz
Pulse duration, CLK high, $t_{w(CLKH)}$	DV_{DD} = 4.5 V to 5.5 V, f_{CLK} = 20 MHz	23			ns
	DV_{DD} = 2.7 V to 3.3 V, f_{CLK} = 10 MHz	46			ns
Pulse duration, CLK low, $t_{w(CLKL)}$	DV_{DD} = 4.5 V to 5.5 V, f_{CLK} = 20 MHz	23			ns
	DV_{DD} = 2.7 V to 3.3 V, f_{CLK} = 10 MHz	46			ns
Rise time, I/O and control, CLK, $\overline{CS}$	50 pF output load	4			ns
Fall time, I/O and control, CLK, $\overline{CS}$	50 pF output load	4			ns

reference specifications

			MIN	NOM	MAX	UNIT
External reference voltage	VREFP	AV_{DD} = 3 V	2		AV_{DD}	V
		AV_{DD} = 5 V	2.5		AV_{DD}	V
	VREFM	AV_{DD} = 3 V	AGND		1	V
		AV_{DD} = 5 V	AGND		2	V
	VREFP – VREFM		2		AV_{DD}–AGND	V

electrical characteristics over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

digital specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic inputs						
I_{IH}	High-level input current	DV_{DD} = 5 V, DV_{DD} = 3 V, Input = DV_{DD}	–1		1	μA
I_{IL}	Low-level input current	DV_{DD} = 5 V, DV_{DD} = 3 V, Input = 0 V	–1		1	μA
C_i	Input capacitance			10	15	pF
Logic outputs						
V_{OH}	High-level output voltage	I_{OH} = 50 μA to 0.5 mA	DV_{DD}–0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 50 μA to 0.5 mA			0.4	V
I_{OZ}	High-impedance-state output current	DV_{DD} = 5 V, DV_{DD} = 3 V, Input = DV_{DD}			1	μA
I_{OL}	Low-impedance-state output current	DV_{DD} = 5 V, DV_{DD} = 3 V, Input = 0 V			–1	μA
C_o	Output capacitance			5		pF
	Internal clock	3 V, AV_{DD} = DV_{DD}	9	10	11	MHz
		5 V, AV_{DD} = DV_{DD}	18	20	22	MHz

dc specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			10		Bits
Accuracy						
	Integral nonlinearity, INL	Best fit		±0.5	±1	LSB
	Differential nonlinearity, DNL			±0.5	±1	LSB
	Missing codes				0	
E_O	Offset error			±0.1%	±0.15%	FSR
E_G	Gain error			±0.1%	±0.2%	FSR
Analog input						
C_i	Input capacitance	AIN, AV_{DD} = 3 V, AV_{DD} = 5 V		15		pF
		MUX input, AV_{DD} = 3 V, AV_{DD} = 5 V		25		pF
I_{lkg}	Input leakage current	V_{AIN} = 0 to AV_{DD}			±1	μA
r_i	Input MUX ON resistance	AV_{DD} = DV_{DD} = 3 V		240	680	Ω
		AV_{DD} = DV_{DD} = 5 V		215	340	Ω
Voltage reference input						
r_i	Input resistance		2			kΩ
C_i	Input capacitance			300		pF
Power supply						
	Operating supply current, I_{DD} + I_{REF}	AV_{DD} = DV_{DD} = 3 V, f_{CLK} = 10 MHz		4	5.5	mA
		AV_{DD} = DV_{DD} = 5 V, f_{CLK} = 20 MHz		7	8.5	mA
PD	Power dissipation	AV_{DD}+DV_{DD} = 3 V		12	17	mW
		AV_{DD}+DV_{DD} = 5 V		35	43	mW
I_{PD}	Supply current in power-down mode, Software	I_{DD} + I_{REF}, AV_{DD} = 3 V		1	8	μA
		I_{DD} + I_{REF}, AV_{DD} = 5 V		2	10	μA
	Supply current in power-down mode, Auto	I_{DD} + I_{REF}, AV_{DD} = 3 V		0.5	1	mA
		I_{DD} + I_{REF}, AV_{DD} = 5 V		0.5	1	mA

electrical characteristics over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted) (continued)

ac specifications, AV_{DD} = DV_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Signal-to-noise ratio, SNR		f_I = 100 kHz, 80% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	56	60		dB
			f_S = 625 KSPS, AV_{DD} = 3 V	58	60		dB
Signal-to-noise ratio + distortion, SINAD		f_I = 100 kHz, 80% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	55	60		dB
			f_S = 625 KSPS, AV_{DD} = 3 V	55	60		dB
Total harmonic distortion, THD		f_I = 100 kHz, 80% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V		–60	–56	dB
			f_S = 625 KSPS, AV_{DD} = 3 V		–60	–56	dB
Effective number of bits, ENOB		f_I = 100 kHz, 80% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V	9	9.3		Bits
			f_S = 625 KSPS, AV_{DD} = 3 V	9	9.3		Bits
Spurious free dynamic range, SFDR		f_I = 100 kHz, 80% of FS	f_S = 1.25 MSPS, AV_{DD} = 5 V		–63	–56	dB
			f_S = 625 KSPS, AV_{DD} = 3 V		–63	–56	dB
Analog input							
Channel-to-channel cross talk					–75		dB
Full-power bandwidth	–1 dB	Full-scale 0 dB input sine wave		12	18		MHz
	–3 dB	Full-scale 0 dB input sine wave			30		MHz
Small-signal bandwidth	–1 dB	–20 dB input sine wave		15	20		MHz
	–3 dB	–20 dB input sine wave			35		MHz
Sampling rate, f_S		AV_{DD} = 4.5 V to 5.5 V		0.0625		1.25	MSPS
		AV_{DD} = 2.7 V to 3.3 V		0.0625		0.625	MSPS

timing requirements, AV_{DD} = DV_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{c(CLK)}$	Cycle time, CLK	DV_{DD} = 4.5 V to 5.5 V	50			ns
		DV_{DD} = 2.7 V to 3.3 V	100			ns
$t_{(sample)}$	Reset and sampling time			6		SYSCLK Cycles
t_c	Total conversion time			10		SYSCLK Cycles
$t_{wL(EOC)}$	Pulse width, end of conversion, EOC			10		SYSCLK Cycles
$t_{wL(INT)}$	Pulse width, interrupt			1		SYSCLK Cycles
$t_{(STARTOSC)}$	Start-up time, internal oscillator		100			ns
$t_{d(CSH\_CSTARTL)}$	Delay time, $\overline{CS}$ high to $\overline{CSTART}$ low			10		ns
$t_{en(RDL\_DAV)}$	Enable time, data out	DV_{DD} = 5 V at 50 pF		20		ns
		DV_{DD} = 3 V at 50 pF		40		ns
$t_{dis(RDH\_DAV)}$	Disable time, data out	DV_{DD} = 5 V at 50 pF		5		ns
		DV_{DD} = 3 V at 50 pF		10		ns
$t_{su(CSL\_WRL)}$	Setup time, $\overline{CS}$ to $\overline{WR}$		5			ns
$t_{h(WRH\_CSH)}$	Hold time, $\overline{CS}$ to $\overline{WR}$		5			ns
$t_{w(WR)}$	Pulse width, write		1			Clock Period
$t_{w(RD)}$	Pulse width, read		1			Clock Period
$t_{su(DAV\_WRH)}$	Setup time, data valid to $\overline{WR}$		10			ns
$t_{h(WRH\_DAV)}$	Hold time, data valid to $\overline{WR}$		5			ns
$t_{su(CSL\_RDL)}$	Setup time, $\overline{CS}$ to $\overline{RD}$			5		ns
$t_{h(RDH\_CSH)}$	Hold time, $\overline{CS}$ to $\overline{RD}$			5		ns
$t_{h(WRL\_EXTXLKH)}$	Hold time $\overline{WR}$ to clock high		5			ns
$t_{h(RDL\_EXTCLKH)}$	Hold time $\overline{RD}$ to clock high		5			ns
$t_{h(CSTARTL\_EXTCLKH)}$	Hold time $\overline{CSTART}$ to clock high		5			ns
$t_{su(WRH\_EXTCLKH)}$	Setup time $\overline{WR}$ high to clock high		5			ns
$t_{su(RDH\_EXTCLKH)}$	Setup time $\overline{RD}$ high to clock high		5			ns
$t_{su(CSTARTH\_EXTCLKH)}$	Setup time $\overline{CSTART}$ high to clock high		5			ns
$t_{d(EXTCLK\_CSTARTL)}$	Delay time clock low to $\overline{CSTART}$ low		5			ns
$t_{d(EOC\_RDL)}$	Delay time, conversion end to RD ↓		5			ns

NOTE: Specifications subject to change without notice.
Data valid is denoted as DAV.

TYPICAL CHARACTERISTICS

ANALOG MUX INPUT RESISTANCE vs INPUT CHANNEL NUMBER

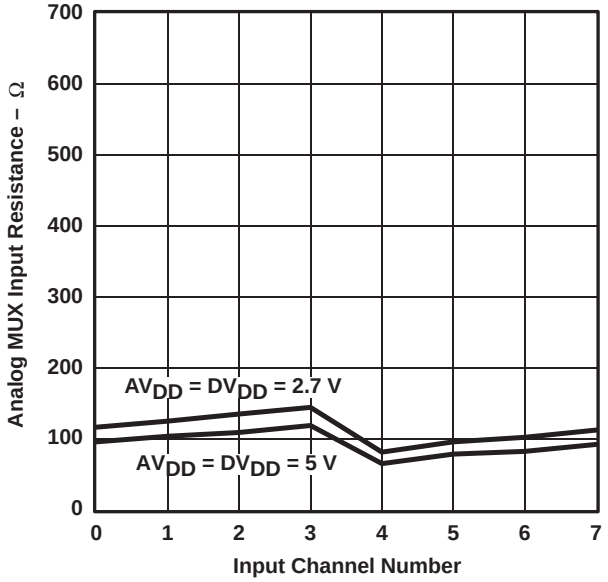


Figure 11

SUPPLY CURRENT vs FREE AIR TEMPERATURE

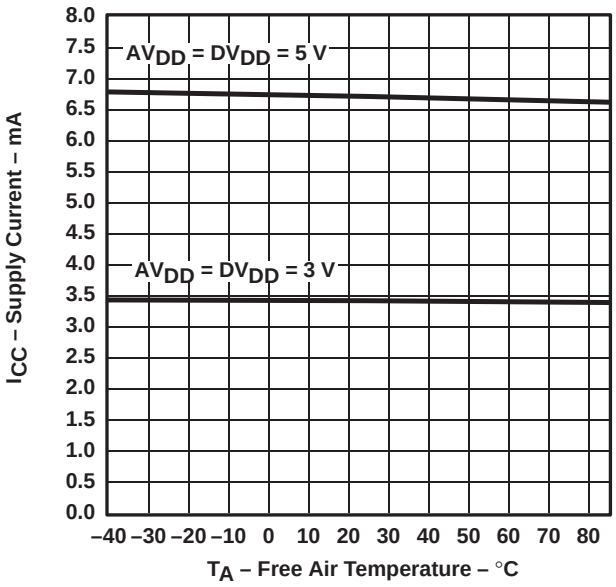


Figure 12

SUPPLY CURRENT vs CLOCK FREQUENCY

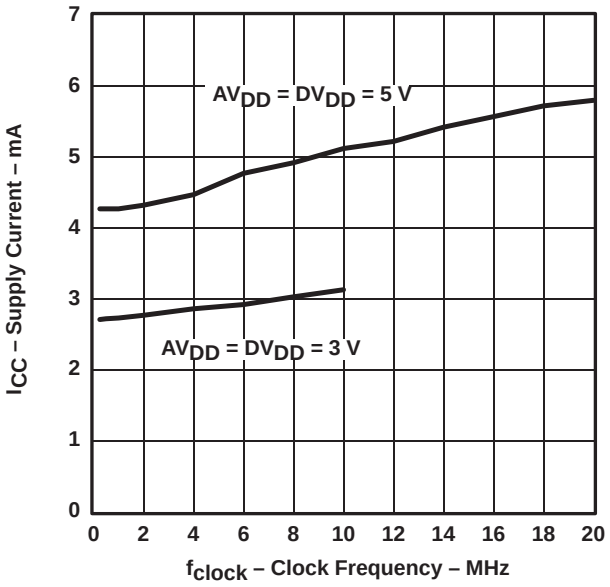


Figure 13

ANALOG INPUT BANDWIDTH vs FREQUENCY

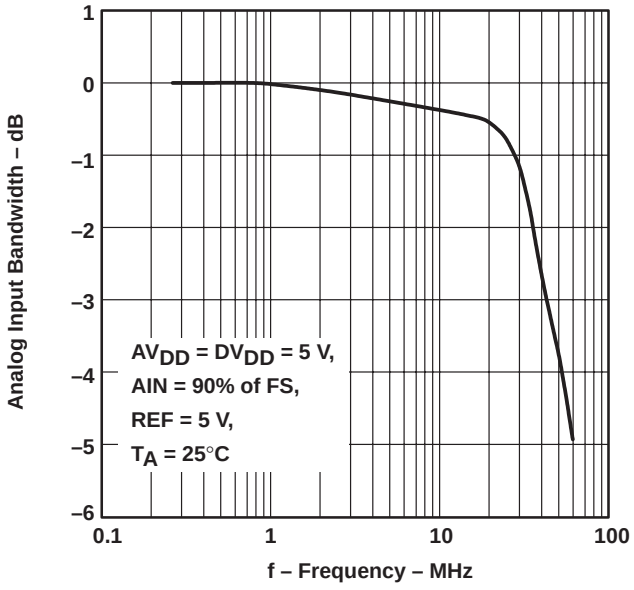


Figure 14

TYPICAL CHARACTERISTICS

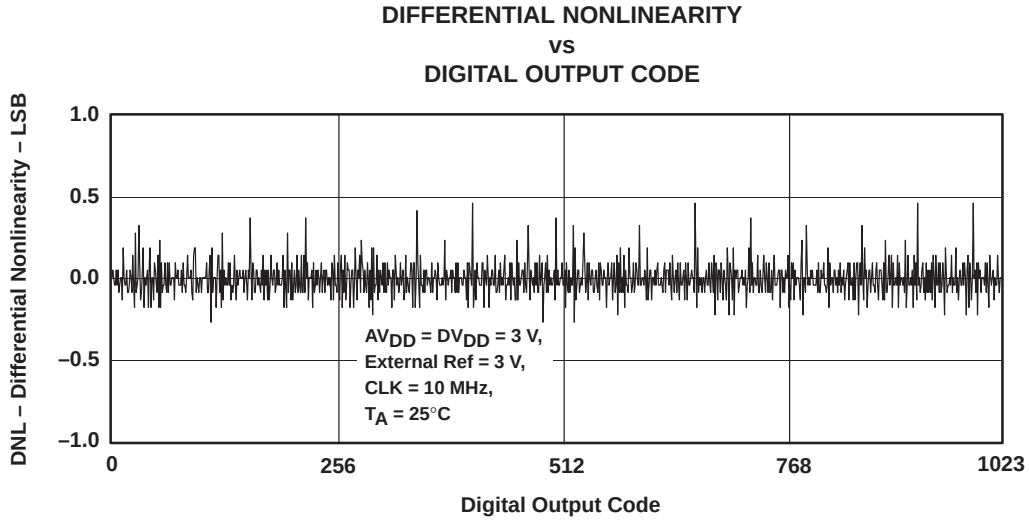


Figure 15

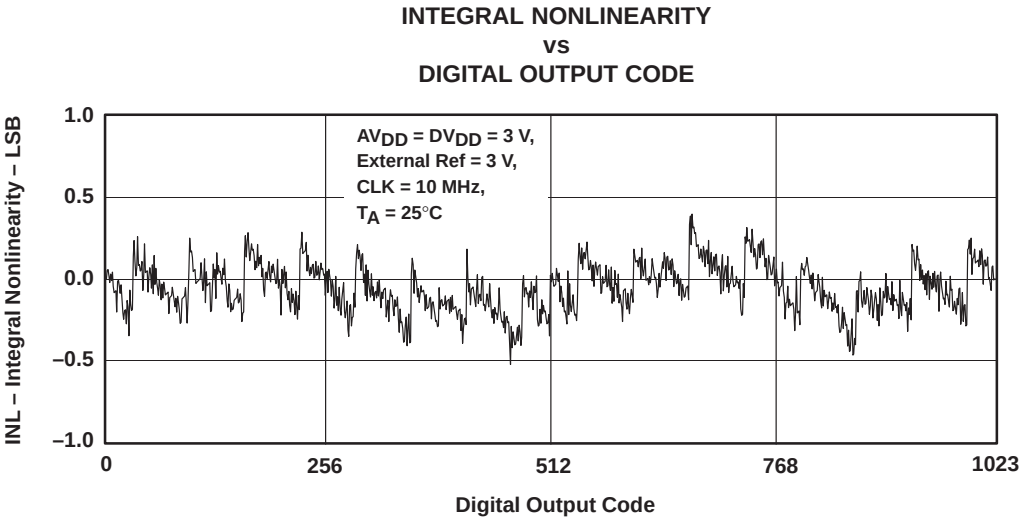


Figure 16

TYPICAL CHARACTERISTICS

DIFFERENTIAL NONLINEARITY vs DIGITAL OUTPUT CODE

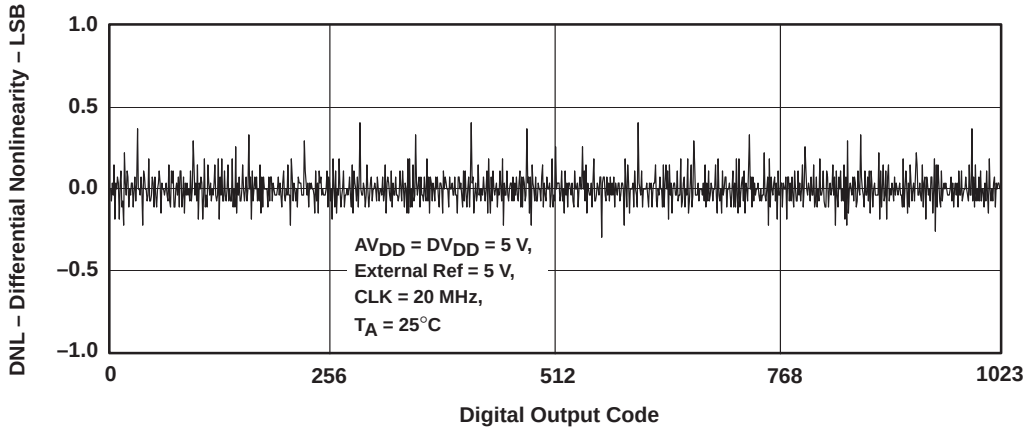


Figure 17

INTEGRAL NONLINEARITY vs DIGITAL OUTPUT CODE

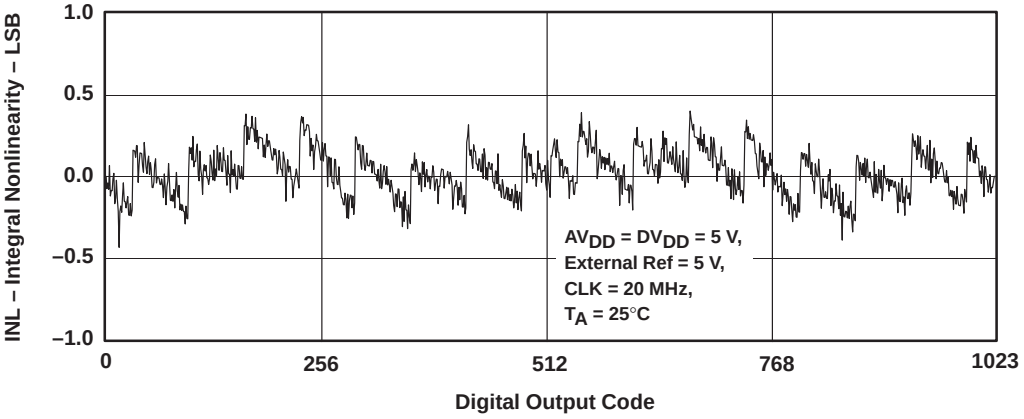


Figure 18

TYPICAL CHARACTERISTICS

EFFECTIVE NUMBER OF BITS vs FREQUENCY

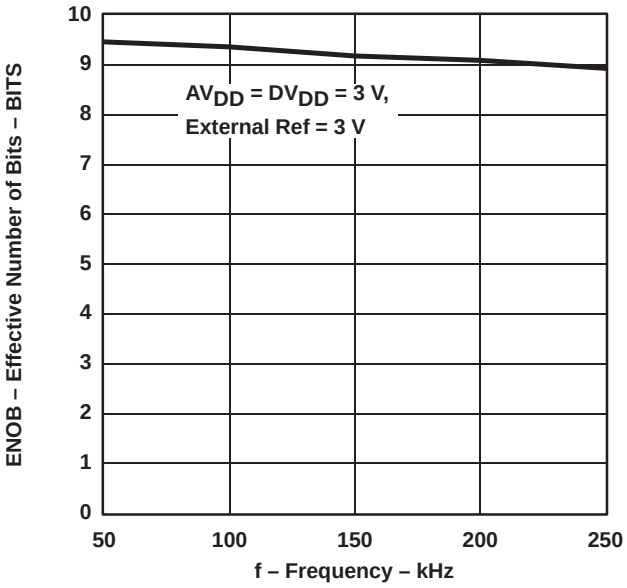


Figure 19

EFFECTIVE NUMBER OF BITS vs FREQUENCY

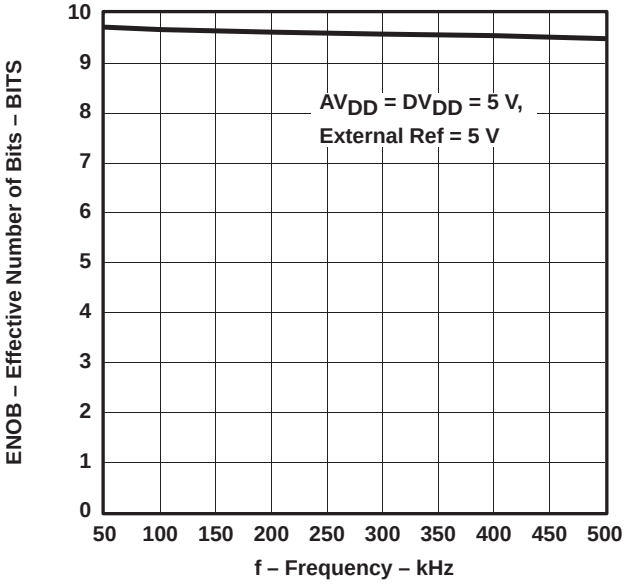


Figure 20

TYPICAL CHARACTERISTICS

FAST FOURIER TRANSFORM MAGNITUDE
vs
FREQUENCY

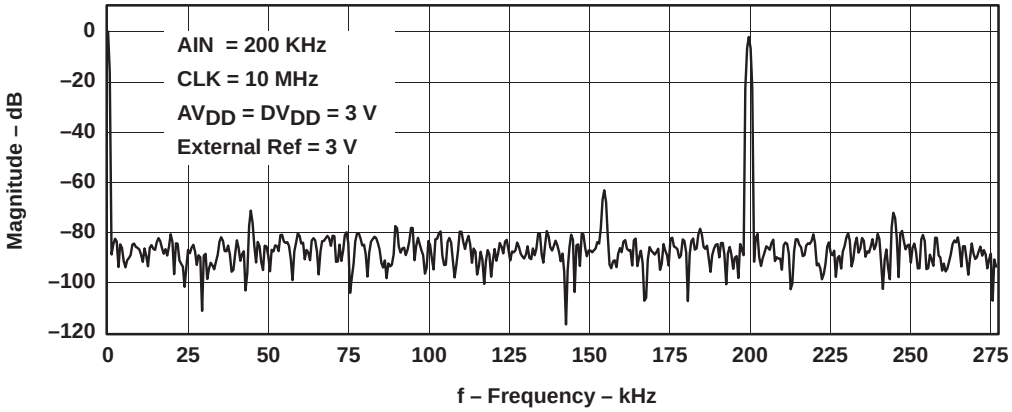


Figure 21

FAST FOURIER TRANSFORM MAGNITUDE
vs
FREQUENCY

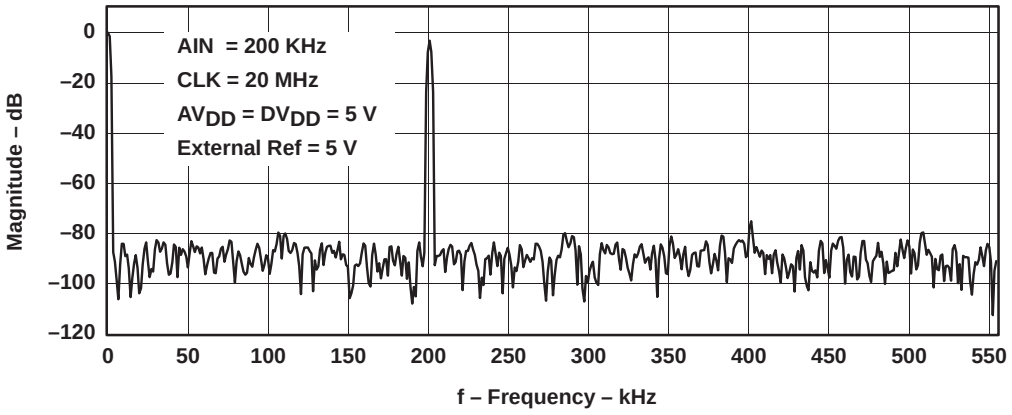
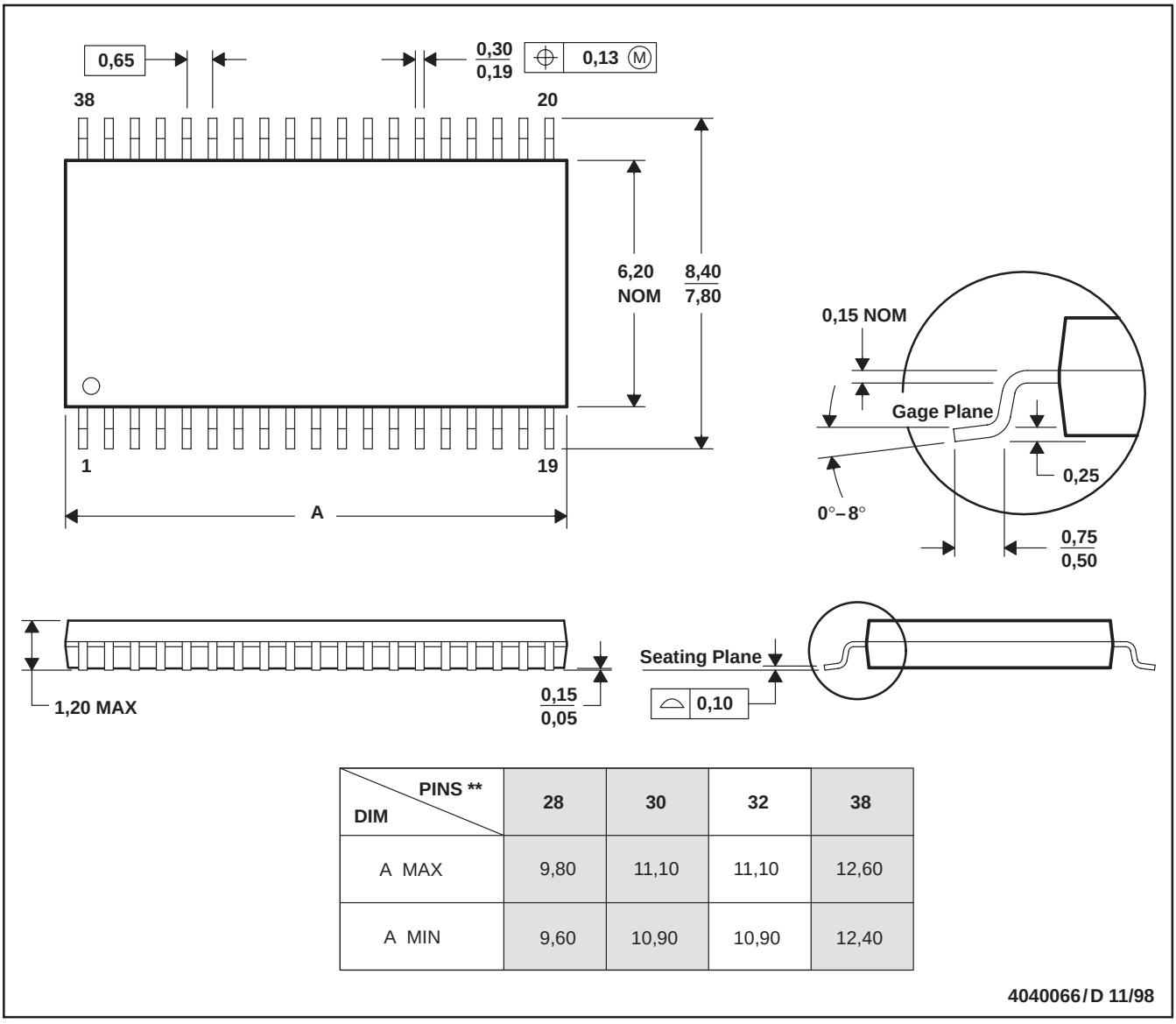


Figure 22

MECHANICAL DATA

DA (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

38 PINS SHOWN



DIM \ PINS **	28	30	32	38
A MAX	9,80	11,10	11,10	12,60
A MIN	9,60	10,90	10,90	12,40

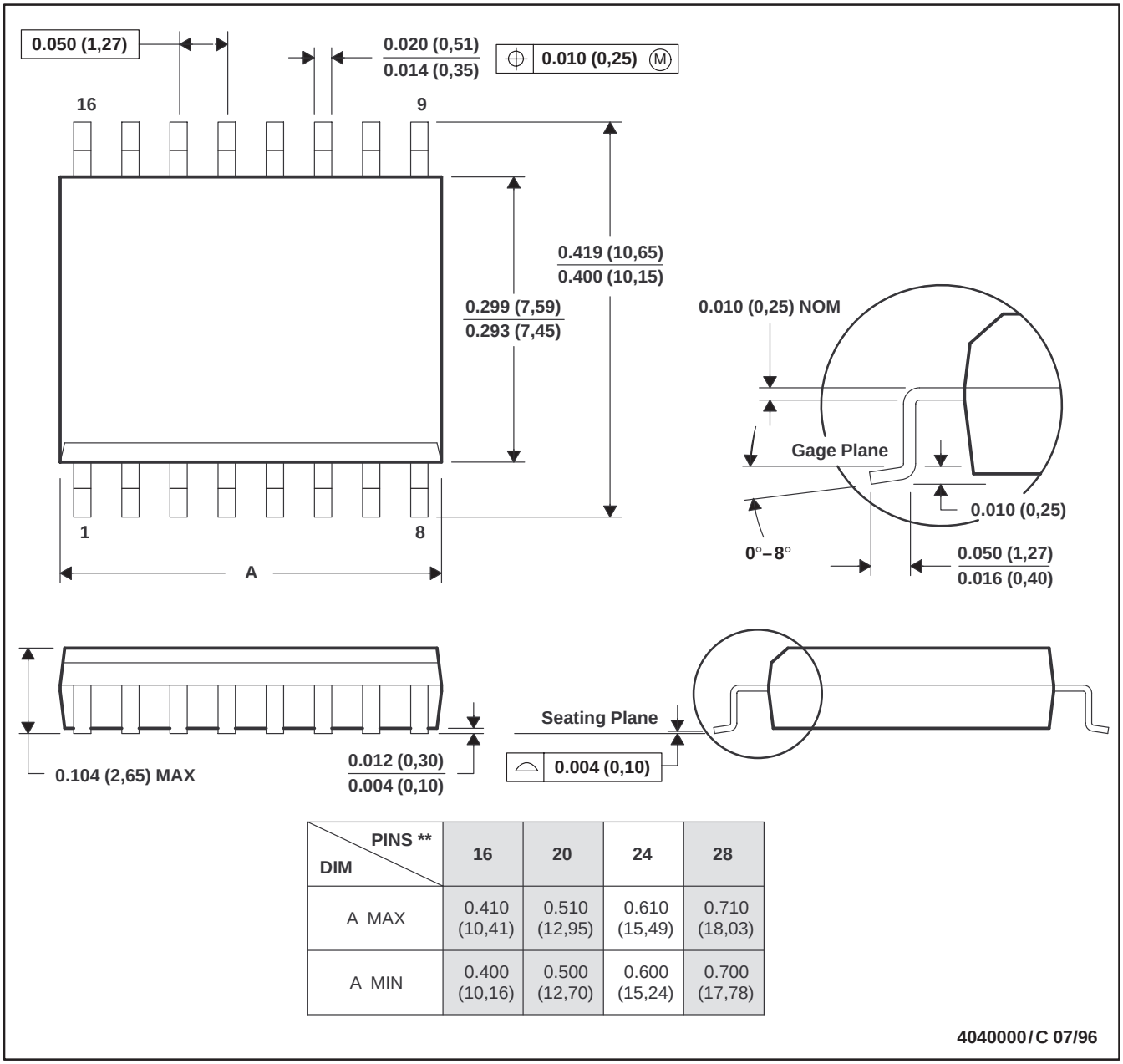
4040066/D 11/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/C 07/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLV1571CDW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1571CDWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1571IDW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1571IDWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV1571IPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV1571IPWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV1578CDA	ACTIVE	TSSOP	DA	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV1578CDAG4	ACTIVE	TSSOP	DA	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV1578CDAR	ACTIVE	TSSOP	DA	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV1578CDARG4	ACTIVE	TSSOP	DA	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV1578IDA	ACTIVE	TSSOP	DA	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV1578IDAG4	ACTIVE	TSSOP	DA	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

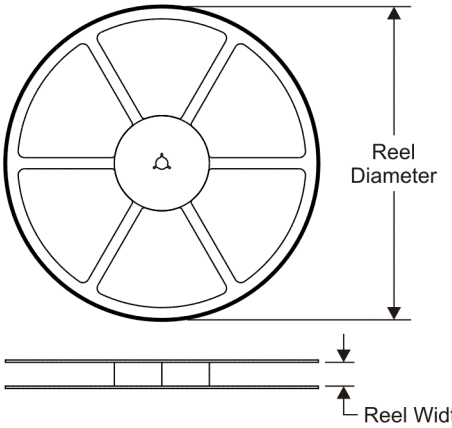
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

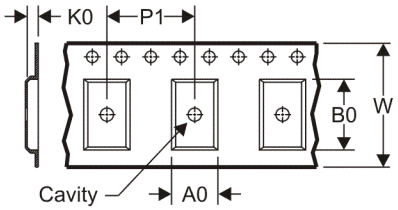
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

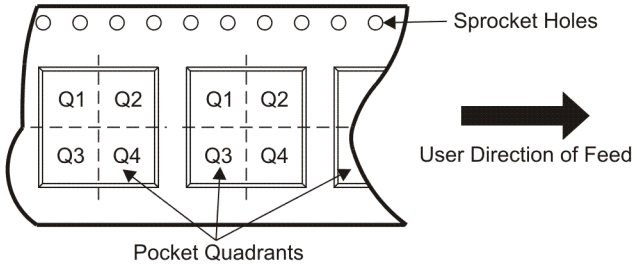


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

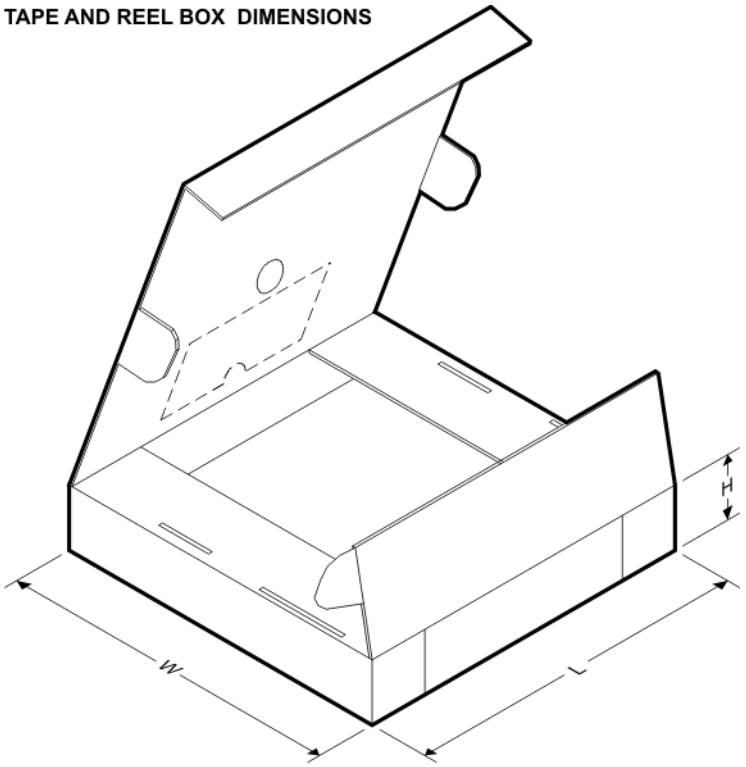


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1578CDAR	TSSOP	DA	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1578CDAR	TSSOP	DA	32	2000	346.0	346.0	41.0

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